



## Features

- Integrated PLL Loop Filter
- ESD Protection (4 kV HBM/200V MM; Except Pin 2: 4 kV HBM/100V MM) also at ANT1/ANT2
- High Output Power (7.5 dBm) with Low Supply Current (9.0 mA)
- Modulation Scheme ASK/ FSK
  - FSK Modulation is Achieved by Connecting an Additional Capacitor Between the XTAL Load Capacitor and the Open Drain Output of the Modulating Microcontroller
- Easy to Design-in Due to Excellent Isolation of the PLL from the PA and Power Supply
- Single Li-cell for Power Supply
- Supply Voltage 2.0V to 4.0V in the Temperature Range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}/125^{\circ}\text{C}$
- Package TSSOP8L
- Single-ended Antenna Output with High Efficient Power Amplifier
- CLK Output for Clocking the Microcontroller
- One-chip Solution with Minimum External Circuitry
- $125^{\circ}\text{C}$  Operation for Tire Pressure Systems



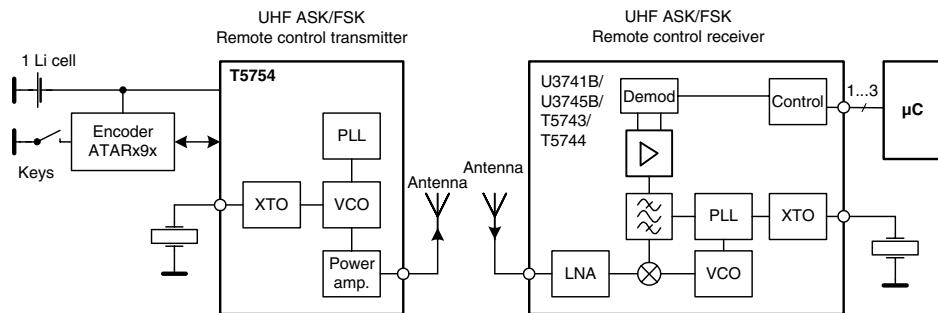
## UHF ASK/FSK Transmitter

## T5754

### 1. Description

The T5754 is a PLL transmitter IC which has been developed for the demands of RF low-cost transmission systems at data rates up to 32 kBaud. The transmitting frequency range is 429 MHz to 439 MHz. It can be used in both FSK and ASK systems.

Figure 1-1. System Block Diagram



## 2. Pin Configuration

Figure 2-1. Pinning TSSOP8L

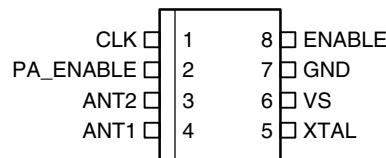


Table 2-1. Pin Description

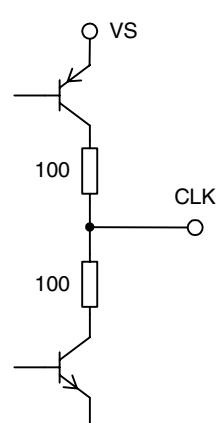
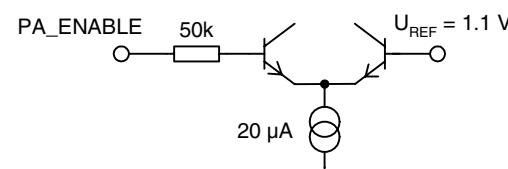
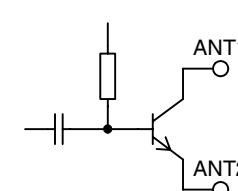
| Pin | Symbol    | Function   | Configuration   |
|-----|-----------|--|---|
| 1   | CLK       | Clock output signal for micro con roller<br>The clock output frequency is set by the crystal to $f_{XTAL}/4$ |   |
| 2   | PA_ENABLE | Switches on power amplifier, used for ASK modulation   |   |
| 3   | ANT2      | Emitter of antenna output stage  |   |
| 4   | ANT1      | Open collector antenna output  |  |

Table 2-1. Pin Description (Continued)

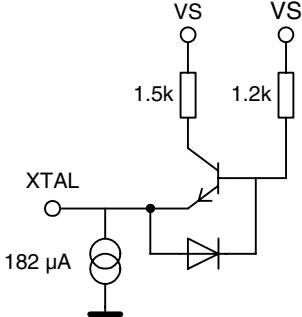
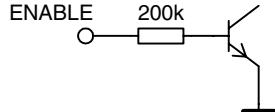
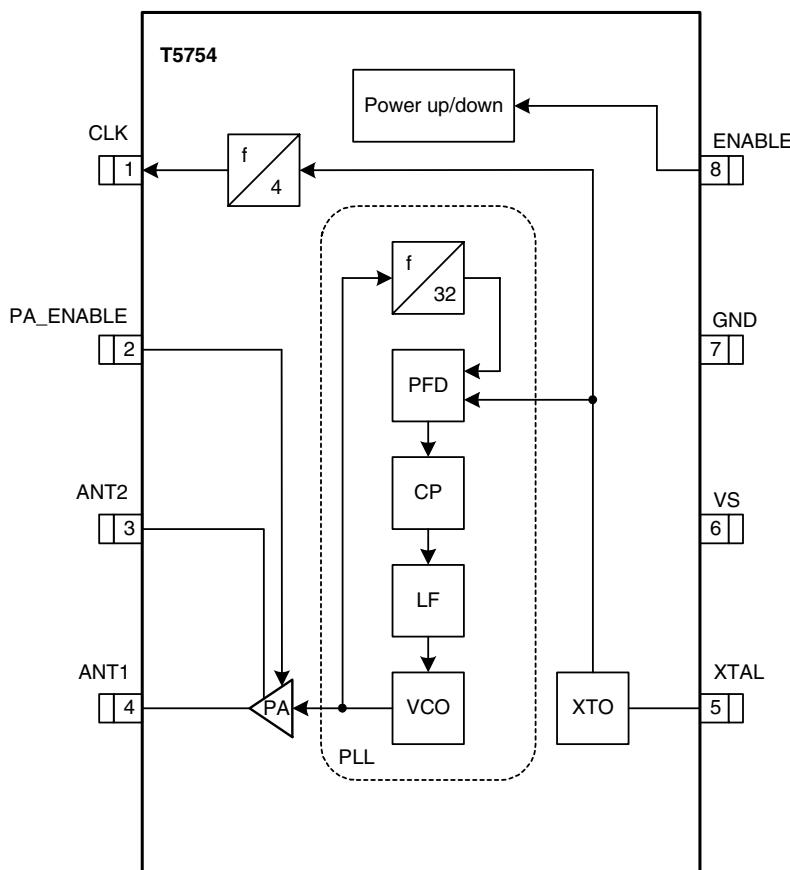
| Pin | Symbol | Function               | Configuration   |
|-----|--------|------------------------|---|
| 5   | XTAL   | Connection for crystal |   |
| 6   | VS     | Supply voltage         | See ESD protection circuitry (see <a href="#">Figure 4-5 on page 9</a> )            |
| 7   | GND    | Ground                 | See ESD protection circuitry (see <a href="#">Figure 4-5 on page 9</a> )            |
| 8   | ENABLE | Enable input           |  |

Figure 2-2. Block Diagram



### 3. General Description

This fully integrated PLL transmitter allows particularly simple, low-cost RF miniature transmitters to be assembled. The VCO is locked to  $32 f_{XTAL}$  hence a 13.56 MHz crystal is needed for a 433.92 MHz transmitter. All other PLL and VCO peripheral elements are integrated.

The XTO is a series resonance oscillator so that only one capacitor together with a crystal connected in series to GND are needed as external elements.

The crystal oscillator together with the PLL needs typically  $< 1$  ms until the PLL is locked and the CLK output is stable. There is a wait time of  $\geq 1$  ms until the CLK is used for the microcontroller and the PA is switched on.

The power amplifier is an open-collector output delivering a current pulse which is nearly independent from the load impedance. The delivered output power is hence controllable via the connected load impedance.

This output configuration enables a simple matching to any kind of antenna or to  $50\Omega$ . A high power efficiency of  $\eta = P_{out}/(I_{S,PA} \cdot V_S)$  of 36% for the power amplifier results when an optimized load impedance of  $Z_{Load} = (166 + j223)\Omega$  is used at 3V supply voltage.

### 4. Functional Description

If ENABLE = L and the PA\_ENABLE = L, the circuit is in standby mode consuming only a very small amount of current so that a lithium cell used as power supply can work for several years.

With ENABLE = H the XTO, PLL and the CLK driver are switched on. If PA\_ENABLE remains L only the PLL and the XTO is running and the CLK signal is delivered to the microcontroller. The VCO locks to 32 times the XTO frequency.

With ENABLE = H and PA\_ENABLE = H the PLL, XTO, CLK driver and the power amplifier are on. With PA\_ENABLE the power amplifier can be switched on and off, which is used to perform the ASK modulation.

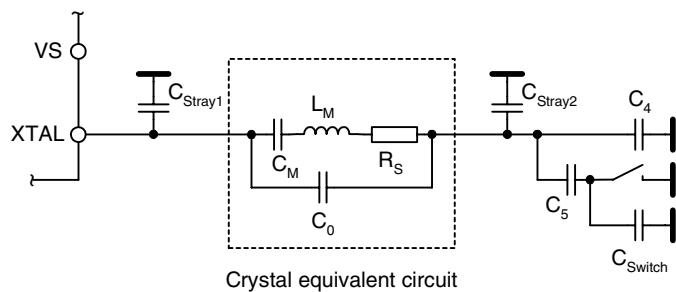
#### 4.1 ASK Transmission

The T5754 is activated by ENABLE = H. PA\_ENABLE must remain L for  $t \geq 1$  ms, then the CLK signal can be taken to clock the microcontroller and the output power can be modulated by means of pin PA\_ENABLE. After transmission PA\_ENABLE is switched to L and the microcontroller switches back to internal clocking. The T5754 is switched back to standby mode with ENABLE = L.

#### 4.2 FSK Transmission

The T5754 is activated by ENABLE = H. PA\_ENABLE must remain L for  $t \geq 1$  ms, then the CLK signal can be taken to clock the microcontroller and the power amplifier is switched on with PA\_ENABLE = H. The chip is then ready for FSK modulation. The microcontroller starts to switch on and off the capacitor between the XTAL load capacitor and GND with an open-drain output port, thus changing the reference frequency of the PLL. If the switch is closed, the output frequency is lower than if the switch is open. After transmission PA\_ENABLE is switched to L and the microcontroller switches back to internal clocking. The T5754 is switched back to standby mode with ENABLE = L.

The accuracy of the frequency deviation with XTAL pulling method is about  $\pm 25\%$  when the following tolerances are considered.

**Figure 4-1.** Tolerances of Frequency Modulation

Using  $C_4 = 9.2 \text{ pF} \pm 2\%$ ,  $C_5 = 6.8 \text{ pF} \pm 5\%$ , a switch port with  $C_{\text{Switch}} = 3 \text{ pF} \pm 10\%$ , stray capacitances on each side of the crystal of  $C_{\text{Stray}1} = C_{\text{Stray}2} = 1 \text{ pF} \pm 10\%$ , a parallel capacitance of the crystal of  $C_0 = 3.2 \text{ pF} \pm 10\%$  and a crystal with  $C_M = 13 \text{ fF} \pm 10\%$ , an FSK deviation of  $\pm 21 \text{ kHz}$  typical with worst case tolerances of  $\pm 16.3 \text{ kHz}$  to  $\pm 28.8 \text{ kHz}$  results.

## 4.3 CLK Output

An output CLK signal is provided for a connected microcontroller, the delivered signal is CMOS compatible if the load capacitance is lower than 10 pF.

### 4.3.1 Clock Pulse Take-over

The clock of the crystal oscillator can be used for clocking the microcontroller. Atmel's ATARx9x has the special feature of starting with an integrated RC-oscillator to switch on the T5754 with ENABLE = H, and after 1 ms to assume the clock signal of the transmission IC, so that the message can be sent with crystal accuracy.

### 4.3.2 Output Matching and Power Setting

The output power is set by the load impedance of the antenna. The maximum output power is achieved with a load impedance of  $Z_{\text{Load, opt}} = (166 + j223)\Omega$ . There must be a low resistive path to  $V_S$  to deliver the DC current.

The delivered current pulse of the power amplifier is 9 mA and the maximum output power is delivered to a resistive load of  $465\Omega$  if the 1.0 pF output capacitance of the power amplifier is compensated by the load impedance.

An optimum load impedance of:

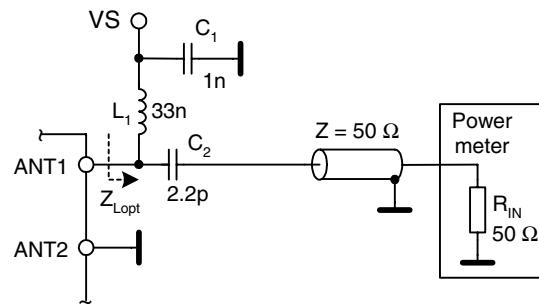
$Z_{\text{Load}} = 465\Omega \parallel j/(2 \times \pi \cdot 1.0 \text{ pF}) = (166 + j223)\Omega$  thus results for the maximum output power of 7.5 dBm.

The load impedance is defined as the impedance seen from the T5754's ANT1, ANT2 into the matching network. Do not confuse this large signal load impedance with a small signal input impedance delivered as input characteristic of RF amplifiers and measured from the application into the IC instead of from the IC into the application for a power amplifier.

Less output power is achieved by lowering the real parallel part of  $465\Omega$  where the parallel imaginary part should be kept constant.

Output power measurement can be done with the circuit of [Figure 4-2 on page 6](#). Note that the component values must be changed to compensate the individual board parasitics until the T5754 has the right load impedance  $Z_{\text{Load, opt}} = (166 + j223)\Omega$ . Also the damping of the cable used to measure the output power must be calibrated out.

**Figure 4-2.** Output Power Measurement



#### 4.4 Application Circuit

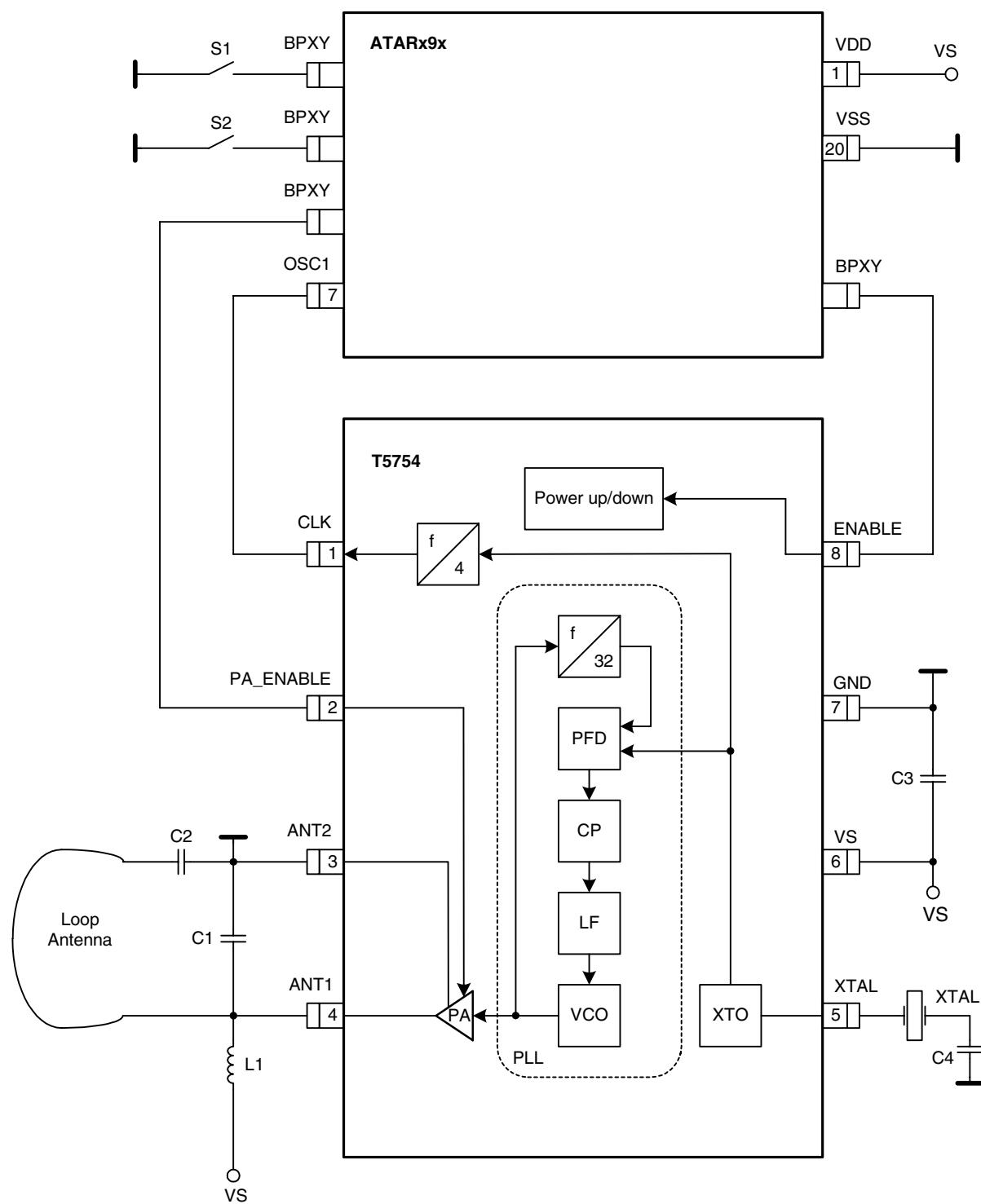
For the supply-voltage blocking capacitor  $C_3$  a value of 68 nF/X7R is recommended (see [Figure 4-3 on page 7](#) and [Figure 4-4 on page 8](#)).  $C_1$  and  $C_2$  are used to match the loop antenna to the power amplifier where  $C_1$  typically is 8.2 pF/NP0 and  $C_2$  is 6 pF/NP0 (10 pF + 15 pF in series); for  $C_2$  two capacitors in series should be used to achieve a better tolerance value and to have the possibility to realize the  $Z_{Load, opt}$  by using standard valued capacitors.

$C_1$  forms together with the pins of T5754 and the PCB board wires a series resonance loop that suppresses the 1<sup>st</sup> harmonic, hence the position of  $C_1$  on the PCB is important. Normally the best suppression is achieved when  $C_1$  is placed as close as possible to the pins ANT1 and ANT2.

The loop antenna should not exceed a width of 1.5 mm, otherwise the Q-factor of the loop antenna is too high.

$L_1$  ([50 nH to 100 nH] can be printed on PCB.  $C_4$  should be selected that the XTO runs on the load resonance frequency of the crystal. Normally, a value of 12 pF results for a 15 pF load-capacitance crystal.

Figure 4-3. ASK Application Circuit



**Figure 4-4.** FSK Application Circuit

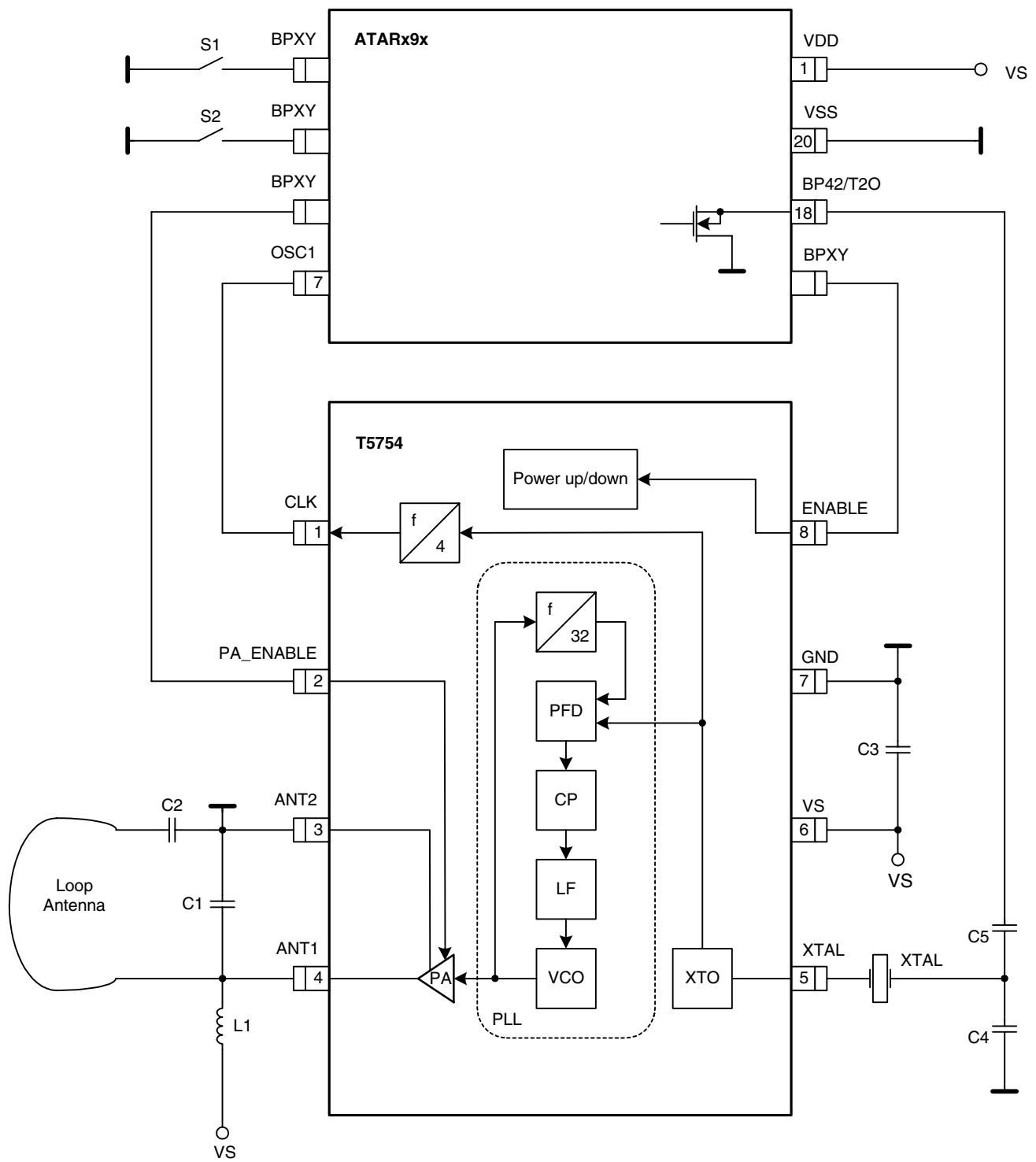
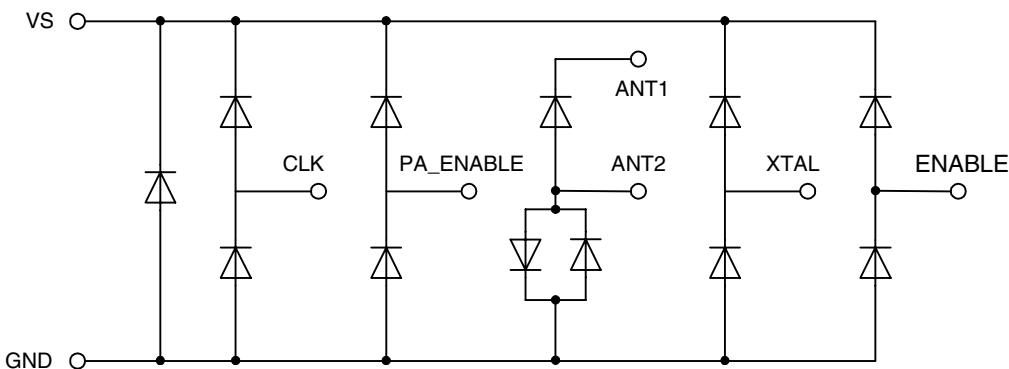


Figure 4-5. ESD Protection Circuit



## 5. Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters           | Symbol              | Minimum | Maximum             | Unit |
|----------------------|---------------------|---------|---------------------|------|
| Supply voltage       | $V_S$               |         | 5                   | V    |
| Power dissipation    | $P_{tot}$           |         | 100                 | mW   |
| Junction temperature | $T_j$               |         | 150                 | °C   |
| Storage temperature  | $T_{stg}$           | -55     | 125                 | °C   |
| Ambient temperature  | $T_{amb}$           | -55     | 125                 | °C   |
| Input voltage        | $V_{maxPA\_ENABLE}$ | -0.3    | $(V_S + 0.3)^{(1)}$ | V    |

Note: 1. If  $V_S + 0.3$  is higher than 3.7V, the maximum voltage will be reduced to 3.7V.

## 6. Thermal Resistance

| Parameters       | Symbol     | Value | Unit |
|------------------|------------|-------|------|
| Junction ambient | $R_{thJA}$ | 170   | K/W  |

## 7. Electrical Characteristics

$V_S$  = 2.0V to 4.0V,  $T_{amb}$  = -40°C to 125°C unless otherwise specified.

Typical values are given at  $V_S$  = 3.0 V and  $T_{amb}$  = 25°C. All parameters are referred to GND (pin 7).

| Parameters     | Test Conditions  | Symbol            | Min. | Typ. | Max.     | Unit           |
|----------------|--|-------------------|------|------|----------|----------------|
| Supply current | Power down<br>$V_{ENABLE} < 0.25V$ , -40°C to 85°C<br>$V_{PA-ENABLE} < 0.25V$ , -40°C to +125°C<br>$V_{PA-ENABLE} < 0.25V$ , 25°C<br>(100% correlation tested) | $I_{S\_off}$      |      | < 10 | 350<br>7 | nA<br>µA<br>nA |
| Supply current | Power up, PA off, $V_S$ = 3V,<br>$V_{ENABLE} > 1.7V$ , $V_{PA-ENABLE} < 0.25V$   | $I_S$             |      | 3.7  | 4.8      | mA             |
| Supply current | Power up, $V_S$ = 3.0V,<br>$V_{ENABLE} > 1.7V$ , $V_{PA-ENABLE} > 1.7V$  | $I_{S\_Transmit}$ |      | 9    | 11.6     | mA             |

Note: 1. If  $V_S$  is higher than 3.6V, the maximum voltage will be reduced to 3.6V.

## 7. Electrical Characteristics (Continued)

$V_S$  = 2.0V to 4.0V,  $T_{amb}$  = -40°C to 125°C unless otherwise specified.

Typical values are given at  $V_S$  = 3.0 V and  $T_{amb}$  = 25°C. All parameters are referred to GND (pin 7).

| Parameters  | Test Conditions   | Symbol                               | Min.             | Typ.        | Max.                     | Unit             |
|---|---|--------------------------------------|------------------|-------------|--------------------------|------------------|
| Output power  | $V_S$ = 3.0V, $T_{amb}$ = 25°C,<br>$f$ = 433.92 MHz, $Z_{Load}$ = (166 + j233)Ω   | $P_{Ref}$                            | 5.5              | 7.5         | 10                       | dBm              |
| Output power variation for the full temperature range       | $T_{amb}$ = -40°C to +85°C,<br>$V_S$ = 3.0V<br>$V_S$ = 2.0V   | $\Delta P_{Ref}$<br>$\Delta P_{Ref}$ |                  |             | -1.5<br>-4.0             | dB<br>dB         |
| Output power variation for the full temperature range       | $T_{amb}$ = -40°C to +125°C,<br>$V_S$ = 3.0V<br>$V_S$ = 2.0V<br>$P_{Out} = P_{Ref} + \Delta P_{Ref}$  | $\Delta P_{Ref}$<br>$\Delta P_{Ref}$ |                  |             | -2.0<br>-4.5             | dB<br>dB         |
| Achievable output-power range                               | Selectable by load impedance  | $P_{Out\_typ}$                       | 0                |             | 7.5                      | dBm              |
| Spurious emission   | $f_{CLK} = f_0/128$<br>Load capacitance at pin CLK = 10 pF<br>$f_O \pm 1 \times f_{CLK}$<br>$f_O \pm 4 \times f_{CLK}$<br>other spurious are lower  |                                      |                  | -55<br>-52  |                          | dBc<br>dBc       |
| Oscillator frequency XTO<br>(= phase comparator frequency)  | $f_{XTO} = f_0/32$<br>$f_{XTAL}$ = resonant frequency of the XTAL,<br>$C_M \leq 10$ fF, load capacitance selected<br>accordingly<br>$T_{amb}$ = -40°C to +85°C<br>$T_{amb}$ = -40°C to +125°C | $f_{XTO}$                            | -30<br>-40       | $f_{XTAL}$  | +30<br>+40               | ppm<br>ppm       |
| PLL loop bandwidth  |   |                                      |                  | 250         |                          | kHz              |
| Phase noise of phase comparator                             | Referred to $f_{PC} = f_{XTO}$ ,<br>25 kHz distance to carrier  |                                      |                  | -116        | -110                     | dBc/Hz           |
| In loop phase noise PLL                                     | 25 kHz distance to carrier  |                                      |                  | -86         | -80                      | dBc/Hz           |
| Phase noise VCO   | at 1 MHz<br>at 36 MHz   |                                      |                  | -94<br>-125 | -90<br>-121              | dBc/Hz<br>dBc/Hz |
| Frequency range of VCO                                      |   | $f_{VCO}$                            | 429              |             | 439                      | MHz              |
| Clock output frequency (CMOS<br>microcontroller compatible) |   |                                      |                  | $f_0/128$   |                          | MHz              |
| Voltage swing at pin CLK                                    | $C_{Load} \leq 10$ pF   | $V_{0h}$<br>$V_{0l}$                 | $V_S \times 0.8$ |             | $V_S \times 0.2$         | V<br>V           |
| Series resonance R of the crystal                           |   | $R_S$                                |                  |             | 110                      | Ω                |
| Capacitive load at pin XTO                                  |   |                                      |                  |             | 7                        | pF               |
| FSK modulation frequency rate                               | Duty cycle of the modulation signal = 50%   |                                      | 0                |             | 32                       | kHz              |
| ASK modulation frequency rate                               | Duty cycle of the modulation signal = 50%   |                                      | 0                |             | 32                       | kHz              |
| ENABLE input  | Low level input voltage<br>High level input voltage<br>Input current high   | $V_{ll}$<br>$V_{lh}$<br>$I_{In}$     | 1.7              |             | 0.25<br>20               | V<br>V<br>μA     |
| PA_ENABLE input   | Low level input voltage<br>High level input voltage<br>Input current high   | $V_{ll}$<br>$V_{lh}$<br>$I_{In}$     | 1.7              |             | 0.25<br>$V_S^{(1)}$<br>5 | V<br>V<br>μA     |

Note: 1. If  $V_S$  is higher than 3.6V, the maximum voltage will be reduced to 3.6V.

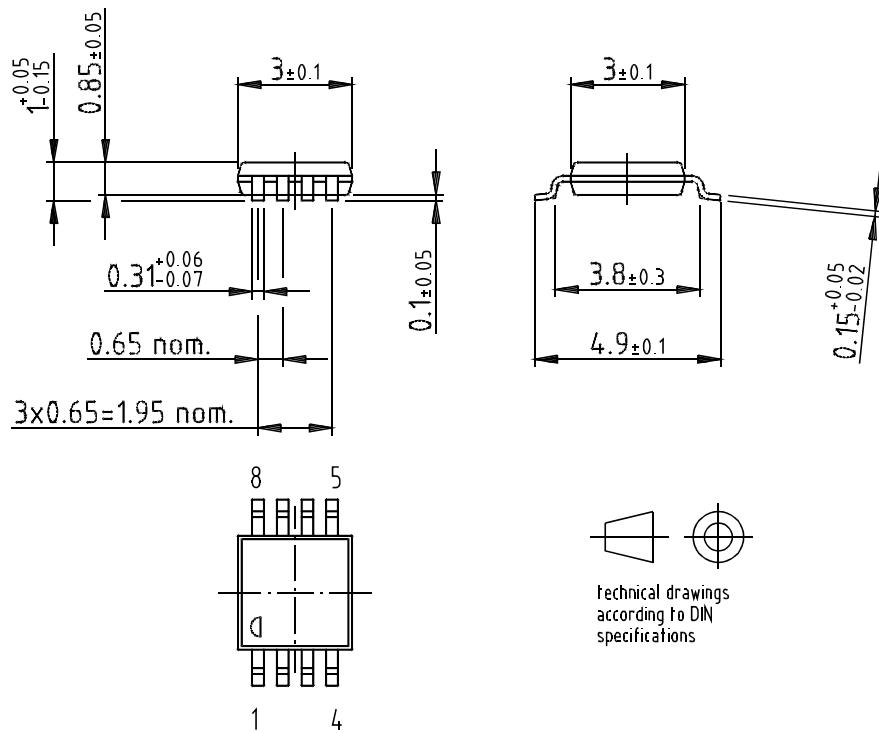
## 8. Ordering Information

| Extended Type Number | Package | Remarks  |
|----------------------|---------|--|
| T574-6AQJ            | TSSOP8L | Taped and reeled, Marking: T574, Pb-free             |
| T574-6APJ            | TSSOP8L | Taped and reeled, Marking: T574, small reel, Pb-free |

## 9. Package Information

Package: TSSOP 8L

Dimensions in mm



Drawing-No.: 6.543-5083.01-4

Issue: 2; 15.03.04

## 10. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No.    | History   |
|-----------------|---|
| 4711H-RKE-09/05 | <ul style="list-style-type: none"><li>• Pb-free Logo on page 1 added</li><li>• Ordering Information on page 11 changed</li></ul>  |
| 4711G-RKE-05/05 | <ul style="list-style-type: none"><li>• Put datasheet in a new template</li><li>• Package Information (page 11): Replace old package drawing through current version</li></ul>  |
| 4711F-RKE-07/04 | <ul style="list-style-type: none"><li>• Abs. Max. Ratings table (page 9): row “Input voltage” added</li><li>• Abs. Max. Ratings table (page 9): table note 1 added</li><li>• El. Char. table (pages 9 to 10): row “PA_ENABLE input” changed</li><li>• El. Char. table (pages 9 to 10): table note 1 added</li><li>• Ordering Information table (page 11): Remarks changed</li></ul> |



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