

Pin Configuration:

- 1. Base
- 2. Collector
- 3. Emitter
- 4. Collector

Features:

- Collector-Emitter sustaining voltage- $V_{CEO(sus)}$ = 50V (Minimum) 2N6109, 2N6290 DC current gain specified to 7A h_{FE} = 2.3 (Minimum) at I_C = 7A 2N6109, 2N6290
- Complementary Silicon Plastic Power Transistors

Maximum Ratings:

Parameter	Symbol	Value	Unit
Collector-Emitter Voltage	V _{CEO}	50	
Collector-Base Voltage	V _{CBO}	60	V
Emitter-Base Voltage	V _{EBO}	5	
Collector Current-Continuous -Peak	I _C	7	Α
Base Current	I _B	3	Α
Total Power Dissipation at TC = 25°C Derate above 25°C	P _D	40 0.32	W W/°C
Operating and Storage Junction Temperature Range	T _J , T _{STG}	-65 to +150	°C

Thermal Characteristic:

Characteristic	Symbol	Max.	Unit
Thermal Resistance Junction to Case	$R_{ heta jc}$	3.125	°C/W



Electrical Characteristics ($T_c = 25^{\circ}C$ unless otherwise noted):

Parameter	Symbol	Min.	Max.	Unit
Off Characteristics	•			
Collector-Emitter Sustaining Voltage (1) (IC = 100mA, IB = 0)	V _{CEO(sus)}	50	-	V
Collector Cut off Current (V _{CE} = 40V, I _B = 0)	I _{CEO}	-	1	
Collector Cut off Current $(V_{CE} = 60V, V_{BE(off)} = 1.5V)$ $(V_{CE} = 50V, V_{BE(off)} = 1.5V, T_{C} = 125^{\circ}C)$	I _{CEX}	-	0.1 2	mA
Emitter Cut off Current $(V_{EB} = 5V, I_{C} = 0)$	I	-	1	
On Characteristics (1)				
DC Current Gain		30		

DC Current Gain $(I_C = 2.5A, V_{CE} = 4V) (I_C = 7A, V_{CE} = 4V)$	h _{FE}	30 2.3	150	-
Collector-Emitter Saturation Voltage $(I_C = 7A, I_B = 3A)$	V	-	3.5	V
Base-Emitter On Voltage (I _C = 7A, V _{CE} = 4V)	V	-	3	V

Dynamic Characteristics

Current Gain-Bandwidth Product (2) $(I_C = 0.5A, V_{CE} = 4V, f = 1MHz)$	f	2.5 10	-	MHz
Small Signal Current Gain ($I_C = 0.5A$, $V_{CE} = 4V$, $f = 50kHz$)	h	20	-	-

⁽¹⁾ Pulse Test: Pulse width ≤300µs, Duty Cycle ≤2%

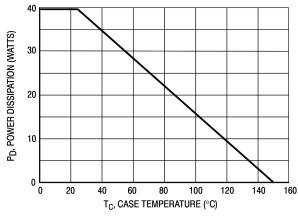


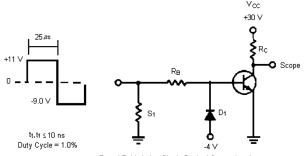
Figure 1. Power Derating

⁽²⁾ $f_T = h_{FE} \cdot f_{TEST}$

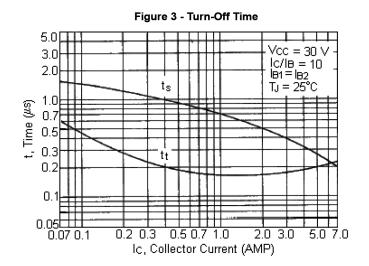




Figure 2 - Switching Time Test Circuit



Reand RcVaried to Obtain Desired Current Levels D1 must be fast recovery type, example: MB05300 used above IB = 100mA MSD6100 used below IB = 100mA



Tյ = 150°C hFE, DC Current Gain 100 50H 20 10E Ö.07 O.1 Ic, Collector Current (AMP)

Figure 4 - DC Current Gain

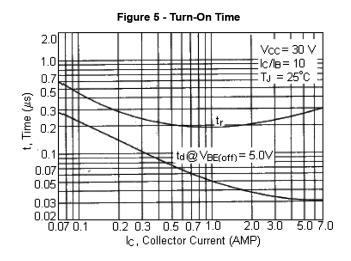
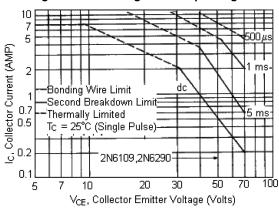




Figure - 6 Active Region Safe Operating Area



There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown safe operating area curves indicate $\rm I_C$ - $\rm V_{CE}$ limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure - 6 curve is based on $T_{J(PK)}$ = 150°C; T_C is variable depending on the power level. Second breakdown pulse limits are valid for duty cycles to 10% provided T_{J(PK)} ≤150°C. At high case temperatures, thermal limitation will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

Figure 7 - Collector Saturation Region

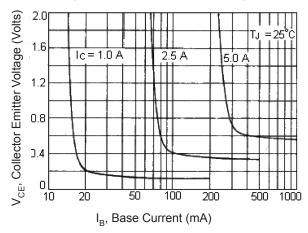
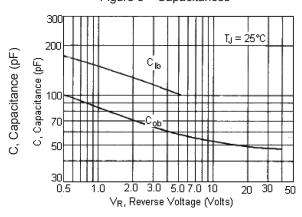


Figure 8 - Capacitances



VR, Reverse Voltage (Volts)



Figure 9 - "ON" Voltage Tj = 25 ℃ 1.6 V, Voltage (Volts) $V_{BE(sat)}@l_C/l_B = 10$ $V_{BE} @ V_{CE} = 4.0 V$ $_{at})@lc/l_{B} = 10$ 0.07 0.1 0.2 0.5 1.0 2.0 4.0 7.0 I_C, Collector Current (Amp)

I_C, Collector Current (µA) 10 101 109 REVERSE 10 0.

Figure 10 - Collector Cut-Off Region

V_{BE}, Base Emitter Voltage (Volts)

Max.

Min.

	-T- SEATING PLANE
→ B ← F	T S S
4	
Q A	<u> </u>
	u_ [↑]
<u>H</u>	
↑_↑	
z	
L_> 	R→ -
v————	J—>
G → ←	
D	
→ N <	

A	14.48	15.75
В	9.66	10.28
С	4.07	4.82
D	0.64	0.91
F	3.61	4.09
G	2.42	2.66
Н	2.8	4.1
J	0.36	0.64
K	12.7	14.27
L	1.15	1.52
N	4.83	5.33
Q	2.54	3.04
R	2.04	2.79
S	1.15	1.39
Т	5.97	6.47
U	0	1.27
V	1.15	-

Pin Configuration:

- 1. Base
- 2. Collector
- 3. Emitter
- 4. Collector

Dimension

Part Number Table

Description	Type	Part Number
Complementary Power Transistor	NPN	2N6290

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2.04

Dimensions: Millimetres