

## HIGH-SIDE CURRENT SENSE AMPLIFIER

### Features

- Complete, unidirectional high-side current sense capability
- 0.2% full-scale accuracy
- +5 to +36 V supply operation
- 85 dB power supply rejection
- 90  $\mu$ A max supply current
- 9  $\mu$ A shutdown current
- Operating Temperature Range: -40 to +85  $^{\circ}$ C
- 5-pin SOT-23 package
- RoHS-compliant

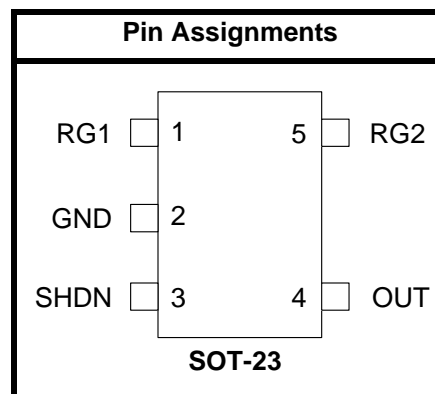
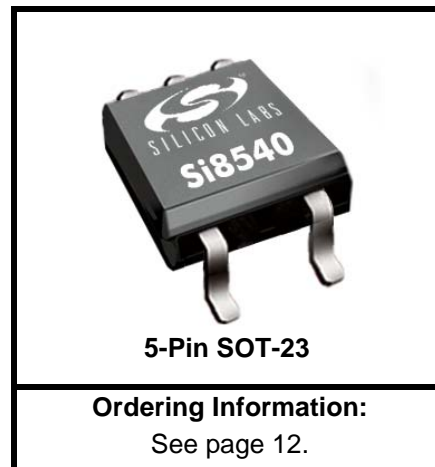
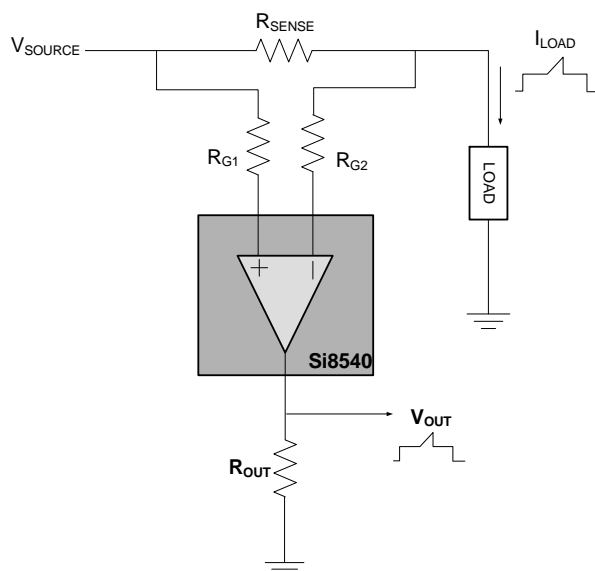
### Applications

- Battery chargers
- Smart battery packs
- DC motor control
- Backup systems
- Current control applications

### Description

The Si8540 is a unidirectional, 36 V (max), high-side current sense amplifier for use in applications requiring current monitoring and/or control. This device draws bias current from the high-side line to which it is attached, eliminating the need for an external supply. It measures current from 0.1 to 10 A by sensing the voltage across an external sense resistor (or PCB trace) from dc to 20 kHz and can achieve measurement accuracies of 0.2% (typical) at full load. The device output is a current signal proportional to measured current and is easily converted to a scaled voltage using a single external resistor. The Si8540 is available in compact SOT-23 package.

### Functional Block Diagram



Patents pending



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## 1. Electrical Specifications

**Table 1. Absolute Maximum Ratings**

Parameter	Value	Unit
Voltage at RG1, RG2, SHDN to GND	−0.3 to +40	V
Differential Input Voltage, RG1 to RG2	±0.3	V
Voltage at OUT	−0.3 to +8	V
Current into SHDN, GND, OUT, RG1, RG2	±50	mA
Continuous Power Dissipation ( $T_A = +70\text{ °C}$ ) 5-pin SOT23 derate 7.1 mW/°C above +70 °C*	571	mW
Operating Temperature Range	−40 to +85	°C
Junction Temperature, $T_{JMAX}$	Up to +150	°C
<b>*Note:</b> The device is mounted on a standard PCB with a 100 mm <sup>2</sup> copper foil connected to the GND pin, no airflow. Permanent device damage may occur if the absolute maximum ratings are exceeded, and prolonged use at the absolute maximum ratings may affect reliability. It is recommended that the device operate within the limits indicated in Table 2, "DC and AC Characteristics".		

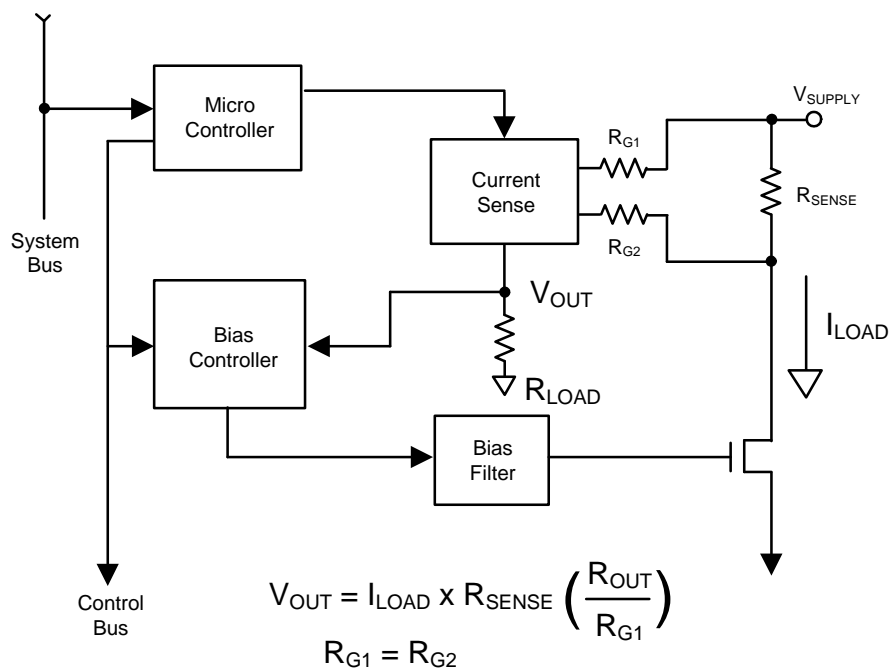
**Table 2. DC and AC Characteristics**(Unless otherwise specified:  $V_{RG1} = +5$  to  $+36$  V,  $R_{G1} = R_{G2} = 200$ ,  $V_{SENSE} = 0$  V,  $T_A = -40$  to  $+85$  °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Voltage	$V_{RG1}$		5	—	36	V
Operating Frequency	F		0	20	—	kHz
Total Input Current	$I_{RG1} + I_{RG2}$	$I_{LOAD} = 0$ A	—	46	90	$\mu$ A
Input Currents	$I_{RG1}$ , $I_{RG2}$	$I_{LOAD} = 0$ A	—	23	45	$\mu$ A
Input Current Matching	$I_{OS}$	$I_{RG1} - I_{RG2}$	—	$\pm 0.4$	$\pm 1.5$	$\mu$ A
Sense Voltage <sup>1</sup>	$V_{SENSE}$		—	100	—	mV
OUT Current Accuracy	$I_{RG}/I_{OUT}$	$V_{SENSE} = 100$ mV	—	$\pm 0.2$	$\pm 1.5$	%
No-Load OUT Error		$V_{RG1} = 10$ V, $V_{SENSE} = 0$ V	—	0.5	15	$\mu$ A
Low-Level OUT Error		$V_{RG1} = 10$ V, $V_{SENSE} = 3$ mV	—	$\pm 0.5$	$\pm 10$	$\mu$ A
Power-Supply Rejection	PSR	$V_{SENSE} = 100$ mV	—	-85	—	dB
Shutdown Supply Current	$I_{RG1} + I_{RG2}$	$V_{SHDN} = 2.4$ V	—	3.5	9	$\mu$ A
SHDN Input Low Voltage	$V_{IL}$		—	—	0.3	V
SHDN Input Low Current	$I_{IL}$	$V_{SHDN} = 0$ V	—	—	1.0	$\mu$ A
SHDN Input High Voltage	$V_{IH}$		2.4	—	—	V
SHDN Input High Current	$I_{IH}$	$V_{SHDN} = 2.4$ V	—	—	1.0	$\mu$ A
OUT Output Voltage Range	$V_{OUT}$	$V_{OUT}$ clamped at 8 V	0	—	$V_{RG1} - 3.5$ ( $< 8$ )	V
OUT Output Resistance (Internal)		$I_{OUT} = 1.5$ mA	1	3	—	M $\Omega$
OUT Rise, Fall Time		$V_{SENSE} = 5$ mV to 150 mV, $R_{OUT} = 2 = k\Omega$ , $C_{OUT} = 50$ pF, 10% to 90% (Note 2)	— —	0.4 0.5	— —	$\mu$ s $\mu$ s
OUT Settling Time to 1% of Final Value		$V_{SENSE} = 5$ to 150 mV, $R_{OUT} = 2 k\Omega$ , $C_{OUT} = 50$ pF (Note 2)	— —	1 2	— —	$\mu$ s $\mu$ s
Maximum Output Current	$I_{OUT}$	For $I_{OUT} > 1.5$ mA the internal current limitation starts to limit the output current	1.5	—	10	mA

**Notes:**

- $V_{SENSE}$  is the voltage across the sense resistor.
- $C_{OUT}$  is the load capacitance seen by the OUT pin.

## 2. Typical Application Schematic



**Figure 1. Connecting the Si8540 in a Power Control Application**

### 3. Functional Description

The Si8540 is designed to operate over an input common-mode range of 5 to 36 V. Figure 2 shows an example Si8540 application with external sense resistor,  $R_{SENSE}$ , external current gain-setting resistors,  $R_{G1}$  and  $R_{G2}$ , and output scaling resistor,  $R_{OUT}$ . The supply current flowing into the Si8540 inverting and non-inverting inputs ( $R_{G1}$ ,  $R_{G2}$ ) is negligible compared to  $I_{LOAD}$  and, as a result, has no appreciable effect on measurement accuracy. The internal current sense amplifier measures the differential input voltage,  $V_{SENSE}$ , and generates an output current proportional to  $I_{LOAD}$ . Resistor  $R_{OUT}$  converts this current to a voltage, and its value determines the output signal gain. The Si8540 is placed in a low-power shutdown mode when SHDN is at  $V_{IH}$ .

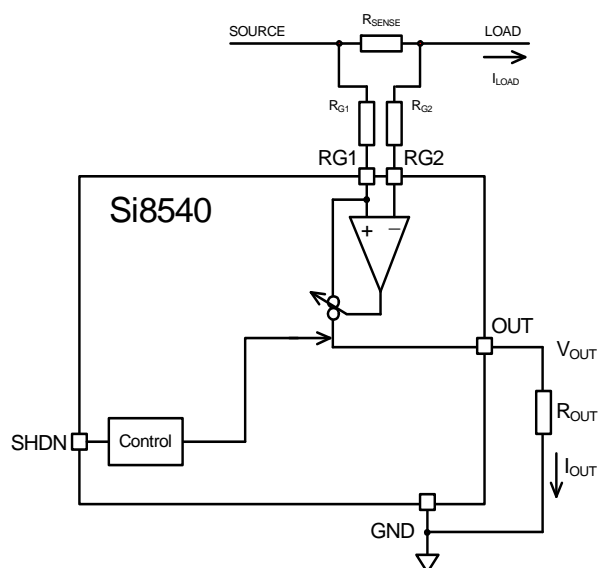


Figure 2. Si8540 Application Circuit

#### 3.1. Application Information

The Si8540 can sense a wide range of currents with different sense resistor values. Table 3 lists typical operational values.

Table 3. Recommended Current Sense Resistor for a Given Full-Scale Load Current

Full-scale Load Current $I_{SENSE}$ (A)	Current-Sense Resistor $R_{SENSE}$ (m $\Omega$ )	Gain-Setting Resistors, $R_{G1} = R_{G2}$ ( $\Omega$ )	Output Resistor, $R_{OUT}$ (k $\Omega$ )	Full-Scale Output Voltage, $V_{OUT}$ (V)	Scale Factor $V_{OUT}/I_{SENSE}$ (V/A)	Typical Error at 1, 10 and 100% of Full Load (%)		
						1%	10%	100%
0.1	1000	200	5	2.5	25	10	1	0.2
1	100	200	5	2.5	2.5	10	1	0.2
5	20	100	2	2	0.4	5	1	0.2
10	5	50	2	2	0.2	5	1	0.4

## 3.1.1. Selecting $R_{SENSE}$

Selecting  $R_{SENSE}$  involves making the best trade-off between power efficiency and accuracy. Low  $R_{SENSE}$  values dissipate less power while higher values maximize accuracy. In general, it is best to choose a relatively high value for  $R_{SENSE}$  in applications where the measured current is small. For higher current applications, the sense resistor should be able to dissipate the heat from its power loss; otherwise, its value may drift or it may fail open, possibly causing a large differential voltage across  $R_{G1}$  and  $R_{G2}$  that may damage the device. In most applications,  $R_{SENSE}$  should have low inductance to reduce the impact of any high-frequency components in the current being measured (low inductance metal film resistors are recommended). Also, note that the Si8540 requires at least 3.5 V of voltage headroom between the voltage at pin  $R_{G1}$  and pin OUT. This voltage headroom decreases as  $R_{SENSE}$  increases. A good guideline for determining the maximum value for  $R_{SENSE}$  is shown in the following equation:

$$R_{SENSEmax} = (V_{SOURCE} - V_{OUTmax} - 3.5 \text{ V}) / I_{LOAD}$$

Where:

$V_{SOURCE}$  is the high-side voltage

$V_{OUTmax}$  is the full-scale output voltage at the OUT pin

$I_{LOAD}$  is the current passing through  $R_{SENSE}$  measured by the Si8540

## 3.1.2. Selecting $R_{G1}$ and $R_{G2}$

The values of resistors  $R_{G1}$  and  $R_{G2}$  determine the sense amp current-gain. These two resistors must have the same value, and resulting current gain is equal to  $R_{SENSE} / R_G$  (where  $R_G = R_{G1} = R_{G2}$ ).

The minimum value of  $R_G$  is determined by the maximum current at the OUT pin (1.5 mA) and by the resistance between the internal current sense amp input and the sense resistor (approximately 0.2  $\Omega$ ). As the value of  $R_G$  is reduced, the input resistance becomes a larger portion of the total gain-setting resistance. This gain error can be compensated by trimming  $R_G$  or  $R_{OUT}$ . A good guideline for determining the maximum value for  $R_G$  is shown in the following equation:

$$R_{Gmax} = (V_{SENSEmax} / 1.5 \text{ mA})$$

Where:

$R_{Gmax}$  is the largest value for  $R_{G1}$  and  $R_{G2}$

$V_{SENSEmax}$  is the value of  $V_{SENSE}$  at maximum  $I_{LOAD}$

Note that for a given value of  $V_{SENSE}$ , a decrease of the  $R_G$  resistor values causes a corresponding increase in current at the OUT pin. This causes additional power to be dissipated in  $R_{OUT}$  rather than in the load, which can reduce efficiency. Note also that mismatches in the currents passing  $R_{G1}$  and  $R_{G2}$  (IOS) together with  $R_G$  affect the full scale error.

This error can be reduced by lowering the values of  $R_{G1}$ ,  $R_{G2}$  and/or lowering their tolerances. This error can also be reduced by increasing the value of  $R_{SENSE}$ .

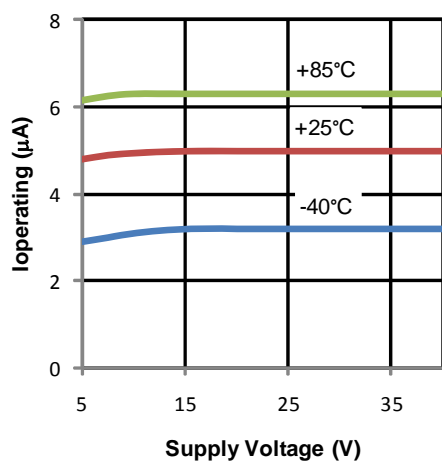
## 3.1.3. Choosing $R_{OUT}$

$R_{OUT}$  must be chosen to generate the required full-scale output voltage at the full scale  $I_{OUT}$ , which, in turn, is determined by  $R_{G1}$ ,  $R_{G2}$ , and  $R_{SENSE}$ . The upper limit of  $R_{OUT}$  is determined by the input impedance of the device that it drives. This input impedance should be much larger than  $R_{OUT}$ ; otherwise, measurement accuracy will be degraded. A good guideline for choosing the value of  $R_{OUT}$  is shown in the following equation:

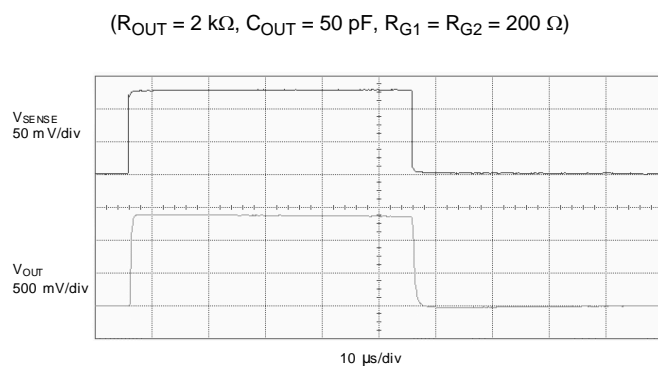
$$(V_{OUTfullscale} \times R_G) / (I_{LOAD} \times R_{SENSE})$$



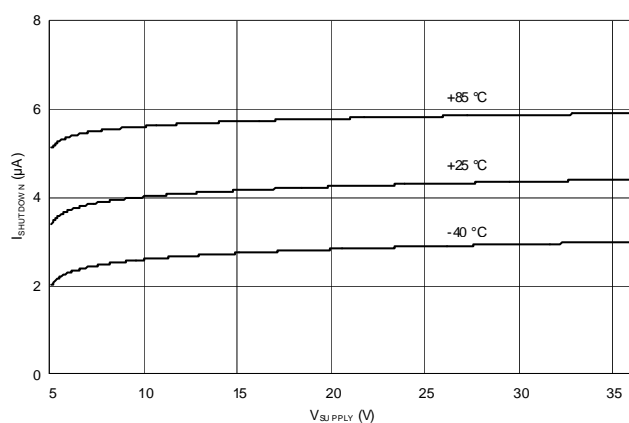
## 4. Typical Performance Data



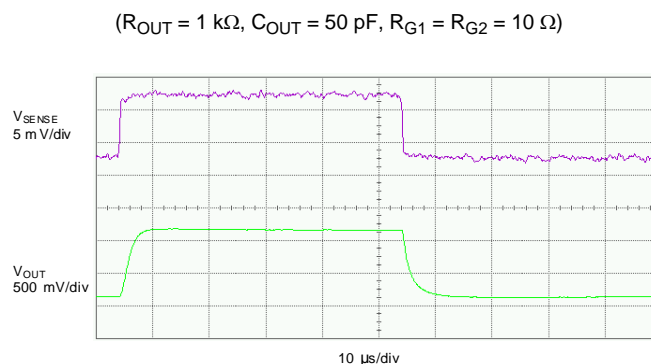
**Figure 3. Supply Current vs. Supply Voltage**



**Figure 4. Transient Response 1**

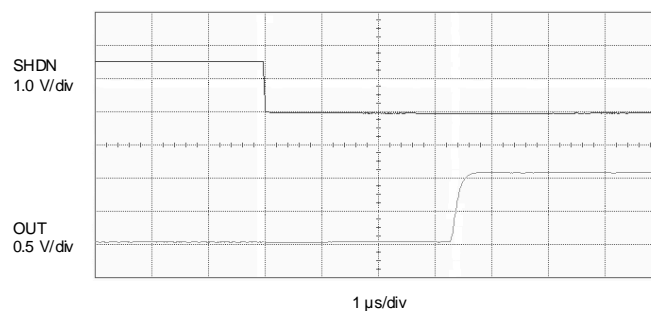


**Figure 5. Shutdown Supply Current vs. Supply Voltage**

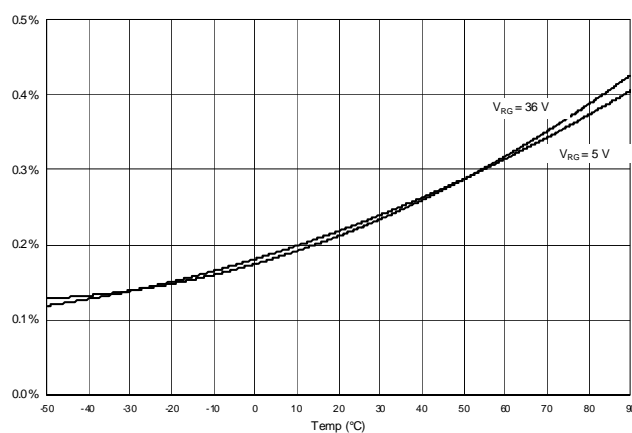


**Figure 6. Transient Response 2**

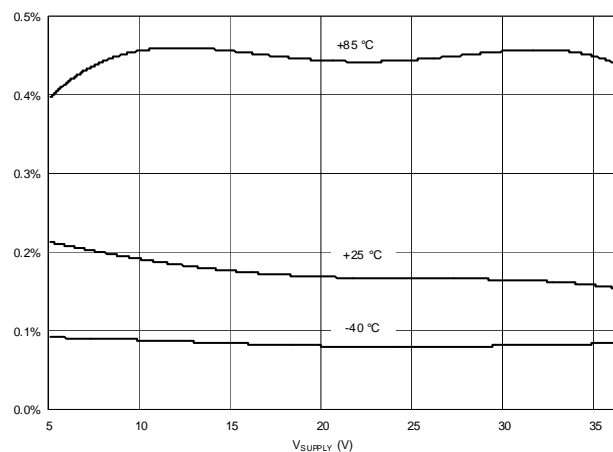
( $R_{\text{OUT}} = 2\text{ k}\Omega$ ,  $C_{\text{OUT}} = 50\text{ pF}$ ,  $R_{\text{G1}} = R_{\text{G2}} = 200\text{ }\Omega$ ,  $V_{\text{SENSE}} = 100\text{ mV}$ )



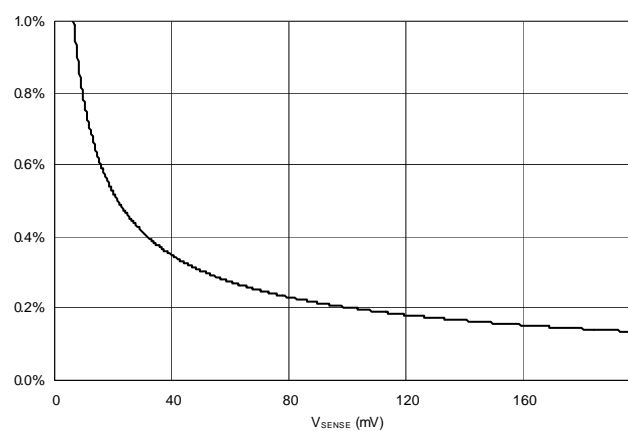
**Figure 7. Startup Delay**



**Figure 8. Output Error vs. Temperature**

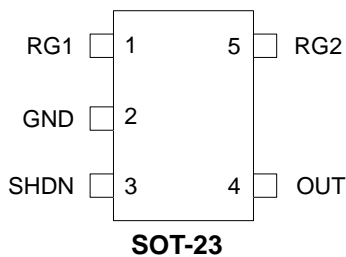


**Figure 9. Output Error vs. Supply Voltage**



**Figure 10. Output Error vs. Sense Voltage**

## 5. Pin Descriptions



**Figure 11. Pin Configuration**

**Table 4. Pin Descriptions**

Pin Number	Name	Description
<b>SOT23</b>		
1	RG1	Power-side input.
2	GND	Ground.
3	SHDN	Shutdown input. Ground for normal operation. High voltage for shutdown.
4	OUT	Current output.
5	RG2	Load-side input.

## 6. Ordering Guide

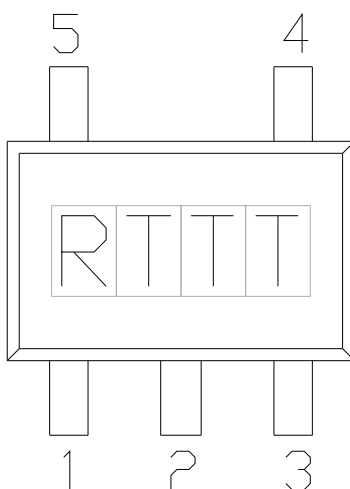
Ordering Part # <sup>1</sup>	Temperature Range	Package
Si8540-B-FW	–40 to +85 °C	SOT-23 <sup>2</sup>

**Notes:**

1. Tape and reel options are specified by adding an “R” suffix to the ordering part number.  
Example: “Si8450-B-FWR” indicates the SOT-23 package option in a tape and reel carrier.
2. Moisture sensitivity level (MSL) is (MSL2A) for SOT-23 package with peak reflow temperature of (260 °C) according to JEDEC industry-standard classifications.

## 6.1. Device Marking

### 6.1.1. SOT-23 Package Top Mark

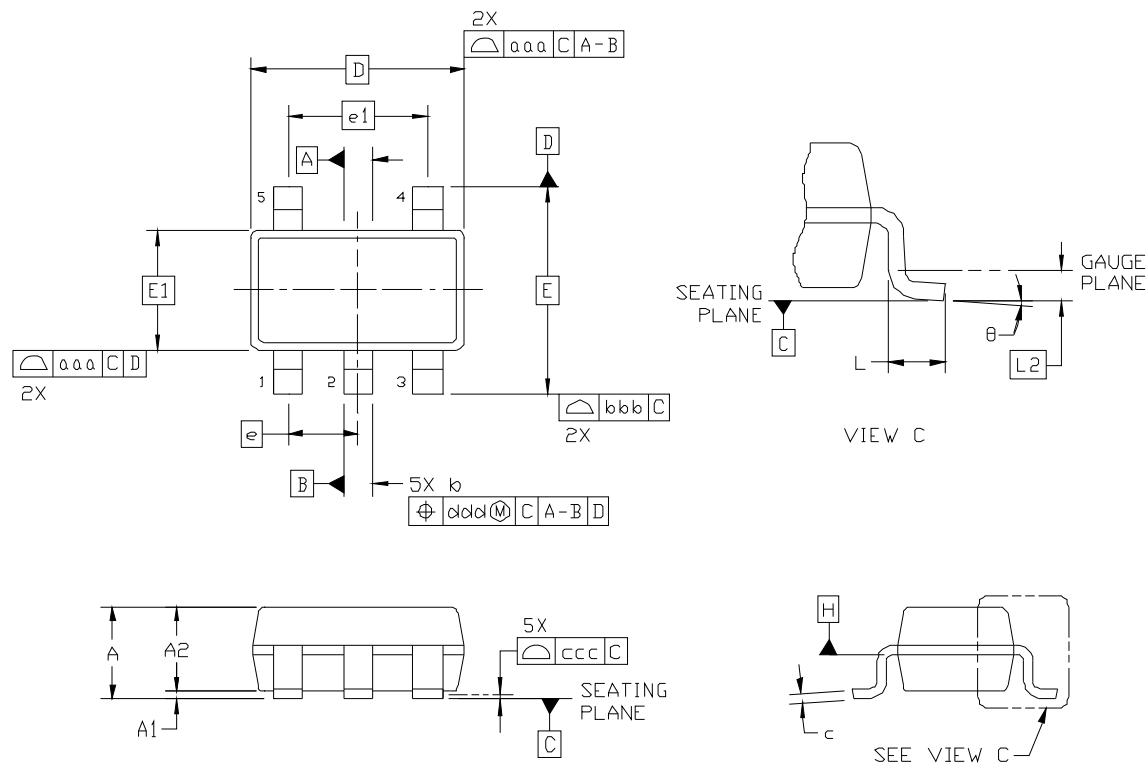


### 6.1.2. Top Marking Explanation

<b>Line 1 Marking:</b>	Manufacturing trace code	R = Device revision (B) TTT = Assembly trace code
------------------------	--------------------------	--

## 7. Package Outline: SOT-23

Figure 12 illustrates the package details for the SOT-23. Table 5 lists the values for the dimensions shown in the illustration.



**Figure 12. SOT-23 Package**

**Table 5. SOT-23 Package Diagram Dimensions**

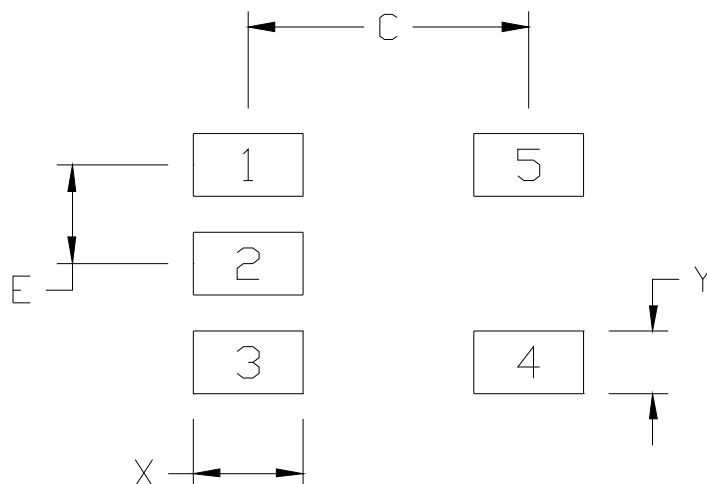
Dimension	Min	Max	Dimension	Min	Max
A	—	1.45	E1	1.90 BSC	
A1	0.00	0.15	L	0.30	0.60
A2	0.90	1.30	L2	0.25 BSC	
b	0.30	0.50	θ	0°	8°
c	0.08	0.20	aaa	0.15	
D	2.90 BSC		bbb	0.20	
E	2.80 BSC		ccc	0.10	
E1	1.60 BSC		ddd	0.20	
e	0.95 BSC				

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-178, Variation AA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

## 8. Land Pattern: SOT-23

Figure 13 illustrates the recommended land pattern details for the SOT-23 device. Table 6 lists the values for the dimensions shown in the illustration.



**Figure 13. SOT-23 Land Pattern**

**Table 6. SOT-23 Land Pattern Dimensions**

Dimension	(mm)
C	2.70
E	0.95
X	1.05
Y	0.60

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

**Card Assembly**

5. A No-Clean, Type-3 solder paste is recommended.
6. The recommended card reflow profile is per the JEDEC/IPC J-STD-020D specification for Small Body Components.

## DOCUMENT CHANGE LIST

### Revision 2.5 (July 2007 Integration Associates) to Revision 1.0 (March 2010 Silicon Laboratories)

- Reformatted document from IA2410 and renamed Si8540.
- Updated " Functional Block Diagram" on page 1.
- Updated " Description" on page 1.
- Updated Table 2 on page 5.
  - OUT current accuracy changed from  $\pm 1$  to  $\pm 1.5\%$ . (max)
  - No-Load OUT Error changed from 5 to 15  $\mu\text{A}$  (max)
  - Low-Level OUT Error changed from  $\pm 5$  to  $\pm 10$   $\mu\text{A}$  (max)
  - Temperature output error test conditions note updated to include temperature range of  $-40$  to TBD° C.
- Updated "3. Functional Description" on page 7.
- Updated "3.1.1. Selecting  $R_{\text{SENSE}}$ " on page 8.
- Updated "3.1.2. Selecting RG1 and RG2" on page 8.
- Updated "3.1.3. Choosing  $R_{\text{OUT}}$ " on page 8.
- Removed temperature sensing function throughout.
- Added recommended PCB Land Pattern sections.
- Reformatted document from "IA2410 Rev 2.5" (Integration Associates) and renamed and re-released as "Si8540 Rev 1.0" (which obsoletes the previous preliminary internal revision 2.6).

### Revision 1.0 to Revision 1.1

- MSL for the SOT-23 package improved to MSL2A (see "6. Ordering Guide" on page 12).
- Added "6.1. Device Marking" on page 13.

### Revision 1.1 to Revision 1.2

- Removed SOIC-8 package throughout document.



**NOTES:**

## CONTACT INFORMATION

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