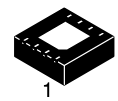
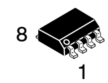
Constant Current Step-Up/ Step-Down/Inverting Switching Regulator for HB-LEDs

1.5 A

NCP3065, NCV3065

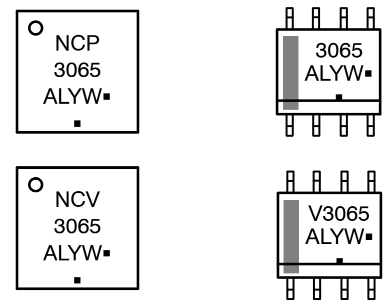


DFN8
MN SUFFIX
CASE 488AF



SOIC−8
D SUFFIX
CASE 751

MARKING DIAGRAMS



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

The NCP3065 is a monolithic switching regulator designed to deliver constant current for powering high brightness LEDs. The device has a very low feedback voltage of 235 mV (nominal) which is used to regulate the average current of the LED string. In addition, the NCP3065 has a wide input voltage up to 40 V to allow it to operate from 12 Vac or 12 Vdc supplies commonly used for lighting applications as well as unregulated supplies such as Lead Acid batteries. The device can be configured in a controller topology with the addition of an external transistor to support higher LED currents beyond the 1.5 A rated switch current of the internal transistor. The NCP3065 switching regulator can be configured in Step−Down (Buck) and Step−Up (Boost) topologies with a minimum number of external components.

Features

- Integrated 1.5 A Switch
- Input Voltage Range from 3.0 V to 40 V
- Low Feedback Voltage of 235 mV
- Cycle−by−Cycle Current Limit
- No Control Loop Compensation Required
- Frequency of Operation Adjustable up to 250 kHz
- Operation with All Ceramic Output Capacitors or No Output Capacitance
- Analog and Digital PWM Dimming Capability
- Internal Thermal Shutdown with Hysteresis
- Automotive Version Available

Applications

- Automotive and Marine Lighting
- High Power LED Driver
- Constant Current Source
- Low Voltage LED Lighting
  (Landscape, Path, Solar, MR16 Replacement)

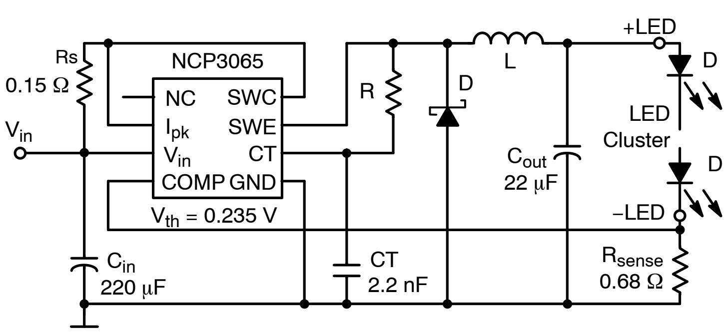


Figure 1. Typical Buck Application Circuit

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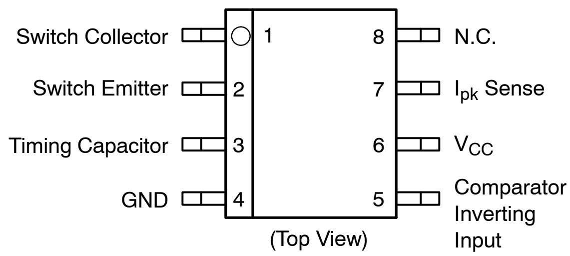


Figure 2. Pin Connections

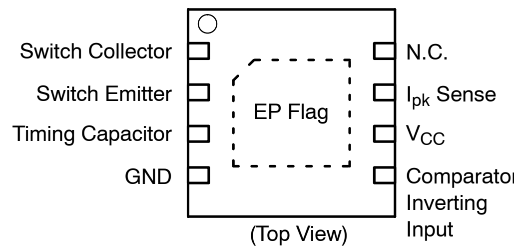


Figure 3. Pin Connections

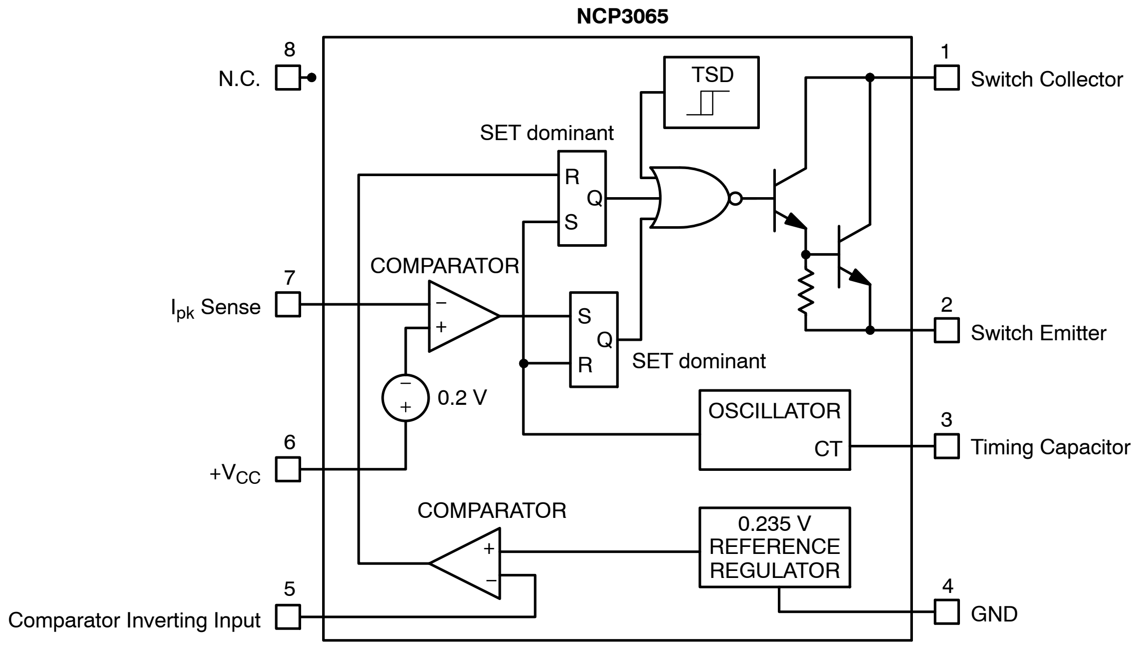


Figure 4. Block Diagram

PIN DESCRIPTION

Pin No.	Pin Name	Description
1	Switch Collector	Internal Darlington switch collector
2	Switch Emitter	Internal Darlington switch emitter
3	Timing Capacitor	Timing Capacitor Oscillator Input, Timing Capacitor
4	GND	Ground pin for all internal circuits
5	Comparator Inverting Input	Inverting input pin of internal comparator
6	V_{CC}	Voltage supply
7	I_{pk} Sense	Peak Current Sense Input to monitor the voltage drop across an external resistor to limit the peak current through the circuit
8	N.C.	Pin not connected

MAXIMUM RATINGS (measured vs. pin 4, unless otherwise noted)

Rating	Symbol	Value	Unit
V_{CC} (Pin 6)	V_{CC}	0 to +40	V
Comparator Inverting Input (Pin 5)	V_{CII}	−0.2 to $+V_{CC}$	V
Darlington Switch Collector (Pin 1)	V_{SWC}	0 to +40	V
Darlington Switch Emitter (Pin 2) (Transistor OFF)	V_{SWE}	−0.6 to $+V_{CC}$	V
Darlington Switch Collector to Emitter (Pins 1−2)	V_{SWCE}	0 to +40	V
Darlington Switch Current	I_{SW}	1.5	A
I_{pk} Sense (Pin 7)	V_{IPK}	−0.2 to V_{CC} + 0.2	V
Timing Capacitor (Pin 3)	V_{TCAP}	−0.2 to +1.4	V
Power Dissipation and Thermal Characteristics			
SOIC−8 Thermal Resistance Junction−to−Air	$R_{\theta JA}$	180	°C/W
DFN−8 Thermal Resistance Junction−to−Air Thermal Resistance Junction−to−Case	$R_{\theta JA}$ $R_{\theta JC}$	78 14	°C/W
Storage Temperature Range	T_{STG}	−65 to +150	°C
Maximum Junction Temperature	$T_{J(MAX)}$	+150	°C
Operating Junction Temperature Range (Note 3) NCP3065, NCV3065	T_J	−40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Pin 1−8: Human Body Model 2000 V per AEC Q100−002; 003 or JESD22/A114; A115
   Machine Model Method 200 V
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.
3. The relation between junction temperature, ambient temperature and Total Power dissipated in IC is $T_J = T_A + R_\theta \bullet P_D$
4. The pins which are not defined may not be loaded by external signals

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V, T_J = −40°C to +125°C, unless otherwise specified)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
OSCILLATOR						
Frequency	(VPin 5 = 0 V, CT = 2.2 nF, T_J = 25°C)	f_{OSC}	110	150	190	kHz
Discharge to Charge Current Ratio	(Pin 7 to V_{CC}, T_J = 25°C)	I_{DISCHG} / I_{CHG}	5.5	6.0	6.5	–
Capacitor Discharging Current	(Pin 7 to V_{CC}, T_J = 25°C)	I_{DISCHG}		1650		μA
Capacitor Charging Current	(Pin 7 to V_{CC}, T_J = 25°C)	I_{CHG}		275		μA
Current Limit Sense Voltage	(T_J = 25°C) (Note 6)	$V_{IPK(Sense)}$	165	185	235	mV
OUTPUT SWITCH (Note 5)						
Darlington Switch Collector to Emitter Voltage Drop	(I_{SW} = 1.0 A, T_J = 25°C) (Note 5)	$V_{SWCE(DROP)}$		1.0	1.3	V
Collector Off−State Current	(V_{CE} = 40 V)	$I_{C(OFF)}$		0.01	100	μA
COMPARATOR						
Threshold Voltage	T_J = 25°C	V_{TH}		235		mV
	T_J = 0 to +85°C			±5		%
	T_J = −40°C to +125°C	V_{TH}	−10		+10	%
Threshold Voltage Line Regulation	(V_{CC} = 3.0 V to 40 V)	REG_{LiNE}	−6.0		6.0	mV
Input Bias Current	(V_{in} = V_{th})	$I_{CII\ in}$	−1000	−100	1000	nA
TOTAL DEVICE						
Supply Current	(V_{CC} = 5.0 V to 40 V, CT = 2.2 nF, Pin 7 = V_{CC}, VPin 5 > V_{th}, Pin 2 = GND, remaining pins open)	I_{CC}			7.0	mA
Thermal Shutdown Threshold				160		°C
Hysteresis				10		°C

5. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient temperature as possible.
6. The $V_{IPK(Sense)}$ Current Limit Sense Voltage is specified at static conditions. In dynamic operation the sensed current turn−off value depends on comparator response time and di/dt current slope. See the Operating Description section for details.
7. NCV prefix is for automotive and other applications requiring site and change control.

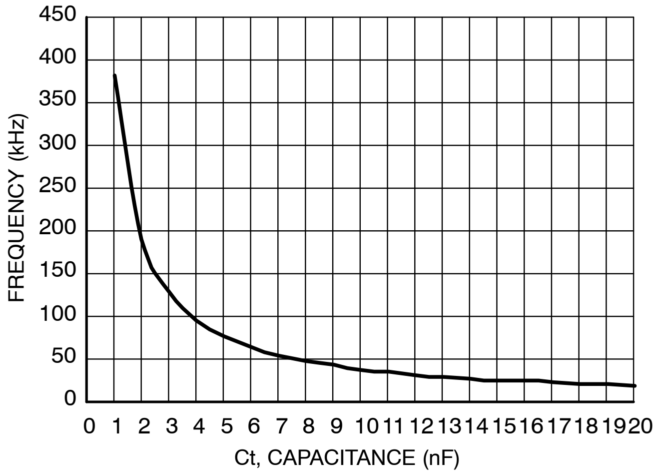


Figure 5. Oscillator Frequency vs. Oscillator Timing Capacitor

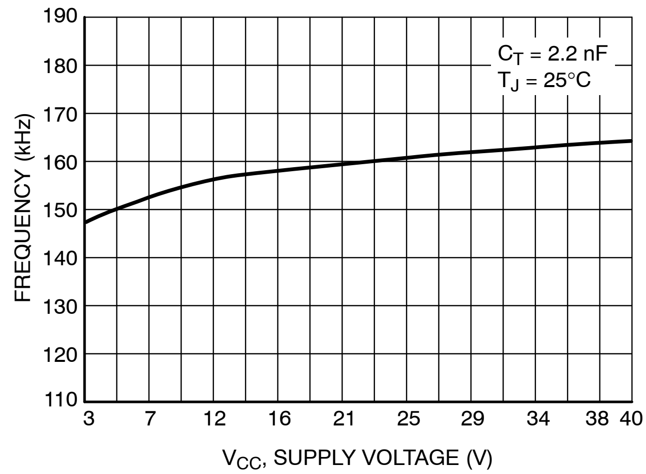


Figure 6. Oscillator Frequency vs. Supply Voltage

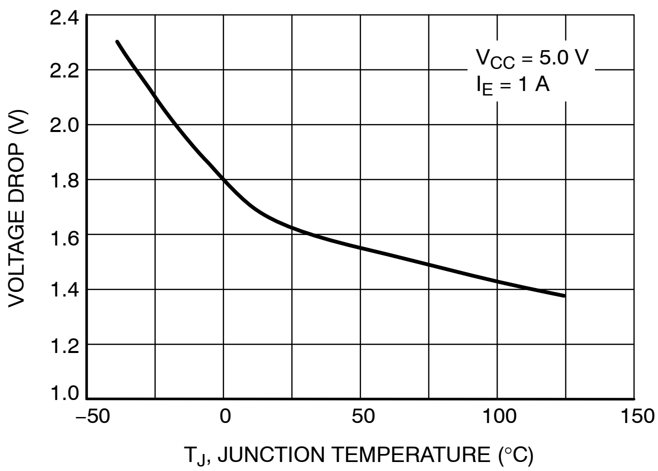


Figure 7. Emitter Follower Configuration Output Darlington Switch Voltage Drop vs. Temperature

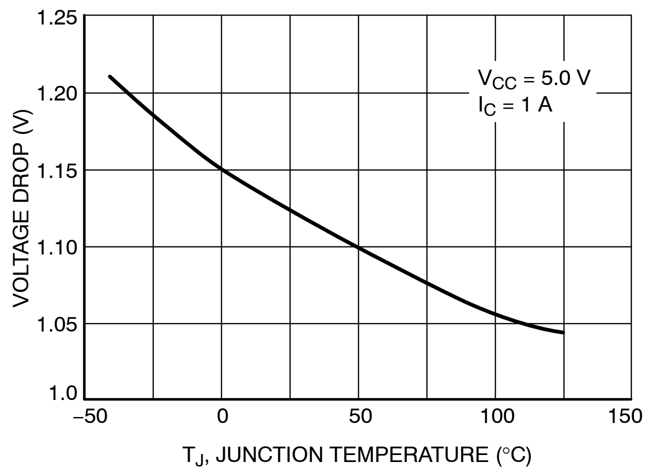


Figure 8. Common Emitter Configuration Output Darlington Switch Voltage Drop vs. Temperature

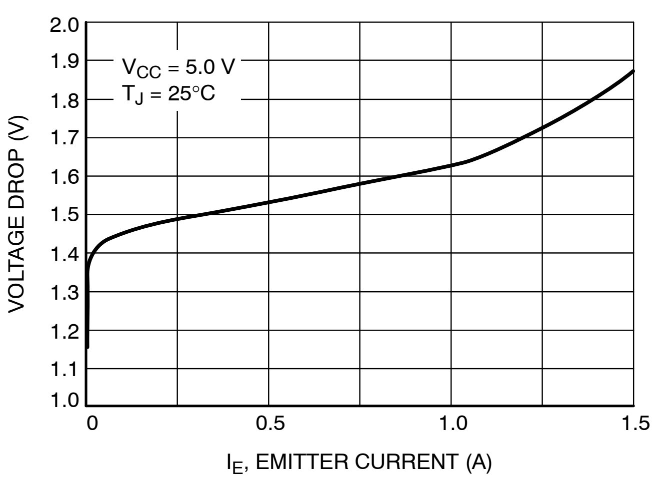


Figure 9. Emitter Follower Configuration Output Darlington Switch Voltage Drop vs. Emitter Current

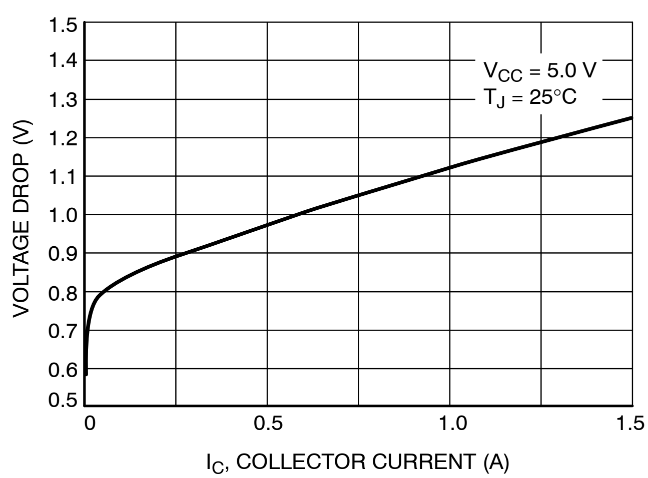


Figure 10. Common Emitter Configuration Output Darlington Switch Voltage Drop vs. Collector Current

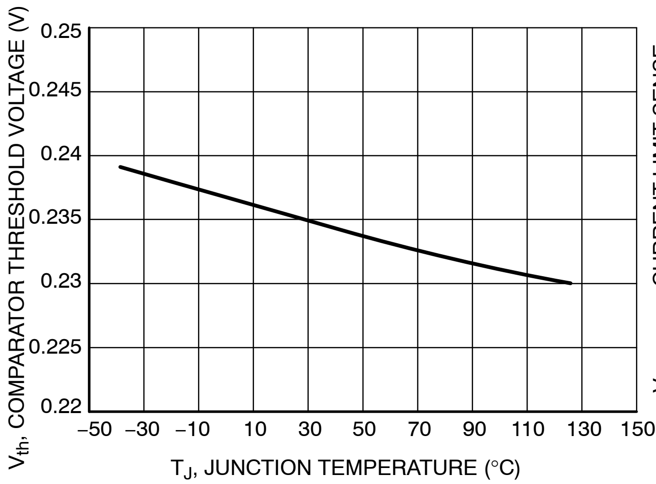


Figure 11. Comparator Threshold Voltage vs. Temperature

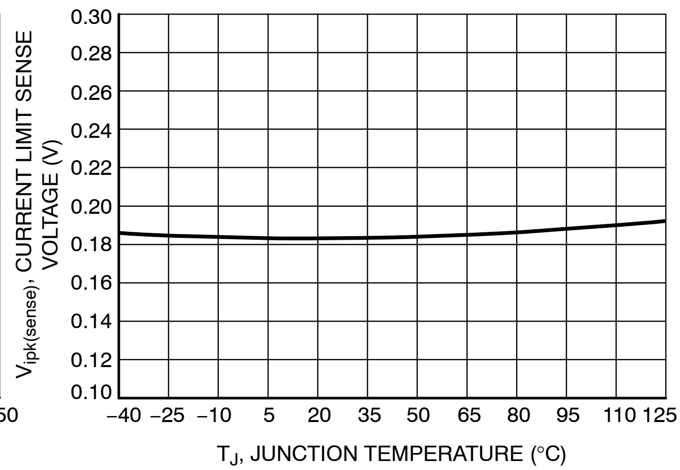


Figure 12. Current Limit Sense Voltage vs. Temperature

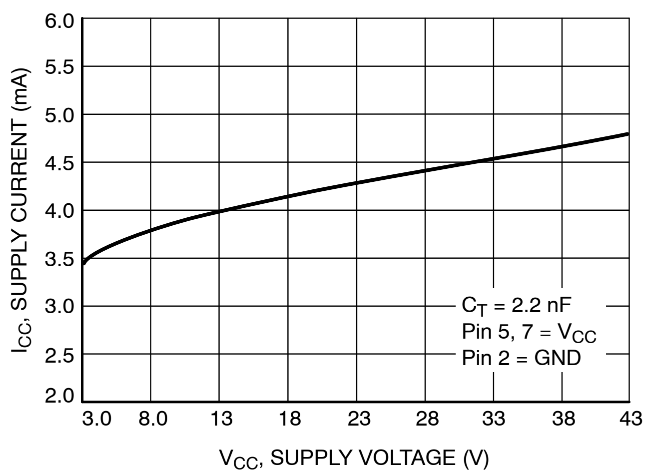


Figure 13. Standby Supply Current vs. Supply Voltage

INTRODUCTION

The NCP3065 is a monolithic power switching regulator optimized for LED Driver applications. Its flexible architecture enables the system designer to directly implement a step−up or step−down topology with a minimum number of external components for driving LEDs. A representative block diagram is shown in Figure 4.

OPERATING DESCRIPTION

The NCP3065 operates as a fixed oscillator frequency output voltage ripple gated regulator. In general, this mode of operation is somewhat analogous to a capacitor charge pump and does not require dominant pole loop compensation for converter stability. The typical operating waveforms are shown in Figure 14. The output voltage waveform shown is for a step−down converter with the ripple and phasing exaggerated for clarity. During initial converter startup, the feedback comparator senses that the output voltage level is below nominal. This causes the output switch to turn on and off at a frequency and duty cycle controlled by the oscillator, thus pumping up the output filter capacitor. When the feedback voltage level reaches nominal comparator value, the output switch cycle is inhibited. When the load current causes the output voltage to fall below the nominal value feedback comparator enables switching immediately. Under these conditions, the output switch conduction can be enabled for a partial oscillator cycle, a partial cycle plus a complete cycle, multiple cycles, or a partial cycle plus multiple cycles.

Oscillator

The oscillator frequency and off−time of the output switch are programmed by the value of the timing capacitor C_T. Capacitor C_T is charged and discharged by a 1 to 6 ratio internal current source and sink, generating a positive going sawtooth waveform at Pin 3. This ratio sets the maximum $t_{ON}/(t_{ON}+t_{OFF})$ of the switching converter as 6/(6+1) or 85.7% (typical). The oscillator peak and valley voltage difference is 500 mV typically. To calculate the C_T capacitor value for required oscillator frequency, use the equations found in Figure 22. An online NCP3065 design tool can be found at www.onsemi.com, which adds in selecting component values.

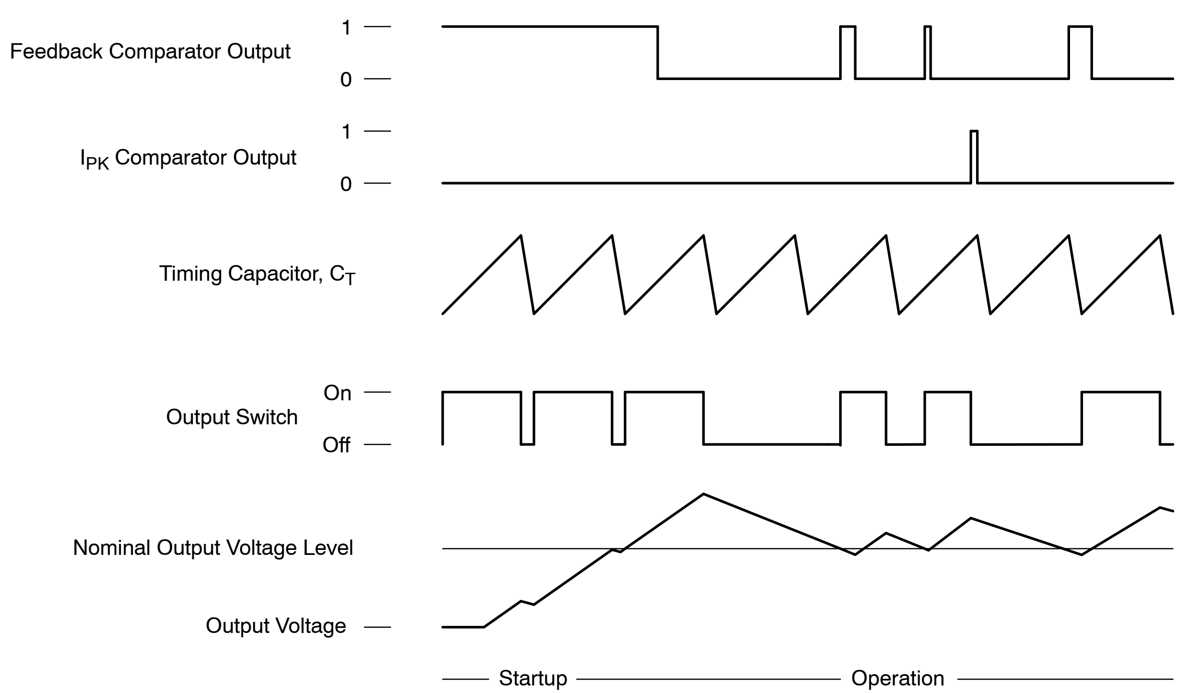
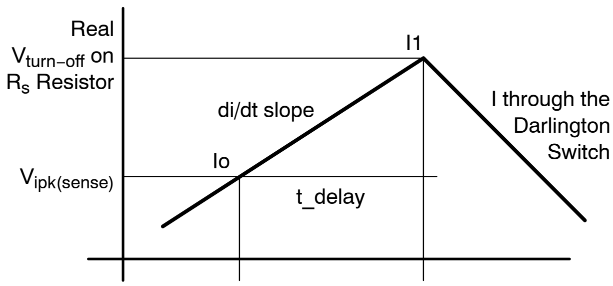


Figure 14. Typical Operating Waveforms

Peak Current Sense Comparator

Under normal conditions, the output switch conduction is initiated by the Voltage Feedback comparator and terminated by the oscillator. Abnormal operating conditions occur when the converter output is overloaded or when feedback voltage sensing is lost. Under these conditions, the I_{pk} Current Sense comparator will protect the Darlington output Switch. The switch current is converted to a voltage by inserting a fractional ohm resistor, R_{SC}, in series with V_{CC} and the Darlington output switch. The voltage drop across R_{SC} is monitored by the Current Sense comparator. If the voltage drop exceeds 200 mV (nom) with respect to V_{CC}, the comparator will set the latch and terminate the output switch conduction on a cycle−by−cycle basis. This Comparator/Latch configuration ensures that the Output Switch has only a single on−time during a given oscillator cycle.



The $V_{IPK(Sense)}$ Current Limit Sense Voltage threshold is specified at static conditions. In dynamic operation the sensed current turn−off value depends on comparator response time and di/dt current slope.

Real $V_{turn-off}$ on R_{sc} resistor

$$V_{turn\_off} = V_{ipk(sense)} + Rsc \cdot (t\_delay \cdot di/dt)$$

Typical I_{pk} comparator response time t_delay is 350 ns. The di/dt current slope is dependent on the voltage difference across the inductor and the value of the inductor. Increasing the value of the inductor will reduce the di/dt slope.

It is recommended to verify the actual peak current in the application at worst conditions to be sure that the max peak current will never get over the 1.5 A Darlington Switch Current max rating.

Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. When activated, typically at 165°C, the Darlington Output Switch is disabled. The temperature sensing circuit is designed with some hysteresis. The Darlington Switch is enabled again when the chip temperature decreases under the low threshold. This feature is provided to prevent catastrophic failures from accidental device overheating. It is not intended to be used as a replacement for proper heatsinking.

LED Dimming

The COMP pin of the NCP3065 is used to provide dimming capability. In digital input mode the PWM input signal inhibits switching of the regulator and reduces the average current through the LEDs. In analog input mode a PWM input signal is RC filtered and the resulting voltage is summed with the feedback voltage thus reduces the average current through the LEDs. Figure 15 illustrated the linearity of the digital dimming function with a 200 Hz digital PWM. For further information on dimming control refer to application note AND8298.

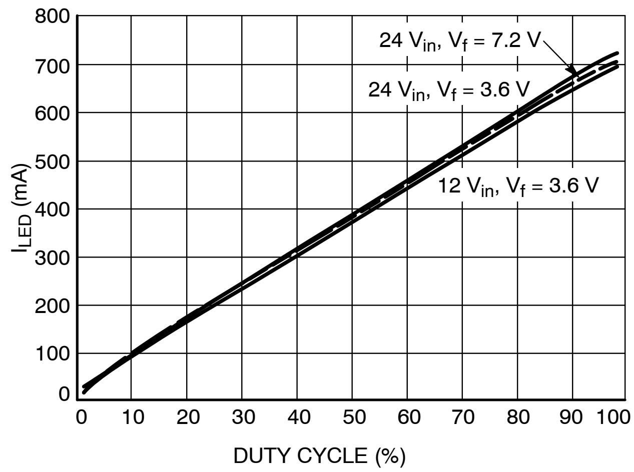


Figure 15.

No Output Capacitor Operation

A constant current buck regulator such as the NCP3065 focuses on the control of the current through the load, not the voltage across it. The switching frequency of the NCP3065 is in the range of 100−250 kHz which is much higher than the human eye can detect. This allows us to relax the ripple current specification to allow higher peak to peak values. This is achieved by configuring the NCP3065 in a continuous conduction buck configuration with low peak to peak ripple thus eliminating the need for an output filter capacitor. The important design parameter is to keep the peak current below the maximum current rating of the LED. Using 15% peak to peak ripple results in a good compromise between achieving max average output current without exceeding the maximum limit. This saves space and reduces part count for applications that require a compact footprint. (Example: See Figure 17) See application note AND8298 for more information.

Output Switch

The output switch is designed in a Darlington configuration. This allows the application designer to operate at all conditions at high switching speed and low voltage drop. The Darlington Output Switch is designed to switch a maximum of 40 V collector to emitter voltage and current up to 1.5 A.

APPLICATIONS

Figures 16 through 24 show the simplicity and flexibility of the NCP3065. Two main converter topologies are demonstrated with actual test data shown below each of the circuit diagrams.

Figure 16 gives the relevant design equations for the key parameters. Additionally, a complete application design aid for the NCP3065 can be found at www.onsemi.com.

(See Notes 8, 9, 10)	Step−Down	Step−Up
$\frac{t_{on}}{t_{off}}$	$\frac{V_{out} + V_F}{V_{in} - V_{SWCE} - V_{out}}$	$\frac{V_{out} + V_F - V_{in}}{V_{in} - V_{SWCE}}$
t_{on}	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$	$\frac{\frac{t_{on}}{t_{off}}}{f\left(\frac{t_{on}}{t_{off}} + 1\right)}$
C_T	$C_T = \frac{381.6 \cdot 10^{-6}}{f_{osc}} - 343 \cdot 10^{-12}$	
$I_{L(avg)}$	I_{out}	$I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$
$I_{pk\,(Switch)}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$	$I_{L(avg)} + \frac{\Delta I_L}{2}$
R_{SC}	$\frac{0.20}{I_{pk\,(Switch)}}$	$\frac{0.20}{I_{pk\,(Switch)}}$
L	$\left(\frac{V_{in} - V_{SWCE} - V_{out}}{\Delta I_L}\right) t_{on}$	$\left(\frac{V_{in} - V_{SWCE}}{\Delta I_L}\right) t_{on}$
$V_{ripple(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 f C_O}\right)^2 + (ESR)^2}$	$\approx \frac{t_{on} I_{out}}{C_O} + \Delta I_L \cdot ESR$
V_{out}	$V_{TH}\left(\frac{R_2}{R_1} + 1\right)$	$V_{TH}\left(\frac{R_2}{R_1} + 1\right)$
I_{out}	V_{ref}/R_{sense}	V_{ref}/R_{sense}

8. V_{SWCE} − Darlington Switch Collector to Emitter Voltage Drop, refer to Figures 7, 8, 9 and 10.
9. V_F − Output rectifier forward voltage drop. Typical value for 1N5819 Schottky barrier rectifier is 0.4 V.
10. The calculated t_{on}/t_{off} must not exceed the minimum guaranteed oscillator charge to discharge ratio.

Figure 16. Design Equations

The Following Converter Characteristics Must Be Chosen:

V_{in} − Nominal operating input voltage.

V_{out} − Desired output voltage.

I_{out} − Desired output current.

ΔI_L − Desired peak−to−peak inductor ripple current. For maximum output current it is suggested that ΔI_L be chosen to be less than 10% of the average inductor current $I_{L(avg)}$. This will help prevent $I_{pk\,(Switch)}$ from reaching the current limit threshold set by R_{SC}. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2(I_{L(avg)})$. This will proportionally reduce converter output current capability.

f − Maximum output switch frequency.

$V_{ripple(pp)}$ − Desired peak−to−peak output ripple voltage. For best performance the ripple voltage should be kept to a low value since it will directly affect line and load regulation. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

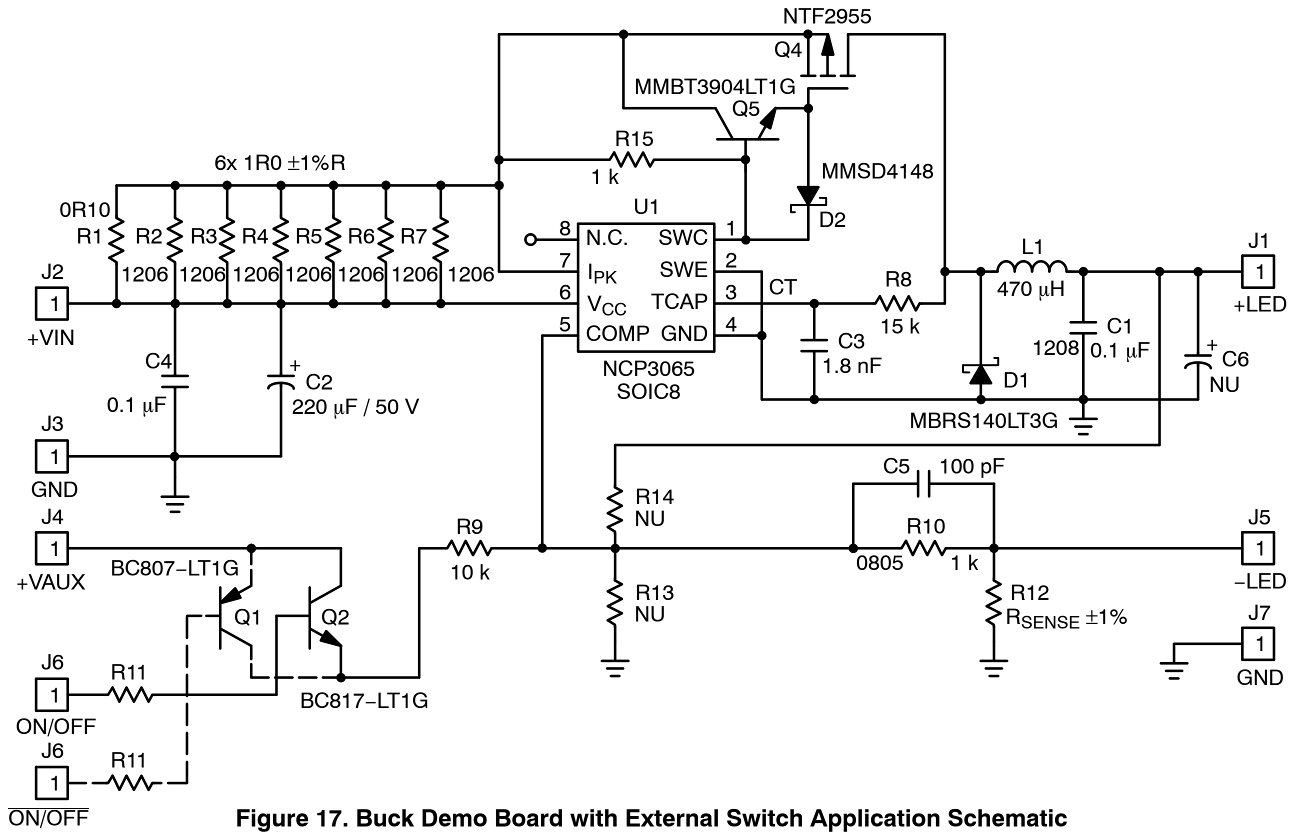


Figure 17. Buck Demo Board with External Switch Application Schematic

This design illustrates the NCP3065 being used as a PFET controller, the design has been optimized for continuous current operation with low ripple which allows the output filter capacitor to be eliminated. Figure 20 illustrates the efficiency with 1 and 2 LEDs and output currents of 350 mA and 700 mA. Additional data and design information can be found of this design in Application Note AND8298.

Value of Components

Name	Value
C1, C4	100 nF, Ceramic Capacitor, 1206
C2	220 µF, 50 V, Electrolytic Capacitor
C3	1.8 nF, Ceramic Capacitor, 0805
C5	100 pF, Ceramic Capacitor, 0805
D1	1 A, 40 V Schottky Rectifier
D2	MMSD4148
L1	470 µH, DO5022P−474ML Coilcraft Inductor
Q4	NTF2955, P−MOSFET, SOT223

Name	Value
Q5	MMBT3904LT1G, SOT23
R1	100 mΩ, 0.5 W
R8	15 k, resistor 0805
R9	10 kΩ, resistor 0805
R10, R15	1 kΩ, resistor 0805
R11	1.2 kΩ, resistor 0805
R12	R_{SENSE} ±1%, 1206
U1	NCP3065, SOIC8

NOTE: R_{SENSE} is used to select LED output current, for 350 mA use 680 mΩ, for 700 mA use 330 mΩ and for 1000 mA use 220 mΩ

Test Results (without output capacitor)

Test	Condition	Results
Line Regulation	V_{in} = 9 V to 19 V, I_o = 350 mA	12 mA
Load Regulation	V_{in} = 12 V, I_o = 350 mA, V_o = 3 V to 8 V	13 mA
Output Ripple	V_{in} = 9 V to 19 V, I_o = 350 mA	< 15% I_O
Efficiency	V_{in} = 12 V, I_o = 350 mA, V_{OUT} = 3 to 8 V	> 75%

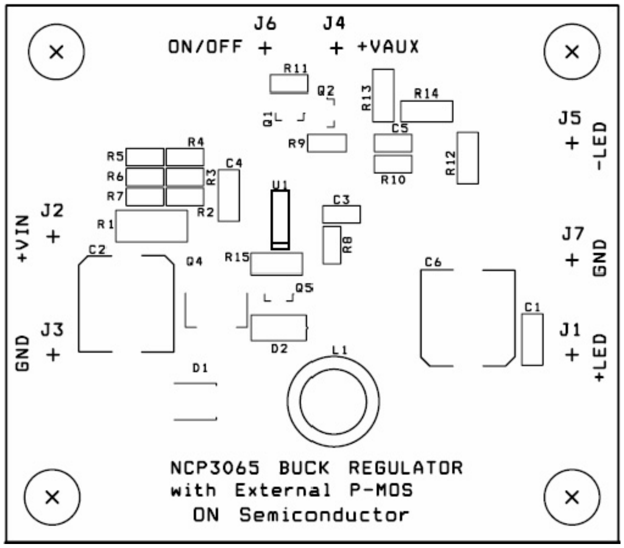


Figure 18. 1.5 A Buck Demoboard Layout

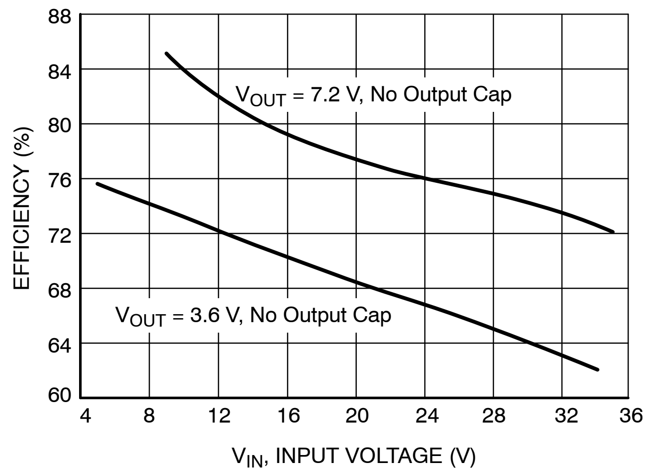


Figure 19. Efficiency vs. Input Voltage for the 1.5 A Buck Demo Board at I_{out} = 700 mA, T_A = 25°C, Without Output Capacitor

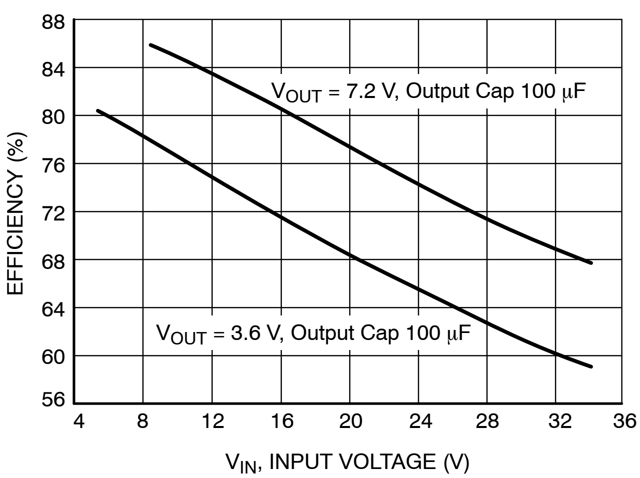


Figure 20. Efficiency vs. Input Voltage for the 1.5 A Buck Demo Board at I_{out} = 350 mA, T_A = 25°C, with 100 μF Output Capacitor

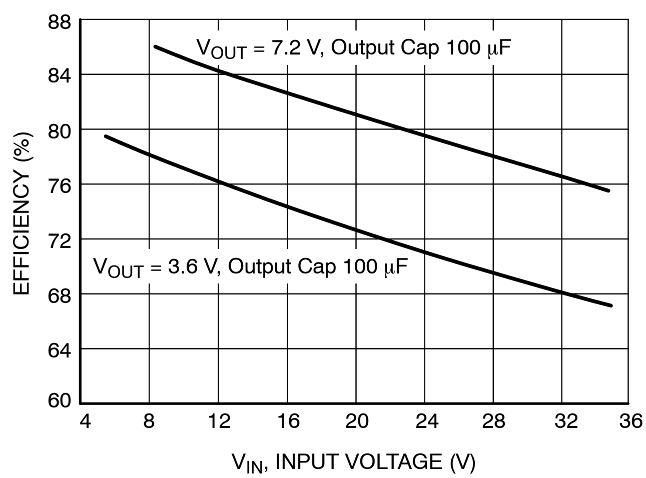


Figure 21. Efficiency vs. Input Voltage for the 1.5 A Buck Demo Board at I_{out} = 700 mA, T_A = 25°C, with 100 μF Output Capacitor

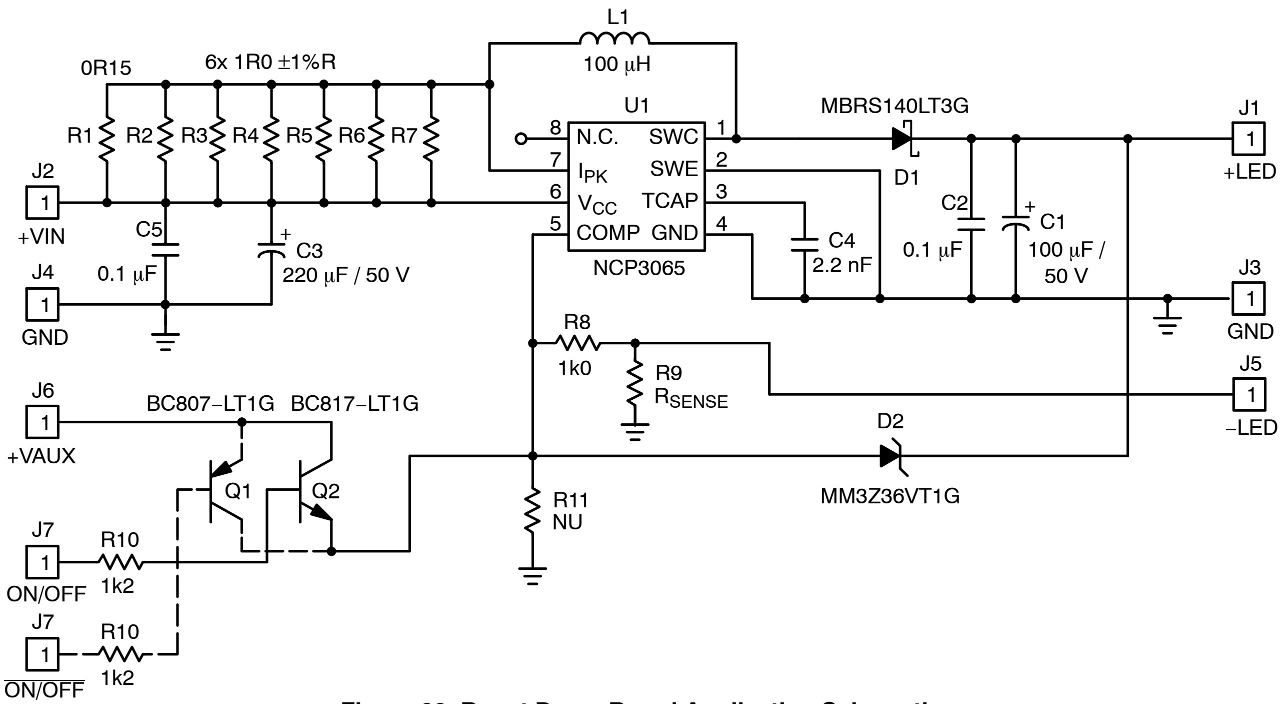


Figure 22. Boost Demo Board Application Schematic

Value of Components

Name	Value
C1	100 μF/50 V, Electrolytic Capacitor
C2, C5	100 nF, Ceramic Capacitor, 1206
C3	220 μF/50 V, Electrolytic Capacitor
C4	2.2 nF, Ceramic Capacitor, 0805
D1	MBRS140LT3G, Schottky diode
D2	MMSZ36VT1G, Zener diode
L1	100 μH, DO3340P−104ML Coilcraft Inductor

Name	Value
Q2	BC817−LT1G, SOT23
R1	150 mΩ, resistor 0.5 W
R8	1 k, resistor 0805
R9	Load current sense resistor, 1206
R10	1.2 k, resistor 0805
U1	NCP3065, SOIC8

Test Results

Test	Condition	Results
Line Regulation	V_{in} = 10 V to 20 V, V_o = 22 V, I_{OAVG} = 350 mA	25 mA
Output Ripple	V_{in} = 8 V to 20 V, V_o = 22 V, I_{OAVG} = 350 mA	50 mA
Efficiency	V_{in} = 10 to 20 V, I_{OAVG} = 350 mA	> 83 %

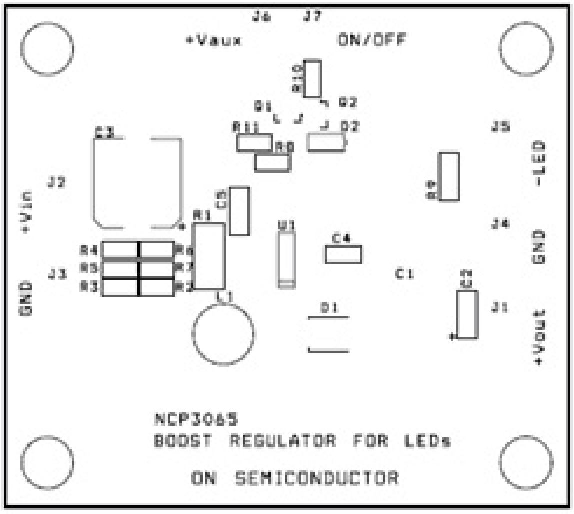


Figure 23. Boost Demoboard Layout

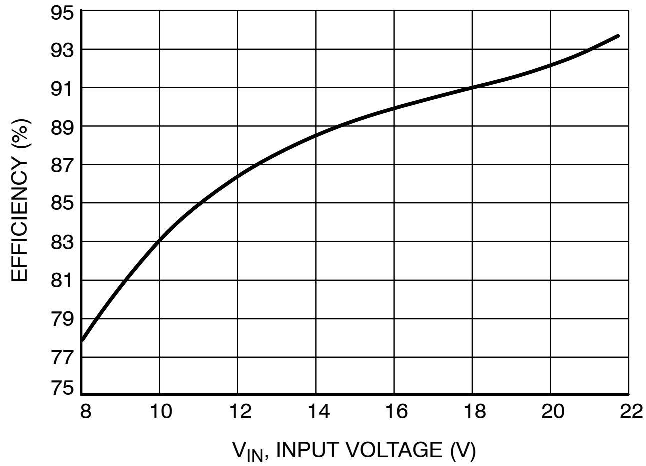


Figure 24. Efficiency vs. Input Voltage for the Boost Demo Board at I_{OUT} = 350 mA, V_{OUT} = 22 V (6xLED with V_F = 3.6 V), T_A = 25°C

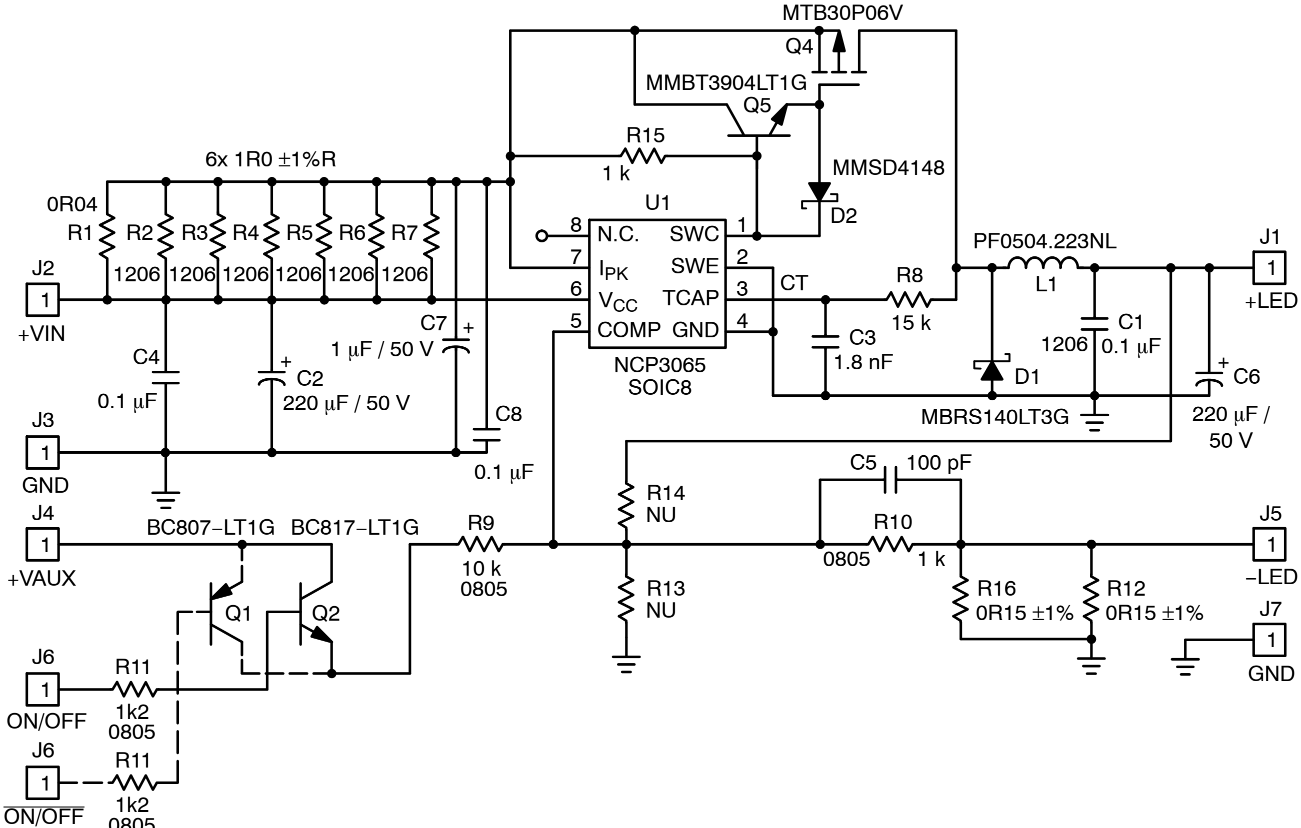


Figure 25. Buck Demoboard with External Switch Application Schematic

Value of Components

Name	Value
C1	100 µF, 50 V, Electrolytic Capacitor
C1, C4, C8	100 nF, Ceramic Capacitor, 1206
C2, C6	220 µF, 50 V, Electrolytic Capacitor
C3	2.2 nF, Ceramic Capacitor, 0805
C5	100 pF, Ceramic Capacitor, 0805
C7	1 µF / 50 V, Ceramic Capacitor, 1206
D1	MBRS540LT3G, Schottky Diode
D2	MMSD4148T1G, Diode
L1	22 µH
Q2	BC817−LT1G, SOT23

Name	Value
Q4	MTB30P06V, P−MOS transistor
Q5	MMBT3904LT1G
R1	40 mΩ, Resistor 0.5 W
R8	6k8, Resistor 0805
R9	10k, Resistor 0805
R10	1k, Resistor 0805
R11	1k2, Resistor 0805
R12, R16	150 mΩ, Resistor 0.5 W
U1	NCP3065, SOIC8

Test Results

Test	Condition	Results
Line Regulation	V_{in} = 8 V to 19 V, I_o = 3000 mA	< 6%
Output Ripple	V_{in} = 12 V, I_o = 3000 mA	< 6%
Efficiency	V_{in} = 12 V, I_o = 3000 mA	> 78%
Short Circuit Current	V_{in} = 12 V, Rload = 0.15 Ω	

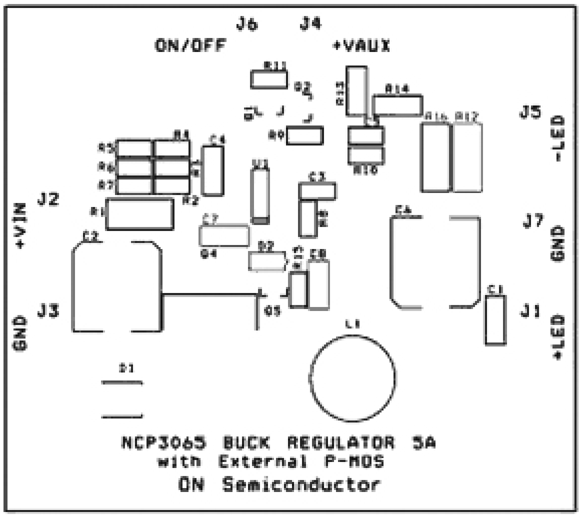


Figure 26. 3 A Buck Demoboard Layout

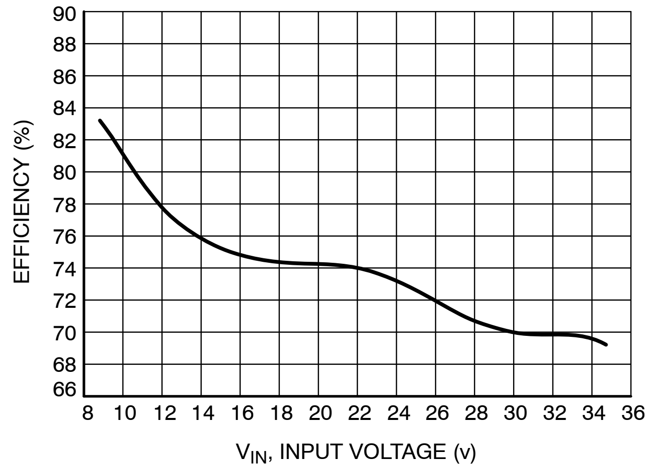
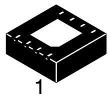


Figure 27. Efficiency vs. Input Voltage for the 3 A Buck Demo Board at I_{OUT} = 3 A, V_{OUT} = 4 V, T_A = 25°C

ORDERING INFORMATION

Device	Package	Shipping†
NCP3065MNTXG	DFN−8 (Pb−Free)	4000 Units / Tape & Reel
NCP3065DR2G	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel
NCV3065MNTXG*	DFN−8 (Pb−Free)	4000 Units / Tape & Reel
NCV3065DR2G*	SOIC−8 (Pb−Free)	2500 Units / Tape & Reel

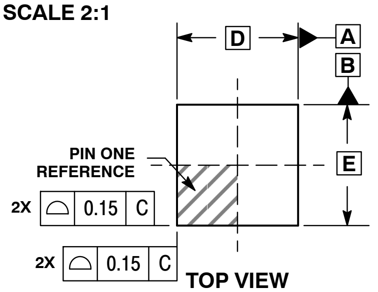
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements.



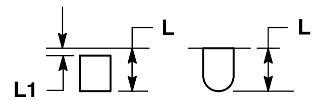
SCALE 2:1

DFN8, 4x4
CASE 488AF
ISSUE C

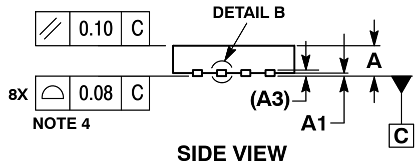
DATE 15 JAN 2009



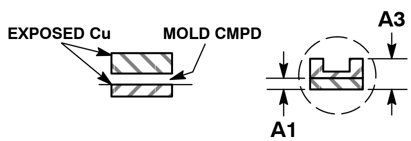
TOP VIEW



DETAIL A
OPTIONAL CONSTRUCTIONS



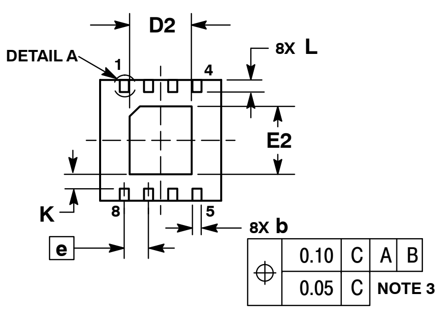
SIDE VIEW



DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DETAILS A AND B SHOW OPTIONAL CONSTRUCTIONS FOR TERMINALS.

	MILLIMETERS	
DIM	**MIN**	**MAX**
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	1.91	2.21
E	4.00 BSC	
E2	2.09	2.39
e	0.80 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15



BOTTOM VIEW

GENERIC MARKING DIAGRAM*

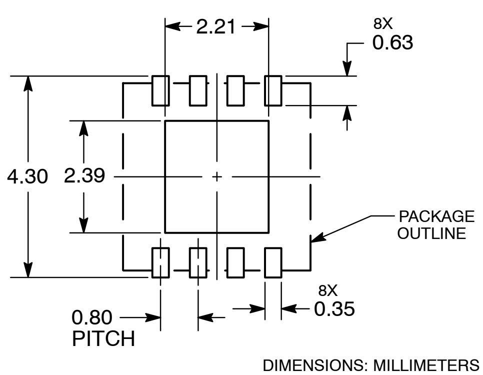
XXXXXX
XXXXXX
ALYW▪
▪

XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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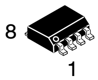
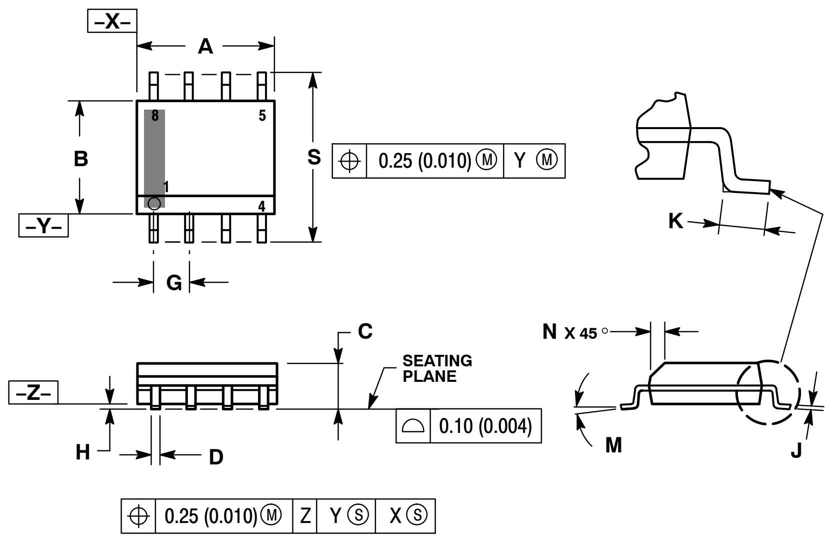


SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

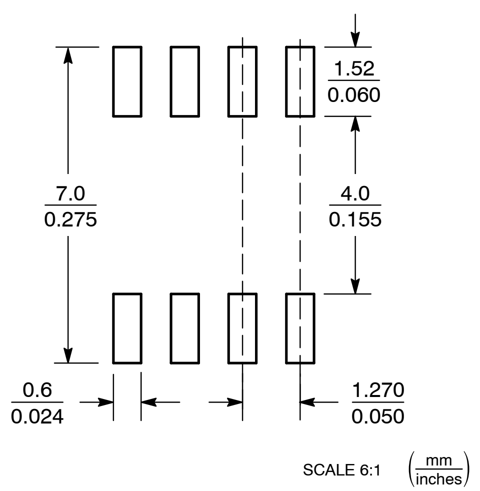
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

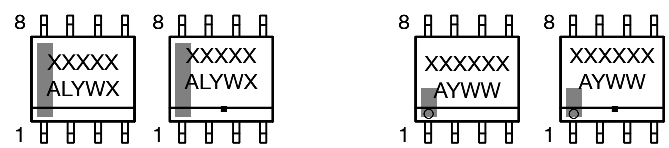
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC **IC (Pb−Free)** **Discrete** **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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