

## Triple Schmitt-Trigger Inverter

Check for Samples: [SN74LVC3G14](#)

### FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.4 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Max  $I_{cc}$
- $\pm 24$ -mA Output Drive at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ C$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ C$
- $I_{off}$  Feature Supports Live Insertion, Partial-Power-Down Mode and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

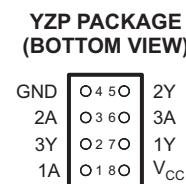
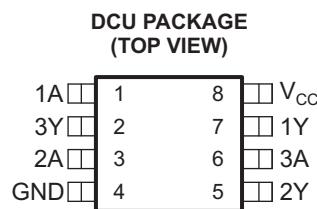
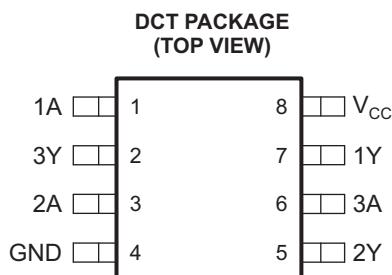
### DESCRIPTION

This triple Schmitt-trigger inverter is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC3G14 contains three inverters and performs the Boolean function  $Y = \bar{A}$ . The device functions as three independent inverters but, because of Schmitt action, it may have different input threshold levels for positive-going ( $V_{T+}$ ) and negative-going ( $V_{T-}$ ) signals.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



See mechanical drawings for dimensions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

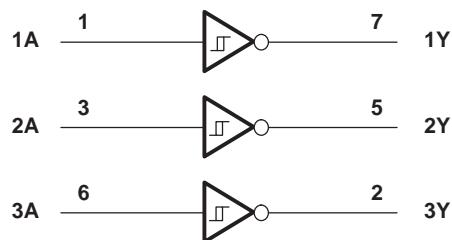


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Function Table  
(Each Inverter)**

INPUT A	OUTPUT Y
H	L
L	H

**Logic Diagram (Positive Logic)**



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current		$\pm 50$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 100$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DCT package	220	°C/W
		DCU package	227	
		YZP package	102	
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		-4	mA
		V <sub>CC</sub> = 2.3 V		-8	
		V <sub>CC</sub> = 3 V		-16	
		V <sub>CC</sub> = 4.5 V		-24	
		V <sub>CC</sub> = 4.5 V		-32	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4	mA
		V <sub>CC</sub> = 2.3 V		8	
		V <sub>CC</sub> = 3 V		16	
		V <sub>CC</sub> = 4.5 V		24	
		V <sub>CC</sub> = 4.5 V		32	
T <sub>A</sub>	Operating free-air temperature		-40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	-40°C to 85°C			-40°C to 125°C			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
V <sub>T+</sub> Positive-going input threshold voltage		1.65 V	0.7	1.4	0.7	1.4			V
		2.3 V	1	1.7	1	1.7			
		3 V	1.3	2.2	1.3	2.2			
		4.5 V	1.9	3.1	1.9	3.1			
		5.5 V	2.2	3.7	2.2	3.7			
V <sub>T-</sub> Negative-going input threshold voltage		1.65 V	0.3	0.7	0.3	0.7			V
		2.3 V	0.4	1	0.4	1			
		3 V	0.6	1.3	0.6	1.3			
		4.5 V	1.1	2	1.1	2			
		5.5 V	1.4	2.5	1.4	2.5			
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> – V <sub>T-</sub> )		1.65 V	0.3	0.8	0.3	0.8			V
		2.3 V	0.4	0.9	0.4	0.9			
		3 V	0.4	1.1	0.4	1.1			
		4.5 V	0.6	1.3	0.6	1.3			
		5.5 V	0.7	1.4	0.7	1.4			
V <sub>OH</sub>	I <sub>OH</sub> = -100 μA	1.65 V to 4.5 V	V <sub>CC</sub> – 0.1		V <sub>CC</sub> – 0.1				V
	I <sub>OH</sub> = -4 mA	1.65 V		1.2		1.2			
	I <sub>OH</sub> = -8 mA	2.3 V		1.9		1.9			
	I <sub>OH</sub> = -16 mA	3 V		2.4		2.4			
	I <sub>OH</sub> = -24 mA	3 V		2.3		2.3			
	I <sub>OH</sub> = -32 mA	4.5 V		3.8		3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 4.5 V		0.1		0.1			V
	I <sub>OL</sub> = 4 mA	1.65 V		0.45		0.45			
	I <sub>OL</sub> = 8 mA	2.3 V		0.3		0.3			
	I <sub>OL</sub> = 16 mA	3 V		0.4		0.4			
	I <sub>OL</sub> = 24 mA	3 V		0.55		0.75			
	I <sub>OL</sub> = 32 mA	4.5 V		0.55		0.75			
I <sub>I</sub>	A inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±5		±5	μA	
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0		±10		±10	μA	
I <sub>CC</sub>		V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V		10		10	μA	
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND V, <sub>I</sub>	3 V to 5.5 V		500		500	μA	
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		4.5			pF	

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC3G14 -40°C to 85°C						UNIT		
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V				
			MIN	MAX	MIN	MAX	MIN	MAX			
t <sub>pd</sub>	A	Y	3.9	9.2	1.9	5.7	2.3	5.4	1.5	4.3	ns

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

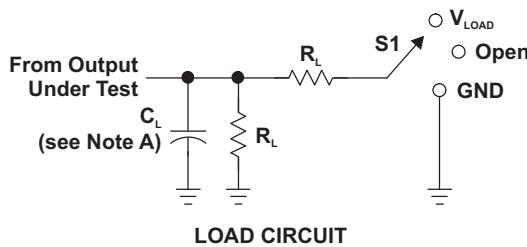
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC3G14 –40°C to 125°C						UNIT		
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V				
			MIN	MAX	MIN	MAX	MIN	MAX			
t <sub>pd</sub>	A	Y	3.9	9.7	1.9	6.2	2.3	5.9	1.5	4.7	ns

## Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT	
		TYP	TYP	TYP	TYP		
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	17	18	19	22	pF

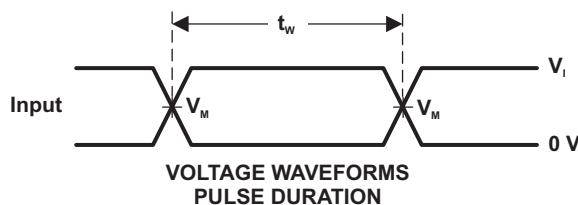
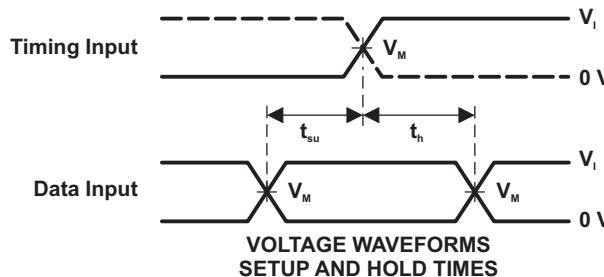
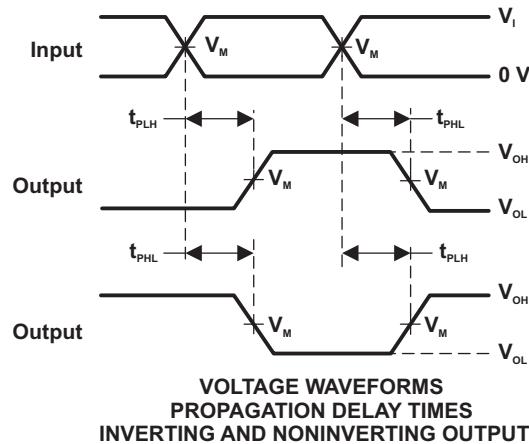
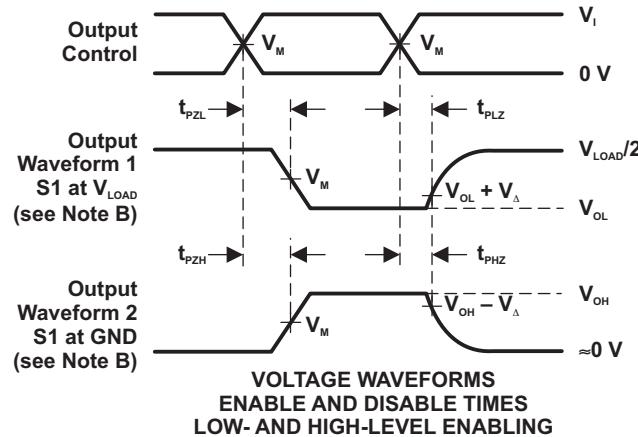
### Parameter Measurement Information



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_\Delta$
	$V_I$	$t_r/t_f$					
$1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC}$	$\leq 2 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3 \text{ V} \pm 0.3 \text{ V}$	3 V	$\leq 2.5 \text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5 \text{ V} \pm 0.5 \text{ V}$	$V_{CC}$	$\leq 2.5 \text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V

VOLTAGE WAVEFORMS  
PULSE DURATIONVOLTAGE WAVEFORMS  
SETUP AND HOLD TIMESVOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTSVOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_o = 50 \Omega$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZH}$  and  $t_{PLZ}$  are the same as  $t_{en}$ .
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## REVISION HISTORY

<b>Changes from Revision I (February 2007) to Revision J</b>	<b>Page</b>
• Updated document to new TI data sheet format. ....	1
• Added ESD warning. ....	2
• Updated operating temperature range. ....	3

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC3G14DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14Z	Samples
SN74LVC3G14DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14Z	Samples
SN74LVC3G14DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14Z	Samples
SN74LVC3G14DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	(14 ~ C14Q ~ C14R) (CR ~ CZ)	Samples
SN74LVC3G14DCURE4	ACTIVE	US8	DCU	8		TBD	Call TI	Call TI	-40 to 125		Samples
SN74LVC3G14DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14R	Samples
SN74LVC3G14DCUT	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 125	(C14Q ~ C14R) CR	Samples
SN74LVC3G14DCUTE4	ACTIVE	US8	DCU	8		TBD	Call TI	Call TI	-40 to 125		Samples
SN74LVC3G14DCUTG4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	C14R	Samples
SN74LVC3G14YZPR	ACTIVE	DSBGA	YZP	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	(CF7 ~ CFN)	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

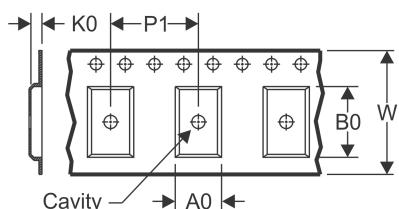
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

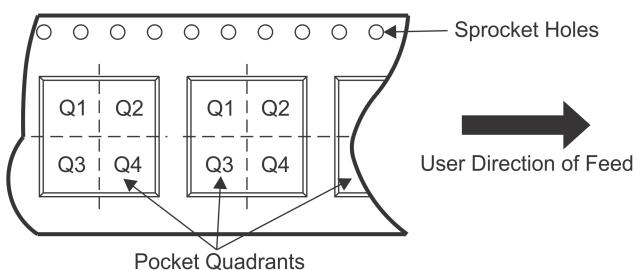
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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC3G14DCUR	US8	DCU	8	3000	180.0	9.0	2.05	3.3	1.0	4.0	8.0	Q3
SN74LVC3G14DCURG4	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC3G14YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

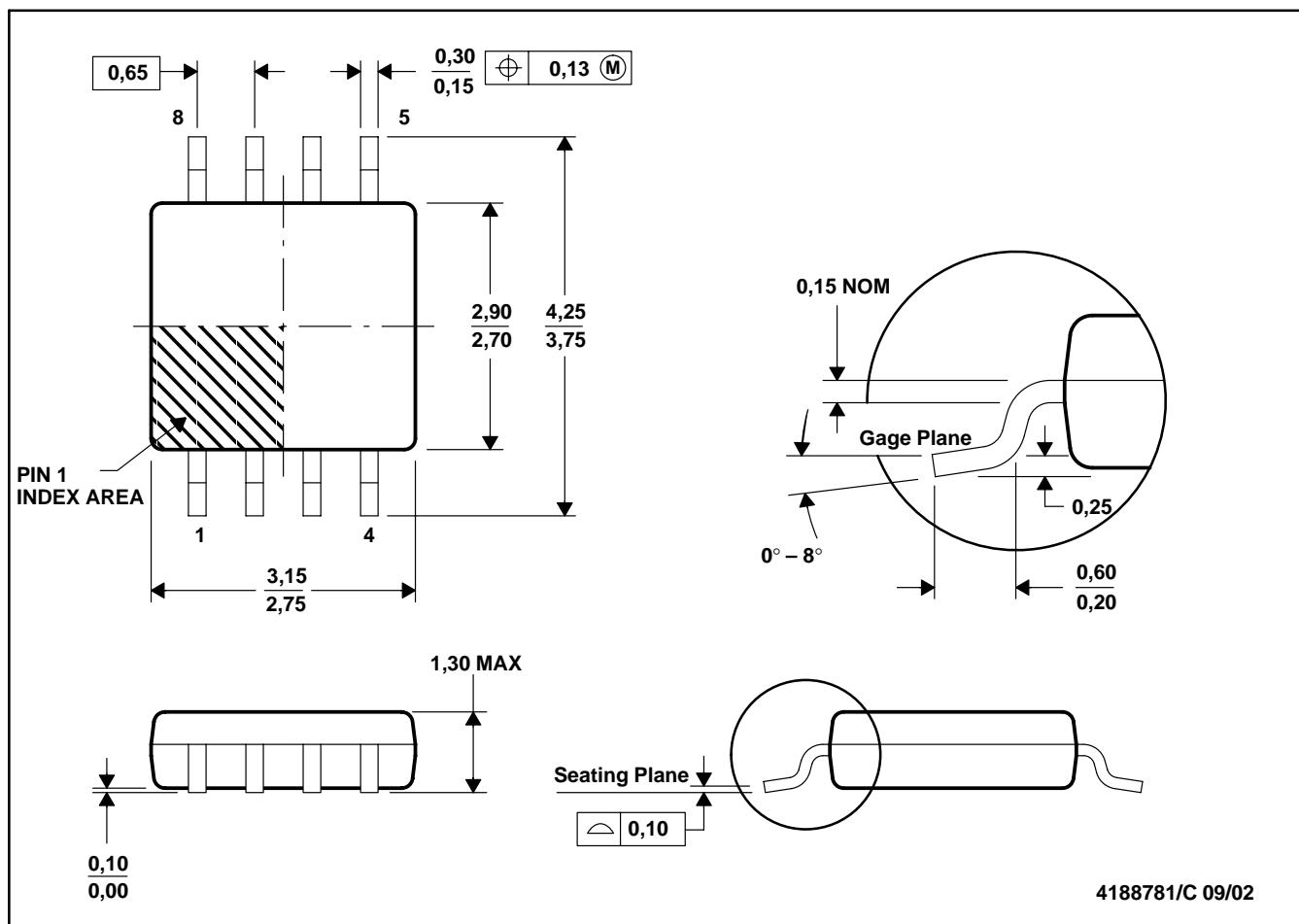
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC3G14DCUR	US8	DCU	8	3000	182.0	182.0	20.0
SN74LVC3G14DCURG4	US8	DCU	8	3000	202.0	201.0	28.0
SN74LVC3G14YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0

## DCT (R-PDSO-G8)

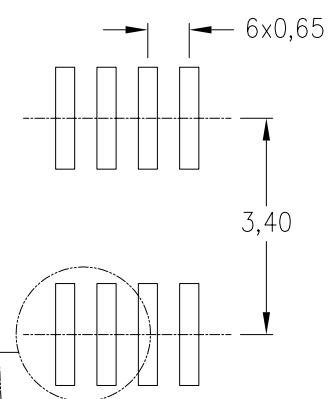
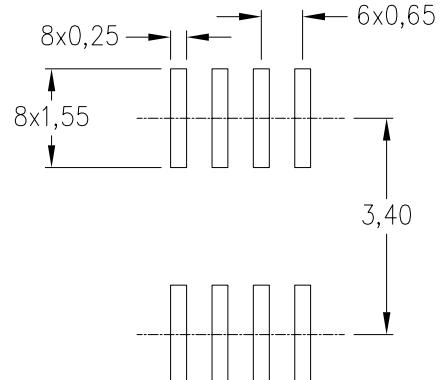
## PLASTIC SMALL-OUTLINE PACKAGE



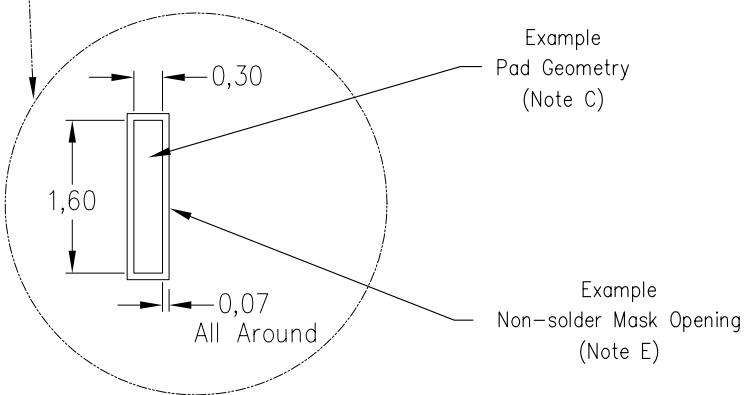
NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion  
 D. Falls within JEDEC MO-187 variation DA.

DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C,E)Example Stencil Design  
(Note D)

Non Solder Mask Defined Pad



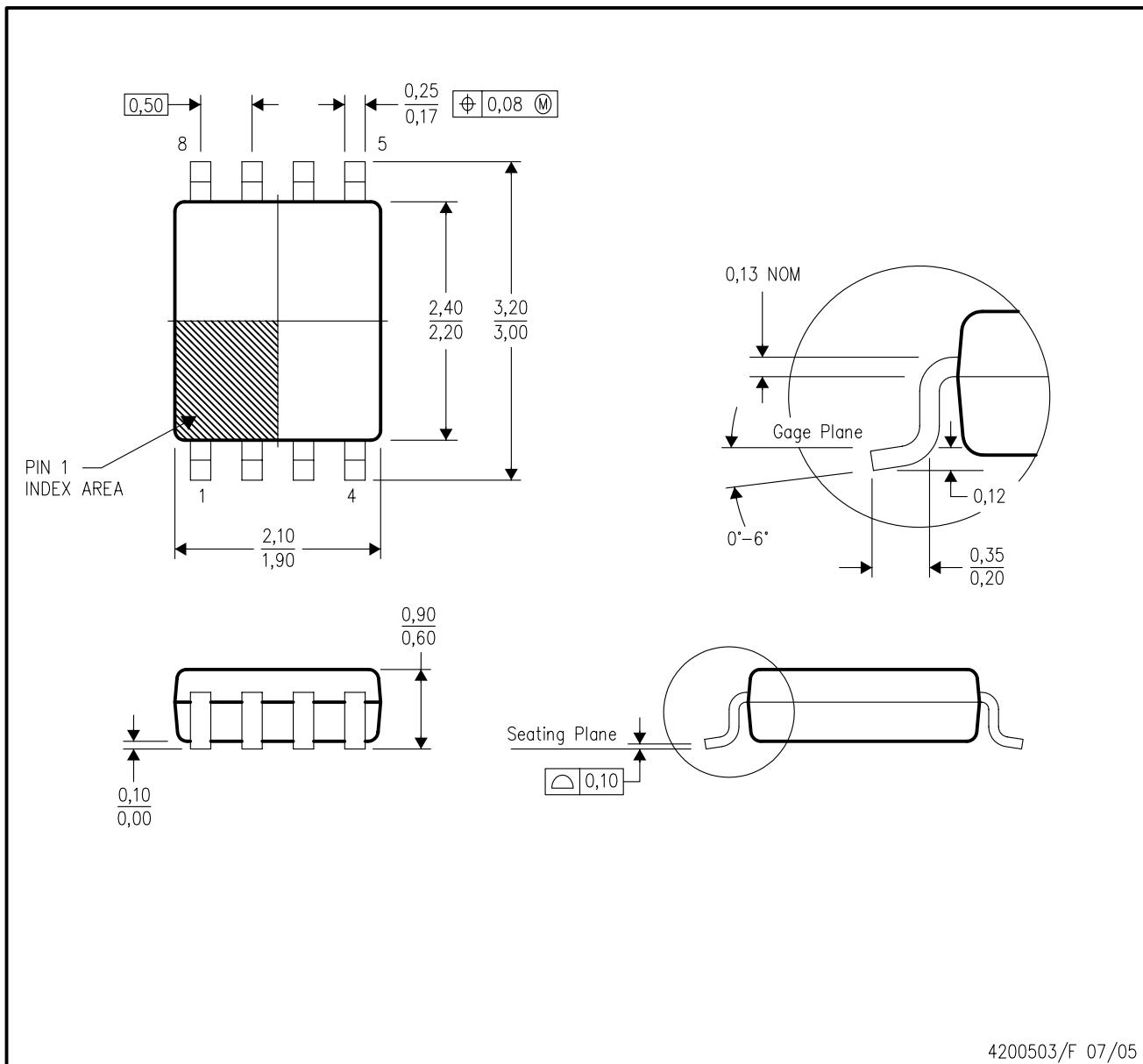
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NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DCU (R-PDSO-G8)

## PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



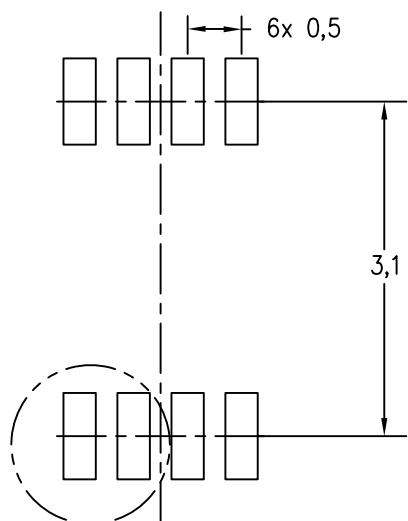
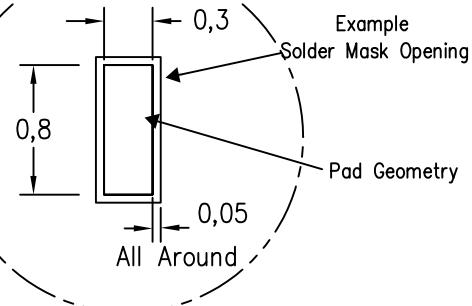
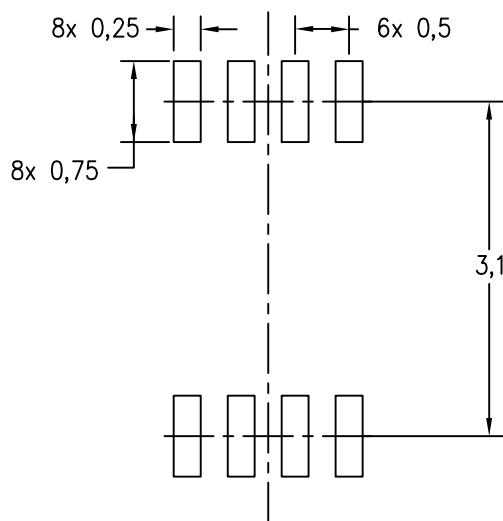
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NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)

Example Board Layout  
(Note C,E)Example Stencil Design  
(Note D)

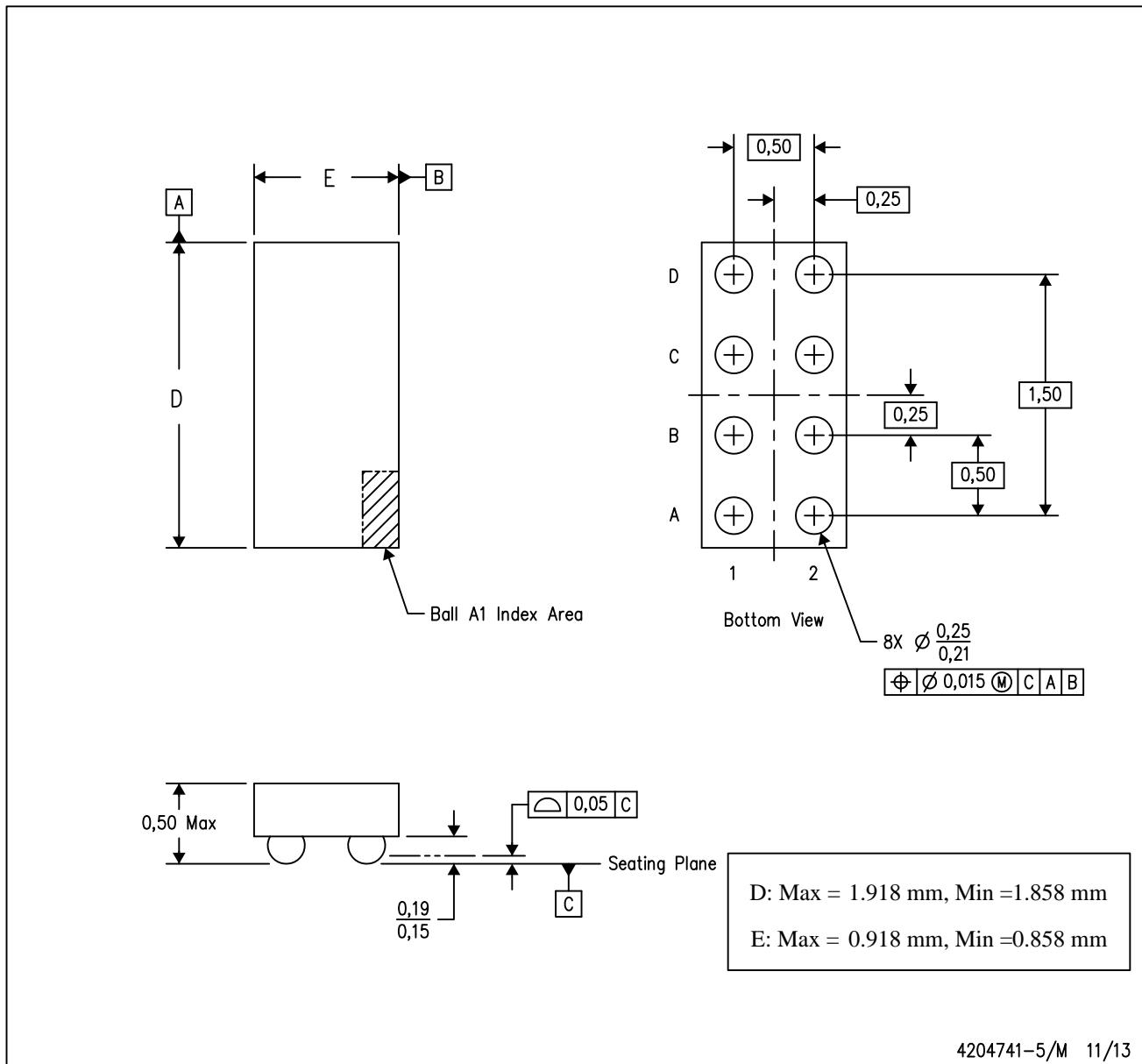
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NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

YZP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



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