A product Line of
Diodes Incorporated

PI3EQX12908A2

8-channel PCI Express Gen 3, 10GbE, SATA3 ReDriver™ with Linear Equalization

Features

- High-speed serial link with linear equalizer
- Support PCIe Gen 1/2/3 protocol, 10GbE, SATA3, SAS3
- Supporting 8 differential channels
- Independent channel configuration of receiver equalization, output swing and flat gain
- Per Channel Activity Detector with selectable input termination between 50Ω to V_{DD} and 200KΩ to V_{DD}
- Per Channel Output Termination Detector on power up with selectable output termination between 50Ω to V_{DD} and High impedance
- Very linear transfer function
- Fully compliant to PCISIG Link Training
- Single-ended mode receiver detection for PCIe
- Input Threshold detection
- Pin strap and I^2C master/slave selectable device programming with external EEPROM
- 4-bit selectable address bit for I^2C
- Supply Voltage: 3.3V±0.3V
- Industrial Temperature Range: -40°C to 85°C
- Packaging (Pb-free & Green):
  - 54-contact TQFN (10mm x 5.5mm x 0.5mm pitch) - flowthrough pinout

Description

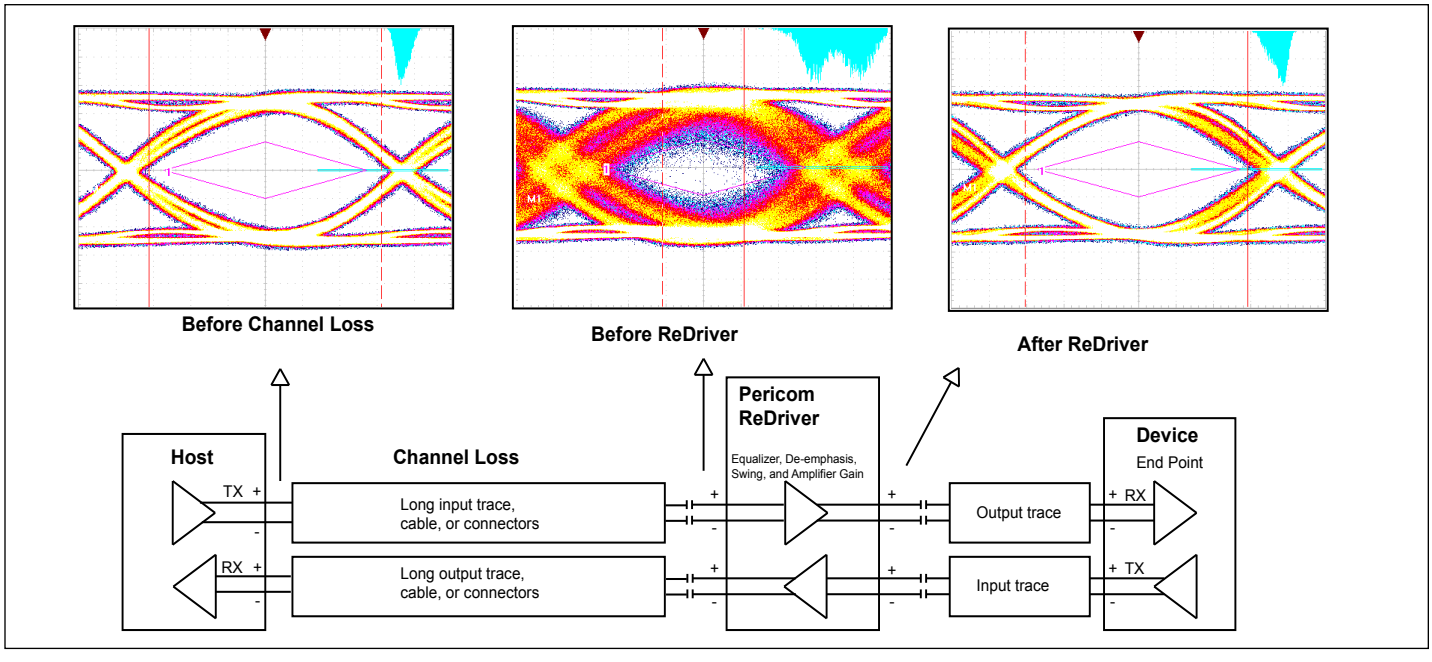
The PI3EQX12908A2 is an 8-channel PCIe Gen 2, 10GbE, SATA3, ReDriver™. The device provides programmable linear equalization, output swing and gain, by either pin strapping option or I^2C Control, to optimize performance over a variety of physical mediums by reducing Inter-symbol interference.

The PI3EQX12908A2 supports eight 100-Ohm Differential CML data I/O's and extends the signals across other distant data pathways on the user's platform.

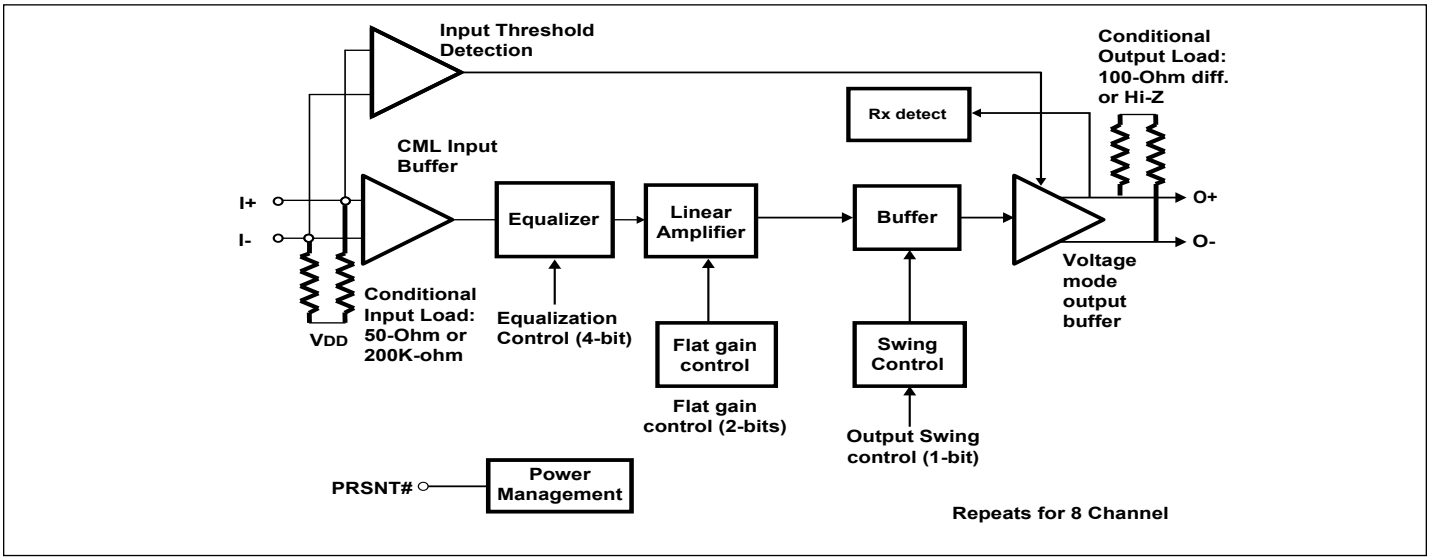
The programmable settings can be applied easily via pins, software (I^2C) or loaded via an external EEPROM. When operating in the EEPROM mode, the configuration information is automatically loaded on power up, which eliminates the need for an external microprocessor or software driver.

The PI3EQX12908A2 offers fully Linear Transfer function to fully comply with all PCIe 3 Link Training signals.

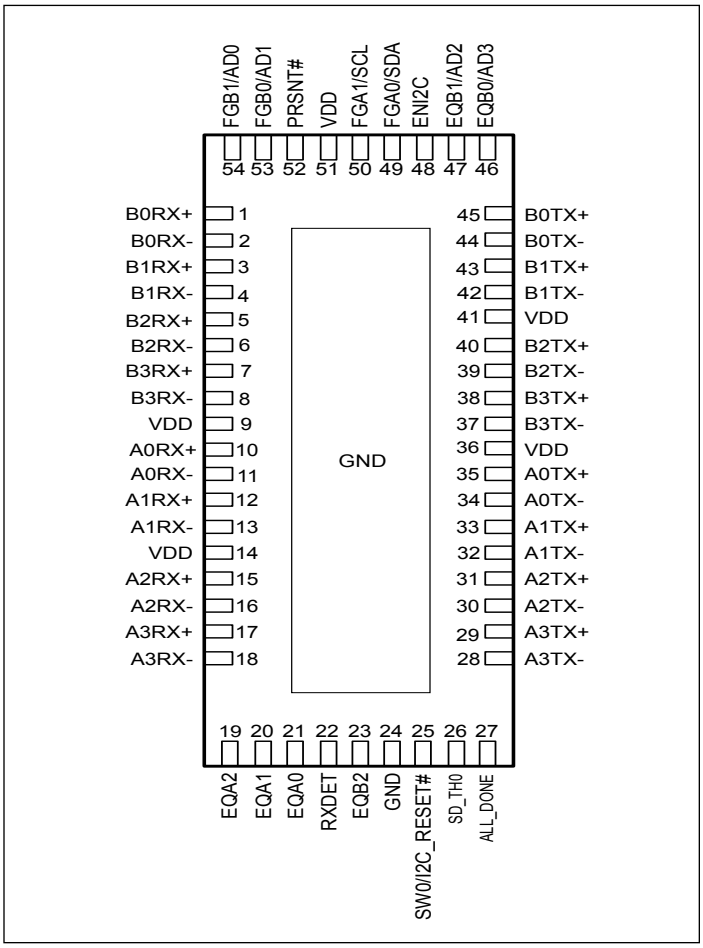
Eye Diagram



Block Diagram



Pin Configuration - Top View (54-TQFN)



Pin Description

(Flow-Thru Pinout)

Pin # (54-TQFN)	Pin Name	Type	Description
Data Signals			
10 11	A0RX+ A0RX-	I I	Differential inputs for Channel A0, with internal 50-Ohm pull-up and >200K-Ohm otherwise.
35 34	A0TX+, A0TX-	O O	Differential outputs for Channel A0
12 13	A1RX+, A1RX-	I I	Differential inputs for Channel A1, with internal 50-Ohm pull-up and >200K-Ohm otherwise.
33 32	A1TX+, A1TX-	O O	Differential outputs for Channel A1
15 16	A2RX+, A2RX-	I I	Differential inputs for Channel A2, with internal 50-Ohm pull-up and >200K-Ohm otherwise.
31 30	A2TX+, A2TX-	O O	Differential outputs for Channel A2
17 18	A3RX+, A3RX-	I I	Differential inputs for Channel A3, with internal 50-Ohm pull-up and >200K-Ohm otherwise.
29 28	A3TX+, A3TX-	O O	Differential outputs for Channel A3
1 2	B0RX+, B0RX-	I I	Differential inputs for Channel B0, with internal 50-Ohm pullup and >200KOhm otherwise.
45 44	B0TX+, B0TX-	O O	Differential outputs for Channel B0
3 4	B1RX+, B1RX-	I I	Differential inputs for Channel B1, with internal 50-Ohm pullup and >200KOhm otherwise.
43 42	B1TX+, B1TX-	O O	Differential outputs for Channel B1
5 6	B2RX+, B2RX-	I I	Differential inputs for Channel B2, with internal 50-Ohm pullup and >200KOhm otherwise.
40 39	B2TX+, B2TX-	O O	Differential outputs for Channel B2
7 8	B3RX+, B3RX-	I I	Differential inputs for Channel B3, with internal 50-Ohm pullup and >200KOhm otherwise.
38 37	B3TX+, B3TX-	O O	Differential outputs for Channel B3

Pin Description Cont.

Pin # (54-TQFN)	Pin Name	Type	Description
Control Signals			
48	ENI2C	I	I^2C Enable Pin. When tied to Low, each channel is programmed by the external pin voltage (Pin Mode). When tied to High, each channel is programmed by the data stored in the I^2C bus (Slave Mode). When FLOAT, data is accesses from external EEPROM (Master Mode). ENI2C has pull-up / pull-down 90k-Ohm resistance (Default = V_{DD} / 2).
When ENI2C = 1 (I^2C Mode)			
50	SCL	I/O	I^2C SCL clock input in I^2C Slave Mode (ENI2C = High). This pin becomes clock output when loading from EEPROM in I^2C Master Mode (ENI2C = FLOAT).
49	SDA	I/O	I^2C SDA data input/output in I^2C Master or Slave Mode.
54, 53, 47, 46	AD[0:3]	I	I^2C programmable address bits in I^2C Master or Slave Mode. AD[0:2] have pull-up 90k-Ohm resistance. AD[3] have pull-up / pull-down 90k-Ohm resistance. (Default = V_{DD}/2)
25	I2C_RESET#	I	Reset Pin for I^2C. When Low, the registers are reset to default value. I^2C_RESET# has pull-up 90k-Ohm resistance
When ENI2C = 0 (Pin mode)			
21, 20, 19	EQA[0:2]	I	These pins set the level of Equalizer in Bank A channels when ENI2C is Low. When ENI2C is High, the I2C registers provide independent control of each channel. See Table 1: Equalizer Settings. EQA[1] has pull-up 90k-Ohm resistance. EQA[0] and EQA[2] have pull-up / pull-down 90k-Ohm resistance (Default = V_{DD} / 2).
46, 47, 23	EQB[0:2]	I	These pins set the level of Equalizer in Bank B channels when ENI2C is Low. When ENI2C is High, the I2C registers provide independent control of each channel, and the EQB[1:0] pins are converted to I^2C AD[2:3] inputs. See Table 1: Equalizer Settings. EQB[1] has pull-up 90k-Ohm resistance. EQB[0] and EQB[2] have pull-up / pull-down 90k-Ohm resistance (Default = V_{DD} / 2).
49, 50	FGA[0:1]	I	These pins control the level of Flat Gain in Bank A channels when ENI2C is Low. When ENI2C is High, the I^2C registers provide independent control of each channel, and the FGA[1:0] pins are converted to I^2C SCL/SDA. See Table 2: Flat Gain Settings.
53, 54	FGB[0:1]	I	These pins control the level of Flat Gain in Bank B channels when ENI2C is Low. When ENI2C is High, the I^2C registers provide independent control of each channel, and FGB[1:0] pins are converted to AD[0:1] inputs. See Table 2: Flat Gain Settings. FGB[0] and FGB[1] have pull-up 90k-Ohm resistance.
25	SW0	I	This pins sets the Output Voltage Swing level in all channels when ENI²C is Low. SW0 has pull-up 90k-Ohm resistance.
26	SD_TH0	I	Internal Signal Detect Threshold. This pin should be tied to V_{DD} for normal operation. Refer to Table 4 for more options. SD_TH0 has pull-up 90k-Ohm resistance.
In both I2C and Pin modes			
22	RXDET	I	Receiver Detection Control Pin. When High, receiver detection is enabled to support PCIe Mode. When Low, receiver detection is disabled to support 10GbE and SATA3 Modes and input is 50-Ohm to V_{DD}. RXDET has pull-up 90k-Ohm resistance.

Pin Description Cont.

Pin # (54-TQFN)	Pin Name	Type	Description
52	PRSNT#	I	Cable Present Detect Input. When High, a cable is not present per PCIe Cabling Specification 1.0, and the device is put in lower power mode. When Low, the device is enabled and in normal operation. PRSNT# has pull-up 90k-Ohm resistance.
Output			
27	ALL_DONE	O	Valid Register Load Status Output. When LOW, the external EEPROM load has failed. When HIGH, the external EEPROM load is successful.
Power Pins			
9, 14, 36, 41, 51	V_{DD}	PWR	3.3V ± 10% Supply Voltage
Center Pad, 24	GND	PWR	Supply GND

Description of Operation

Output Receiver Detector:

On power up or when PRSNT# becomes low, the output resistance is set to high impedance, and the input resistance is set to 200K ohms. The device continually looks to detect an external 50 ohm termination resistor on a per channel basis. If no 50 ohms is detected in the first 40us of time, the channel is continually polled with 40us detection cycle until detection occurs. This operation can only be reinitiated when PRSNT# or I2C_RESET# are toggled again.

Input Activity Detector:

When the input voltage on individual channel basis falls below Vth-, the output is driven to the common mode voltage so as to eliminate output chatter. When the input voltage is higher than Vth+, the channel is resumed immediately.

Power Enable function:

One pin control or I2C control, when PRSNT# is set to high, the IC goes into power down mode, both input and output termination set to 200K and high impedance respectively. Individual channel enabling is done through the I2C register programming.

Equalization Setting:

EQA[2:0] and EQB[2:0] are the selection pins for the equalization selection for each of the channels of A and B respectively.

Table 1. Equalization Setting

Equalizer setting (dB)									
EQ2	**EQ1**	**EQ0**	**EQ 4 Bits**	**@ 1.25GHz**	**@ 2.5GHz**	**@ 3GHz**	**@ 4GHz**	**@ 5GHz**	**@ 6GHz**
0	0	0	0000	0	0.6	1.0	1.5	2.4	2.8
0	0	1	0001	0.15	1.2	1.7	2.4	3.5	4
0	1	0	0010	0.4	1.9	2.5	3.3	4.5	5
0	1	1	0011	0.6	2.5	3.2	4.2	5.3	5.8
1	0	0	0100	1.8	3.4	4.1	4.9	6.0	6.4
1	0	1	0101	2.1	3.9	4.7	5.6	6.7	7.1
1	1	0	0110	2.3	4.4	5.2	6.2	7.3	7.7
1	1	1	0111	2.5	4.9	5.7	6.8	7.9	8.2
HIZ	0	0	1000	3.4	5.6	6.4	7.3	8.4	8.7
HIZ	0	1	1001	3.6	6.0	6.9	7.8	8.9	9.1
HIZ	1	0	1010	3.8	6.4	7.3	8.3	9.3	9.5
HIZ	1	1	1011	4.1	6.8	7.7	8.7	9.7	9.9
0	0	HIZ	1100	5.1	7.5	8.3	9.2	10.1	10.2
0	1	HIZ	1101	5.3	7.8	8.6	9.5	10.4	10.5
1	0	HIZ	1110	5.4	8.1	8.9	9.8	10.7	10.8
1	1	HIZ	1111	5.6	8.4	9.2	10.1	11	11.1

Flat Gain Setting:

Flat Gain settings: FGA[0:1] and FGB[0:1] are the selection bits for Flat Gain value for A and B channels.

Table 2. Flat Gain Setting

FGA1 FGB1	FGA0 FGB0	(dB)
0	0	-4
0	1	-2
1	0	0
1	1	2

Output Swing Setting:

SW0 is the selection bit for output swing for A and B channels.

Table 3. Output Swing Setting

SW0	mVp-p
0	900
1	1,000

Signal Detect Threshold Level:

Table 4. Signal Detect Threshold Level Setting via I^2C Bus Mode

SD_TH1 <I^2C bit>	SD_TH0	Threshold ON (mVppd)	Threshold OFF (mVppd)
0	0	130	30
0	1	150	50
1	0	170	70
1	1	210	110

I²C Programming

Address assignment							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
1	1	1	AD3	AD2	AD1	AD0	1=R, 0=W

BYTE 0				
Bit	**Type**	**Power up condition**	**Control affected**	**Comment**
7	R		A3 Signal Detector Output	1= Activity 0=no activity
6	R		A2 Signal Detector Output	
5	R		A1 Signal Detector Output	
4	R		A0 Signal Detector Output	
3	R		B3 Signal Detector Output	
2	R		B2 Signal Detector Output	
1	R		B1 Signal Detector Output	
0	R		B0 Signal Detector Output	
BYTE 1				
Bit	**Type**	**Power up condition**	**Control affected**	**Comment**
7	R		A3 RX Detector Output	1 = Far-end 50 -ohm detected 0 = Not detected
6	R		A2 RX Detector Output	
5	R		A1 RX Detector Output	
4	R		A0 RX Detector Output	
3	R		B3 RX Detector Output	
2	R		B2 RX Detector Output	
1	R		B1 RX Detector Output	
0	R		B0 RX Detector Output	
BYTE 2				
Bit	**Type**	**Power up condition**	**Control affected**	Comment
7	R/W	0	A3 Power down	1 = Power down
6	R/W	0	A2 Power down	
5	R/W	0	A1 Power down	
4	R/W	0	A0 Power down	
3	R/W	0	B3 Power down	
2	R/W	0	B2 Power down	
1	R/W	0	B1 Power down	
0	R/W	0	B0 Power down	

I²C Programming Cont.

BYTE 3					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel A0 configuration	EQ3	Equalizer See Table 1
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat Gain See Table 2
2	R/W	0		FG0	
1	R/W	0		Reserved	Swing See Table 3
0	R/W	0		SW0	

BYTE 4					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel A1 configuration	EQ3	Equalizer See Table 1
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat Gain See Table 2
2	R/W	0		FG0	
1	R/W	0		Reserved	Swing See Table 3
0	R/W	0		SW0	

BYTE 5					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel A2 configuration	EQ3	Equalizer See Table 1
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat Gain See Table 2
2	R/W	0		FG0	
1	R/W	0		Reserved	Swing See Table 3
0	R/W	0		SW0	

I²C Programming Cont.

BYTE 6					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel A3 configuration	EQ3	Equalizer See Table 1
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat Gain See Table 2
2	R/W	0		FG0	
1	R/W	0		Reserved	Swing See Table 3
0	R/W	0		SW0	

BYTE 7					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel B0 configuration	EQ3	Equalizer See Table 1
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat Gain See Table 2
2	R/W	0		FG0	
1	R/W	0		Reserved	Swing See Table 3
0	R/W	0		SW0	

BYTE 8					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel B1 configuration	EQ3	Equalizer See Table 1
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat Gain See Table 2
2	R/W	0		FG0	
1	R/W	0		Reserved	Swing See Table 3
0	R/W	0		SW0	

I²C Programming Cont.

BYTE 9					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel B2 configuration	EQ3	Equalizer See Table 1
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat Gain See Table 2
2	R/W	0		FG0	
1	R/W	0		Reserved	Swing See Table 3
0	R/W	0		SW0	

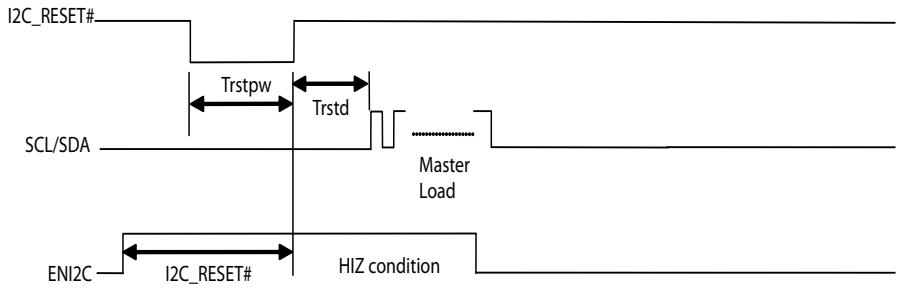
BYTE 10					
Bit	**Type**	**Power up condition**		**Control affected**	Comment
7	R/W	0	Channel B3 configuration	EQ3	Equalizer See Table 1
6	R/W	0		EQ2	
5	R/W	0		EQ1	
4	R/W	0		EQ0	
3	R/W	0		FG1	Flat Gain See Table 2
2	R/W	0		FG0	
1	R/W	0		Reserved	Swing See Table 3
0	R/W	0		SW0	

BYTE 11				
Bit	**Type**	**Power up condition**	**Control affected**	Comment
7	R/W	0	A3 Signal Detector	1=Power Down
6	R/W	0	A2 Signal Detector	
5	R/W	0	A1 Signal Detector	
4	R/W	0	A0 Signal Detector	
3	R/W	0	B3 Signal Detector	
2	R/W	0	B2 Signal Detector	
1	R/W	0	B1 Signal Detector	
0	R/W	0	B0 Signal Detector	

I²C Programming Cont.

BYTE 12				
Bit	**Type**	**Power up condition**	**Control affected**	Comment
7	R/W	0	A3 RX Detector	1=Power Down
6	R/W	0	A2 RX Detector	
5	R/W	0	A1 RX Detector	
4	R/W	0	A0 RX Detector	
3	R/W	0	B3 RX Detector	
2	R/W	0	B2 RX Detector	1=disable
1	R/W	0	B1 RX Detector	
0	R/W	0	B0 RX Detector	
BYTE 13				
Bit	**Type**	**Power up condition**	**Control affected**	Comment
7	R/W	0	Reserved	
6	R/W	0		
5	R/W	0		
4	R/W	0		
3	R/W	0		
2	R/W	0		
1	R/W	0	SD_TH1	Signal Detector Threshold
0	R/W	0	SD_TH0	
BYTE 14 to 15 have '0' as Power-up condition				

Reset and I²C Master Timing Diagram



Recommended minimum reset pulse width T_{rstpw}= 1µs
I²C master cycle start from I2C_RESET# pulse go high, T_{rstd} = 200µs
ENI2C = HIZ to I2C_RESET#(high) (min), Ti2cm_rst = 1 uS.

I²C Operation

The integrated I2C interface operates as a master or slave device depending on the pin ENI2C being HIZ or HIGH respectively. Standard mode (100Kbps) is supported with 7-bit addressing. The data byte format is 8-bit bytes, and supports the format of indexing to be compatible with other bus devices. In the Slave mode (ENI2C = HIGH), the device supports Read/Write. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred.
Address bits A3 to A0 are programmable to support multiple chips environment. The Data is loaded until a Stop sequence is issued.

In the master mode (ENI2C = HIZ), PI3EQX12908A2 supports up to 16 masters connected in daisy chain through connecting I2C_DONE pin to I2C_RESET# pin of the next part.

Master EEPROM data starting address of the device address is indicated in the table below:

AD3, AD2,AD1,AD0	EEPROM Data Starting Location
0000	00h
0001	10h
0010	20h
0011	30h
0100	40h
0101	50h
0110	60h
0111	70h
1000	80h
1001	90h
1010	A0h
1011	B0h
1100	C0h
1101	D0h
1110	E0h
1111	F0h

When tying multiple PI3EQX12908A2 devices to the SDA and SCL bus, use the guidelines below to configure the devices. The user also can refer the application notes for detail information.

• Use AD[3:0] address bits so that each device can loaded it's configuration from the EEPROM.
Example below is for 4 devices. The first device in the sequence must be address 0x00h;
subsequent devices must follow the address order listed below.
– U1: AD[3:0] = 0000 = 0x00h,
– U2: AD[3:0] = 0001 = 0x10h,
– U3: AD[3:0] = 0010 = 0x20h,
– U4: AD[3:0] = 0011 = 0x30h

• For I2C Slave Mode operation, use a 2Kohms pull-up resistor on SDA and SCL pins. For I2C Master Mode operation, use a 1Kohm pull-up resistor on SDA and SCL pins.

• Daisy-chain I2C_RESET# and ALL_DONE from one device to the next device in the sequence so that they do not compete for the EEPROM at the same time.

1. Tie ALL_DONE of U1 to I2C_RESET# of U2
2. Tie ALL_DONE of U2 to I2C_RESET# of U3
3. Tie ALL_DONE of U3 to I2C_RESET# of U4
4. Optional: Tie ALL_DONE output of U4 to a LED to show the devices has been loaded successfully

Below is an example of a 2 kbits (256 x 8-bit) EEPROM in hex format for 4pcs PI3EQX12908A2 device. Bold fonts in yellow are register setting from Byte0 to Byte15 for each device in each line. Bold fonts in red is the EEPROM data location.

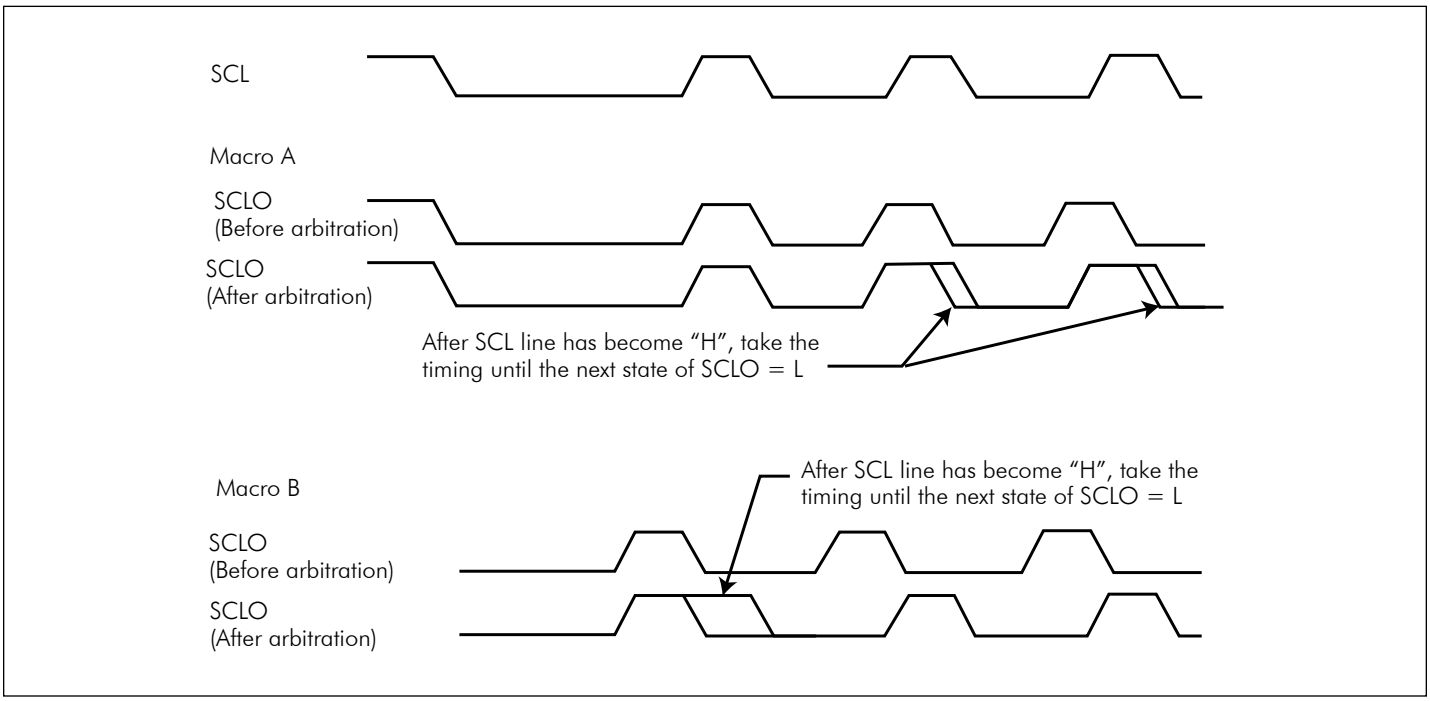
```
:1000000000000000FF0000FFFFFFFFFF0000FF620194
:1000100000000000FFFF0000FFFFFFFF0000FF620184
:1000200000000000FFFFFF0000FFFFFF0000FF620174
:1000300000000000FFFFFFFF0000FFFF0000FF620164
:10004000000000000000000000000000000000000B0
:10005000000000000000000000000000000000000A0
:100060000000000000000000000000000000000090
:100070000000000000000000000000000000000080
:100080000000000000000000000000000000000070
:100090000000000000000000000000000000000060
:1000A0000000000000000000000000000000000050
:1000B0000000000000000000000000000000000040
:1000C0000000000000000000000000000000000030
:1000D0000000000000000000000000000000000020
:1000E0000000000000000000000000000000000010
:1000F0000000000000000000000000000000000000
:00000001FF
```

2k bits (256 x 8-bit) EEPROM Date Example

Below is the sample of the I2C master reading waveform based on the setup above.

SCL Synchronization

When more than one I2C device becomes a master device and drives the SCL line, each device senses the state of SCL line and automatically adjust the the drive timing by adjusting the timing to the timing to the slowest one.



Transferring Data

Every byte put on the SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I2C Data Transfer diagram). The PI3EQX12908A2 will never hold the clock line SCL LOW to force the master into a wait state.

Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, the PI3EQX12908A2 will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I2C Data Transfer diagram. The PI3EQX12908A2 will generate an acknowledge after each byte has been received.

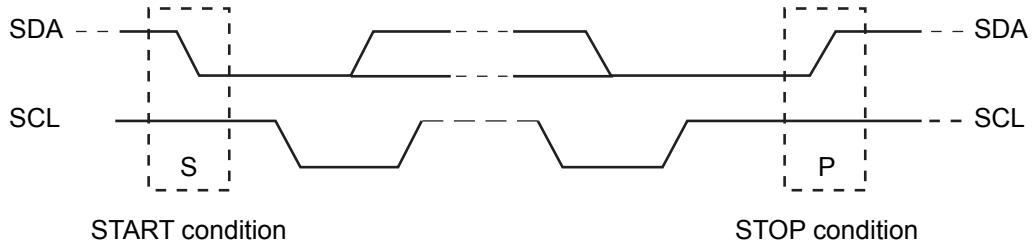
Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, the PI3EQX12908A2 will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. For a write cycle, the first data byte following the address byte is an index byte that is used by the PI3EQX12908A2. Data is transferred with the most significant bit (MSB) first.

I²C Data Transfer

Start & Stop Conditions

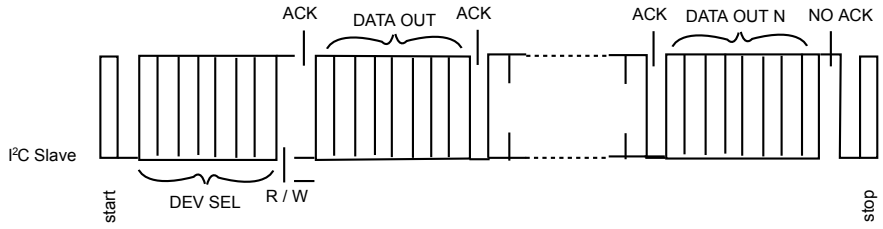
A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below. When a STOP condition is detected, index byte value will be reset to 0.



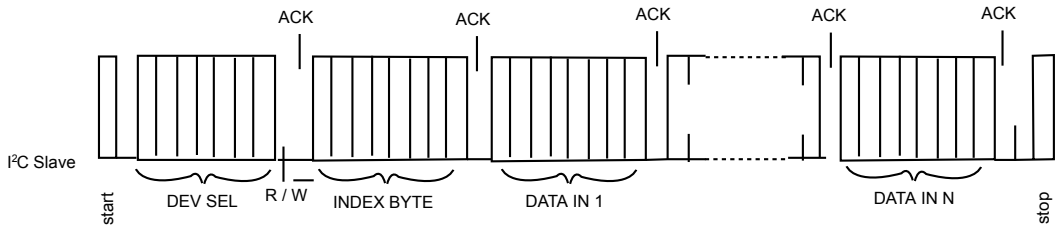
I²C START and STOP conditions.

I²C Data Transfer Sequence

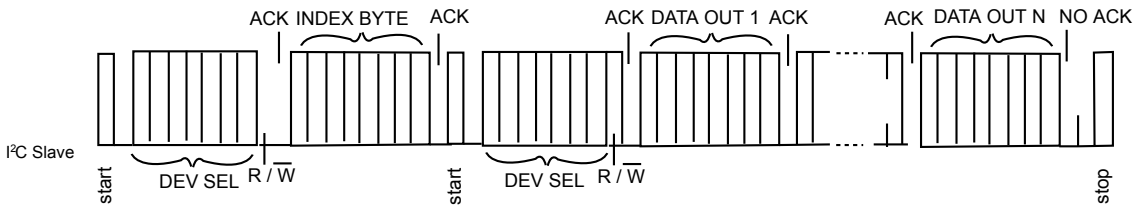
1. Read sequence



2. Write sequence



3. Combined sequence



Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage	-0.5V to +4.0V
LVCMOS Input/Output Voltage	-0.5V to +4.0V
CML Input Voltage	-0.5V to (V_{DD}+0.5)
CML Input Current	-30 to +30 mA
I^2C pins	V_{DD}+0.3 V
Storage Temperature	–65°C to +150°C
Max. Junction Temperature	125 °C
ESD HBM	2kV

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

LVCMOS I/O DC Specifications (V_{DD} = 3.3 ± 10%, T_A = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC input logic high		V_{DD}/2 + 0.7		V_{DD} + 0.3	V
V_{IL}	DC input logic low		-0.3		V_{DD}/2 - 0.7	V
V_{OH}	DC output logic high	At I_{OH} = -200µA	V_{DD} - 0.2			V
V_{OL}	DC output logic low	At I_{OL} = +200µA			0.2	V
V_{hys}	Hysteresis of Schmitt trigger input		0.8			V

SDA and SCL I/O for I^2C-bus (V_{DD} = 3.3 ± 10%, T_A = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC input logic high		V_{DD}/2 + 0.7		V_{DD} + 0.3	V
V_{IL}	DC input logic low		-0.3		V_{DD}/2 - 0.7	V
V_{OL}	DC output logic low	I_{OL} = 3mA			0.4	V
V_{hys}	Hysteresis of Schmitt trigger input		0.8			V
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}	Bus capacity = 10 to 400pF		250		ns
f_{SCLK}	SCLK clock frequency			100		kHz

High Speed I/O AC/DC Specifications (V_{DD} = 3.3 ± 10%, T_A = -40 to 85°C)

Receiver Input (100Ω differential)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{RX}	RX AC coupling capacitance			220		nF
S_{11}	Input return loss	10MHz to 4GHz differential		13		dB
		1GHz to 4GHz common mode		4		

High Speed I/O AC/DC Specifications Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
S_{22}	Output return loss	10MHz to 4GHz differential		21		dB
		1GHz to 4GHz common mode		4		
R_{IN}	DC single-ended input impedance			50		Ω
	DC differential input impedance			100		
R_{OUT}	DC single-ended output impedance			50		Ω
	DC differential output impedance			100		
Z_{RX-HIZ}	DC input CM input impedance during reset or power down			200		kΩ
$V_{RX-DIFF-PP}$	Differential Input Peak-to-peak Voltage	Operational			1.2	V_{ppd}
	Input source common-mode noise	DC – 200MHz			150	mV_{ppd}
$T_{TX-IDLE-SET-TO-IDLE}$	Max time to electrical idle after sending an EIOS			4	8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Max time to valid diff signal after leaving electrical idle			4	8	ns
V_{th+}	On threshold of signal detector	Signal swing @ 4GHz	130		210	mV_{ppd}
V_{th-}	Off threshold of signal detector	Signal swing @ 100MHz	30		110	mV_{ppd}
V_{DD}	Power supply voltage		3	3.3	3.6	V
P_{max}	Max Supply power	PRSNT#=0			1	W
I_{max}	Max Supply current				330	mA
P_{idle}	Supply power	PRSNT#=1			36	mW
G_{P5GHZ}	Peaking gain (Compensation at 5GHz, relative to 100MHz, 100mVp-p sine wave input) SW<1:0>=01, FG<1:0>=10	EQ<3:0> = 1111 EQ<3:0> = 1000 EQ<3:0> = 0000		16.1 13.5 8.0		dB
		Variation around typical	-3		+3	
G_{P6GHZ}	Peaking gain (Compensation at 6GHz, relative to 100MHz, 100mVp-p sine wave input) SW<1:0>=01, FG<1:0>=10	EQ<3:0> = 1111 EQ<3:0> = 1000 EQ<3:0> = 0000		17.2 14.8 9.0		dB
		Variation around typical	-3		+3	
G_F	Flat gain (100MHz, EQ<3:0> = 1000, SW<1:0> = 01)	FG<1:0> = 11 FG<1:0> = 10 FG<1:0> = 01 FG<1:0> = 00		+2.0 -0.5 -2.0 -4.0		dB
		Variation around typical	-3		+3	
V_{1dB_100M}	-1dB compression point of output swing (at 100MHz)	SW0=1 SW0=0		1000 900		mV_{ppd}
V_{1dB_6G}	-1dB compression point of output swing (at 6GHz) FG= 0dB, EQ = 0000 or 0(h)	SW0=1 SW0=0		600 540		mV_{ppd}

High Speed I/O AC/DC Specifications Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{Coup}	Channel isolation	100MHz to 5GHz, Figure 1 (Note 1)		28		dB
V_{noise_input}	Input-referred noise	100MHz to 5GHz, FG<1:0> = 11, EQ<3:0> = 0000, Figure 2		0.5		mV_{RMS}
		100MHz to 5GHz, FG<1:0> = 11, EQ<3:0> = 1010, Figure 2		0.4		
V_{noise_output}	Output-referred noise (Note 2)	100MHz to 5GHz, FG<1:0> = 11, EQ<3:0> = 0000, Figure 2		0.7		mV_{RMS}
		100MHz to 5GHz, FG<1:0> = 11, EQ<3:0> = 1010, Figure 2		0.8	1.6	
Latency						
t_{pd}	Latency	From input to output		0.2		ns
Jitter						
R_j	Additive Random Jitter at 8Gb/s (worst case)	PRBS31@24hrs 36" 5mils FR4 VID = 0.8mVp-p DE = 0dB EQ = 0100		0.0258		UI

Note 1: Measured using a vector-network analyzer (VNA) with -15dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω.

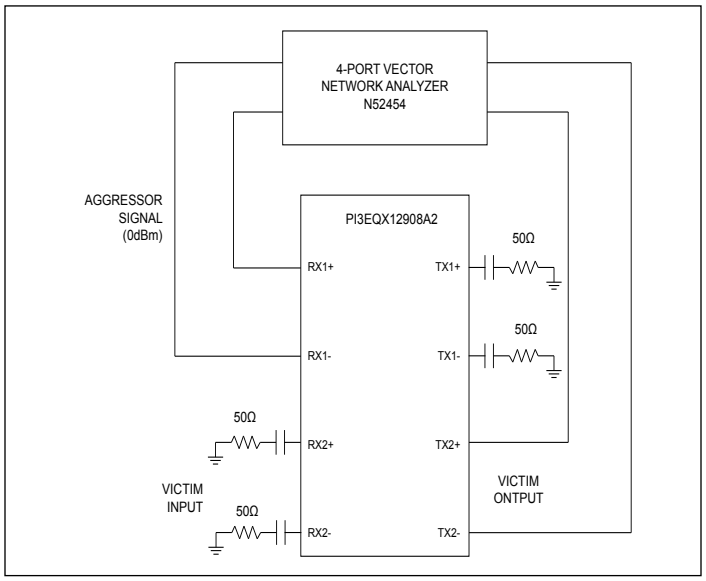
Note 2: Guaranteed by design and characterization.

Characteristics of the SDA and SCl bus lines for Standard Mode I²C-bus devices(1)

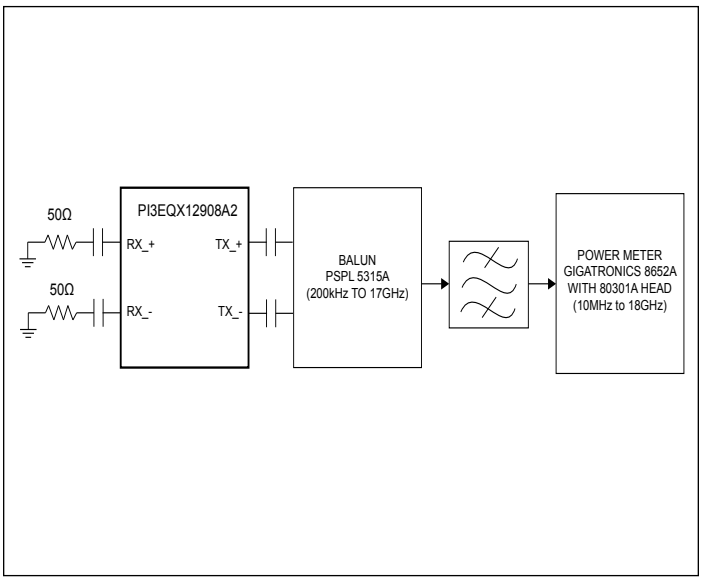
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{SCL}	SCL clock frequency			100	_	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.		4.0		_	µs
t_{LOW}	LOW period of the SCL clock		4.7		_	
t_{HIGH}	HIGH period of the SCL clock		4.0		_	
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7		_	
$t_{HD;DAT}$	Data hold time		10		_	ns
$t_{SU;DAT}$	Data set-up time		250		_	ns
t_r	Rise time of both SDA and SCL signals		-		1000	
t_f	Fall time of both SDA and SCL signals				300	
$t_{SU;STO}$	Set-up time for STOP condition		4.0		_	µs
t_{BUF}	Bus free time between a STOP and STOP condition		4.7		_	
C_b	Capacitive load for each bus line		-		400	pF

Notes:

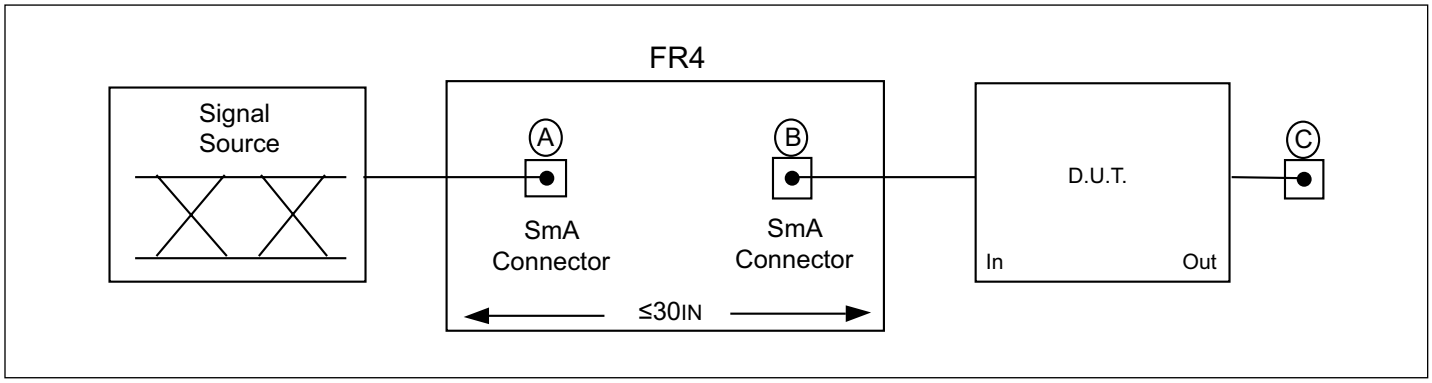
1. All values referred to VIH min and VIL max levels



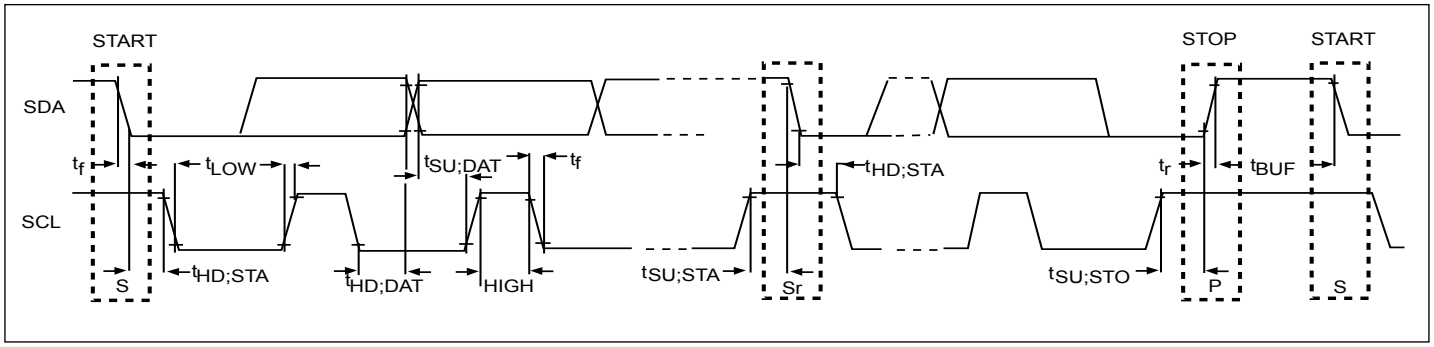
Channel-Isolation Test Configuration



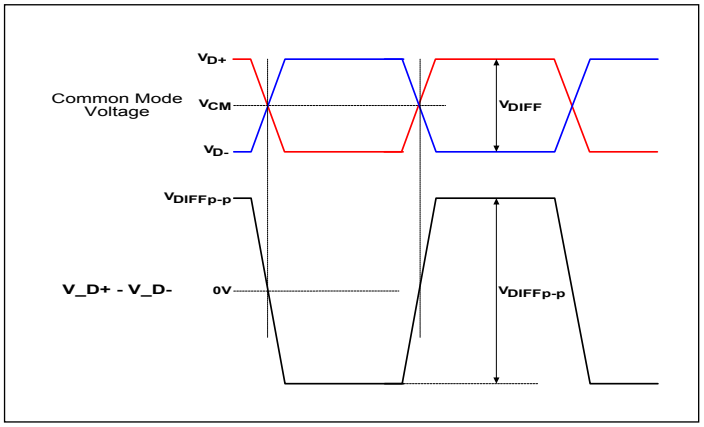
Noise Test Configuration



AC Test Circuit Referenced in the Electrical Characteristic Table

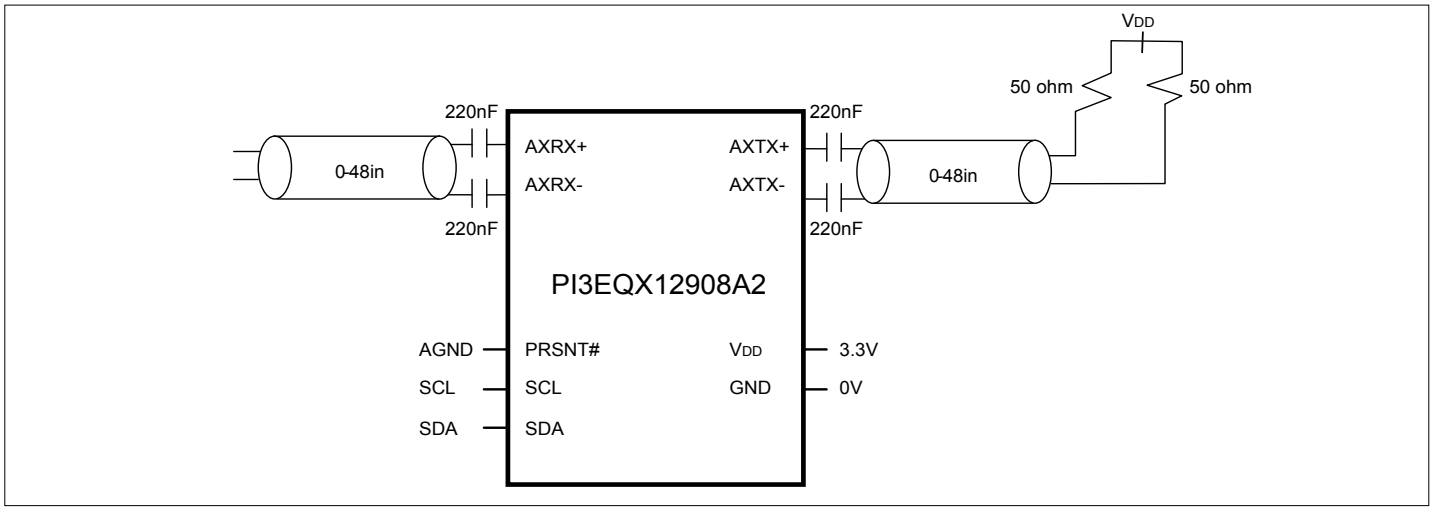


I²C Timing



Definition of Differential Voltage and Differential Voltage Peak-to-Peak

Application Diagrams



Applications Information

GENERAL RECOMMENDATIONS

The PI3EQX12908A2 is a high performance circuit capable of delivering excellent performance. Careful attention must be paid to the details associated with high-speed design as well as providing a clean power supply. Refer to the information below and Revision 4 of the LVDS Owner's Manual for more detailed information on high speed design tips to address signal integrity design issues.

PCB LAYOUT CONSIDERATIONS FOR DIFFERENTIAL PAIRS

The Differential inputs and LPDS outputs have been optimized to work with interconnects using a controlled differential impedance of 85 - 100Ω. It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces. The use of vias should be avoided if possible. If vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair. Whenever differential vias are used the layout must also provide for a low inductance path for the return currents as well. Route the differential signals away from other signals and noise sources on the printed circuit board.

POWER SUPPLY BYPASSING

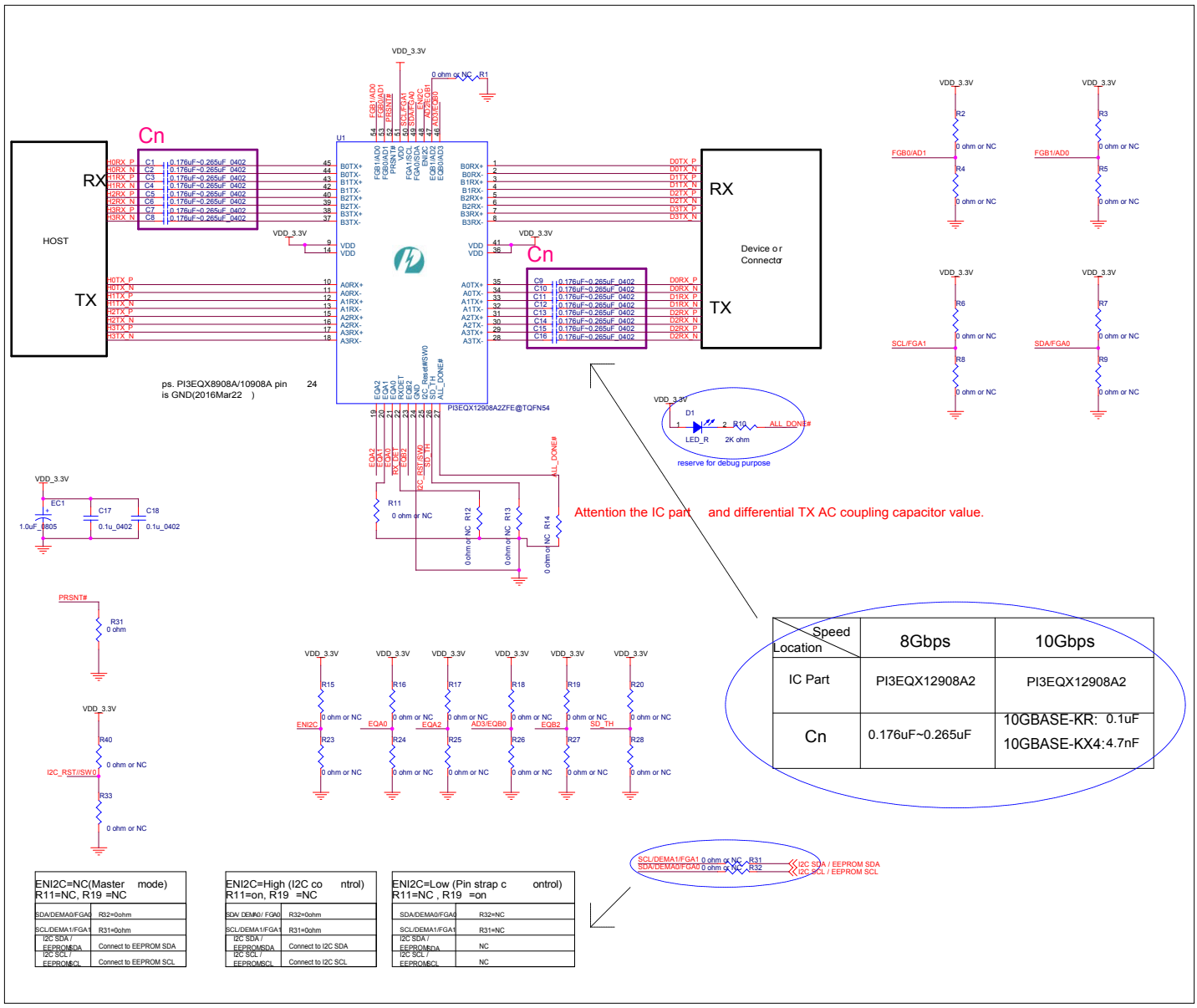
Two approaches are recommended to ensure that the PI3EQX12908A2 is provided with an adequate power supply. First, the supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of theprinted circuit board. The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance. Second, careful attention to supply bypassing through the proper use of bypass capacitors is required. A 0.1 µF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to the PI3EQX12908A2. Smaller body size capacitors can help facilitate proper component placement. Additionally, capacitor with capacitance in the range of 1 µF to 10 µF should be incorporated in the power supply bypassing design as well. These capacitors can be either tantalum or an ultra-low ESR ceramic.

Notes:

Hot Plug Detect feature operation is dependent on certain channel conditions, such as length.

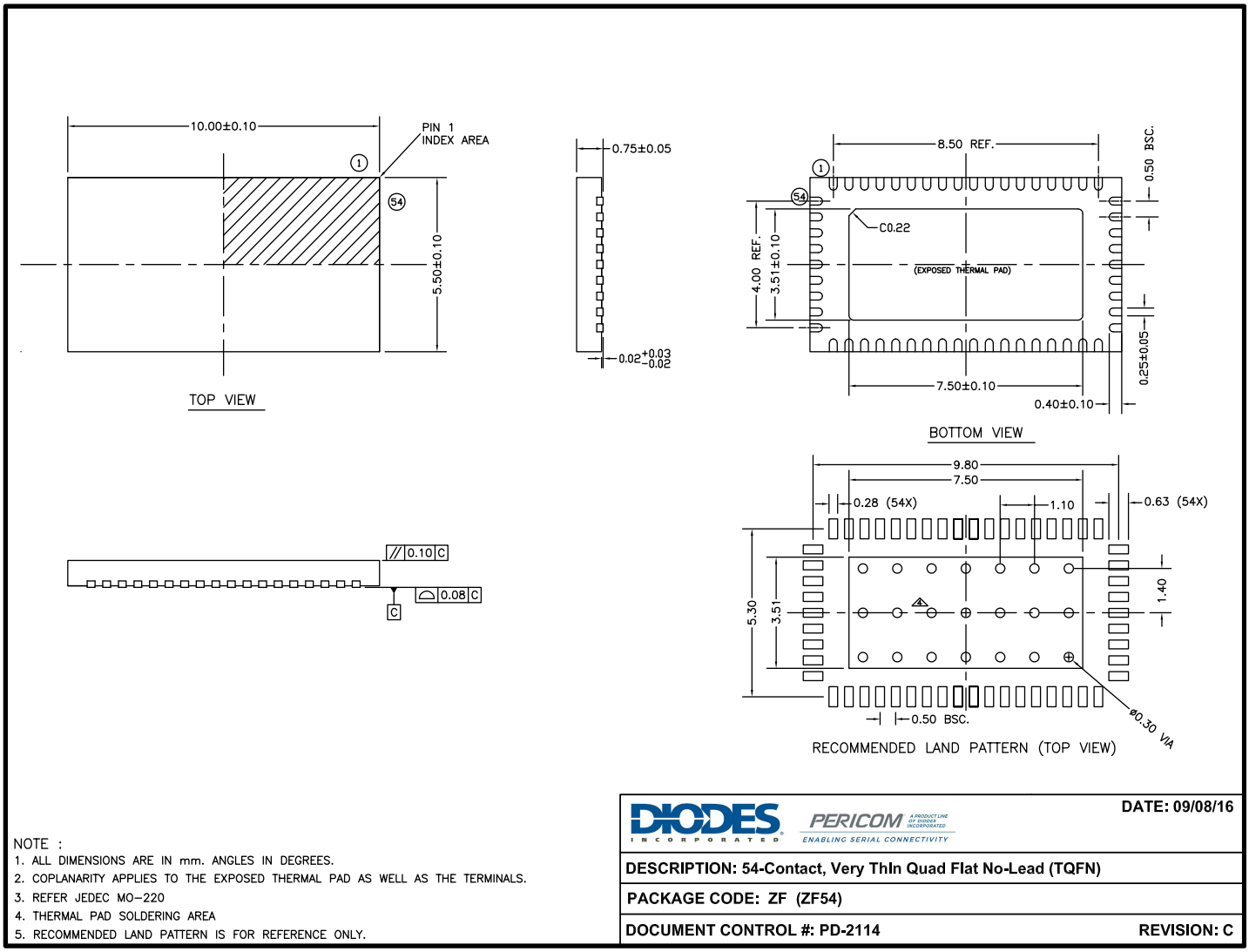
For hot plug detect, reset will automatically go back to receiver detect (RXDET) cycle.

Application Schematics



Speed / Location	8Gbps	10Gbps
IC Part	PI3EQX12908A2	PI3EQX12908A2
Cn	0.176uF~0.265uF	10GBASE-KR: 0.1uF 10GBASE-KX4:4.7nF

Packaging Information 54-TQFN (ZF)



NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220
4. THERMAL PAD SOLDERING AREA
5. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.

DATE: 09/08/16

DESCRIPTION: 54-Contact, Very Thin Quad Flat No-Lead (TQFN)

PACKAGE CODE: ZF (ZF54)

DOCUMENT CONTROL #: PD-2114 REVISION: C

16-0180

Thermal Resistance - 54-contact ZF Package/72-contact ZL Package:

θJC .....11.5°C/W

θJA .....No Airflow, 4 layer JEDEC 19.1°C/W

For latest package info.

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

Ordering Information

Ordering Number	Package Code	Package Description
PI3EQX12908A2ZFEX	ZF	54-Contact, Very Thin Quad Flat No-Lead (TQFN)

Notes:

- Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel

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