

## SRAM NV Controller With Reset

### Features

- Power monitoring and switching for nonvolatile control of SRAMs
- Write-protect control
- Input decoder allows control of up to 2 banks of SRAM
- 3-volt primary cell input
- 3-volt rechargeable battery input/output
- Reset output for system power-on reset
- Less than 10ns chip enable propagation delay
- 5% or 10% supply operation

### General Description

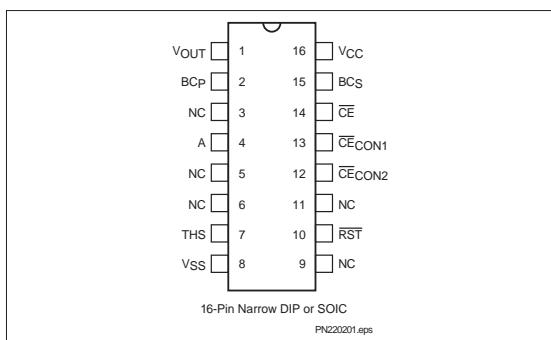
The CMOS bq2202 SRAM Nonvolatile Controller With Reset provides all the necessary functions for converting one or two banks of standard CMOS SRAM into nonvolatile read/write memory.

A precision comparator monitors the 5V V<sub>CC</sub> input for an out-of-tolerance condition. When out-of-tolerance is detected, the two conditioned chip-enable outputs are forced inactive to write-protect both banks of SRAM.

Power for the external SRAMs is switched from the V<sub>CC</sub> supply to the battery-backup supply as V<sub>CC</sub> decays. On a subsequent power-up, the V<sub>OUT</sub> supply is automatically switched from the backup supply to the V<sub>CC</sub> supply. The external SRAMs are write-protected until a power-valid condition exists. The reset output provides power-fail and power-on resets for the system.

During power-valid operation, the input decoder selects one of two banks of SRAM.

### Pin Connections



### Pin Names

V <sub>OUT</sub>	Supply output
RST	Reset output
THS	Threshold select input
CE	Chip enable active low input
CECON1, CECON2	Conditioned chip enable outputs
A	Bank select input
BCP	3V backup supply input
BCS	3V rechargeable backup supply input/output
NC	No connect
V <sub>CC</sub>	+5 volt supply input
V <sub>SS</sub>	Ground

### Functional Description

Two banks of CMOS static RAM can be battery-backed using the V<sub>OUT</sub> and conditioned chip-enable output pins from the bq2202. As the voltage input V<sub>CC</sub> slews down during a power failure, the two conditioned chip enable outputs, CECON1 and CECON2, are forced inactive independent of the chip enable input CE.

This activity unconditionally write-protects external SRAM as V<sub>CC</sub> falls to an out-of-tolerance threshold VPFD. VPFD is selected by the threshold select input pin, THS. If THS is tied to V<sub>SS</sub>, the power-fail detection occurs at 4.62V typical for 5% supply operation.

If THS is tied to V<sub>CC</sub>, power-fail detection occurs at 4.37V typical for 10% supply operation. The THS pin must be tied to V<sub>SS</sub> or V<sub>CC</sub> for proper operation.

If a memory access is in process to any of the two external banks of SRAM during power-fail detection, that memory cycle continues to completion before the memory is write-protected. If the memory cycle is not terminated within time tWPT (150 $\mu$ sec maximum), the two chip enable outputs are unconditionally driven high, write-protecting the controlled SRAMs.

## bq2202

As the supply continues to fall past V<sub>PFD</sub>, an internal switching device forces V<sub>OUT</sub> to the internal backup energy source.  $\overline{CECON1}$  and  $\overline{CECON2}$  are held high by the V<sub>OUT</sub> energy source.

During power-up, V<sub>OUT</sub> is switched back to the 5V supply as V<sub>CC</sub> rises above the backup cell input voltage sourcing V<sub>OUT</sub>. Outputs  $\overline{CECON1}$  and  $\overline{CECON2}$  are held inactive for time t<sub>CER</sub> (120ms maximum) after the power supply has reached V<sub>PFD</sub>, independent of the CE input, to allow for processor stabilization.

During power-valid operation, the  $\overline{CE}$  input is passed through to one of the two  $\overline{CECON}$  outputs with a propagation delay of less than 10ns. The CE input is output on one of the two  $\overline{CECON}$  output pins; depending on the level of bank select input A, as shown in the Truth Table.

Bank select input A is usually tied to a high-order address pin so that a large nonvolatile memory can be designed using lower-density memory devices. Nonvolatility and decoding are achieved by hardware hookup as shown in Figure 1.

The reset output ( $\overline{RST}$ ) goes active within t<sub>PF</sub> (150 $\mu$ sec maximum) after V<sub>PFD</sub>, and remains active for a minimum of 40ms (120ms maximum) after power returns valid. The  $\overline{RST}$  output can be used as the power-on reset for a microprocessor. Access to the external RAM may begin when  $\overline{RST}$  returns inactive.

### Energy Cell Inputs—BCP, BCs

Two backup energy source inputs are provided on the bq2202—a primary cell BCP and a secondary cell BCs. The primary cell input is designed to accept any 3V primary battery (non-rechargeable), typically some type of lithium chemistry. If a primary cell is not to be used, the BCP pin should be grounded. The secondary cell input BCs is designed to accept constant-voltage current-limited rechargeable cells.

During normal 5V power valid operation, 3.3V is output on the BCs pin and is current-limited internally.

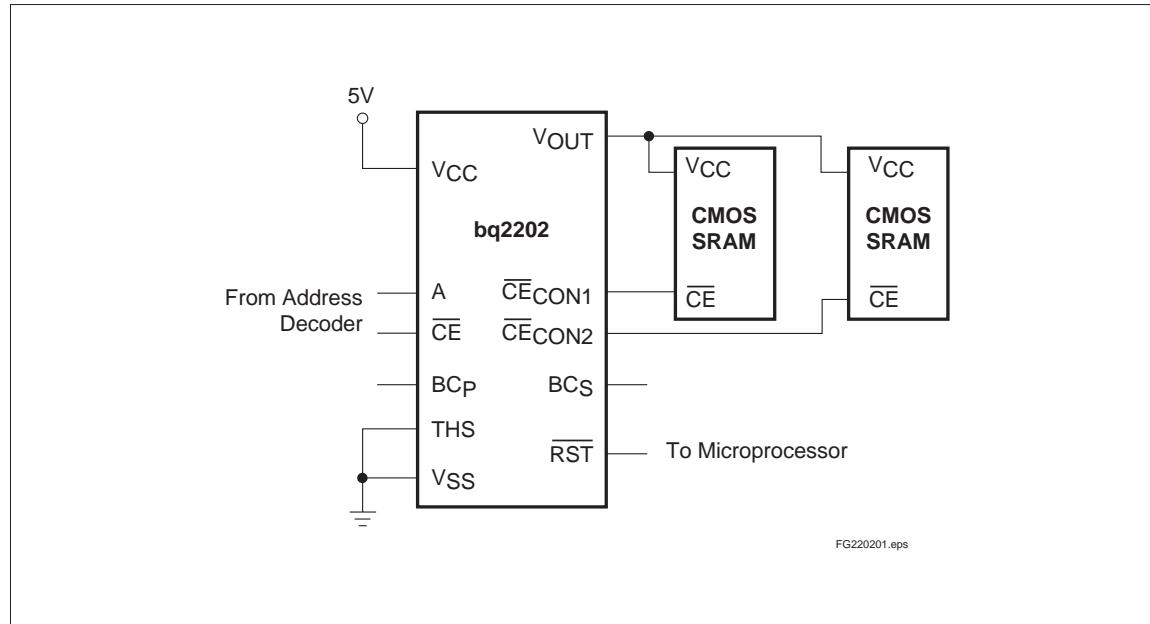


Figure 1. Hardware Hookup (5% Supply Operation)

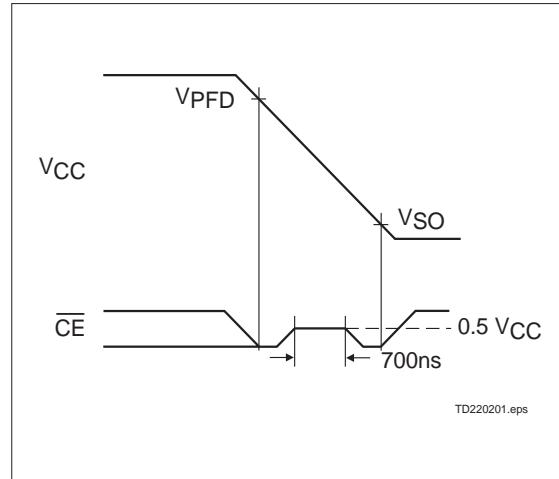
If a secondary cell is not to be used, the BCS pin must be tied directly to VSS. If both inputs are used, during power failure the VOUT and  $\overline{\text{CECON}}$  outputs are forced high by the secondary cell so long as it is greater than 2.5V. Only the secondary cell is loaded by the data retention current of the SRAM until the voltage at the BCS pin falls below 2.5V. When and if the voltage at BCS falls below 2.5V, an internal isolation switch automatically transfers the load from the secondary cell to the primary cell.

To prevent battery drain when there is no valid data to retain, VOUT,  $\overline{\text{CECON1}}$ , and  $\overline{\text{CECON2}}$  are internally isolated from BCP and BCS by either:

- Initial connection of a battery to BCP or BCS or
- Presentation of an isolation signal on  $\overline{\text{CE}}$ .

A valid isolation signal requires  $\overline{\text{CE}}$  low as  $V_{CC}$  crosses both VPFD and VSO during a power-down. See Figure 2. Between these two points in time,  $\overline{\text{CE}}$  must be brought to  $V_{CC} * (0.48 \text{ to } 0.52)$  and held for at least 700ns. The isolation signal is invalid if  $\overline{\text{CE}}$  exceeds  $V_{CC} * 0.54$  at any point between  $V_{CC}$  crossing VPFD and VSO.

The battery is connected to VOUT,  $\overline{\text{CECON1}}$ , and  $\overline{\text{CECON2}}$  immediately on subsequent application and removal of  $V_{CC}$ .



**Figure 2. Battery Isolation Signal**

## Truth Table

Input		Output	
$\overline{\text{CE}}$	A	$\overline{\text{CECON1}}$	$\overline{\text{CECON2}}$
H	X	H	H
L	L	L	H
L	H	H	L

# bq2202

---

## Absolute Maximum Ratings

Symbol	Parameter	Value	Unit	Conditions
VCC	DC voltage applied on VCC relative to VSS	-0.3 to +7.0	V	
VT	DC voltage applied on any pin excluding VCC relative to VSS	-0.3 to +7.0	V	VT $\leq$ VCC + 0.3
TOPR	Operating temperature	0 to +70	°C	Commercial
		-40 to +85	°C	Industrial "N"
TSTG	Storage temperature	-55 to +125	°C	
TBIAS	Temperature under bias	-40 to +85	°C	
TSOLDER	Soldering temperature	260	°C	For 10 seconds
IOUT	VOUT current	200	mA	

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

## Recommended DC Operating Conditions (TA = TOPR)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
VCC	Supply voltage	4.75	5.0	5.5	V	THS = VSS
		4.50	5.0	5.5	V	THS = VCC
VBCP	Backup cell input voltage	2.0	-	4.0	V	VCC < VBC
		2.5	-	4.0		
VSS	Supply voltage	0	0	0	V	
VIL	Input low voltage	-0.3	-	0.8	V	
VIH	Input high voltage	2.2	-	VCC + 0.3	V	
THS	Threshold select	-0.3	-	VCC + 0.3	V	

**Note:** Typical values indicate operation at TA = 25°C, VCC = 5V or VBC.

**DC Electrical Characteristics (TA = TOPR, VCC = 5V ± 10%)**

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions/Notes
ILI	Input leakage current	-	-	± 1	µA	VIN = VSS to VCC
VOH	Output high voltage	2.4	-	-	V	IOH = -2.0mA
VOHB	VOH, backup supply	VBC - 0.3	-	-	V	VBC > VCC, IOH = -10µA
VOL	Output low voltage	-	-	0.4	V	IOL = 4.0mA
ICC	Operating supply current	-	3	6	mA	No load on VOUT, $\overline{CE}_{CON1}$ , and $\overline{CE}_{CON2}$
VPFD	Power-fail detect voltage	4.55	4.62	4.75	V	THS = VSS
		4.30	4.37	4.50	V	THS = VCC
VSO	Supply switch-over voltage	-	VBC	-	V	
ICCDR	Data-retention mode current	-	-	100	nA	No load on VOUT, $\overline{CE}_{CON1}$ , and $\overline{CE}_{CON2}$
VOUT1	VOUT voltage	VCC - 0.2	-	-	V	VCC > VBC, IOUT = 100mA
		VCC - 0.3	-	-	V	VCC > VBC, IOUT = 160mA
VOUT2	VOUT voltage	VBC - 0.2	-	-	V	VCC < VBC, IOUT = 100µA
VBC	Active backup cell voltage	-	VBCS	-	V	VBCS > 2.5V
		-	VBCP	-	V	VBCS < 2.5V
RBCS	BCS charge output internal resistance	500	1000	1750	Ω	VBCSO ≥ 3.0V
VBCSO	BCS charge output voltage	3.0	3.3	3.6	V	VCC > VPFD, $\overline{RST}$ inactive, full charge or no load
IOUT1	VOUT current	-	-	160	mA	VOUT ≥ VCC - 0.3V
IOUT2	VOUT current	-	100	-	µA	VOUT ≥ VBC - 0.2V

**Note:** Typical values indicate operation at TA = 25°C, VCC = 5V or VBC.

**Capacitance (TA = 25°C, F = 1MHz, VCC = 5.0V)**

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Conditions
CIN	Input capacitance	-	-	8	pF	Input voltage = 0V
COUT	Output capacitance	-	-	10	pF	Output voltage = 0V

**Note:** This parameter is sampled and not 100% tested.

# bq2202

---

## AC Test Conditions

Parameter	Test Conditions
Input pulse levels	0V to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V (unless otherwise specified)

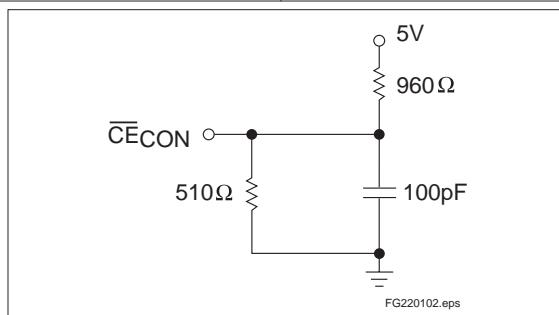


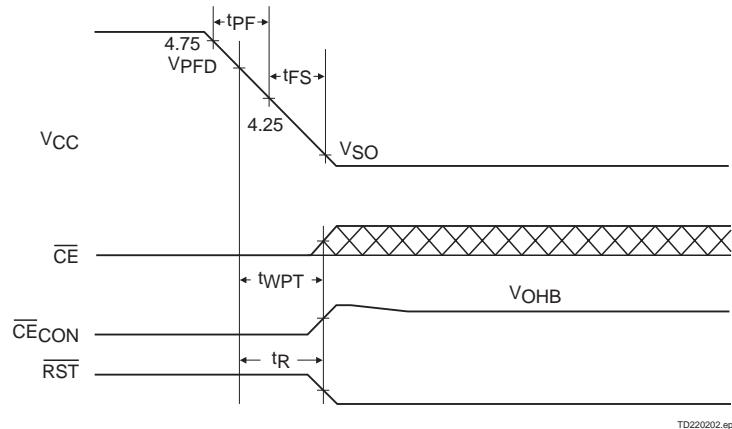
Figure 3. Output Load

## Power-Fail Control ( $T_A = \text{TOPR}$ )

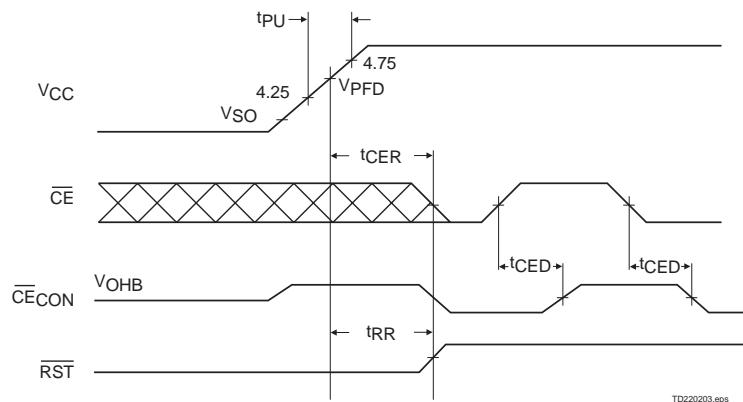
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tPF	$V_{CC}$ slew 4.75 to 4.25V	300	-	-	μs	
tFS	$V_{CC}$ slew 4.25 V to $V_{SO}$	10	-	-	μs	
tPU	$V_{CC}$ slew 4.25 to 4.75V	0	-	-	μs	
tCED	Chip-enable propagation delay	-	7	10	ns	
tCER	Chip-enable recovery time	tRR	-	tRR	ms	Time during which SRAM is write-protected after $V_{CC}$ passes VPFD on power-up
tRR	VPFD to $\overline{RST}$ inactive	40	80	120	ms	Time, after $V_{CC}$ becomes valid, before $\overline{RST}$ is cleared
tAS	Input A set up to $\overline{CE}$	0	-	-	ns	
tWPT	Write-protect time	tR	-	tR	μs	Delay after $V_{CC}$ slews down past VPFD before SRAM is write-protected
tR	VPFD to $\overline{RST}$ active	40	100	150	μs	Delay after $V_{CC}$ slews down past VPFD before $\overline{RST}$ is active

**Note:** Typical values indicate operation at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5\text{V}$ .

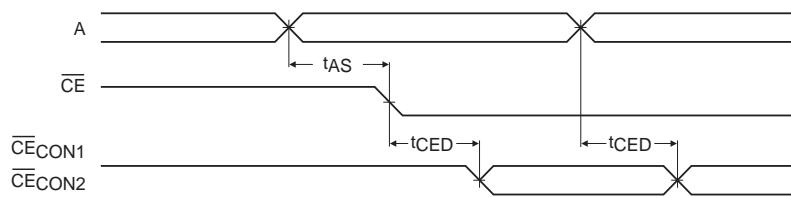
## Power-Down Timing



## Power-Up Timing



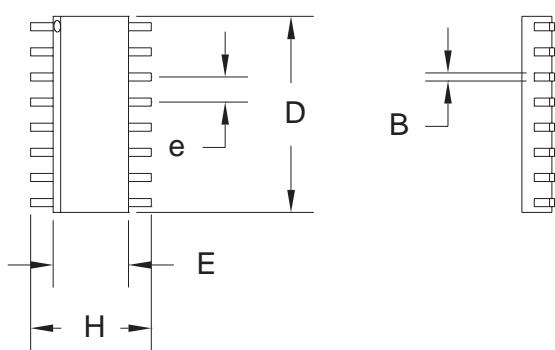
## Address-Decode Timing



## bq2202

---

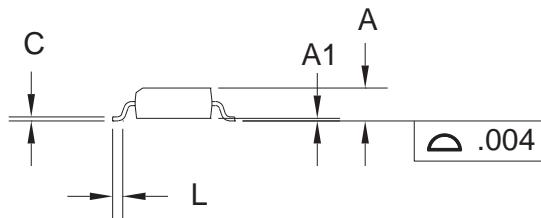
### 16-Pin SOIC Narrow



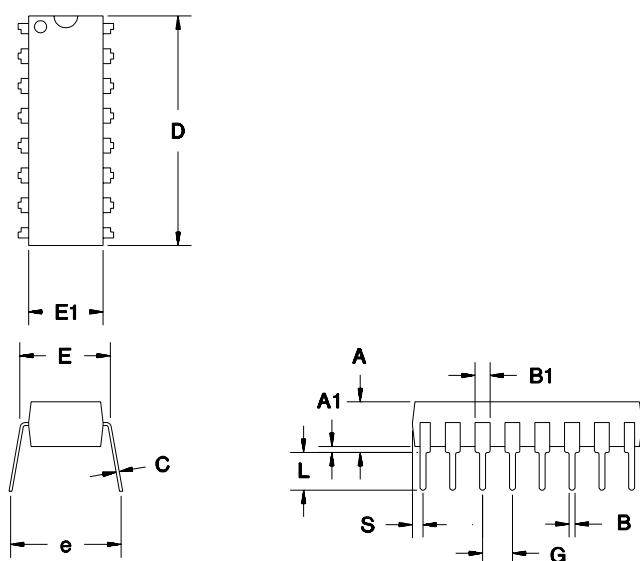
16-Pin SOIC Narrow (SN)

Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.385	0.400
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

All dimensions are in inches.



### 16-Pin DIP Narrow



16-Pin DIP Narrow (PN)

Dimension	Minimum	Maximum
A	0.160	0.180
A1	0.015	0.040
B	0.015	0.022
B1	0.055	0.065
C	0.008	0.013
D	0.740	0.770
E	0.300	0.325
E1	0.230	0.280
e	0.300	0.370
G	0.090	0.110
L	0.115	0.150
S	0.020	0.040

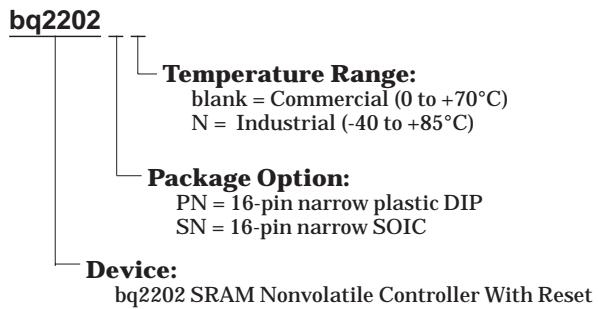
All dimensions are in inches.

## Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	2	Deleted last sentence	Clarification
1	5	VBCSO—BCS charge output voltage	Was: 3.15 min, 3.3 typ, 3.45 max Is: 3.0 min, 3.3 typ, 3.6 max
2	5	Changed maximum charge output internal resistance (RBCS)	Was: $1500\Omega$ Is: $1750\Omega$
3	1, 4, 5	10% supply operation	Was: THS tied to V <sub>OUT</sub> Is: THS tied to V <sub>CC</sub>

**Note:** Change 1 = Dec. 1992 B changes from Sept. 1991 A.  
Change 2 = Nov. 1994 C changes from Dec. 1992 B.  
Change 3 = Sept. 1997 D changes from Nov. 1994 C.

## Ordering Information



### **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1999, Texas Instruments Incorporated