

## MM74HC4538

### Dual Retriggerable Monostable Multivibrator

#### General Description

The MM74HC4538 high speed monostable multivibrator (one shots) is implemented in advanced silicon-gate CMOS technology. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The MM74HC4538 is retriggerable. That is, it may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended.

Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply:  $PW = 0.7(R)(C)$  where PW is in seconds, R is in ohms, and C is in farads. This device is pin compatible with the CD4528, and the CD4538 one shots. All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

#### Features

- Schmitt trigger on A and B inputs
- Wide power supply range: 2–6V
- Typical trigger propagation delay: 32 ns
- Fanout of 10 LS-TTL loads
- Low input current: 1  $\mu$ A max

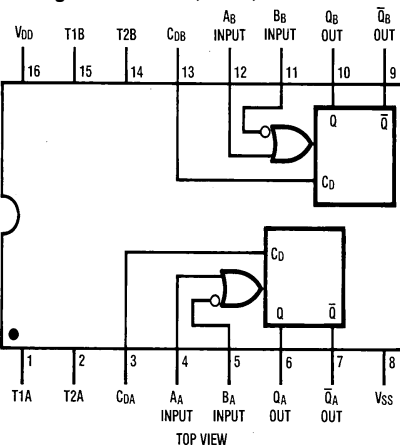
#### Ordering Code:

Order Number	Package Number	Package Description
MM74HC4538M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
MM74HC4538SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4538MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4538N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP

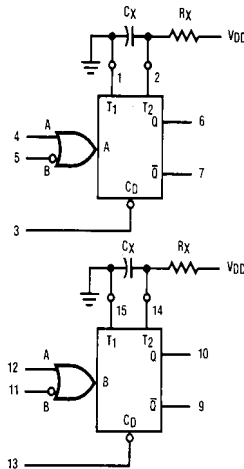


#### Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⌋	⌋
H	↑	H	⌋	⌋

H = HIGH Level  
L = LOW Level  
↑ = Transition from LOW-to-HIGH  
↓ = Transition from HIGH-to-LOW  
⌋ = One HIGH Level Pulse  
⌋ = One LOW Level Pulse  
X = Irrelevant

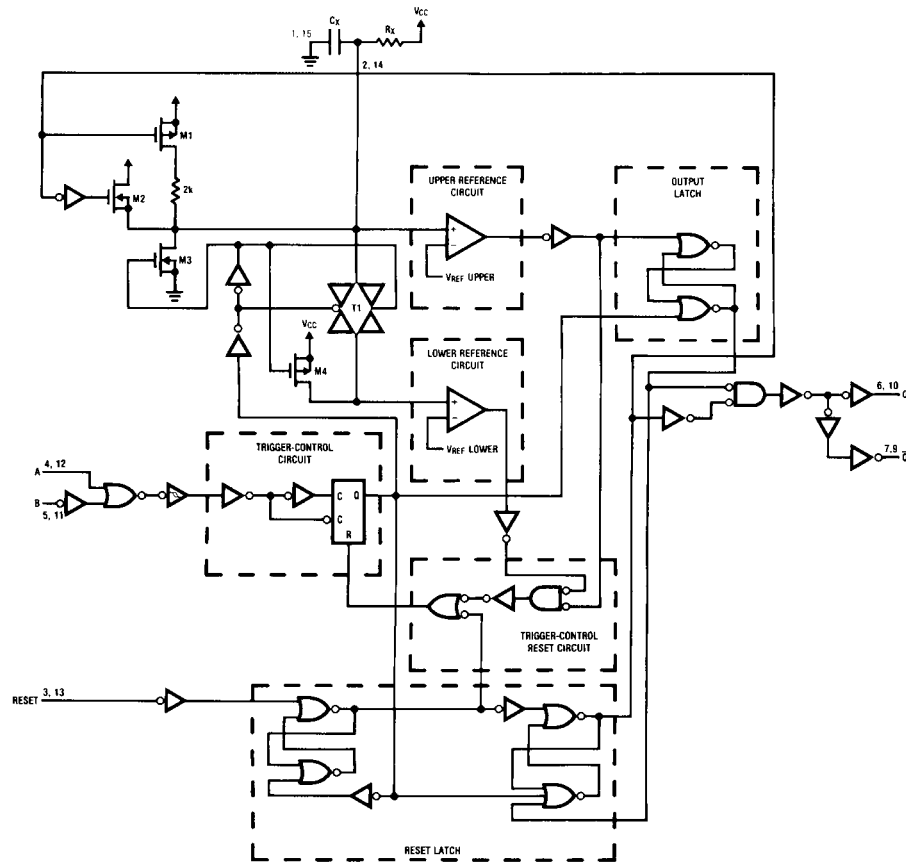
## Block Diagrams



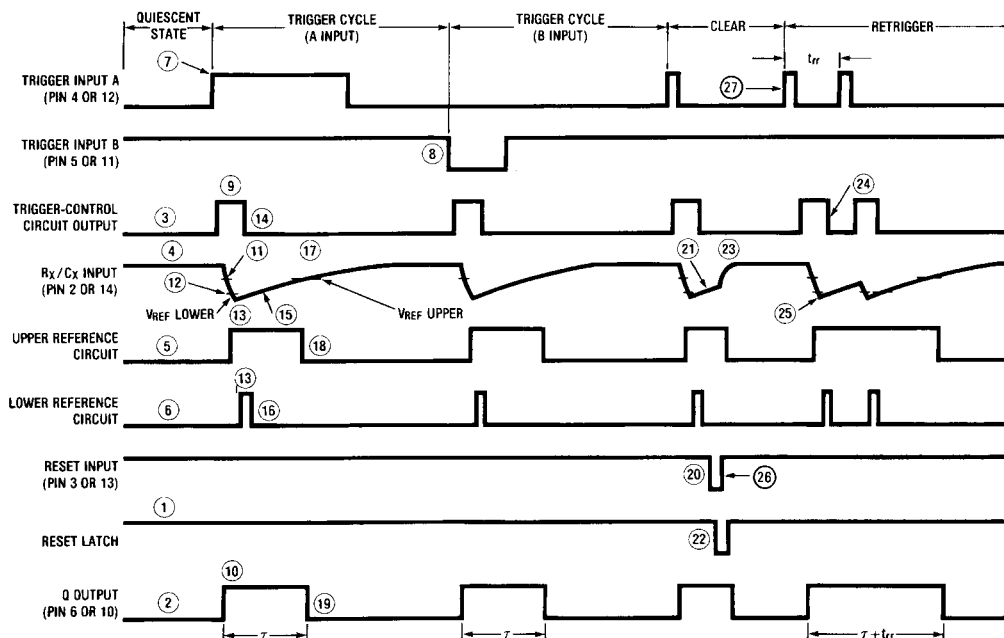
R<sub>X</sub> AND C<sub>X</sub> ARE EXTERNAL COMPONENTS

Note: Pin 1 and Pin 15 must be hard-wired to GND.

## Logic Diagram



## Timing Diagram



## Circuit Operation

The MM74HC4538 operates as follows (refer to logic diagram). In the quiescent state, the external timing capacitor,  $C_X$ , is charged to  $V_{CC}$ . When a trigger occurs, the Q output goes HIGH and  $C_X$  discharges quickly to the lower reference voltage ( $V_{REF\ Lower} = \frac{1}{3} V_{CC}$ ).  $C_X$  then charges, through  $R_X$ , back up to the upper reference voltage ( $V_{REF\ Upper} = \frac{2}{3} V_{CC}$ ), at which point the one-shot has timed out and the Q output goes LOW.

The following, more detailed description of the circuit operation refers to both the logic diagram and the timing diagram.

### QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is HIGH and the reset latch is HIGH (#1 in logic diagram).

Thus the Q output (pin 6 or 10) of the monostable multivibrator is LOW (#2, timing diagram).

The output of the trigger-control circuit is LOW (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor,  $C_X$ , is charged to  $V_{CC}$  (#4), and the upper reference circuit has a LOW output (#5). Transistor M4 is turned ON and transmission gate T1 is turned OFF. Thus the lower reference circuit has  $V_{CC}$  at the noninverting input and a resulting LOW output (#6).

In addition, the output of the trigger-control reset circuit is LOW.

### TRIGGER OPERATION

The MM74HC4538 is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Truth Table. Either trigger signal will cause the output of the trigger-control circuit to go HIGH (#9).

The trigger-control circuit going HIGH simultaneously initiates three events. First, the output latch goes LOW, thus taking the Q output of the HC4538 to a HIGH State (#10). Second, transistor M3 is turned on, which allows the external timing capacitor,  $C_X$ , to rapidly discharge toward ground (#11). (Note that the voltage across  $C_X$  appears at the input of the upper reference circuit comparator.) Third, transistor M4 is turned off and transmission gate T1 is turned ON, thus allowing the voltage across  $C_X$  to also appear at the input of the lower reference circuit comparator.

When  $C_X$  discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be HIGH (#13). The trigger-control reset circuit goes HIGH, resetting the trigger-control circuit flip-flop to a LOW State (#14). This turns transistor M3 OFF again, allowing  $C_X$  to begin to charge back up toward  $V_{CC}$ , with a time constant  $t = R_X C_X$  (#15). In addition, transistor M4 is turned ON and transmission gate T1 is turned OFF. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go LOW (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes LOW.

When  $C_X$  charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference

circuit goes LOW (#18). This causes the output latch to toggle, taking the Q output of the HC4538 to a LOW State (#19), and completing the time-out cycle.

#### RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the HC4538 to a LOW State.

The timing diagram illustrates the case in which reset occurs (#20) while  $C_X$  is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes LOW (#22), turning ON transistor M1. Thus  $C_X$  is allowed to quickly charge up to  $V_{CC}$  (#23) to await the next trigger signal.

Recovery time is the required delay after reset goes inactive to a new trigger rising edge. On the diagram it is shown as (#26) to (#27).

#### RETRIGGER OPERATION

In the retriggerable mode, the HC4538 may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after  $C_X$  has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time,  $t_{rr}$  is a function of internal propagation delays and the discharge time of  $C_X$ :

$$t_{rr}(\text{ns}) \approx 72 + \frac{V_{CC}(\text{volts}) \cdot C_X(\text{pF})}{30.5}$$

at room temperature

#### POWER-DOWN CONSIDERATIONS

Large values of  $C_X$  may cause problems when powering down the MM74HC4538 because of the amount of energy

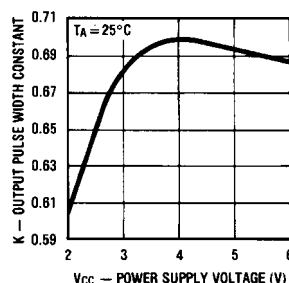
stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from  $V_{CC}$  through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn-off time of the  $V_{CC}$  power supply must not be faster than  $t = V_{CC} \cdot C_X / (30 \text{ mA})$ . For example, if  $V_{CC} = 5\text{V}$  and  $C_X = 15 \mu\text{F}$ , the  $V_{CC}$  supply must turn OFF no faster than  $t = (15\text{V}) \cdot (15 \mu\text{F}) / 30 \text{ mA} = 2.5 \text{ ms}$ . This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of  $V_{CC}$  to zero volts occurs, the MM74HC4538 may sustain damage. To avoid this possibility, use an external clamping diode,  $D_X$ , connected from  $V_{CC}$  to the  $C_X$  pin.

#### SET UP RECOMMENDATIONS

Minimum  $R_X = 1 \text{ k}\Omega$

Minimum  $C_X = 0 \text{ pF}$ .



**Absolute Maximum Ratings** (Note 1)

(Note 2)

Supply Voltage ( $V_{CC}$ )	−0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	−1.5 to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	−0.5 to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{IK}, I_{OK}$ )	±20 mA
DC Output Current, per pin ( $I_{OUT}$ )	±25 mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	±50 mA
Storage Temperature Range ( $T_{STG}$ )	−65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering 10 seconds)	260°C

**Recommended Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )	−40	+85	°C
Input Rise or Fall Times (Reset only)			
( $t_r, t_f$ ) $V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

**Note 1:** Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power Dissipation Temperature Derating: Plastic "N" Package: −12mW/°C from 65°C to 85°C.

**DC Electrical Characteristics** (Note 4)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40 \text{ to } 85^\circ C$		$T_A = -55 \text{ to } 125^\circ C$		Units
				Typ	Guaranteed Limits					
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5		1.5		V
			4.5V		3.15	3.15		3.15		V
			6.0V		4.2	4.2		4.2		V
$V_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5		0.5		V
			4.5V		1.35	1.35		1.35		V
			6.0V		1.8	1.8		1.8		V
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9		1.9		V
			4.5V	4.5	4.4	4.4		4.4		V
			6.0V	6.0	5.9	5.9		5.9		V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0 \text{ mA}$ $ I_{OUT}  \leq 5.2 \text{ mA}$	4.5V		3.98	3.84		3.7		V
			6.0V		5.48	5.34		5.2		V
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1		0.1		V
			4.5V	0	0.1	0.1		0.1		V
			6.0V	0	0.1	0.1		0.1		V
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0 \text{ mA}$ $ I_{OUT}  \leq 5.2 \text{ mA}$	4.5V		0.26	0.33		0.4		V
			6.0V		0.26	0.33		0.4		V
$I_{IN}$	Maximum Input Current (Pins 2, 14) (Note 5)	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0		±1.0		μA
$I_{IN}$	Maximum Input Current (all other pins)	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0		±1.0		μA
$I_{CC}$ Active	Maximum Active Supply Current	Pins 2, 14 = 0.5 $V_{CC}$ Q1, Q2 = HIGH $V_{IN} = V_{CC}$ or GND	6.0V		150	250		400		μA
$I_{CC}$ Quiescent	Maximum Quiescent Supply Current	Pins 2, 14 = OPEN Q1, Q2 = LOW $V_{IN} = V_{CC}$ or GND	6.0V		130	220		350		μA

**Note 4:** For a power supply of 5V ±10% the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**DC Electrical Characteristics** (Continued)

Note 5: The device must be set up with 3 steps before measuring  $I_{IN}$ :

	Clear	A	B
1.	H	L	H
2.	H	H	H
3.	H	L	H

**AC Electrical Characteristics**

$V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15 pF$ ,  $t_r = t_f = 6 ns$

Symbol	Parameter	Conditions	Typ	Limit	Units
$t_{PLH}$	Maximum Propagation Delay A, or B to Q		23	45	ns
$t_{PHL}$	Maximum Propagation Delay A, or B to $\bar{Q}$		26	50	ns
$t_{PHL}$	Maximum Propagation Delay Clear to Q		23	45	ns
$t_{PLH}$	Maximum Propagation Delay Clear to $\bar{Q}$		26	50	ns
$t_W$	Minimum Pulse Width A, B or Clear		10	16	ns

**AC Electrical Characteristics**

$C_L = 50 pF$ ,  $t_r = t_f = 6 ns$  (unless otherwise specified)

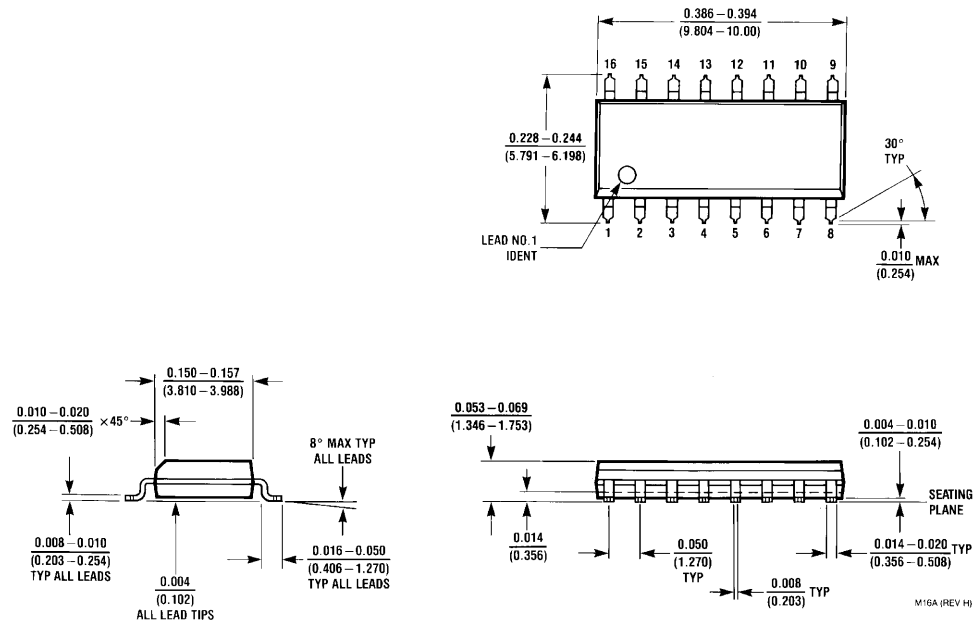
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units
				Typ	Guaranteed Limits			
$t_{PLH}$	Maximum Propagation Delay A, or B to Q		2.0V	100	250	315	373	ns
			4.5V	25	50	63	75	ns
			6.0V	21	43	54	63	ns
$t_{PHL}$	Maximum Propagation Delay A, or B to $\bar{Q}$		2.0V	110	275	347	410	ns
			4.5V	28	55	69	82	ns
			6.0V	23	47	59	70	ns
$t_{PHL}$	Maximum Propagation Delay Clear to Q		2.0V	100	250	315	373	ns
			4.5V	25	50	63	75	ns
			6.0V	21	43	54	63	ns
$t_{PLH}$	Maximum Propagation Delay Clear to $\bar{Q}$		2.0V	110	275	347	410	ns
			4.5V	28	55	69	82	ns
			6.0V	23	47	59	70	ns
$t_{TLH}, t_{THL}$	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	8	13	16	19	ns
$t_r, t_f$	Maximum Input Rise and Fall Time (Reset only)		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
$t_W$	Minimum Pulse Width A, B, Clear		2.0V		80	101	119	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
$t_{REC}$	Minimum Recovery Time, Clear Inactive to A or B		2.0V	-5	0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
$t_{WQ}$	Output Pulse Width	$C_X = 12 pF$ $R_X = 1 k\Omega$	Min	3.0V	283	190		ns
				5.0V	147	120		ns
			Max	3.0V	283	400		ns
				5.0V	147	185		ns
$t_{WQ}$	Output Pulse Width	$C_X = 100 pF$ $R_X = 10 k\Omega$	Min	3.0V	1.2			$\mu s$
				5.0V	1.0			$\mu s$
			Max	3.0V	1.2			$\mu s$
				5.0V	1.0			$\mu s$

**AC Electrical Characteristics** (Continued)

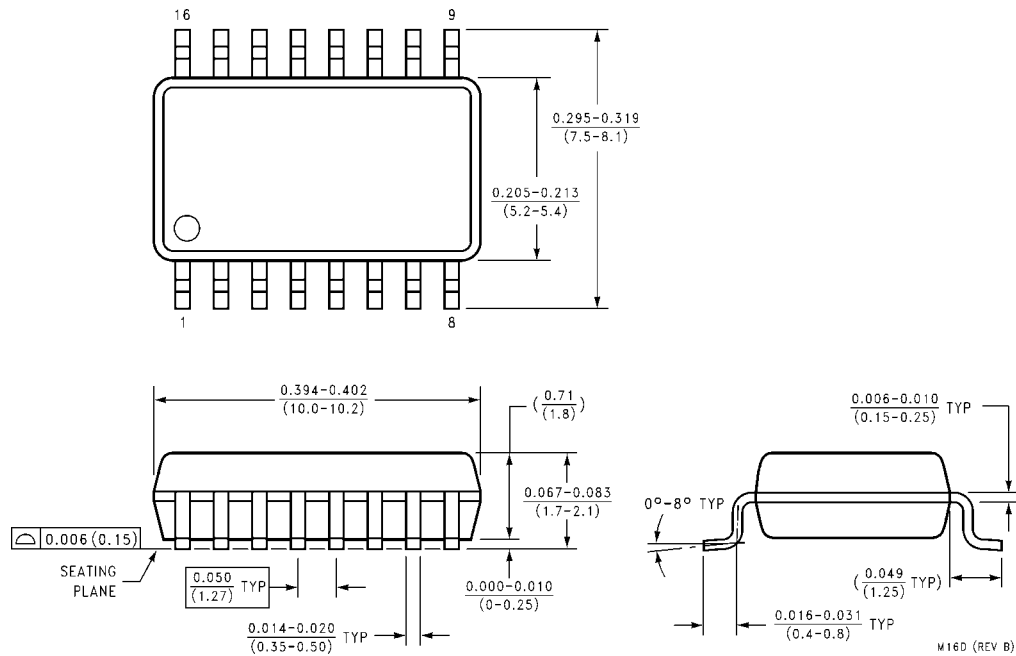
Symbol	Parameter	Conditions	V <sub>CC</sub>	T <sub>A</sub> = -25°C		T <sub>A</sub> = -40 to 85°C	T <sub>A</sub> = -55 to 125°C	Units
				Typ	Guaranteed Limits			
t <sub>WQ</sub>	Output Pulse Width	C <sub>X</sub> = 1000 pF R <sub>X</sub> = 10 kΩ	Min	3.0V	10.5	9.4		μs
				5.0V	10.0	9.3		μs
			Max	3.0V	10.5	11.6		μs
				5.0V	10.0	10.7		μs
t <sub>WQ</sub>	Output Pulse Width	C <sub>X</sub> = 0.1 μF R <sub>X</sub> = 10k	Min	5.0V		0.63	0.602	ms
			Max	5.0V		0.77	0.798	ms
C <sub>IN</sub>	Maximum Input Capacitance (Pins 2 & 14)			25				pF
C <sub>IN</sub>	Maximum Input Capacitance (other inputs)			5	10	10	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 6)	(per one shot)		150				pF
Δt <sub>WQ</sub>	Pulse Width Match Between Circuits in Same Package			±1				%

**Note 6:** C<sub>PD</sub> determines the no load dynamic consumption, P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>, and the no load dynamic current consumption, I<sub>S</sub> = V<sub>CC</sub> f + I<sub>CC</sub>.

# Physical Dimensions inches (millimeters) unless otherwise noted

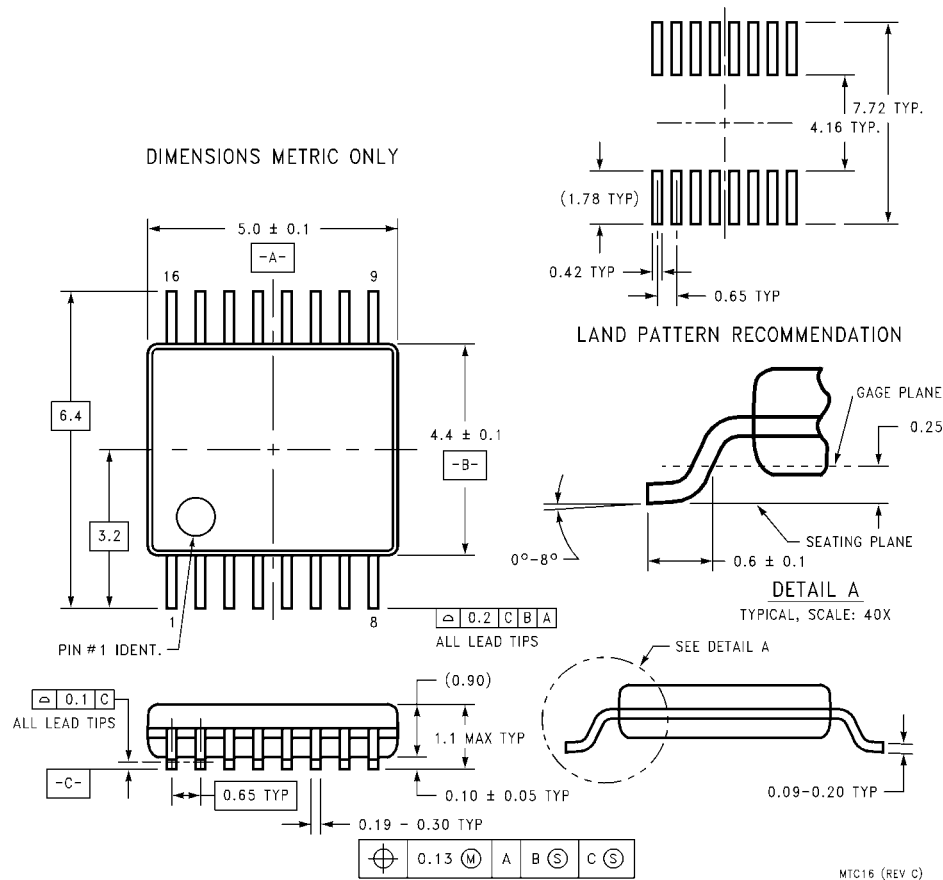


**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body  
Package Number M16A**



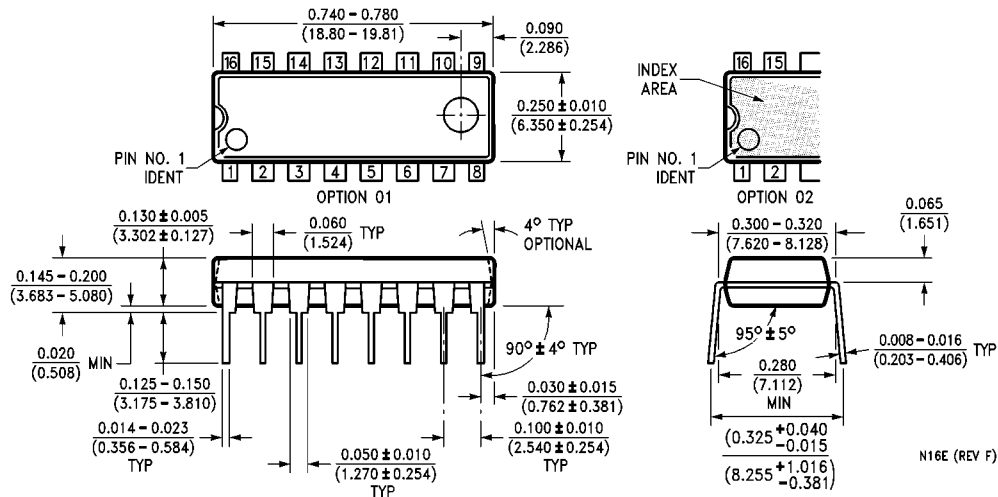
**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M16D**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)


**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N16E

N16E (REV F)

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