

## 2 CHANNEL BRIDGE DRIVER IC

## ■ GENERAL DESCRIPTION

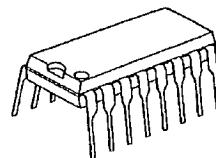
The NJW4301 is a 2 channel bridge driver for CD, CD-ROM, MO and others. It operates at more than 4V, and then features high output voltage swing.

Its output circuit consists of MOS-FET. The MOS-FET type output realizes lower consumption than bipolar type output, so that radiation design becomes simple and total costs are reduced.

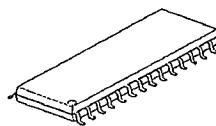
## ■ FEATURES

- Operating Voltage ( $V^+ = 4V \sim 12V$ )
- Low Saturation Output ( $V_{sat} = \pm 0.5V_{MAX.}$  at  $I_o = 300mA$ )
- Supply Current (35mA MAX.)
- 2 channel BTL Output
- Mute Function
- Bi-MOS Technology
- Package Outline DIP16, SDMP30

## ■ PACKAGE OUTLINE

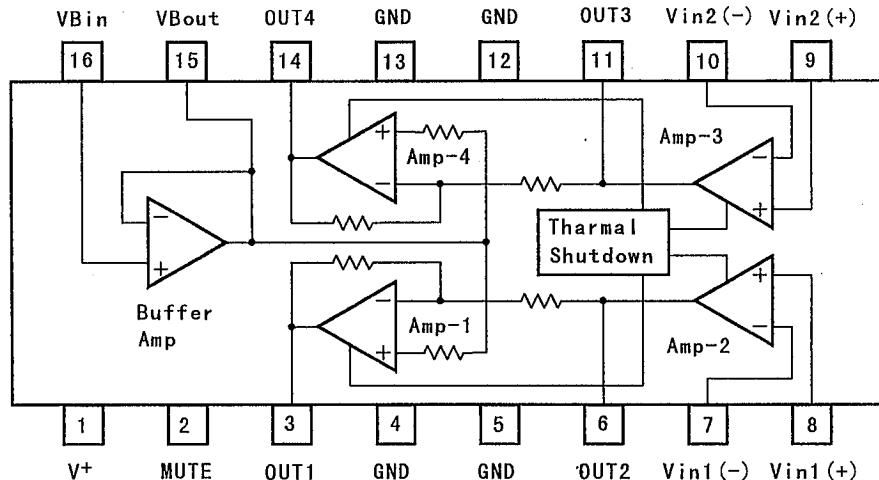


NJW4301D



NJW4301M

## ■ BLOCK DIAGRAM



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(Package DIP-16)

## ■ ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

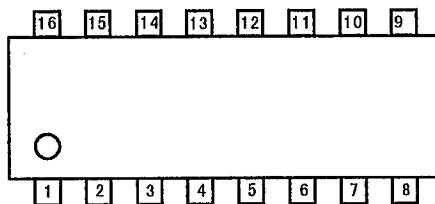
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V <sup>+</sup>	15	V
Operating Current	I <sub>o</sub>	1	A
Mute Terminal Current	I <sub>M</sub>	1.0	mA
Power Dissipation	P <sub>o</sub>	(DIP16) 1.9 (SDMP30) 1.8 (note 1)	W
Operating Temperature Range	T <sub>op</sub>	-40~+85	°C
Storage Temperature Range	T <sub>stg</sub>	-40~+150	°C

(note 1) At on PC board.

## ■ ELECTRICAL CHARACTERISTICS (V<sup>+</sup> = 5V, Ta = 25°C)

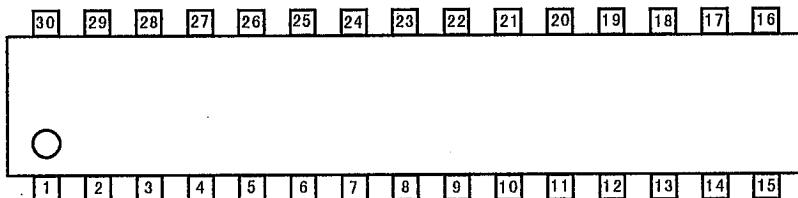
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
[ALL]						
Operating Supply Voltage Range	V <sup>+</sup>		4	5	12	V
Mute OFF Current Dissipation	I <sub>cc1</sub>	V <sub>M</sub> =4.2V, V <sub>IN</sub> =2.5V	-	20	35	mA
Mute ON Current Dissipation	I <sub>cc2</sub>	V <sub>M</sub> =0V, V <sub>IN</sub> =2.5V	-	2	3.5	mA
[POWER AMPLIFIER]						
Output Offset Voltage	V <sub>OF</sub>	OUT1-OUT2, GAIN=1 OUT4-OUT3, GAIN=1	-50	-	50	mV
Input Common Mode Voltage Range	V <sub>ICM</sub>	AMP2 AMP3	0	-	V <sup>+</sup>	V
Input Bias Current	I <sub>B</sub>	AMP2 AMP3	-	-	300	nA
Maximum Output Voltage 1	V <sub>o1</sub>	OUT1-OUT2, I <sub>L</sub> =300mA OUT4-OUT3, I <sub>L</sub> =300mA	4.0	4.2	-	V
Maximum Output Voltage 2	V <sub>o2</sub>	OUT1-OUT2, I <sub>L</sub> =500mA OUT4-OUT3, I <sub>L</sub> =500mA	3.0	3.5	-	V
Open Loop Voltage Gain	A <sub>V</sub>	AMP2, R <sub>L</sub> =2kΩ, V <sub>IN</sub> =2.5V AMP3, R <sub>L</sub> =2kΩ, V <sub>IN</sub> =2.5V	35	50	-	dB
[BUFFER AMPLIFIER]						
Input Output Potential Difference	V <sub>BIO</sub>		-30	0	30	mV
Input Voltage Range	V <sub>BICM</sub>		1.5	2.5	3.5	V
Output Voltage Range	ΔV <sub>BO</sub>	V <sub>IN</sub> =2.5V, I <sub>L</sub> =-5mA V <sub>IN</sub> =2.5V, I <sub>L</sub> =+5mA	-	-	-50	mV
[MUTING]						
Mute OFF Voltage	V <sub>MH</sub>		3.5	4.2	-	V
Mute ON Voltage	V <sub>ML</sub>		-	0.8	1.0	V
Mute Sink Current	I <sub>M</sub>	V <sub>M</sub> =5V	70	100	130	μA

## ■ PIN CONFIGURATION



D I P - 1 6

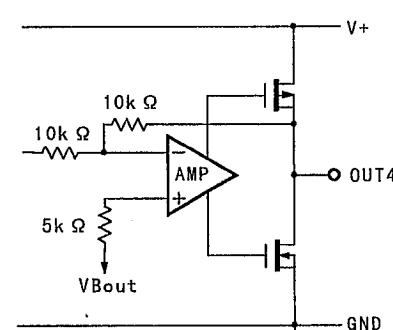
1 : V <sup>+</sup>	9 : V <sub>in</sub> 2 (+)
2 : MUTE	10 : V <sub>in</sub> 2 (-)
3 : OUT 1	11 : OUT 3
4 : GND	12 : GND
5 : GND	13 : GND
6 : OUT 2	14 : OUT 4
7 : V <sub>in</sub> 1 (-)	15 : V <sub>Bout</sub>
8 : V <sub>in</sub> 1 (+)	16 : V <sub>Bin</sub>



S D M P - 3 0

1 : GND	16 : GND
2 : GND	17 : GND
3 : OUT 4	18 : OUT 2
4 : NC	19 : NC
5 : NC	20 : NC
6 : V <sub>Bout</sub>	21 : V <sub>in</sub> 1 (-)
7 : V <sub>Bin</sub>	22 : V <sub>in</sub> 1 (+)
8 : NC	23 : NC
9 : V <sup>+</sup>	24 : V <sub>in</sub> 2 (+)
10 : MUTE	25 : V <sub>in</sub> 2 (-)
11 : NC	26 : NC
12 : NC	27 : NC
13 : OUT 1	28 : OUT 3
14 : GND	29 : GND
15 : GND	30 : GND

## ■ TERMINAL EXPLANATION

PIN NO.		PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
DIP	SDMP - 1 6			
	4 5 1 2 1 3	G N D	Recommend expand- ing the island in order to heat ra- diation proper- ties.	
1 4	3	O U T 4	Output terminal of AMP. 4. OUT4 signal is op- posite phase a- gainst OUT3.	
—	4 5 8 1 1 1 2 1 9 2 0 2 3 2 6 2 7	N C	Non-connection terminal. Recommend connect- ing to GND.	

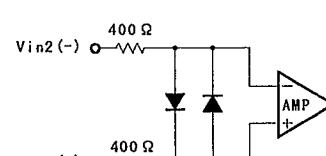
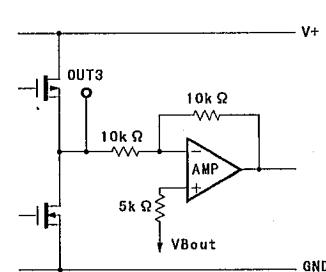
## ■ TERMINAL EXPLANATION

PIN NO.		PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
DIP	SDMP			
—16	—30	15 6	V Bout	An buffer amplifier output.
16	7	16 7	V Bin	An buffer amplifier input.
1	9	1 9	Vcc	Supply Voltage.
2	10	2 10	MUTE	An mute input. Pulldown by 50kΩ (TYP) resistor.

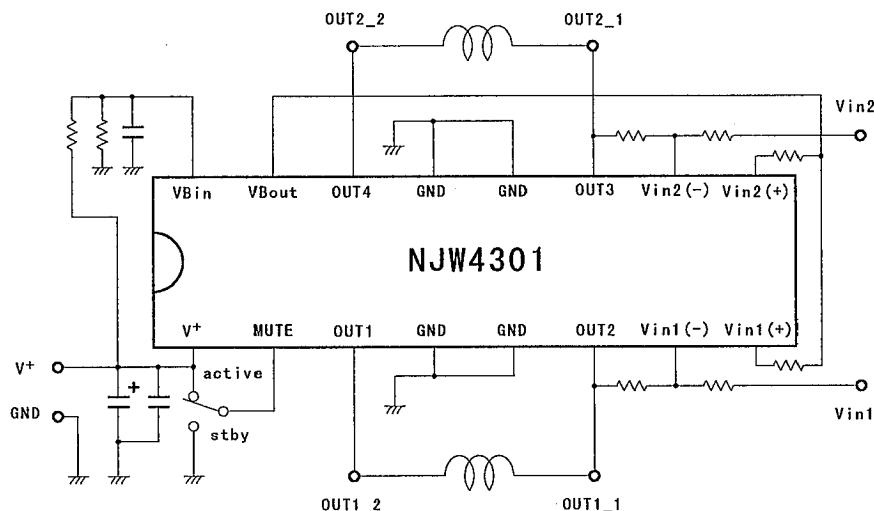
## ■ TERMINAL EXPLANATION

PIN NO.		PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
DIP	SDMP - 1 6	1 3	OUT 1	Output terminal of AMP. 1. OUT1 signal is opposite phase against OUT2.
6	1 8	1 8	OUT 2	Output terminal of AMP. 2.
7	2 1	2 1	Vin1(-)	Inverting input terminal of AMP. 2.
8	2 2	2 2	Vin1(+)	Non-inverting input terminal of AMP. 2.

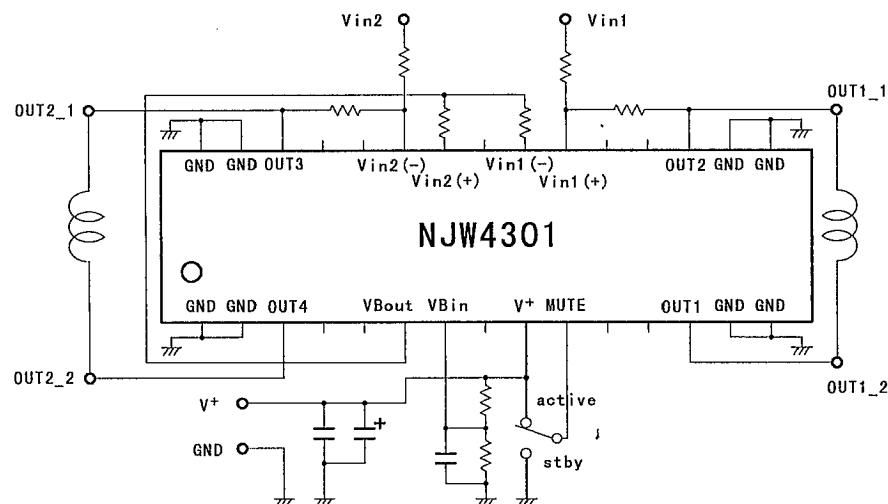
## ■ TERMINAL EXPLANATION

PIN NO.		PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
DIP	SDMP -16			
9	24	Vin2(+)	Inverting input terminal of AMP. 3.	
10	25	Vin2(-)	Non-inverting input terminal of AMP. 3.	
11	28	OUT3	Output terminal of AMP. 3.	

## ■ APPLICATION CIRCUITS

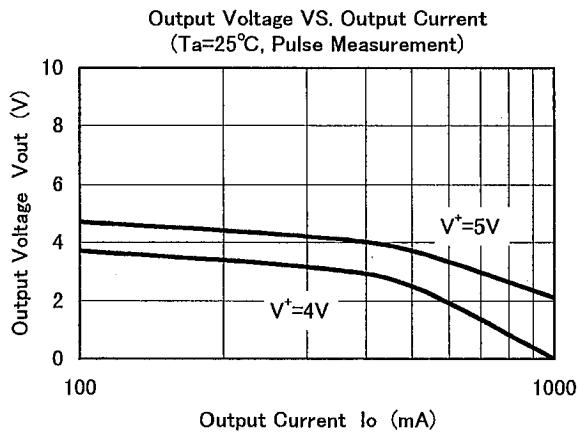
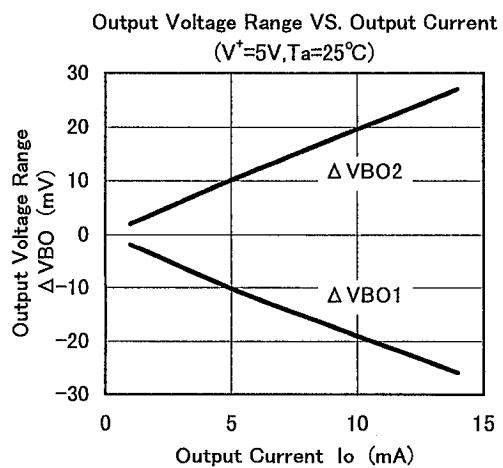
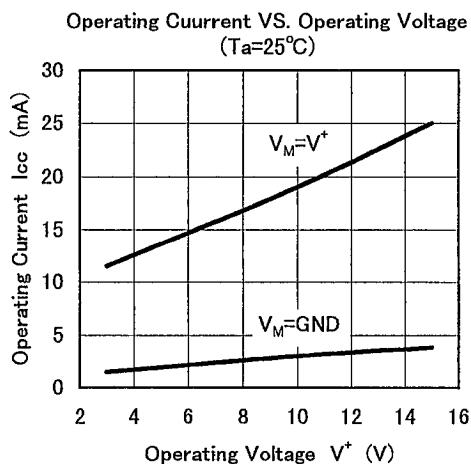
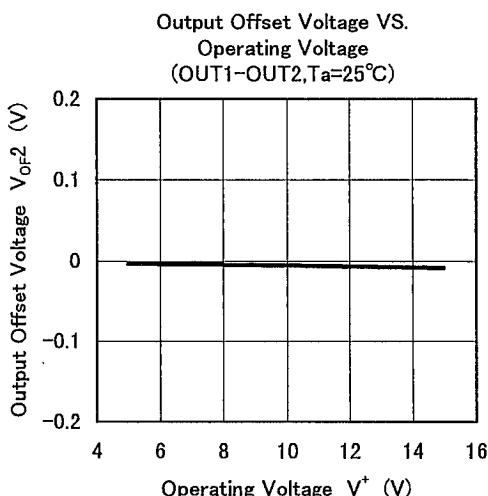
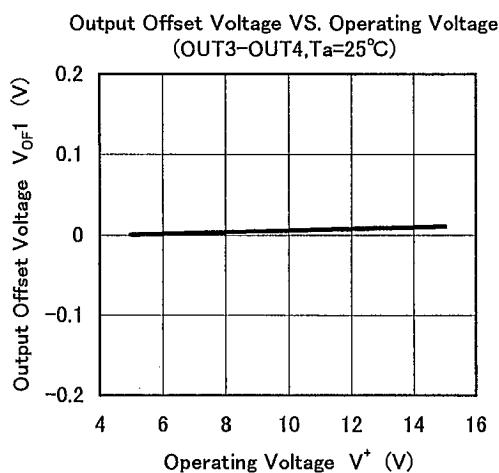


NJW4301 (DIP-16) Application Circuit

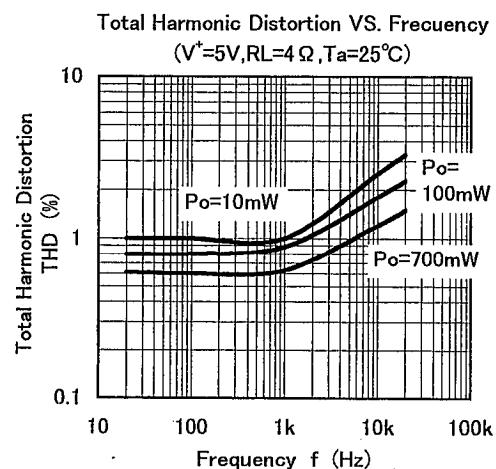
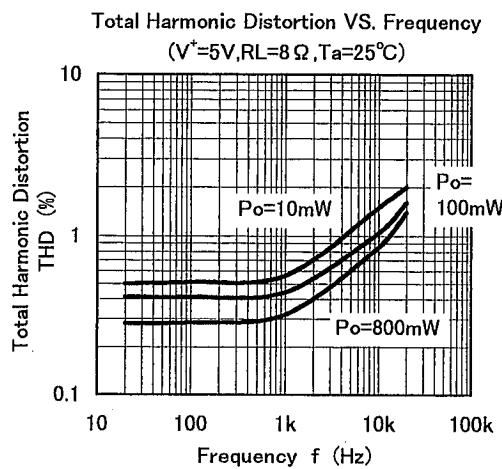
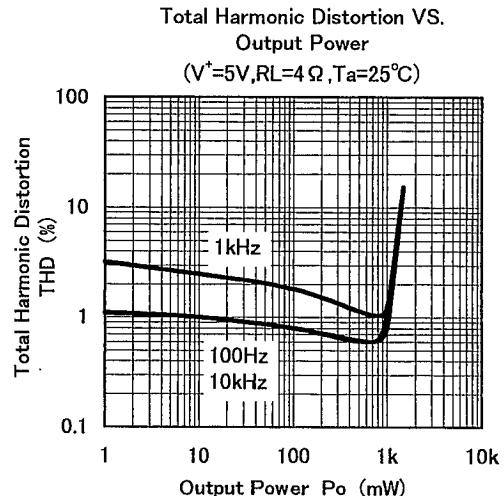
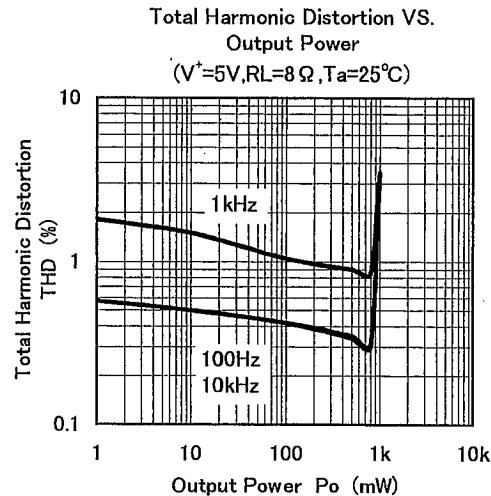


### NJW4301 (SDMP-30) Application Circuit

## ■ TYPICAL CHARACTERISTICS



## ■ TYPICAL CHARACTERISTICS



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## MEMO

<注意事項>  
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