Product Datasheet

January 1997 Version 4.25

MB86680B

ATM Switch Element (SRE)

FML/NPD/SRE/DS/1265

The FUJITSU MB86680B is a self-routing switch element for use in ATM switch fabrics. It is ideally suited to applications in a variety of customer premises equipment such as ATM hubs and network access controllers. The device is organized as a 4 x 4 switch with separate input and output ports for matrix expansion. The main features of the device are listed below:-

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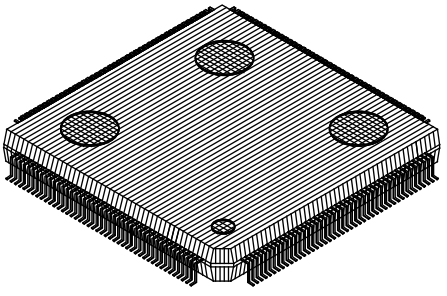
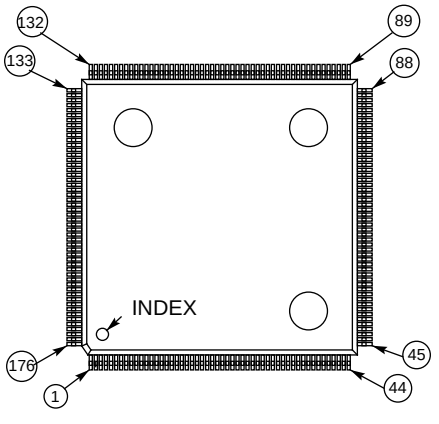
SQFP176



PIN ASSIGNMENT



Features

- Highly integrated 4x4 structure.
- Active matrix expansion ports for row and column interconnect.
- Selectable high and low priority output queues.
- Output port buffer capacity of 75 cells, which can be divided into a 50 cell low priority queue and a 25 cell high priority queue.
- Multicast support.
- Selective cell discard based on CLP bit and selectable queue level.
- Selectable Explicit Forward Congestion Indication (EFCI) function.
- Flexible tag processing to allow a variety of switch fabric architectures to be realized.
- All input / output ports operate at up to 20MHz using an 8-bit data format.
- Separate input clock signals for each interface.
- Separate cell synchronization signals for each port.
- JTAG pins compatible with IEEE1149.1 are provided.
- Fabricated in sub-micron CMOS technology with CMOS/TTL compatible I/O and a single +5V power supply.

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1 Introduction

1.1 Outline

The Fujitsu MB86680B is a Self-Routing ATM cell switch Element (SRE) which can be used as a basic building block for a variety of 155Mb/s ATM switch fabrics.

The device provides 4 output data queues, one for each output port and each with an aggregate storage capacity of 75 cells per output port. A 24 bit routing tag is used to decide into which output queue a particular cell will be loaded.

Each output queue is divided into a high and low priority section. A control bit in the routing tag determines the cell priority. High priority cells will always be forwarded in preference to low priority cells. Hence cells using the high priority queues will suffer less queueing delay and will have a lower cell loss rate than cells using the low priority queues (assuming that high priority traffic only forms a small portion of total traffic).

The switch element includes four expansion inputs, which are provided to facilitate easy expansion in the form of a matrix. Cells received via the expansion inputs are directed into the attached output data queue.

1.2 Matrix Configuration

Various interconnection topologies can be applied to the SRE. However, the device is ideally suited to interconnection in the form of a matrix. In this case the SRE provides re-timed active outputs which allow direct connection to nearest neighbours. This eliminates the need for passive buses and reduces device interconnect problems at the board level. A matrix architecture is illustrated in Figure 1.

The number of switch elements required for an N x N switch is proportional to N^2 and hence is only appropriate for relatively small switch fabrics (e.g. 32 X 32). For larger switches, individual matrices can be interconnected using a multi-path delta arrangement.

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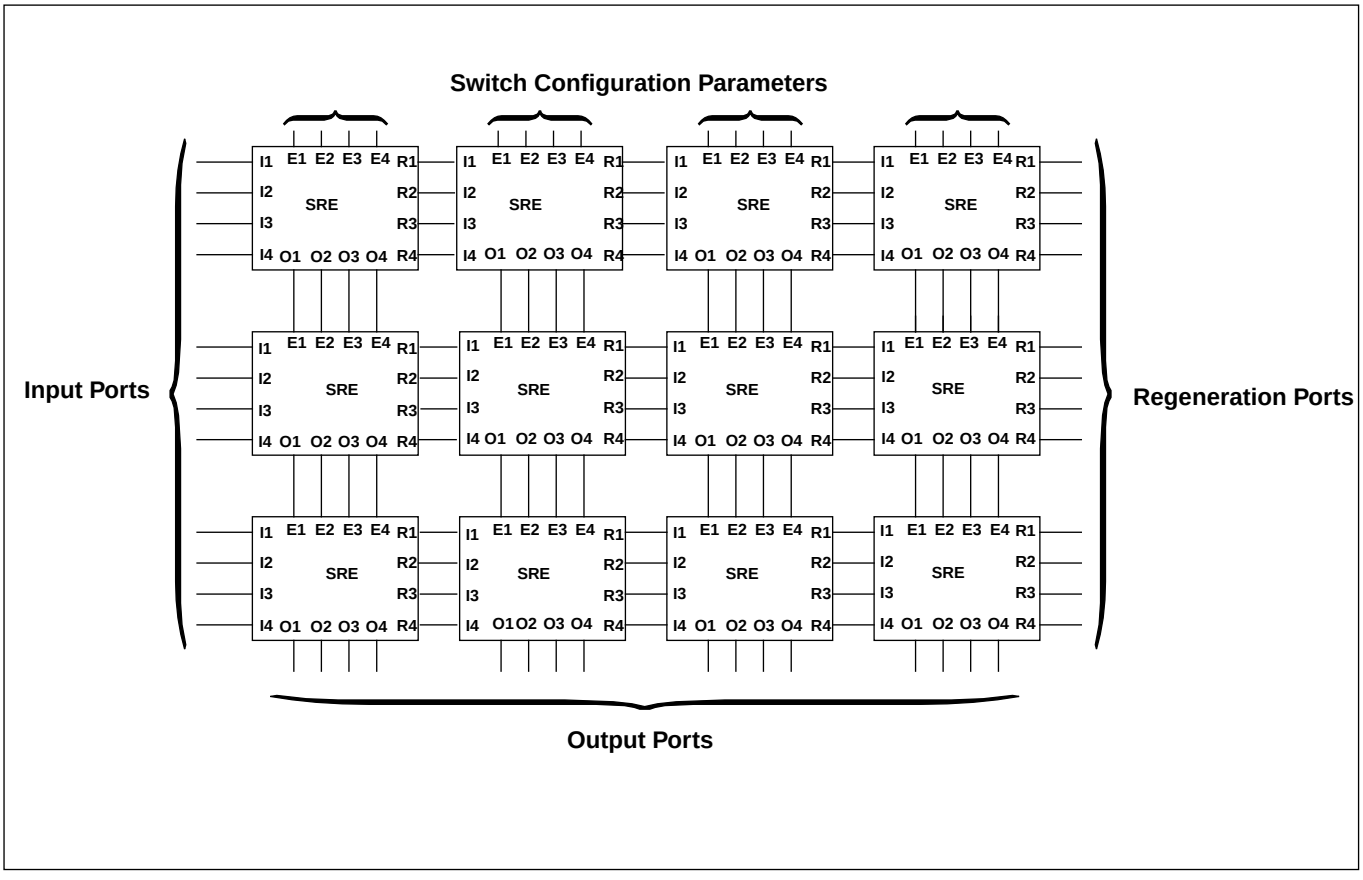

Figure 1 SRE Matrix Interconnect

1.3 Delta Configuration

Larger switches may be realized by connecting SRE matrices into switch topologies similar to the two stage delta configuration as illustrated in Delta Switch Configuration.

Each switch element allows a selectable region of the tag field to be used for address filtering.
This is illustrated in Delta Switch Configuration where SRE elements in stages 1 and 2 are configured with different Address Location Fields. Consequently, stage 2, SRE switch elements are configured to examine a different portion of the ATM cell's routing tag from that examined by SRE elements in stage 1.

As a consequence of the selectable address field multi-path, delta switches can be constructed without the need for intermediate address translation/tag generation.

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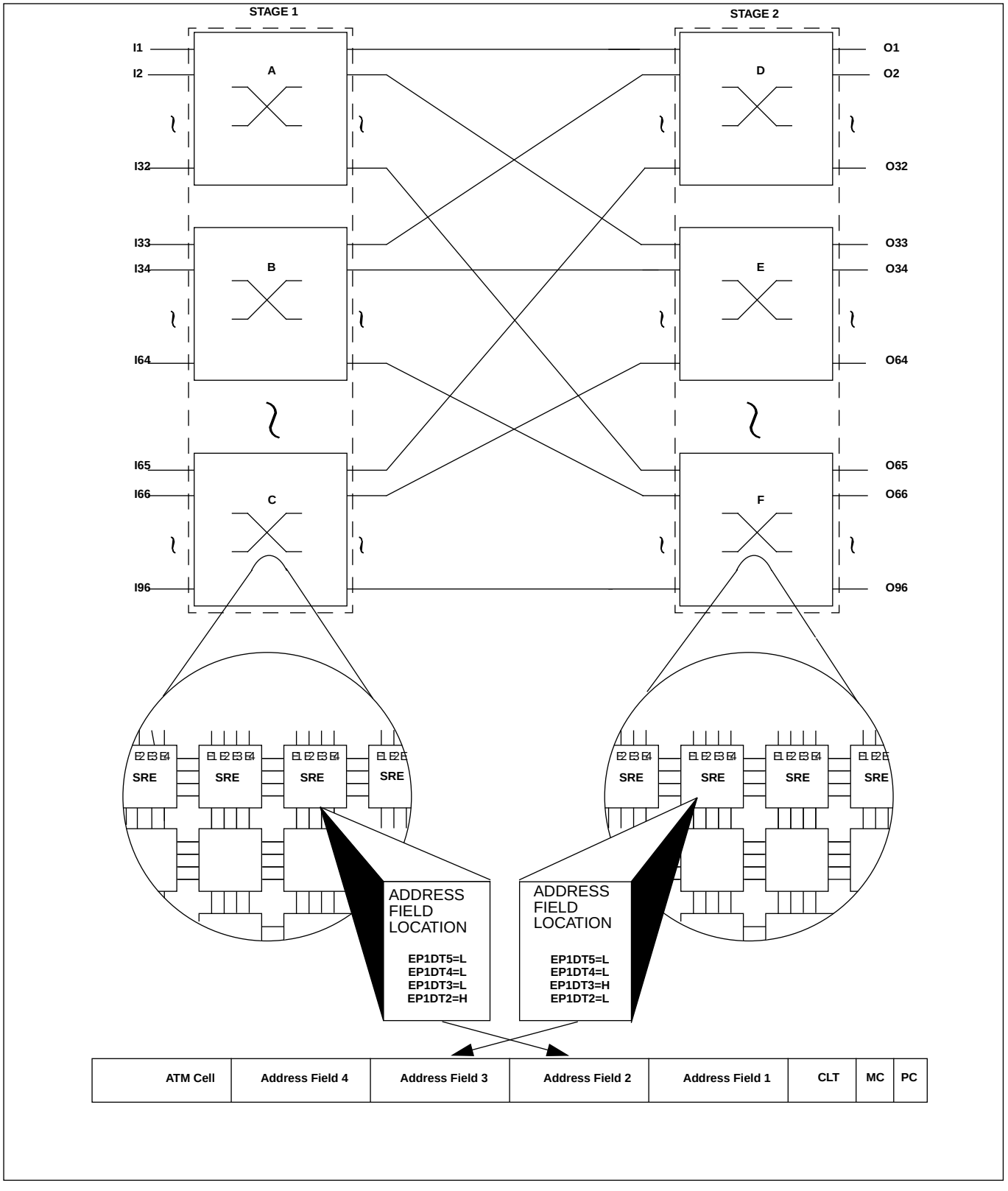

Figure 2 Delta Switch Configuration

2 External Interfaces

2.1 Logical Outline

A logical view of the MB86680B's external pins is illustrated in Figure 3 and a physical pin assignment is shown in Appendix D.

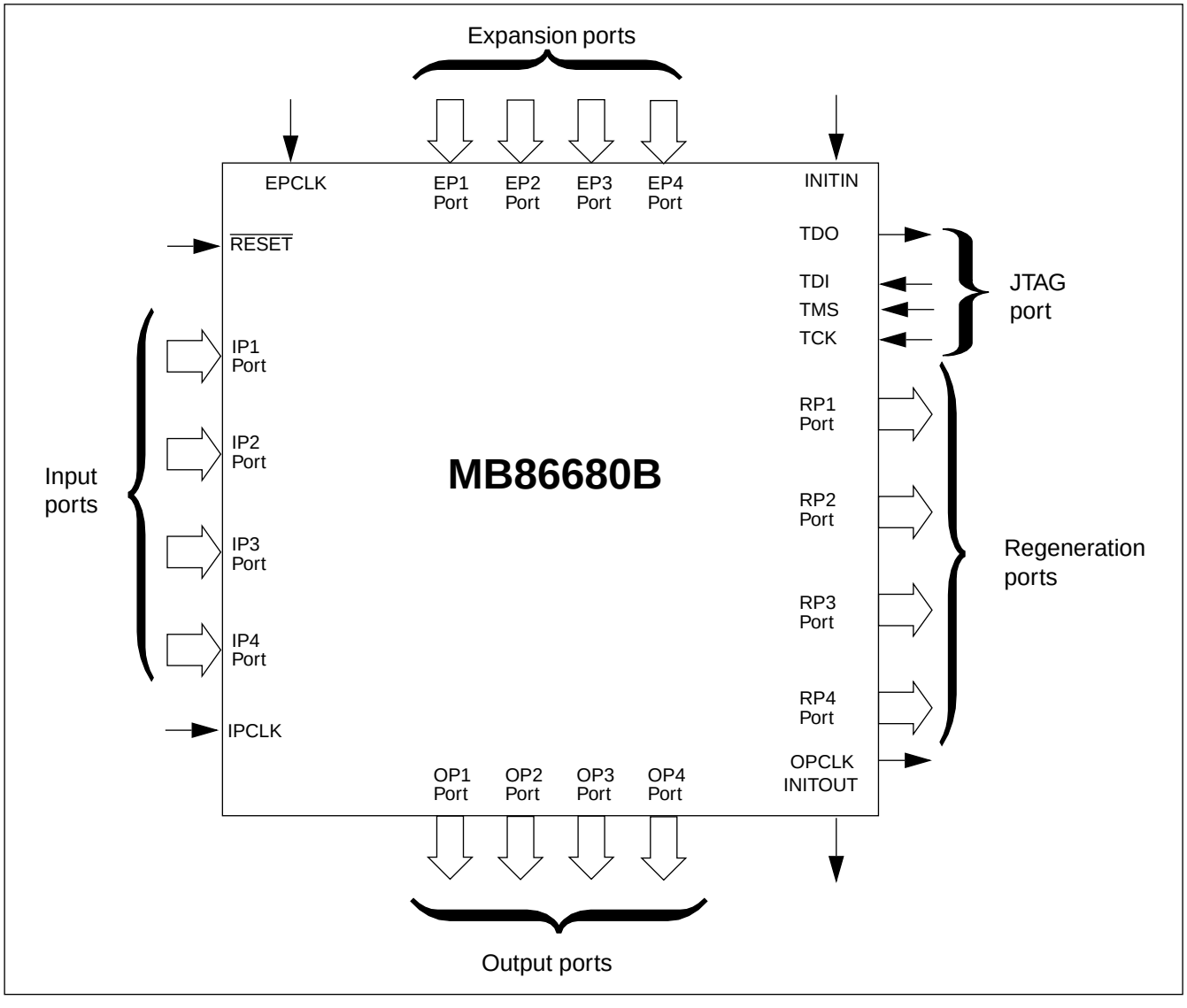

Figure 3 MB86680B I/O Block Diagram

2.2 Detailed Description

A brief description of each of the MB86680B's input and output pins shall now be given.

$\overline{\text{RESET}}$
An active low pulse applied to the MB86680B's $\overline{\text{RESET}}$ pin will cause an MB86680B switch element to execute an internal Reset instruction cycle. The instruction will only be executed when a clock signal is applied to the IPCLK pin. A minimum of 2 IPCLK clock cycles will be required to complete the Reset instruction cycle.

IPCLK
Data present on the input ports IP1DTx to IP4DTx is sampled on the rising edge of this clock. This clock needs to be present if a complete Reset instruction cycle is to be executed following an active low transition on the $\overline{\text{RESET}}$ pin.

EPCLK
Data present on the input ports EP1DTx to EP4DTx is sampled on the rising edge of this clock.

The EPCLK input pin can also be used by an MB86680B switch element to determine whether the switch element should act as **Master** or as a **Slave**. If the EPCLK input pin is permanently tied to V_{SS} then the switch element is deemed to be a Master switch element.

If however a clock is present on the EPCLK input pin then the MB86680B switch element is deemed to be a Slave switch element.

INPUT PORTS (IPxSOC, IPxDTx)
The device comprises four primary input ports, (IP1SOC, IP1DTx) to (IP4SOC, IP4DTx), each of which is organized as 8-bit parallel data together with a start of cell (IPxSOC) bit. All primary input data is sampled on the rising edge of an input clock signal (IPCLK). Incoming data comprises a 3 byte routing tag followed by a 53 byte ATM cell.

Any unused I-input ports should have their unused IPxSOC pin tied to V_{SS}.

EXPANSION PORTS (EPxSOC, EPxDTx)
The four expansion ports, (EP1SOC, EP1DTx) to (EP4SOC, EP4DTx), are provided for column interconnect in a matrix architecture. The data format on the expansion ports is similar to the primary input port format, except that data is synchronized to an expansion port clock (EPCLK), which is usually provided by the vertically opposite nearest neighbour switch element.

Master Switch elements at the top of each column do not need their expansion ports, in this case, the input pins will take on different functions in order to allow the routing tag characteristics to be defined. Pin functions are described in Section 3.5.

The alternative functions are selected by connecting the EPCLK input signal to V_{SS}.

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Any unused Expansion ports should have their unused EPxSOC pin tied to V_{SS}.

INITIN
The INITIN is used by Slave MB86680B switch elements to acquire configuration data immediately following a RESET instruction cycle.

The configuration data may be supplied via the INITOUT pin of a Master switch element or from a device emulating the configuration capability of a Master switch element.

When the MB86680B switch element is deemed to be Master i.e its EPCLK input is tied to V_{SS}, the INITIN pin is not used and should be tied to $V_{DD.}$

INITOUT
The INITOUT pin is used by Master switch elements to convey the configuration data, acquired through their Expansion port pins, in a serial format to the attached Slave elements.

Slave switch elements do not use their INITOUT pin. When a switch element is configured as a Slave, the INITOUT pin is driven permanently high.

Following an active low transition on the $\overline{\text{RESET}}$ pin the INITOUT pin shall be driven to it's logic "1" state.

REGENERATION PORTS (RPxSOC, RPxDTx)
Four regeneration ports, (RP1SOC, RP1DTx) to (RP4SOC, RP4DTx), are provided for matrix interconnection. The Regeneration port data is logically identical to primary input port data but is re-timed to an output clock (OPCLK) which can be directly connected to the IPCLK input of the next horizontally adjacent switch element.

The Flexible Transmission Mode (FTM) feature of the SRE permits the synchronous transmission of the Regeneration-Port data to take place on either the rising or falling edge of the OPCLK.

Following a $\overline{\text{RESET}}$ instruction cycle the Regeneration-Port pins are driven to their logic "0" state.

OUTPUT PORTS (OPxSOC, OPxDT)
Four output ports, (OP1SOC, OP1DTx) to (OP4SOC, OP4DTx), provide the primary switch output data. The data format is identical to all other ports.

As in the case of the Regeneration-Port data, the Flexible Transmission Mode (FTM) feature of the SRE permits the synchronous transmission of the Output-Port data to take place on either the rising or falling edge of the OPCLK.

Following a $\overline{\text{RESET}}$ instruction cycle the Output-Port pins are driven to their logic "0" state.

When no data is being output the SRE shall drive these outputs to their logic "0" state.

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TCK
The TCK input pin provides the clock signal for the JTAG internal test logic. Data received on the TDI input pin shall be sampled on the rising edge of TCK clock signal.

TMS
The TMS input pin shall be sampled on the rising edge of the TCK clock and decoded by the JTAG internal test logic to control test operations.

An External pull-up should be connected to this input to ensure that when this input is not driven, a response identical to the application of a logical 1 results.

TDI
The TDI input pin shall provide a port through which JTAG serial test data and instructions may be received by the internal test logic.

An External pull-up should be connected to this input to ensure that when this input is not driven, a response identical to the application of a logical “1” results.

TDO
The TDO output pin represents a tristate serial output JTAG port through which test instructions and data from the internal test logic may be conveyed. Changes in the state of the signal driven through TDO shall only occur following the falling edge of TCK.When no signal is being driven through the TDO port the output pin should revert to its tristate condition.

Immediately following power-up the TDO output pin shall remain in its undriven tristate.

TST1..TST4
Four test pins are provided for internal use only. It is recommended that test pins TST1, TST2 and TST3 are connected to $V_{SS.}$

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3 Initialization and Configuration

3.1 Overview

A block diagram of the switch element is illustrated in Figure 4. From this, it can be seen that each of the I-input ports is connected in parallel to an address filter via a high speed multiplexer. The address filter processes the address bits contained in a 24 bit routing tag and if appropriate, the associated cell will be routed through to the desired FIFO buffer. The MB86680B switch element permits each output FIFO to be sub-divided into a high and low priority section. The address filter examines each received cell's routing tag to determine its priority level.

Each output port is serviced by a High/ Low priority multiplexer which removes cells from the high and low priority queues. The multiplexer will always give preference to high priority cells.
The above functions are described in more detail in the following paragraphs.

3.2 Reset Operation

The MB86680B provides an active low $\overline{\text{RESET}}$ pin. Asynchronous transitions on this pin are captured internally by the MB86680B and synchronized to the IPCLK clock. The internal synchronous $\overline{\text{RESET}}$ operation of the MB86680B is deemed to be complete 2 IPCLK clock periods after the removal of the active low $\overline{\text{RESET}}$ signal.

All outputs shall be reset to their inactive states within 2 IPCLK clock periods after an active low pulse has been applied to the $\overline{\text{RESET}}$ pin.

The MB86680B requires the presence of the IPCLK clock signal to complete a $\overline{\text{RESET}}$ operation.

3.3 Initialization.

The Configuration Manager block illustrated in Figure 4 is responsible for initialising an MB86680B switch element. An MB86680B switch element may be initialised/configured by one of two mechanisms depending on whether the element is a Master or a Slave element.

Figure 5 illustrates how the INITIN and INITOUT pins of Master and Slave elements may be connected in order to allow initialisation of the respective elements.

Master MB86680B switch elements obtain their configuration data from the unused Expansion port pins as shown in Figure 5a, while Slave elements may obtain their configuration data from either the INITOUT pin of a Master element (as in Figure 5a) or from a Programmable Logic Device (PLD), such as that shown in Figure 5b, capable of transferring a serial data stream identical to that shown in Figure 8.

MB86680B elements enter their Initialization phase when the $\overline{\text{RESET}}$ operation described above is complete.

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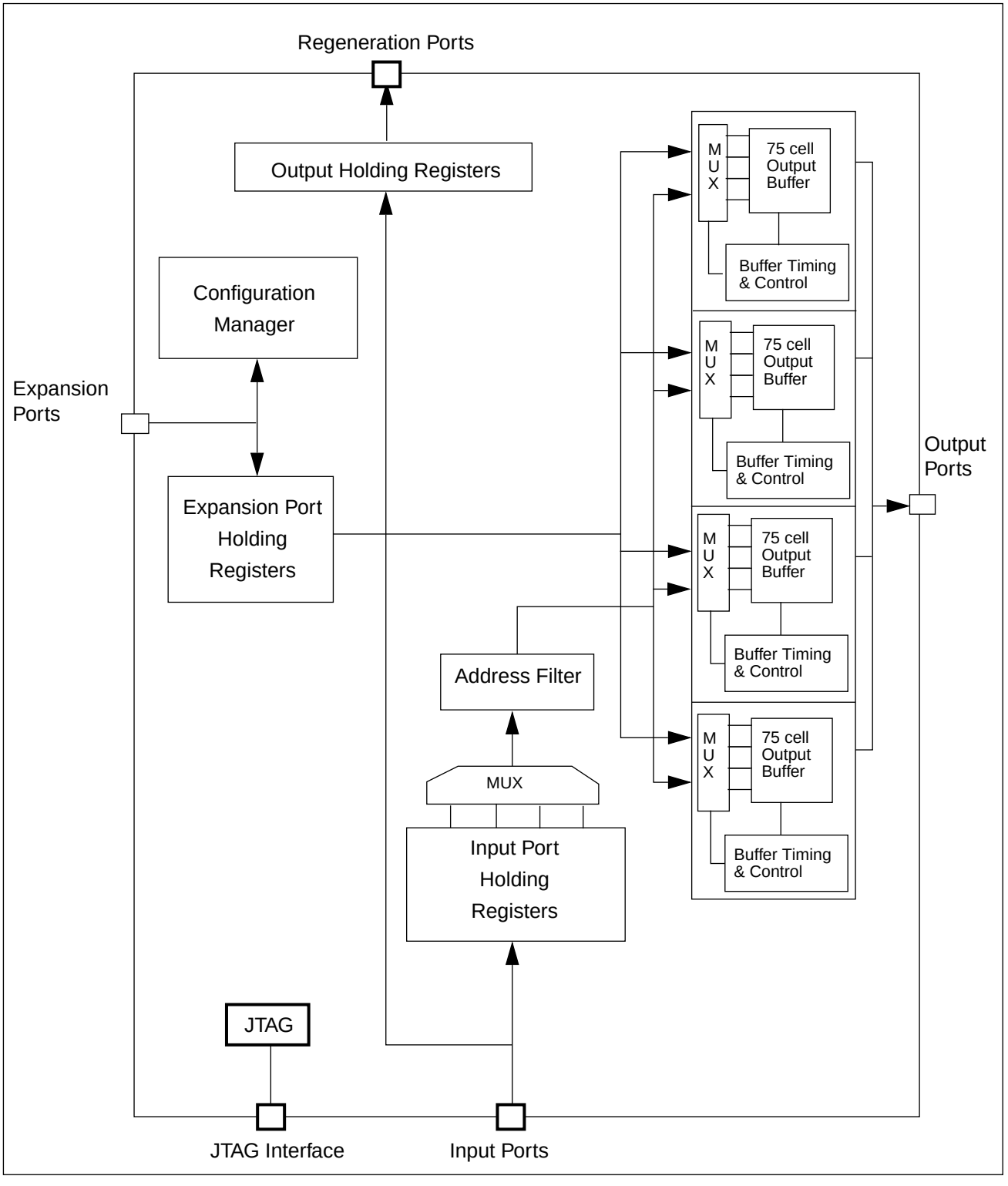

Figure 4 MB86680B Block Diagram

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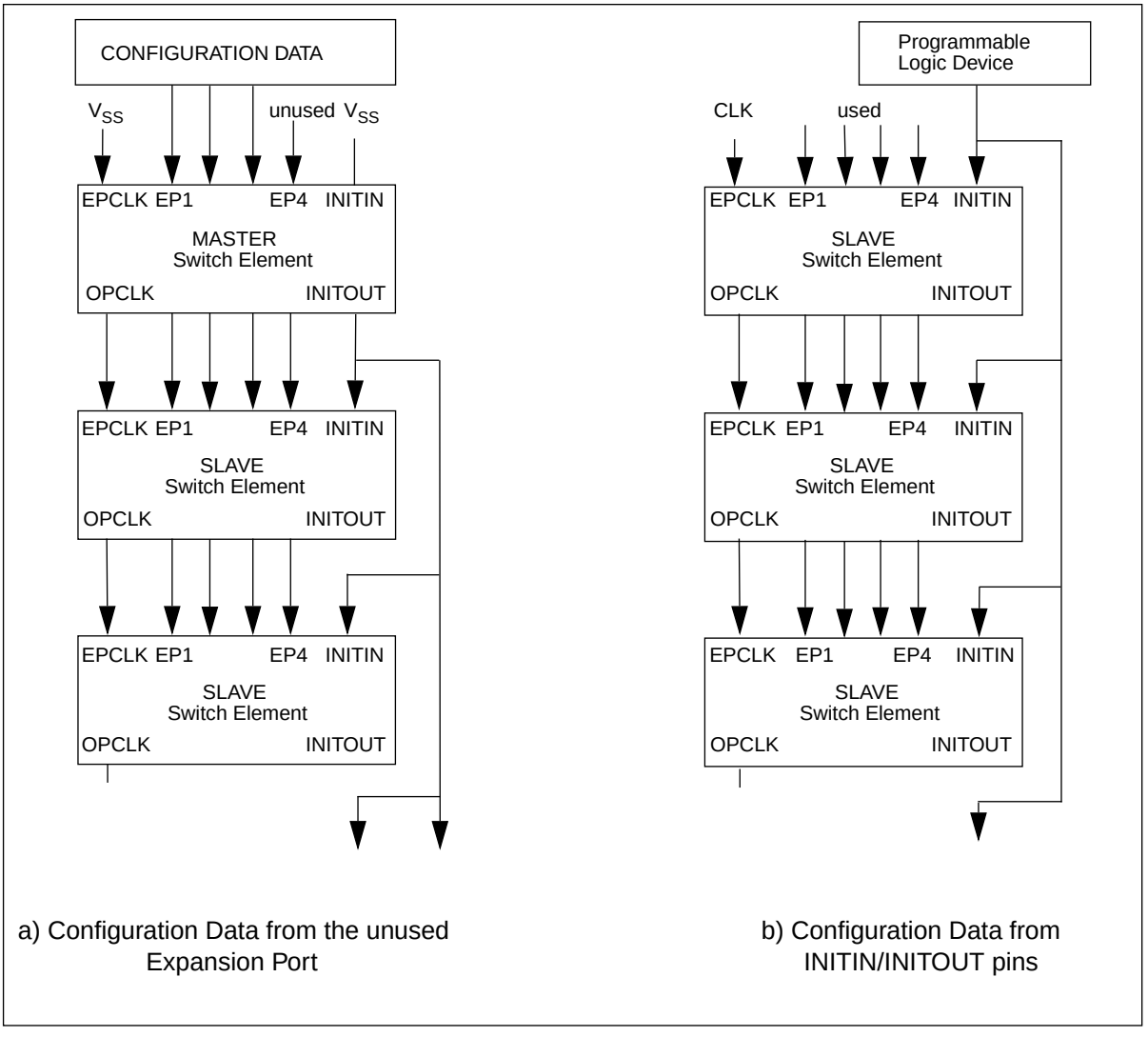

Figure 5 Use of INITIN and INITOUT pins for Initialization

3.4 Initialization of a Master SRE Switch Element.

An MB86680B switch element is deemed to be a Master when its EPCLK pin is permanently tied to Vss. In such a configuration, the SRE switch element may be internally configured via the data present on Expansion ports EP1DTx, EP2DTx & EP3DTx.

The data present on the three expansion ports is immediately parallel loaded into the eleven Master switch element Configuration registers, following a master RESET operation.

A total of 14 input pins are used to configure the operating modes of the MB86680B. These inputs are

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shared with Expansion port inputs and are selected by configuring the switch element as a Master.

Once configured, a Master switch element commences transferring the contents of it's Configuration registers to the connected Slave elements. The transfer of Configuration data between the Master and Slave elements is accomplished by the Master switch element transmitting the contents of it's Configuration registers in a serial format via the INITOUT pin to connected Slave device's INITIN pin, as shown in
Figure 5.

3.5 Configuration Registers

The MB86680B switch element provides 7 user definable configuration registers. The configuration registers may be configured via the Expansion port pins for Master devices or via the serial input port, INITIN, for the Slave devices.

A list of the eleven Configuration registers together with the associated Expansion port pins used to configure them on a Master device is given below.

1. **Address Field Size**
   AFS1..AFS0(EP1DT7..EP1DT6)

2. **Address Field Location**
   AFL3..AFL0(EP1DT5..EP1DT2)

3. **Column Address**
   CA2..CA0(EP2DT7..EP2DT5)

4. **High Priority Queue Enable**
   HPQE(EP2DT4)

5. **EFCI Enable / Disable control**
   EFCIE(EP2DT3)

6. **EFCI Thresholds**
   EFCIT1..EFCIT0(EP2DT2..EP2DT1)

7. **Flexible Transmission Mode**
   FTM(EP3DT7)

A description of the different functions associated with these Configuration registers is now given.

3.5.1 Address Field Size / Location Configuration Registers

The Expansion port pins EP1DT7 to EP1DT2 are used by Master MB86680B switch elements to configure their Address Field Size (AFS) and Location (AFL) registers immediately following a master RESET instruction cycle. The Address Field Size and Location registers are two inter-dependent registers, used by the MB86680B device to select a subset of routing tag bits which are to be used for address filtering.

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The address field size may vary from 2 bits (for Batcher/Banyan type topologies) to a maximum of 5 bits (for a 32 X 32 matrix).

With a 5-bit address field, there are 4 possible locations within the 24-bit tag (note the upper 4 bits are used for control information). With a 2-bit address field there are 10 possible locations. The relationship between address field size and location within the routing tag is illustrated in Figure 6.

Figure 6 also illustrates how the switch elements shall interpret the Address size/location inter-relationship table to acquire the valid address field within the routing tag, when configured with an address size of four bits and a start address field location of PA8.

Note:
The AFS field in the configuration registers is not applicable to multicast cells.

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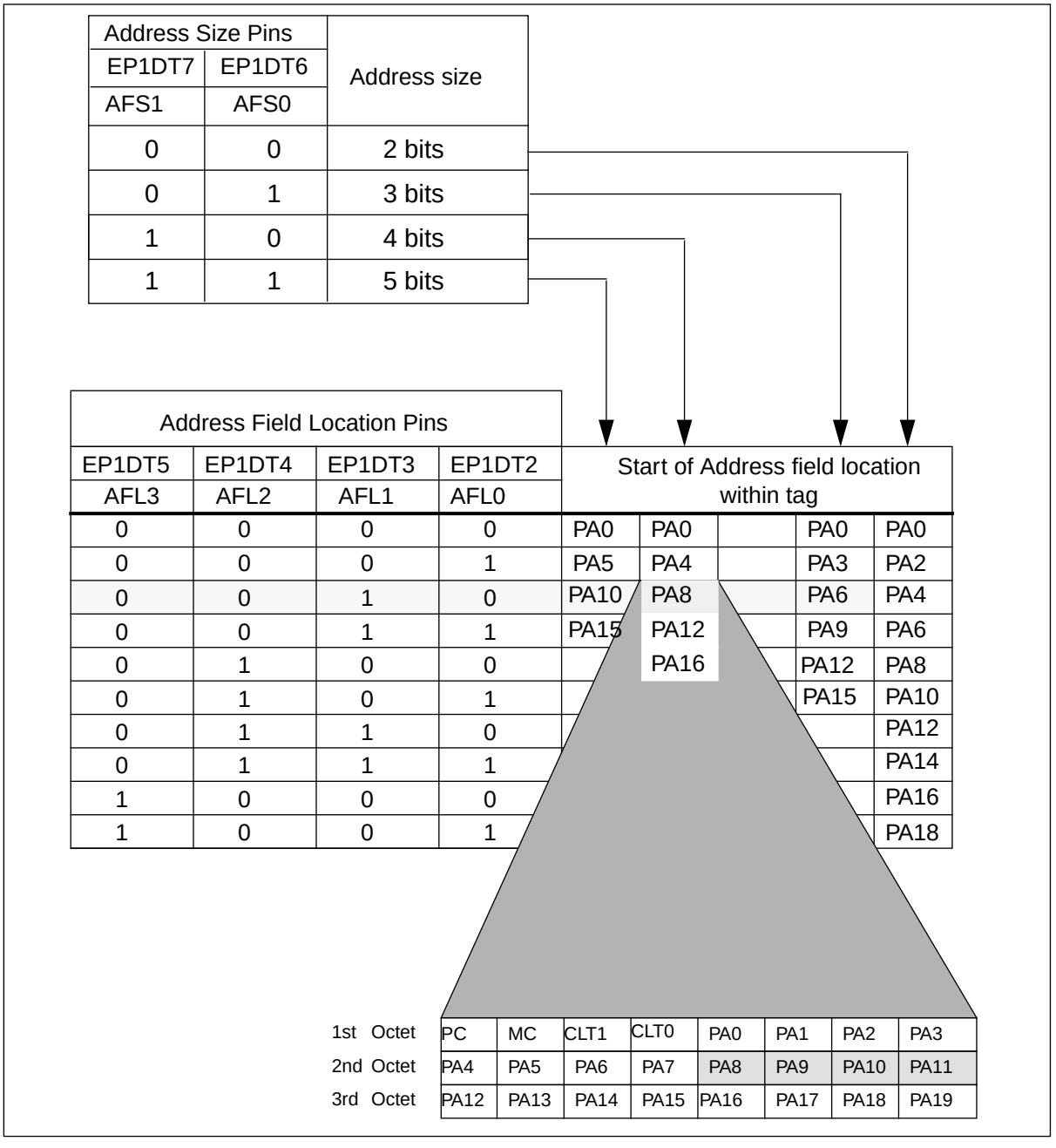

Figure 6 Address Size/Location Inter-relationship

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3.5.2 Column Address Configuration Register

The Expansion port pins EP2DT7 to EP1DT5 are used by Master MB86680B switch elements to configure their Column Address register immediately following a master $\overline{\text{RESET}}$ instruction cycle. The 3 bit Column Address Configuration register is used to define the base address for the switch element when it is used in a matrix configuration. The Column Address allows the switch element to determine which of the switch matrix Columns it resides in and hence the group of output ports to which it is attached.

Column Address			Column Group
CA1 EP2DT7	CA2 EP2DT6	CA3 EP2DT5	
0	0	0	1-4
0	0	1	5-8
0	1	0	9-12
0	1	1	13-16
1	0	0	17-20
1	0	1	21-24
1	1	0	25-28
1	1	1	29-32

Table 1 Column Address Coding

Table 1 illustrates the valid Column Address permutations whilst Figure 7 illustrates how individual elements may be configured within a switch matrix.

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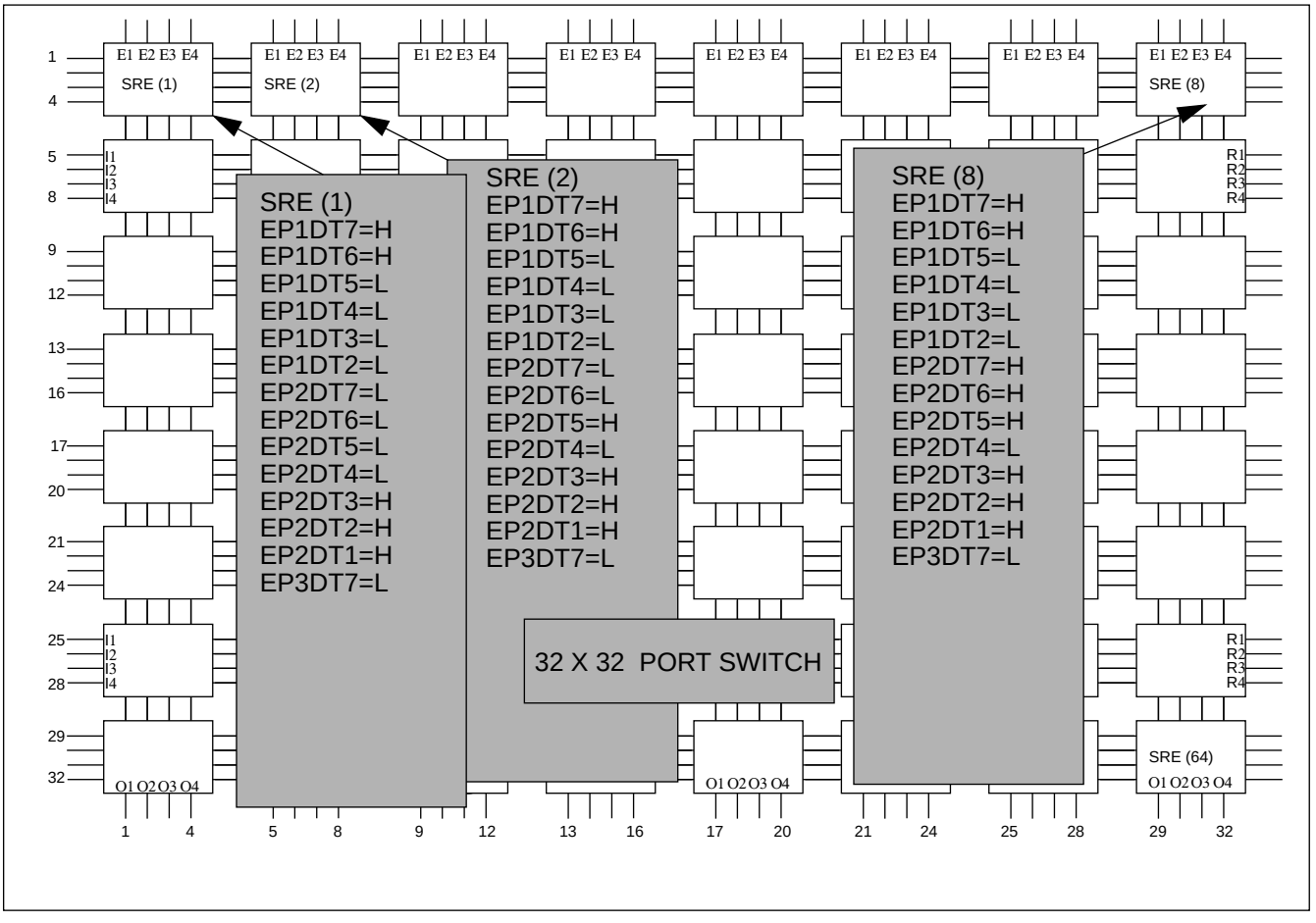

Figure 7 Column Addressing

3.5.3 High Priority Queue Enable Configuration Register

The Expansion port input pin EP2DT4 is used by Master switch elements, immediately following a master RESET instruction cycle, to enable or disable the high priority queue mechanism associated with each output buffer. When tied to V_{SS}, the **Dual queue** per port mode of operation is invoked. In this configuration mode the high priority queue is enabled providing the user with a 25 cell High priority queue and a 50 cell Low priority queue per output port.

When the Expansion port input pin EP2DT4 is tied to V_{DD}, for a Master switch element, the **Mono queue** per port mode of operation is invoked. In this operating mode the two output queues are merged to form a single 75 cell output queue per port.

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3.5.4 EFCI Enable / Disable Configuration Register

On a Master MB86680B switch element, the Expansion port input pin (EP2DT3) may be used to Enable/ Disable the Explicit Forward Congestion Indication (EFCI) function. When this pin is tied to V_{SS} on a Master MB86680B element, the EFCI function will be disabled both on the Master switch element and any attached Slave elements (note Slave elements are configured by the INITIN and INITOUT configuration illustrated in Figure 5a).

When the EP2DT3 pin is tied to V_{DD}, on a Master switch element, the EFCI function will be enabled on both the Master element and any attached Slave elements.

3.5.5 EFCI Threshold Configuration Register

The Expansion port pins (EP2DT2 and EP2DT1) on a Master switch element may be used to select the Output data queue fill level thresholds at which the EFCI function may be implemented. Table 2 illustrates how the logic levels applied to these pins are interpreted by the Master and attached Slave elements.

EFCIT 1 EP2DT2	EFCIT 0 EP2DT1	EFCI Threshold
0	0	Not Used
0	1	20% full
1	0	50% full
1	1	80% full

Table 2 EFCI Threshold Coding

3.5.6 Flexible Transmission Mode Configuration Register

The Expansion port pin (EP3DT7) on a Master SRE may be used to select a transmission edge for the O and R-Port data.

When the EP3DT7 pin is tied to V_{SS} the data present on the O and R-ports is transmitted synchronous to the falling edge of the OPCLK. This transmission mode is referred to as the Fujitsu Cell Stream (FCS) mode of operation.

When the EP3DT7 pin is tied to V_{DD} the data present on the O and R-ports is transmitted synchronous to the rising edge of the OPCLK.This transmission mode is referred to as the Inverse Fujitsu Cell Stream (IFCS) mode of operation.

When operating in the FCS mode, data present on each input is sampled on the rising edge of its respective clock whilst data transitions on the Output and Regeneration ports take place on the falling edge of the OPCLK signal.

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When operating in the IFCS mode, data present on the Inputs will be sampled on the rising edge of their respective clocks whilst data transitions on the Cell Stream Output Ports and Regeneration ports will take place on the rising edge of the OPCLK signal.

3.6 Initialization of a Slave SRE Switch Element

Immediately following a RESET operation, Slave switch elements commence monitoring their INITIN pins. Unlike Master devices, the Slave switch elements use their serial INITIN input port to acquire configuration data.

On detecting the active low Start sync bit, as shown in Figure 8, the Slave switch element uses its IPCLK clock signal to determine the nominal centre bit position of the serial data stream. Multiple sampling of the serial data stream is carried out to eliminate the possible detection of a false start polarity.

On detecting the valid Start sync bit, the Slave switch element shall sample each bit of the received initialization character by counting 5 clock periods from the preceding bit's nominal centre until all the necessary configuration data has been acquired and loaded into the Configuration registers.

On acquiring their configuration data, the Slave switch elements cease to monitor their INITIN pins.
Figure 8 in conjunction with Table 3 illustrates the format of the data on this serial highway together with the order of transmission.

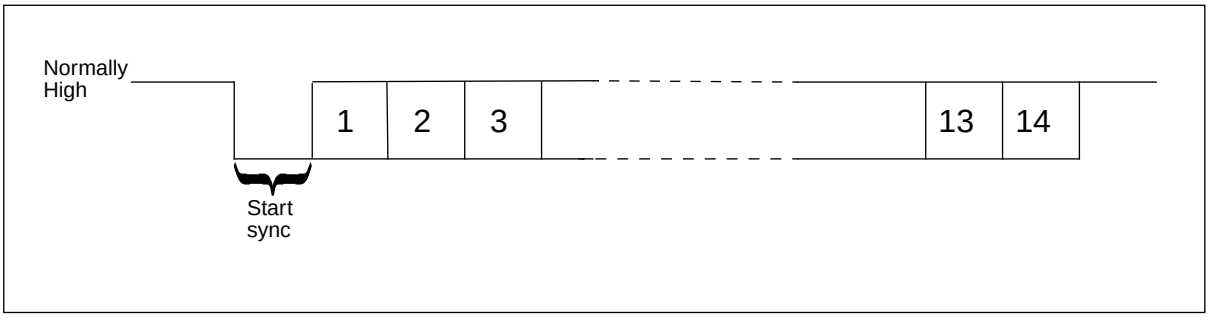

Figure 8 Init line serial data format

Transmission of data on the serial INITOUT/INITIN serial highway shall primarily be of an asynchronous format with data bit periods equal to the IPCLK/5. The transmitted data will not necessarily be phase aligned to the IPCLK. The INITOUT port data transitions are synchronised to the falling edge of IPCLK/5 and are sampled by Slave switch elements on the rising edge of their IPCLK.

Master switch elements commence transmission by driving the INITOUT pin low. The configuration data will then be transmitted in the format shown in Figure 8.

Figure 8 shows how the configuration data presented at the Expansion ports of a Master switch element

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is translated into the serial bit stream illustrated in Figure 8. The data is transmitted serially with the most significant bits occupying the lower bit positions of the INITOUT line.

All other unused Expansion port input pins are reserved for internal use and should be connected to V_{SS}.

Function	Expansion Port Pins (Master Configuration)	Init line Bit Position(s) (Slave Configuration)
Address Field size	EP1DT7..EP1DT6	Bits 1..2
Address Field location	EP1DT5..EP1DT2	Bits 3..6
Column Group	EP2DT7..EP2DT5	Bits 7..9
High Priority Queue Enable	EP2DT4	Bit 10
EFCI Enable/Disable control	EP2DT3	Bit 11
EFCI Thresholds	EP2DT2..EP2DT1	Bits 12..13
FTM	EP3DT7	Bit 14

Table 3 Master/Slave Configuration table

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4 Functional Description

4.1 Address Filtering Normal Operation

ATM Cells arriving at the ingress side of the MB86680B element will have a 3 byte routing tag appended to the head of the ATM Cell. The 3 byte routing tag is used by the MB86680B switch elements to carry out Address filtering functions in conjunction with selective cell discard operations on the incoming cell. Figure 9 illustrates the main principles of operation.

The switch elements use the Start Of Cell (IPxSOC) signal to locate the 3 byte routing tag. On acquiring the routing tag the MB86680B switch elements commence the interpretation of the various fields therein. Figure 9 illustrates how the MB86680B switch elements receives ATM Cells 1 and 2 on it's ingress side and then proceeds to route both the Cell and it's associated routing tag to the required output port.
The MB86680B switch element is capable of distinguishing between two types of cells. The two cell types are differentiated by the formats of their routing tags. The two routing tag formats are referred to as:

1. The normal routing tag format
2. The Multicast routing tag format

The normal routing tag format is illustrated in Figure 9 appended to ATM Cells 1 and 2, whilst a more detailed description of the significance of the bits in this routing tag is shown in Figure 10.

4.1.1 Normal Routing Tag Control Field Format

A description of the function of the bits within this routing tag shall now be given commencing with the Priority control bit.

Priority Control (PC) Bit

The Priority Control (PC) bit determines whether the associated cell is loaded into the high priority queue or the low priority queue. This bit should be set on a per virtual circuit basis in order to guarantee that cell sequence numbering is preserved.

High priority channels should only be used for delay sensitive (or loss sensitive) data, and the total amount of traffic allocated to high priority channels should form a small percentage of the total available output bandwidth.

When the switch elements are configured for single / mono queue mode of operation the PC bit has no significance.

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Cell Loss Threshold Field CLT0,CLT1

The Cell Loss Threshold bits, CLT0 and CLT1, are used to control the treatment of cells which have the CLP bit in their ATM cell header set. They determine the output queue fill level at which the cells will be selectively discarded.

CLT 1	CLT 0	Discard Threshold
0	0	No discard
0	1	20% full
1	0	50% full
1	1	80% full

Table 4 Discard Threshold Coding

Note:
When operating in the Dual queue mode, the Cell loss Threshold field is only applicable to ATM Cells with their PC bit set to "0".

When operating in the Mono queue mode, all ATM cells are treated as Low priority cells irrespective of the Status of their PC bit and consequently will be subject to selective cell discard if the above criteria are met.

Routing Field PA0-PA19

The routing Field PA0 to PA19 is used by the MB86680B switch elements to determine the port destination of the received cell. The validity of the bits in the 20 bit routing field are determined by the programmed Address Field Size and location parameters as specified in section 3.5.1.

In Figure 9, SRE's (C) and (D) are configured with the parameters:

1. Address Field Size: 3 bits
2. Address Field Location: PA0
3. Column Address : 5-8

Whilst SRE's (A) and (B) are configured with the alternative parameter:

4. Column Address : 1-4

As a result of these configurations ATM Cell 1 passes transparently through SRE (A), merely being re-timed at SRE (A)'s R-ports prior to being presented at the corresponding ingress port of SRE (C).

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In Figure 10 the left most justified bits of the routing field are deemed to be most significant.
SRE (C) is configured to analyse the routing field PA0 to PA2. As a result ATM Cell 1 is routed to port 8 of SRE (C).

On being routed, the ATM Cell 1 traverses the matrix vertically eventually arriving at SRE (D)'s output port as shown.
Like SRE (C), SRE (B) is configured to analyse the routing field PA0 to PA2. As a result ATM Cell 2 is routed to port 3 of SRE (B).

The unused routing fields in the 20 bit routing tag may be used to route the cells through numerous stages prior to further address translation operations being required.

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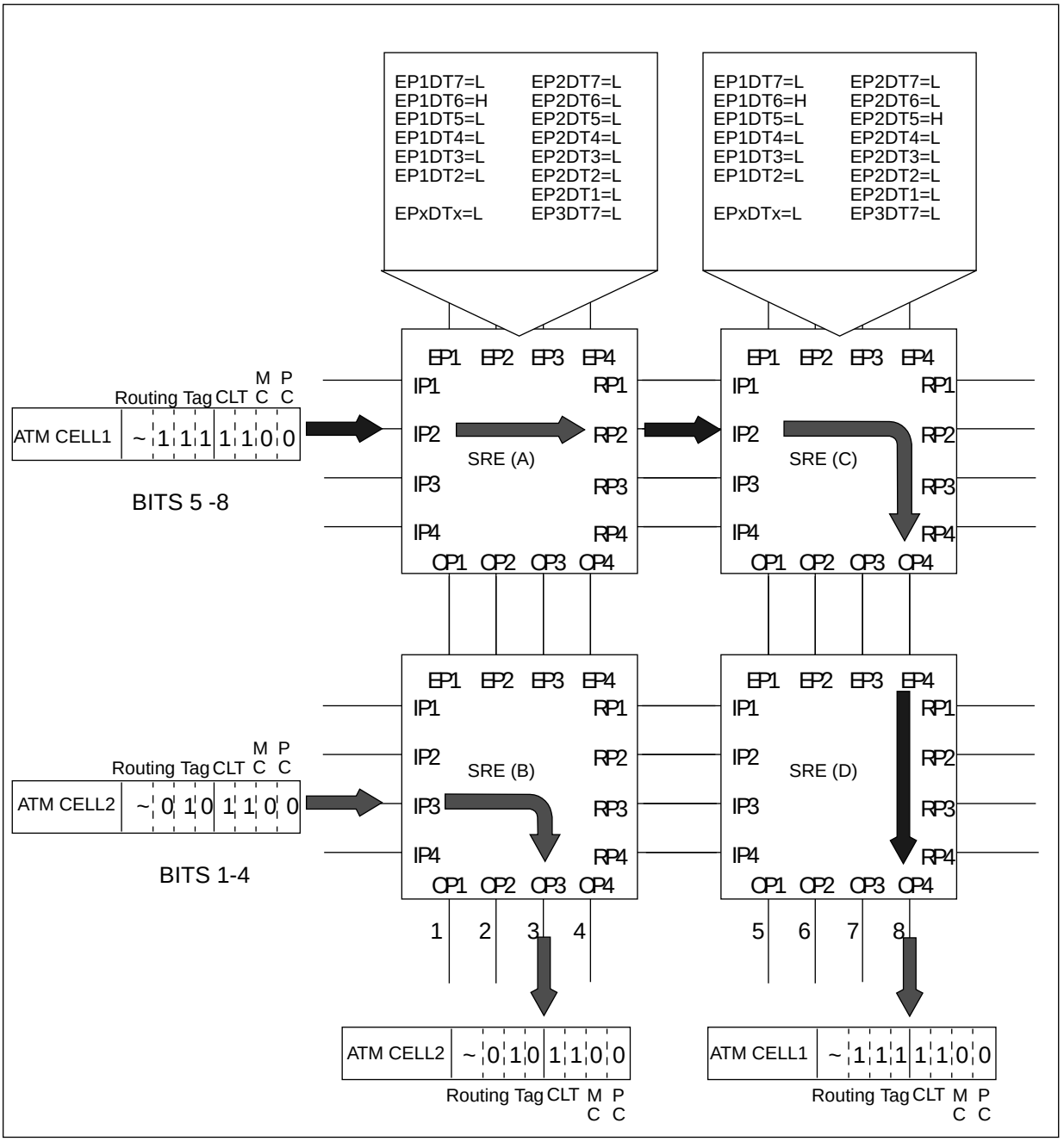

Figure 9 Address Filtering

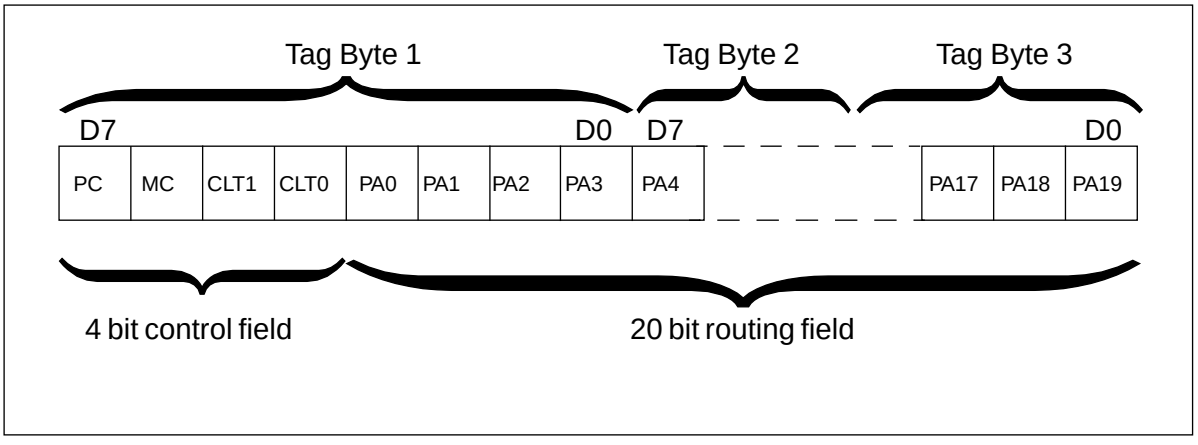

Figure 10 Normal Routing Tag Format

4.1.2 Multicast Routing Tag Control Field Format

The MB86680B switch elements are capable of performing cell replication. The cell replication operation of the switch elements permits it to transmit a single ATM cell to more than one output port. This operational mode of cell replication is known as Multicasting.

The Multicasting function is invoked by setting the Multicast Control (MC) bit of the Multicast routing tag as shown in Figure 11.

The Multicast routing tag illustrated in Figure 11 is comprised of 5 fields. A brief description of the significance of these fields is now given.

Priority Control (PC) Bit

The Priority Control (PC) bit has exactly the same definition as that described for the normal routing tag in section 4.1.1.

Multicast Control (MC) Bit

The Multicast Control (MC) bit is used by the MB86680B switch elements to tag the received ATM Cell as a Multicast cell. This cell will therefore be subject to replication by MB86680B devices configured to carry out this function.

Relay Link Address Field

The Relay Link Address Field shown in Figure 11 is used as the cell routing field by MB86680B devices

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not configured to carry out the cell replication function indicative of Multicasting.
Devices not configured to carry out cell replication will interpret the Relay Link Address Field as a 5 bit routing field, with RL4 representing the most significant bit of the field.
The received cell will therefore be treated like a cell with a normal routing tag format and routed to the port specified in the Relay Link Address Field.

Output Group Select (OGS) Bit

The Output Group Select (OGS) bit is used by the MB86680B elements to determine the band of output ports over which the received cell may be Multicasted to.
The OGS bit in the Multicast routing tag is only used by MB86680B devices configured to carry out the Multicast operation.

Multicast Bit mask field

The Multicast bit mask field is used to select the desired ports to which a received cell may be Multicasted. The Multicast bit mask field is only used by MB86680B devices configured to carry out the Multicast operation.

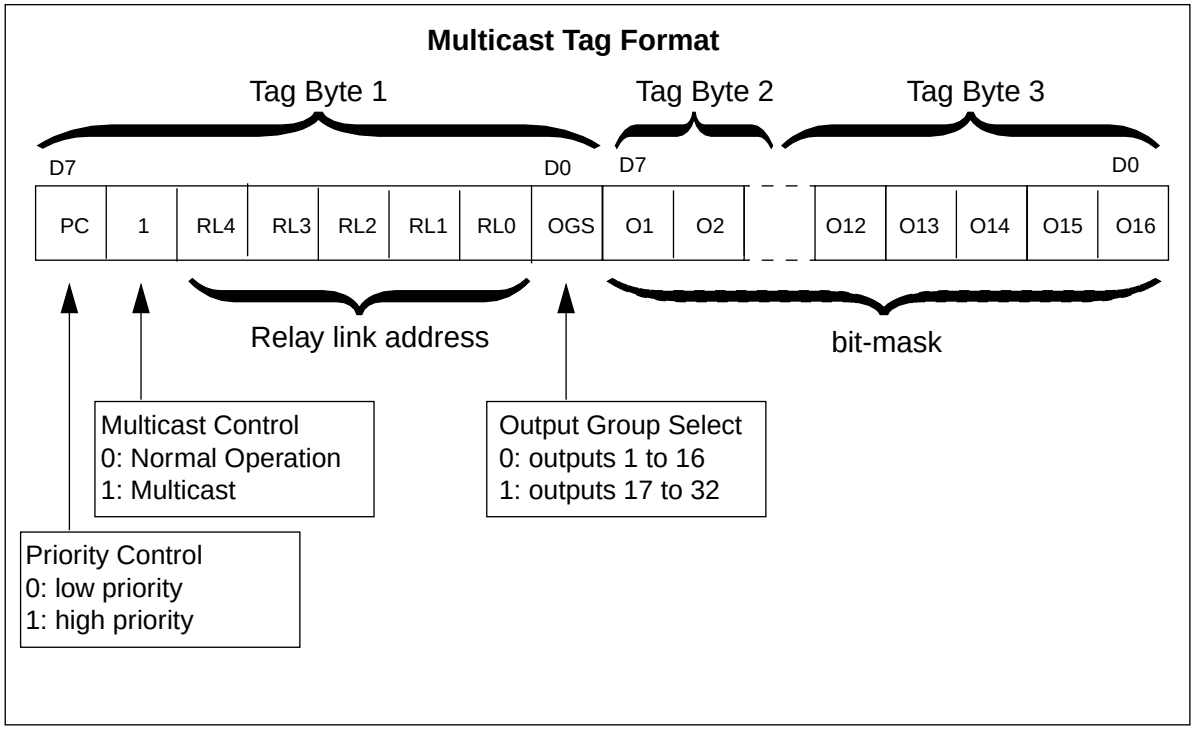

Figure 11 Routing Tag Format for Multicast operation

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4.2 Address Filtering Multicast Operation

The MB86680B Multicast function is invoked by setting the Multicast Control (MC) bit in the received cell's routing tag. When this bit is set it changes the way in which the tag field is interpreted.

In Multicast mode the tag is divided into a 16 bit mask field, an output group select field and a relay link address field. The PC and MC bit positions are unchanged. The multicast routing tag is illustrated in Figure 11.

The following generic description assumes a two stage 64X64 switch comprising four 32X32 matrices, as shown in Figure 12.

For the purposes of this description, a Multicast server is defined as a matrix comprised of MB86680B devices configured to perform the Multicast operation, i.e cell replication.

Multicast server matrices are constructed from MB86680B devices configured with their Address Location Field set to zero. Matrices configured in this manner are assumed to provide the primary outputs as shown in the multi-stage configuration in Figure 12.

In Figure 12 matrices B and D provide the primary outputs and consequently have their Address Location Field set to zero. As a result matrices B and D are referred to as Multicast servers.
Switch Matrices A and C are configured with MB86680B devices whose Address Location Fields are > 0. As a result these matrices are referred to as Non-Multicast servers

A description of the Multicast routing mechanism is now explained using the set-up illustrated in Figure 12. ATM Cell 1 is configured with a Multicast routing tag. This cell is applied to input port 2 of the Non-Multicast server matrix A.
Matrix A analyses the received cell's Relay Link Address Field and routes the cell plus appended routing tag to output port 32.

The routed cell then arrives at input port 1 of the Multicast server matrix D. The receiving MB86680B devices within the switch matrix will interrogate the OGS bit and bit mask fields of the received cell's routing tag to determine if cell replication is necessary.

The bit mask field in conjunction with the OGS bit will determine the outputs to be selected for cell transmission. A logical '1' in the bit mask field will cause the cell to be forwarded on the corresponding output port and a logical '0' will cause the cell to be discarded.

This mechanism allows a single primary input cell to be directed to up to 16 primary outputs associated with a single output group. Hence, for the 64X64 switch illustrated in Figure 12, an input cell may need to be copied up to 4 times in order to achieve full coverage. The copying process may be performed by the Fujitsu Network Termination Controller (MB86683X) which will provide sufficient buffering to absorb the short 4-cell burst.

Thus as shown in Figure 12 ATM Cell 1 is Multicasted to the 16 primary outputs 1 to 16 of the switch matrix D.

On the other hand ATM Cell 2 is applied to input port 31 of the Non-Multicast server matrix C. The cell is routed to output port 1 of matrix C, permitting the cell to enter the Multicast server matrix B via input port 32.

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As previously described both the Cell's OGS and Bit mask fields are interrogated by the MB86680B devices within matrix B. In Figure 12, ATM Cell 2's OGS bit is set. This permits the cell to be Multicasted to any of the output ports 17 to 32. As a result of the bit mask status shown the cell is Multicasted to output ports 17, 31 and 32 of matrix B.

During multicast operation, the user does not have control of the cell loss threshold at which Multicast cells may be discarded. A default cell loss threshold of 80% is assumed. If no discard is required then the CLP bit must be set to zero. The user does, however, have control over queue priority. If the PC bit is set to 1 then all relay and multicast operation will use the high priority queues.

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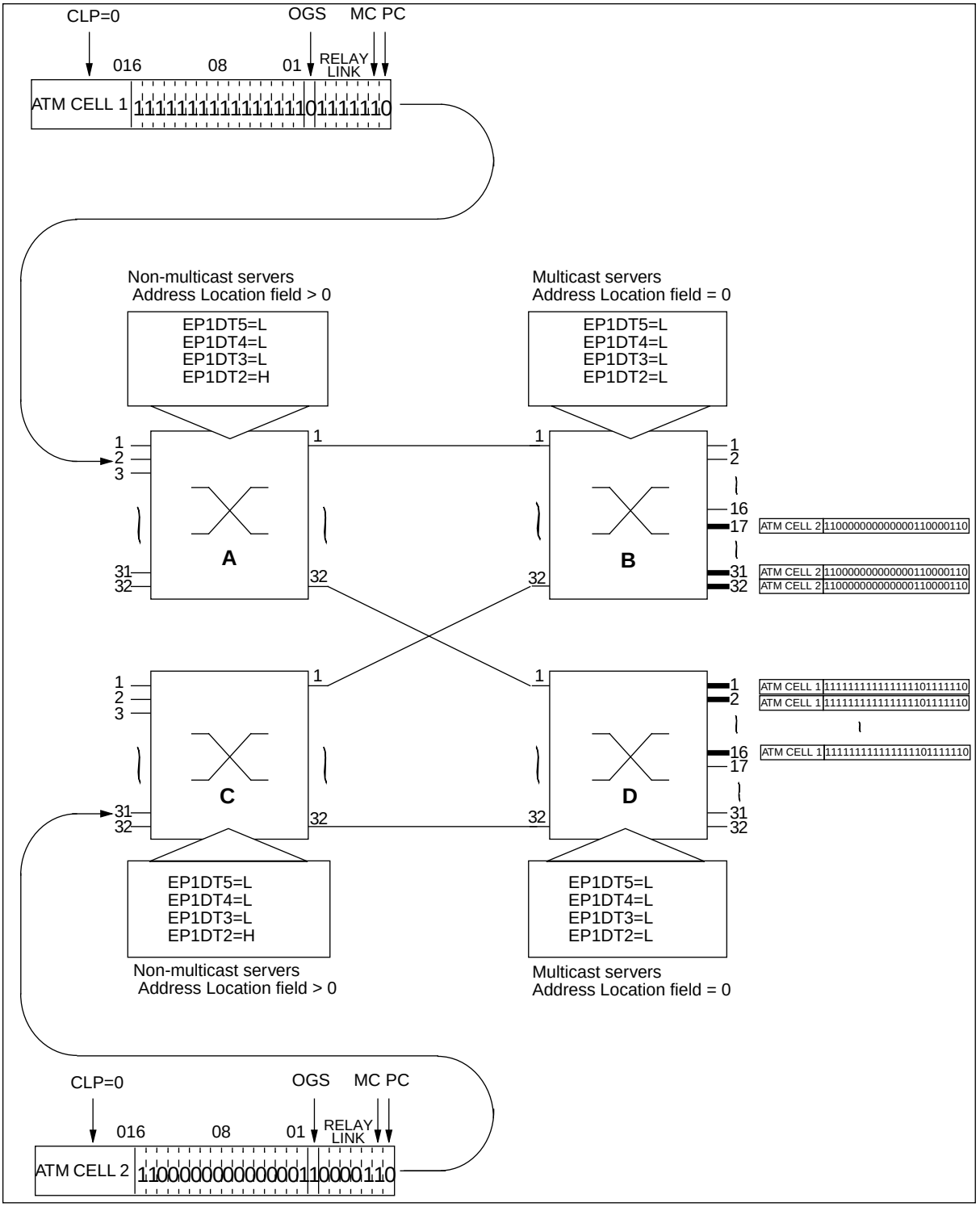

Figure 12 Multicast Operation with a 64 x 64 Switch

4.3 Explicit Forward Congestion Indication (EFCI) function

The MB86680B switch element's Explicit Forward Congestion Indication (EFCI) function is enabled when the element's internal EFCI Enable/Disable Configuration register is set to a logical "1", as described in Section 3.5.4.

When enabled, the EFCI function permits Low Priority (LP) cells entering an output data queue to experience EFCI marking when the criteria indicating congestion are satisfied.

A LP cell will experience EFCI marking if the MSB of the PTI field in it's ATM cell header is set to a logic "0" and the fill level of the output queue from which it is **exiting** is greater than or equal to the programmed EFCI threshold configuration register value, as illustrated in Table 2.

When the above criteria for EFCI marking is met, bit 2 of the 3 bit PTI field is set to a logic "1".

Note:
The MB86680B switch element does not regenerate the ATM Cell header's HEC field when it alters the PTI field.

No EFCI marking will be carried out on Cells that have their EFCI Threshold field set to "00" irrespective of whether the EFCI function has been enabled or not.

Multicast cells satisfying the criteria for EFCI marking are marked when the threshold fill level of the output data queue from which they exit exceeds or equals the 80% threshold fill level.

4.4 JTAG

4.4.1 Introduction

This device contains Boundary Scan Test Circuitry compliant with IEEE 1149.1 (JTAG). This requires the addition of the 5 pins identified below. See Appendix C for a full BSDL description.

The JTAG circuitry allows easier board level testing by allowing the signal pins on the device to form a serial scan chain around the device. The test modes are controlled by accessing an internal Test Access Port Controller (TAP), which is in turn controlled from the TAP.

4.4.2 Test Access Port (TAP)

Five pins are dedicated to JTAG:TDO; TDI; TMS & TCK.
The functions of these signals are described in Section 2.2 of this datasheet.

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4.5 Test Instructions

The following JTAG instructions are implemented:- BYPASS
SAMPLE/PRELOAD
EXTEST
INTEST.

BYPASS
The BYPASS instruction is used to bypass a component that is connected in series with other components. This allows more rapid movement of test data through the components of the board, bypassing the ones that do not need to be tested. The BYPASS operation enables the bypass register, which is a single stage shift register, between TDI and TDO.

1. The binary code for the BYPASS instruction is “11”.

2. The BYPASS instruction is forced into the instruction register output latches during the Test_Logic_Reset state. Note the distinction between the “01” content of the instruction shift register and the “11” of the instruction register output latch. Therefore, at the start of the instruction-shift cycle, a “01” pattern will be seen instead of “11”.

3. The BYPASS operation does not interfere with the component operation at all. If the TDI input trace to the component is somehow disconnected, the test logic will see a “11” at TDI input during the instruction-shift state. Therefore, no unwarranted interference with the on-chip system logic occurs.

SAMPLE/PRELOAD
The SAMPLE/PRELOAD instruction is used to sample the state of the component pins. The sampled values can be examined by shifting out the data through TDO. This instruction selects the boundary scan-cell output latches with specific values. The preloaded values are then enabled to the output pins by the EXTEST.

1. The binary code for the instruction is “01”.

2. The SAMPLE/PRELOAD instruction selects the boundary-scan cells to be connected between TDI and TDO in the Shift_DR TAP controller state.

3. The values of the component pins are sampled on the rising edge of TCK in the Capture_DR TAP controller state.

4. The preload values shifted in the boundary scan cells are latched into the boundary-scan output latch at the falling edge of TCK in the Update_DR TAP controller state.

EXTEST
The EXTEST instruction allows testing of off-chip circuitry and board level interconnections. The PRELOAD /SAMPLE instruction is used to preload the data into the latched parallel outputs of the boundary-scan shift register stages. Then, the EXTEST instruction enables the preloaded values to the components output pins.

1. The binary code for the instruction is “00”.

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2. The device outputs the preloaded data to the pins at the falling edge of TCK in the Update_IR TAP controller state at which point the JTAG instruction register is updated with the EXTEST.

3. The EXTEST instruction selects the boundary-scan cells to be connected between TDI and TDO in the SHIFT-DR test logic controller state.

4. Once the EXTEST instruction is effective, the output pins can change at the falling edge of TCK in the Update_DR TAP controller state.

INTEST

This instruction allows testing of the on-chip system logic. Test stimuli are shifted in, one at a time, and applied to the on-chip logic. The test results are captured into the boundary scan register (BSR) and are examined by subsequent shifting. The PRELOAD/SAMPLE instruction is used to preload the data into the latched parallel outputs of the boundary-scan shift register stages prior to INTEST being selected.
The binary code for the instruction is “10”.

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5 Developers Notes

5.1 External Interfaces

External interfaces of the switch element are illustrated in MB86680B I/O Block Diagram and are described in the following paragraphs.

5.1.1 ATM Cell Structure

The structure of an ATM cell is illustrated in Figure 3. The only bit in the cell that is processed by the MB86680B switch element is the CLP bit. This bit is used to determine whether a cell should be discarded when the output queue fill level exceeds a programmable threshold.

Note: When EFCI functions are disabled, none of the bits in an ATM cell will be modified by the MB86680B switch elements. The switch elements will not discard idle cells; it is assumed that idle cells will be discarded before data is applied to the switch (e.g. by the FUJITSU Network Termination Controller).

5.1.2 External Data Structure

All input/output data for the MB86680B switch elements is comprised of 8 data bits together with a Start of Cell (SOC) bit and a clock signal. The data for one cell period comprises a 3 byte tag field followed by a 53 byte ATM cell. The cell stream may be continuous or discontinuous.

In both cases the SOC bit marks the first tag byte associated with a cell period. The clock rate should be selected to be as close as possible to 56/53 X ATM cell data rate. For SDH STM-1 applications a value of 155.52MHz / 8 provides a good match.

A diagram of the external data interface format for both Fujitsu Cell Steam (FCS) and the Inverse FCS (IFCS) modes of operation is illustrated in Cell Stream Transmission Timing.

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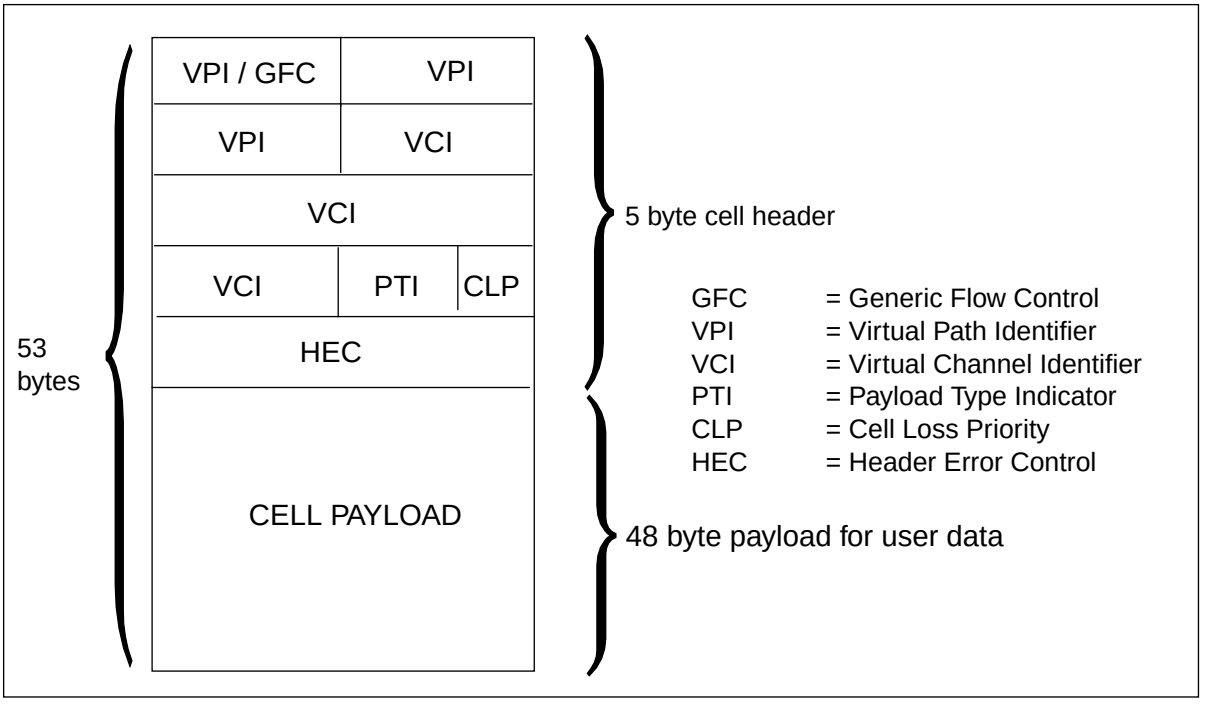

Figure 13 ATM Cell Header Structure

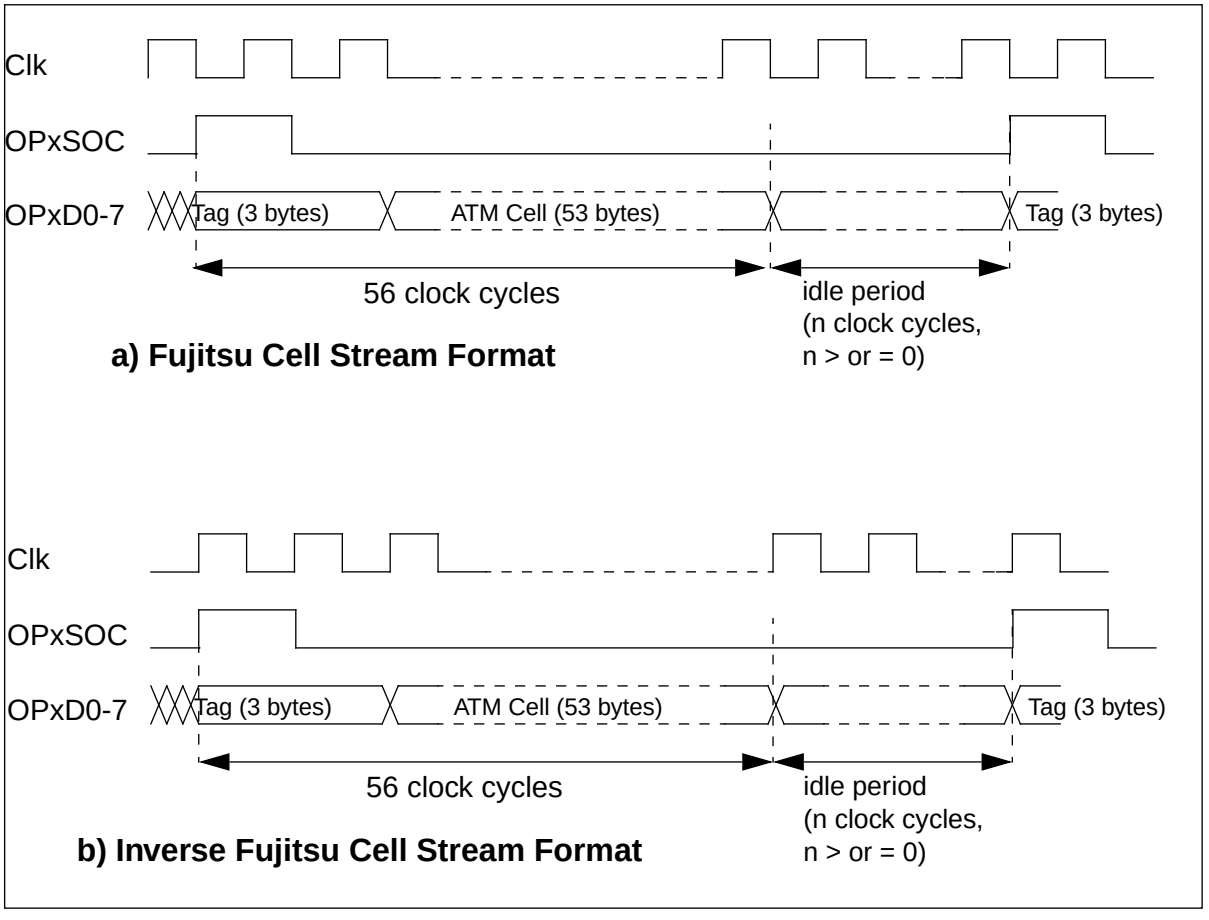

Figure 14 Cell Stream Transmission Timing

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A Electrical Specification

A.1 Absolute Maximum Ratings

Rating	Symbol	Values		Units
		Min	Max	
Positive Supply Voltage	$+V_{DD}$	-0.5	6.0	V
Input Voltage	V_{DIN}	-0.5	$+V_{DD}$ + 0.5	V
Output Voltage	V_{O1}	-0.5	$+V_{DD}$ + 0.5	V
Storage Temperature	T_{STG}	-40	+125	^oC

A.2 DC Characteristics

Parameter	Symbol	Pin	Test Condition	Value			Unit
				Min	Typ.	Max	
Positive Supply Current	IDDS		Static no load	-	-	100	mA
Input High Voltage (TTL)	V_{IH}			2.2	-	$+V_{DD}$	V
Input Low Voltage (TTL)	V_{IL}			0	-	0.8	V
Input Leakage Current	I_L		$0<=V_I<=+_{VDD}$	-10	-	10	µA
Output Low Voltage	V_{OL}		I_{OL}=3.2mA	V_{SS}	-	0.4	V
Output High Voltage	V_{OH}		I_{OH}=-2mA	4.2	-	V_{DD}	V
Output Off Leakage Current	I_{LO}			-10	-	10	mA
Operating Current (normal)	I_{DD}			-	115	210	mA
Operating Temperature	T_A			0	-	70	^oC
Power Dissipation (operating)	P_O			-	800	-	mW

NOTE:
Permanent device damage may occur if the **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this datasheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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B AC Characteristics

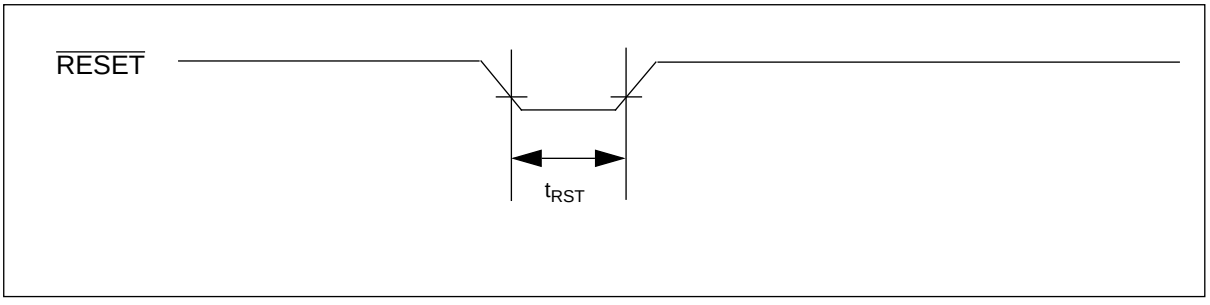

Figure 15 Reset Timing

Parameter	Ref. Signal	Abbrev.	Values			Units
			Min	Typical	Max	
Reset Pulse Width	$\overline{RESET}$	t_{RST}	5	-	-	ns

Table 5 Reset AC Timing Parametrics

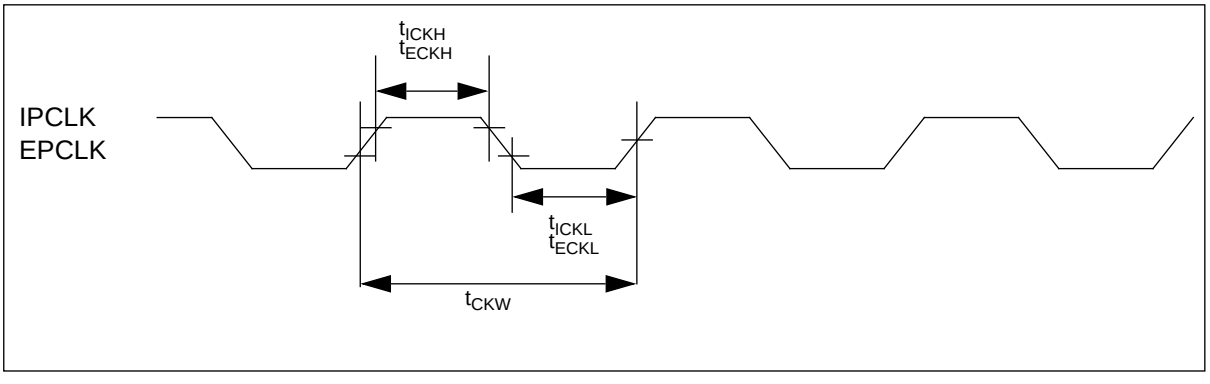

Figure 16 Input Clock Timing

Parameter	Ref. Signal	Abbrev	Values			Units
			Min	Typical	Max	
IPCLK High time	IPCLK	t_{ICKH}	18	-	-	ns
EPCLK High time	EPCLK	t_{ECKH}	18	-	-	ns
IPCLK Low time	IPCLK	t_{ICKL}	18	-	-	ns
EPCLK Low time	EPCLK	t_{ECKL}	18	-	-	ns
IP/EPCLK Frequency		t_{CKW}	50	-	-	ns

Table 6 IPCLK/EPCLK AC Timing Parameters

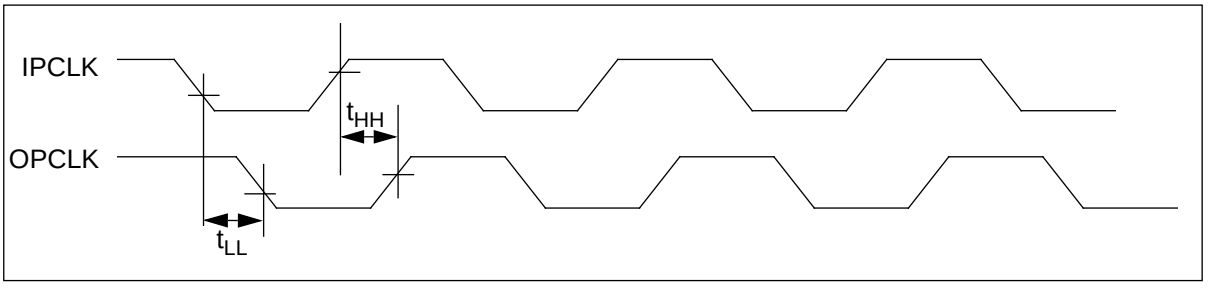

Figure 17 IPCLK to OPCLK Timing Relationship

Parameter	Ref. Signal	Abbrev	Values			Units
			Min	Typical	Max	
IPCLK low to OPCLK low	IPCLK	t_{LL}	7	-	-	ns
IPCLK high to OPCLK high	IPCLK	t_{HH}	6	-	-	ns

Table 7 IPCLK to OPCLK AC Timing Parameters

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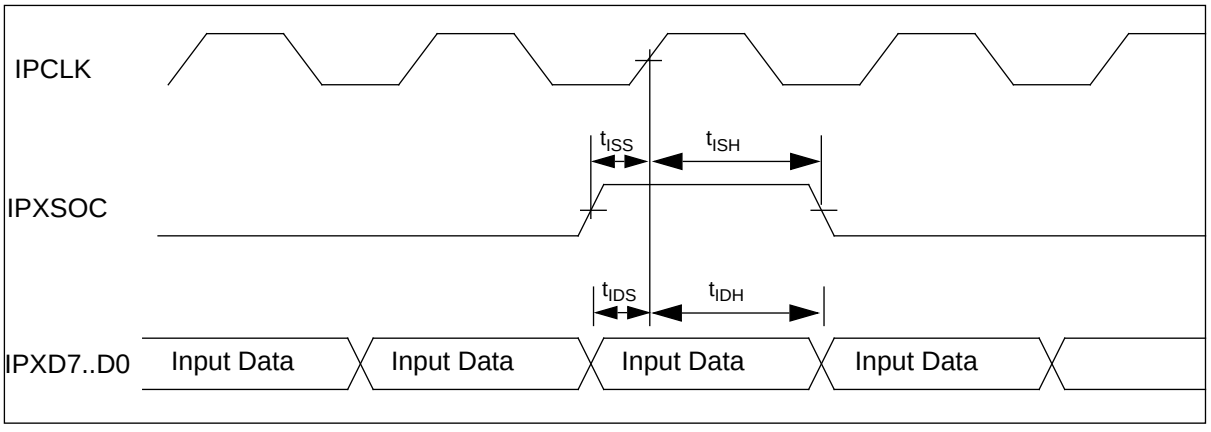

Figure 18 I-Input Port Timing

Parameter	Ref. Signal	Abbrev	Values			Units
			Min	Typical	Max	
IPXSOC Data setup Time	IPCLK	t_{ISS}	0	-	-	ns
IPXSOC Data Hold Time	IPCLK	t_{ISH}	7	-	-	ns
IPXD7..D0 Data setup Time	IPCLK	t_{IDS}	0	-	-	ns
IPXD7..D0 Data Hold Time	IPCLK	t_{IDH}	8	-	-	ns

Table 8 I-Input Port AC Timing Parameters

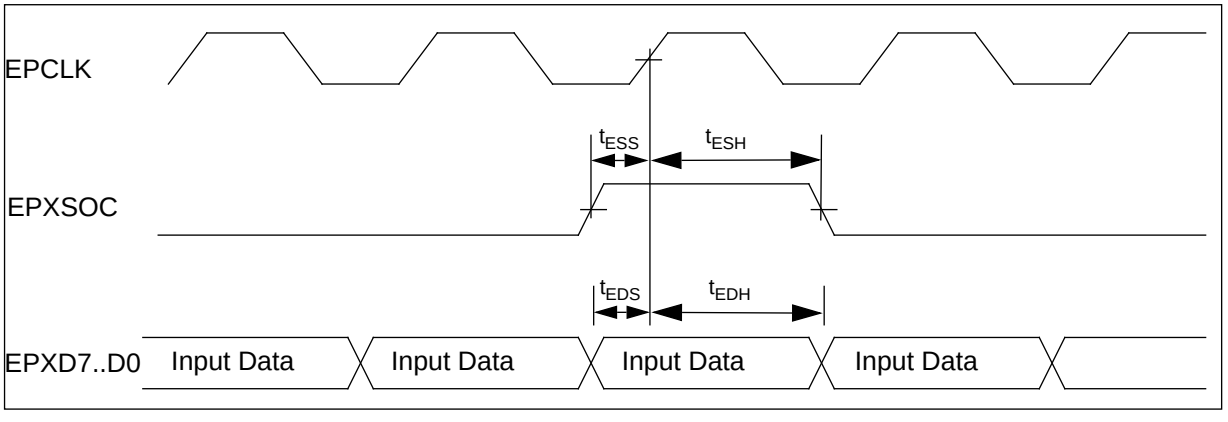

Figure 19 E-Input Port Timing

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Parameter	Ref. Signal	Abbrev.	Values			Units
			Min	Typical	Max	
EPXSOC Data setup Time	EPCLK	t_{ESS}	0	-	-	ns
EPXSOC Data Hold Time	EPCLK	t_{ESH}	3	-	-	ns
EPXD7..D0 Data setup Time	EPCLK	t_{EDS}	0	-	-	ns
EPXD7..D0 Data Hold Time	EPCLK	t_{EDH}	3	-	-	ns

Table 9 E-Input Port AC Timing Parameters

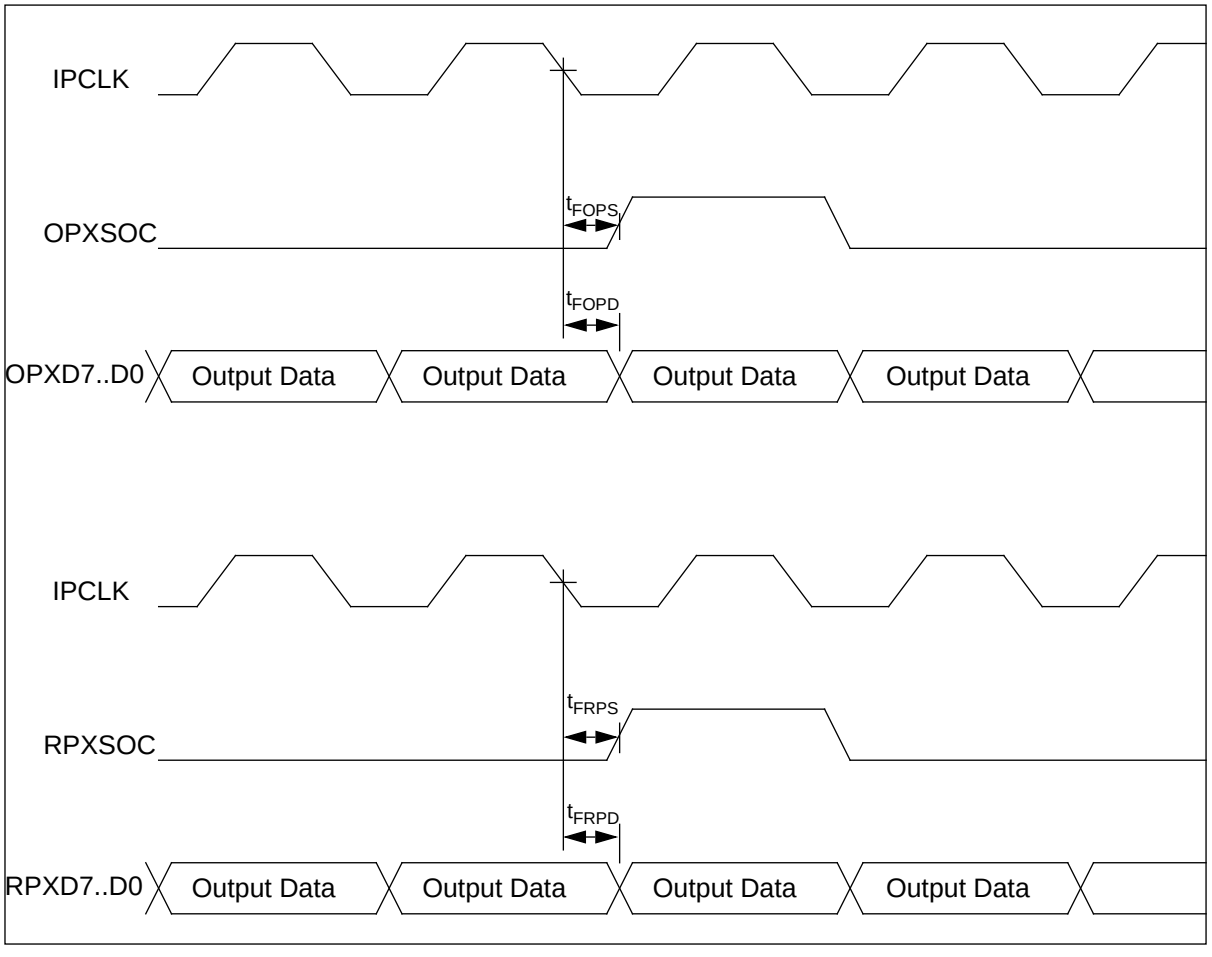

Figure 20 Output Port Timing-FCS

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Parameter	Ref. Signal	Abbrev.	Values			Units
			Min	Typical	Max	
OPXSOC output delay	IPCLK	t_{FOPS}	11	-	25	ns
OPXD7..D0 output delay	IPCLK	t_{FOPD}	16	-	25	ns
RPXSOC output delay	IPCLK	t_{FRPS}	12	-	25	ns
RPXD7..D0 output delay	IPCLK	t_{FRPD}	15	-	26	ns

Table 10 Output Port FCS Mode AC Timing Parameters

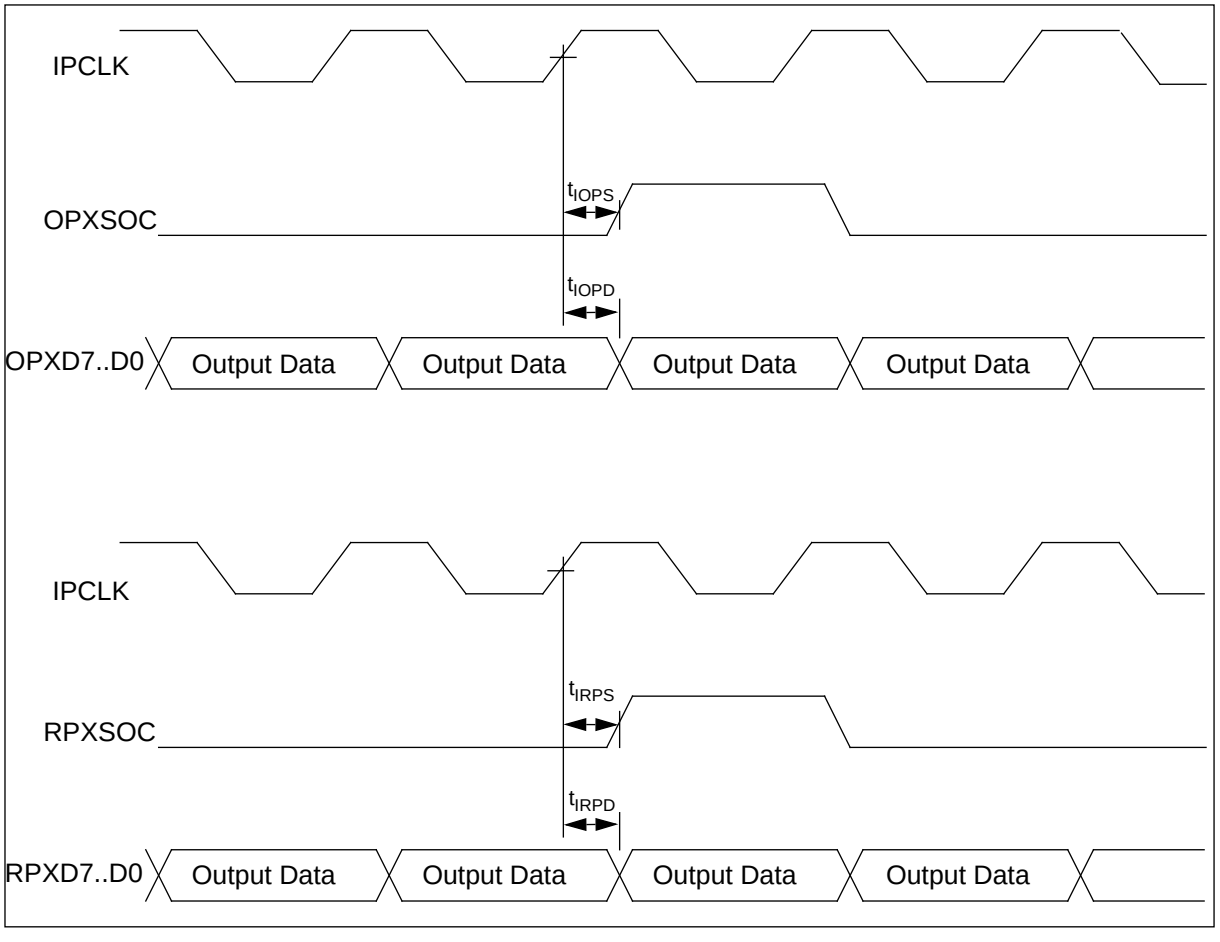

Figure 21 Output Port Timing-IFCS Mode

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Parameter	Ref. Signal	Abbrev.	Values			Units
			Min	Typical	Max	
OPXSOC output delay	IPCLK	t_{IOPS}	11	-	28	ns
OPXD7..D0 output delay	IPCLK	t_{IOPD}	15	-	29	ns
RPXSOC output delay	IPCLK	t_{IRPS}	11	-	25	ns
RPXD7..D0 output delay	IPCLK	t_{IRPD}	11	-	25	ns

Table 11 Output Port IFCS Mode AC Timing Parameters

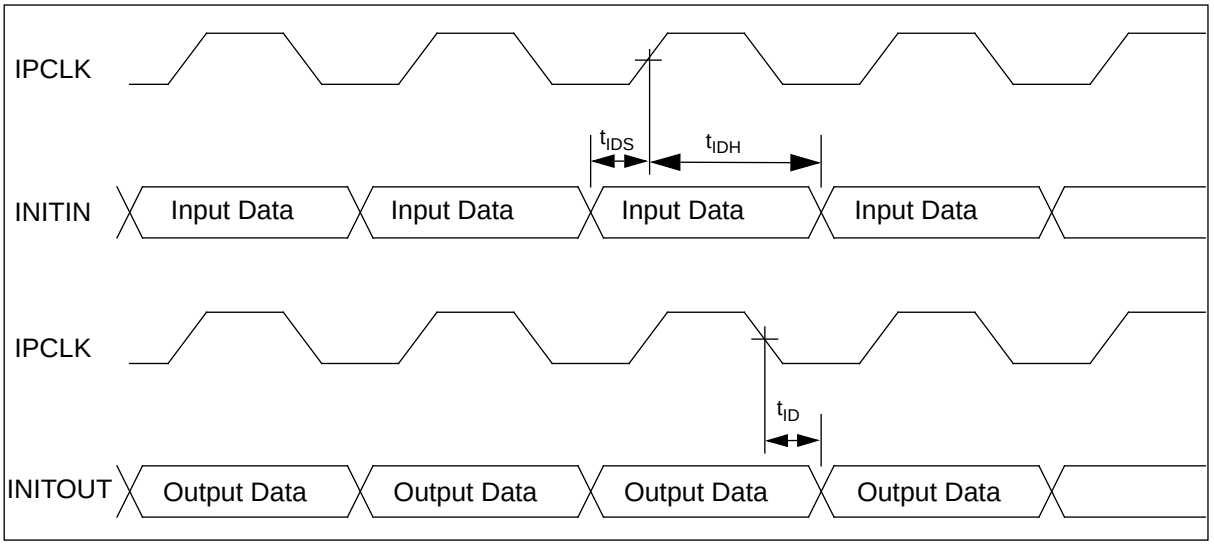

Figure 22 INIT Port Timing

Parameter	Ref. Signal	Abbrev.	Values			Units
			Min	Typical	Max	
INITIN Data Setup Time	IPCLK	t_{IDS}	5	-	-	ns
INITIN Data Hold Time	IPCLK	t_{IDH}	7	-	-	ns
INITOUT Out Delay	IPCLK	t_{ID}	12	-	23	ns

Table 12 INIT Port AC Timing Parameters

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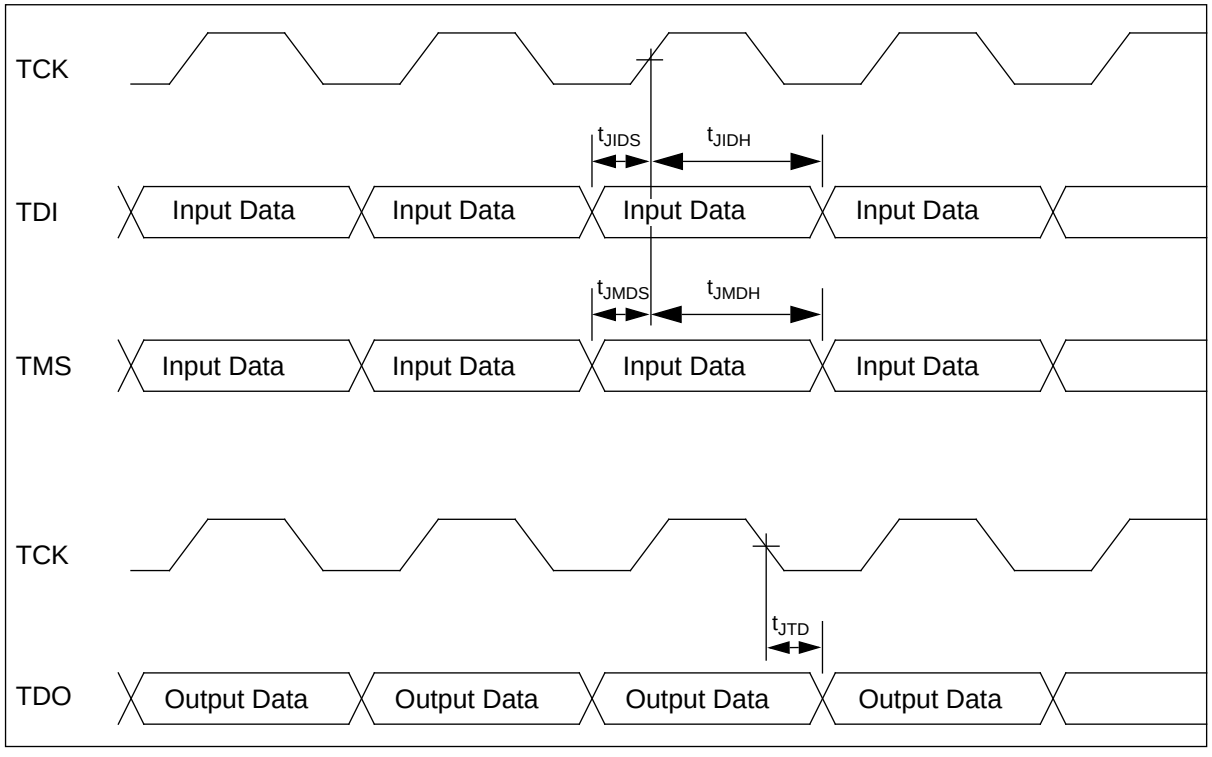

Figure 23 JTAG Port Timing

Parameter	Ref. Signal	Abbrev.	Values			Units
			Min	Typical	Max	
JTAG TMS Data Setup Time	TCK	t_{JMDS}	3	-	-	ns
JTAG TMS Data Hold Time	TCK	t_{JMDH}	1	-	-	ns
JTAG TDI Data Setup Time	TCK	t_{JIDS}	3	-	-	ns
JTAG TDI Data Hold Time	TCK	t_{JIDH}	1	-	-	ns
JTAG TDO Out Delay	TCK	t_{JTD}	5	-	11	ns

Table 13 JTAG Port AC Timing Parameters

NOTE:
All timings are characterized over the temperature range -40° to 70° Centigrade for device operation up to and including 20Mhz.

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C JTAG Boundary Scan Description

```
entity mb86680b is
 generic (PHYSICAL_PIN_MAP: string:="SQFP176_PACKAGE");
 port (      reset       :in bit;
             ipclk       :in bit;
             epclk       :in bit;
             tst1        :in bit;

             ip1soc      :in bit;
             ip1dt       :in bit_vector (0 to 7);
             ip2soc      :in bit;
             ip2dt       :in bit_vector (0 to 7);
             ip3soc      :in bit;
             ip3dt       :in bit_vector (0 to 7);
             ip4soc      :in bit;
             ip4dt       :in bit_vector (0 to 7);
             ep1soc      :in bit;
             ep1dt       :in bit_vector (0 to 7);
             ep2soc      :in bit;
             ep2dt       :in bit_vector (0 to 7);
             ep3soc      :in bit;
             ep3dt       :in bit_vector (0 to 7);
             ep4soc      :in bit;
             ep4dt       :in bit_vector (0 to 7);
             initin      :in bit;
             tst2        :in bit;
             tst3        :in bit;
             tck         :in bit;
             tms         :in bit;
             tdi         :in bit;
             vd5         :linkage bit_vector (0 to 5);
             vss         :linkage bit_vector (0 to 11);
             op1soc      :buffer bit;
             op1dt       :buffer bit_vector (0 to 7);
             op2soc      :buffer bit;
             op2dt       :buffer bit_vector (0 to 7);
             op3soc      :buffer bit;
             op3dt       :buffer bit_vector (0 to 7);
             op4soc      :buffer bit;
             op4dt       :buffer bit_vector (0 to 7);
             rp1soc      :buffer bit;
             rp1dt       :buffer bit_vector (0 to 7);
             rp2soc      :buffer bit;
             rp2dt       :buffer bit_vector (0 to 7);
```

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```
        rp3soc      :buffer bit;
        rp3dt       :buffer bit_vector (0 to 7);
        rp4soc      :buffer bit;
        rp4dt       :buffer bit_vector (0 to 7);
        opclk       :buffer bit;
        initout     :buffer bit;
        tst4        :buffer bit;
        tdo         :out bit);

use STD_1149_1_1990.all;   -- Get Std 1149.1-1994 attributes and definitions

attribute COMPONENT_CONFORMANCE of mb86680b: ENTITY IS ”STD_1149_1_1993”;

attribute PIN_MAP of mb86680b: entity is PHYSICAL_PIN_MAP;

constant FPT_208P_PACKAGE:

PIN_MAP_STRING:=        ”reset :111,”&
                        ”ipclk :175,
                        “epclk :092”,&
                        “tst1 :173,”&
                        ”ip1soc:139,”&
                        ”ip1dt   :(133,134,136,137,138,140,141,142),”&
                        ”ip2soc:149,”&
                        ”ip2dt   :(143,145,146,147,148,150,151,152),”&
                        ”ip3soc:159,”&
                        ”ip3dt   :(153,155,156,157,158,160,161,162),”&
                        ”ip4soc:169,”&
                        ”ip4dt   :(163,165,166,167,168,170,171,172),”&
                        ”ep1soc:126,”&
                        ”ep1dt  :(131,130,129,128,127,125,124,123),”&
                        ”ep2soc:116,”&
                        ”ep2dt  :(122,121,119,118,117,115,114,113),”&
                        ”ep3soc:105,”&
                        ”ep3dt  :(112,109,108,107,106,104,103,102),”&
                        ”ep4soc:095,”&
                        ”ep4dt  :(101,099,098,097,096,094,093,090),”&
                        ”initin :089,”&
                        ”tst2  :176,”&
                        ”tst3  :132,”&
                        ”tdi :042,”&
                        ”tms :043,”&
                        ”tck :044,”&
```

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```
                                ”vd5:(022,066,086,110,154,174),”&

                                ”vss:(003,012,032,047,056,076,091,100,120,135,144,164),”&
                                ”op1soc:007,”&
                                ”op1dt :(001,002,004,005,006,008,009,010),”&
                                ”op2soc:017,”&
                                ”op2dt :(011,013,014,015,016,018,019,020),”&
                                ”op3soc:027,”&
                                 ”op3dt :(021,023,024,025,026,028,029,030),”&
                                ”op4soc:037,”&
                                ”op4dt :(031,033,034,035,036,038,039,040),”&
                                ”rp1soc:082,”&
                                ”rp1dt :(088,087,085,084,083,081,080,079),”&
                                ”rp2soc:072,”&
                                ”rp2dt :(078,077,075,074,073,071,070,069),”&
                                ”rp3soc:062,”&
                                ”rp3dt :(068,067,065,064,063,061,060,059),”&
                                ”rp4soc:052,”&
                                ”rp4dt  :(058,057,055,054,053,051,050,049),”&

                                ”opclk :046,”&
                                ”initout :048,”&
                                ”tst4 :045,”&
                                ”tdo :041”;

attribute   TAP_SCAN_IN       of TDI     : signal is true;
attribute   TAP_SCAN_MODE     of TMS     : signal is true;
attribute   TAP_SCAN_OUT      of TDO     : signal is true;
attribute   TAP_SCAN_CLOCK    of TCK     : signal is (20.0e6, BOTH);

attribute   INSTRUCTION_LENGTH of mb86680b: entity is 2;
attribute INSTRUCTION_OPCODE of mb86680b: entity is
            ”BYPASS           (11),” &
            ”EXTEST           (00),” &
            ”SAMPLE           (01),” &
            ”INTEST           (10)”;

attribute   INSTRUCTION_CAPTURE     of mb86680b       : entity is “01”;
attribute   BOUNDARY_CELLS          of mb86680b       : entity is “BC_1, BC_4”;
attribute   BOUNDARY_LENGTH         of mb86680b       : entity is 154;
attribute BOUNDARY_REGISTER of mb86680b               : entity is
```

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num	cell	port	function	safe
”000	(BC_1,	INITOUT,	OUTPUT2,	X),”&
”001	(BC_1,	TST4,	OUTPUT2,	X),”&
”002	(BC_1,	OPCLK,	OUTPUT2,	X),”&
”003	(BC_1,	RP4DT(0),	OUTPUT2,	X),”&
”004	(BC_1,	RP4DT(1),	OUTPUT2,	X),”&
”005	(BC_1,	RP4DT(2),	OUTPUT2,	X),”&
”006	(BC_1,	RP4DT(3),	OUTPUT2,	X),”&
”007	(BC_1,	RP4DT(4),	OUTPUT2,	X),”&
”008	(BC_1,	RP4DT(5),	OUTPUT2,	X),”&
”009	(BC_1,	RP4DT(6),	OUTPUT2,	X),”&
”010	(BC_1,	RP4DT(7),	OUTPUT2,	X),”&
”011	(BC_1,	RP4SOC,	OUTPUT2,	X),”&
”012	(BC_1,	RP3DT(0),	OUTPUT2,	X),”&
”013	(BC_1,	RP3DT(1),	OUTPUT2,	X),”&
”014	(BC_1,	RP3DT(2),	OUTPUT2,	X),”&
”015	(BC_1,	RP3DT(3),	OUTPUT2,	X),”&
”016	(BC_1,	RP3DT(4),	OUTPUT2,	X),”&
”017	(BC_1,	RP3DT(5),	OUTPUT2,	X),”&
”018	(BC_1,	RP3DT(6),	OUTPUT2,	X),”&
”019	(BC_1,	RP3DT(7),	OUTPUT2,	X),”&
”020	(BC_1,	RP3SOC,	OUTPUT2,	X),”&
”021	(BC_1,	RP2DT(0),	OUTPUT2,	X),”&
”022	(BC_1,	RP2DT(1),	OUTPUT2,	X),”&
”023	(BC_1,	RP2DT(2),	OUTPUT2,	X),”&
”024	(BC_1,	RP2DT(3),	OUTPUT2,	X),”&
”025	(BC_1,	RP2DT(4),	OUTPUT2,	X),”&
”026	(BC_1,	RP2DT(5),	OUTPUT2,	X),”&
”027	(BC_1,	RP2DT(6),	OUTPUT2,	X),”&
”028	(BC_1,	RP2DT(7),	OUTPUT2,	X),”&
”029	(BC_1,	RP2SOC,	OUTPUT2,	X),”&
”030	(BC_1,	RP1DT(0),	OUTPUT2,	X),”&
”031	(BC_1,	RP1DT(1),	OUTPUT2,	X),”&
”032	(BC_1,	RP1DT(2),	OUTPUT2,	X),”&
”033	(BC_1,	RP1DT(3),	OUTPUT2,	X),”&
”034	(BC_1,	RP1DT(4),	OUTPUT2,	X),”&
”035	(BC_1,	RP1DT(5),	OUTPUT2,	X),”&
”036	(BC_1,	RP1DT(6),	OUTPUT2,	X),”&
”037	(BC_1,	RP1DT(7),	OUTPUT2,	X),”&
”038	(BC_1,	RP1SOC,	OUTPUT2,	X),”&
”039	(BC_1,	INITIN,	INPUT,	X),”&
”040	(BC_1,	TST3,	INPUT,	X),”&
”041	(BC_1,	RESET,	INPUT,	X),”&
”042	(BC_4,	EPCLK,	CLOCK,	X),”&

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num	cell	port	function	safe
”043	(BC_1,	EP4DT(0),	INPUT,	X),”&
”044	(BC_1,	EP4DT(1),	INPUT,	X),”&
”045	(BC_1,	EP4DT(2),	INPUT,	X),”&
”046	(BC_1,	EP4DT(3),	INPUT,	X),”&
”047	(BC_1,	EP4DT(4),	INPUT,	X),”&
”048	(BC_1,	EP4DT(5),	INPUT,	X),”&
”049	(BC_1,	EP4DT(6),	INPUT,	X),”&
”050	(BC_1,	EP4DT(7),	INPUT,	X),”&
”051	(BC_1,	EP4SOC,	INPUT,	X),”&
”052	(BC_1,	EP3DT(0),	INPUT,	X),”&
”053	(BC_1,	EP3DT(1),	INPUT,	X),”&
”054	(BC_1,	EP3DT(2),	INPUT,	X),”&
”055	(BC_1,	EP3DT(3),	INPUT,	X),”&
”056	(BC_1,	EP3DT(4),	INPUT,	X),”&
”057	(BC_1,	EP3DT(5),	INPUT,	X),”&
”058	(BC_1,	EP3DT(6),	INPUT,	X),”&
”059	(BC_1,	EP3DT(7),	INPUT,	X),”&
”060	(BC_1,	EP3SOC,	INPUT,	X),”&
”061	(BC_1,	EP2DT(0),	INPUT,	X),”&
”062	(BC_1,	EP2DT(1),	INPUT,	X),”&
”063	(BC_1,	EP2DT(2),	INPUT,	X),”&
”064	(BC_1,	EP2DT(3),	INPUT,	X),”&
”065	(BC_1,	EP2DT(4),	INPUT,	X),”&
”066	(BC_1,	EP2DT(5),	INPUT,	X),”&
”067	(BC_1,	EP2DT(6),	INPUT,	X),”&
”068	(BC_1,	EP2DT(7),	INPUT,	X),”&
”069	(BC_1,	EP2SOC,	INPUT,	X),”&
”070	(BC_1,	EP1DT(0),	INPUT,	X),”&
”071	(BC_1,	EP1DT(1),	INPUT,	X),”&
”072	(BC_1,	EP1DT(2),	INPUT,	X),”&
”073	(BC_1,	EP1DT(3),	INPUT,	X),”&
”074	(BC_1,	EP1DT(4),	INPUT,	X),”&
”075	(BC_1,	EP1DT(5),	INPUT,	X),”&
”076	(BC_1,	EP1DT(6),	INPUT,	X),”&
”077	(BC_1,	EP1DT(7),	INPUT,	X),”&
”078	(BC_1,	EP1SOC,	INPUT,	X),”&
”079	(BC_1,	TST2,	INPUT,	X),”&
”080	(BC_4,	TST1,	CLOCK,	X),”&
”081	(BC_4,	IPCLK,	CLOCK,	X),”&
”082	(BC_1,	IP4DT(0),	INPUT,	X),”&
”083	(BC_1,	IP4DT(1),	INPUT,	X),”&
”084	(BC_1,	IP4DT(2),	INPUT,	X),”&
”085	(BC_1,	IP4DT(3),	INPUT,	X),”&

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num	cell	port	function	safe
”086	(BC_1,	IP4DT(4),	INPUT,	X),”&
”087	(BC_1,	IP4DT(5),	INPUT,	X),”&
”088	(BC_1,	IP4DT(6),	INPUT,	X),”&
”089	(BC_1,	IP4DT(7),	INPUT,	X),”&
”090	(BC_1,	IP4SOC,	INPUT,	X),”&
”091	(BC_1,	IP3DT(0),	INPUT,	X),”&
”092	(BC_1,	IP3DT(1),	INPUT,	X),”&
”093	(BC_1,	IP3DT(2),	INPUT,	X),”&
”094	(BC_1,	IP3DT(3),	INPUT,	X),”&
”095	(BC_1,	IP3DT(4),	INPUT,	X),”&
”096	(BC_1,	IP3DT(5),	INPUT,	X),”&
”097	(BC_1,	IP3DT(6),	INPUT,	X),”&
”098	(BC_1,	IP3DT(7),	INPUT,	X),”&
”099	(BC_1,	IP3SOC,	INPUT,	X),”&
”100	(BC_1,	IP2DT(0),	INPUT,	X),”&
”101	(BC_1,	IP2DT(1),	INPUT,	X),”&
”102	(BC_1,	IP2DT(2),	INPUT,	X),”&
”103	(BC_1,	IP2DT(3),	INPUT,	X),”&
”104	(BC_1,	IP2DT(4),	INPUT,	X),”&
”105	(BC_1,	IP2DT(5),	INPUT,	X),”&
”106	(BC_1,	IP2DT(6),	INPUT,	X),”&
”107	(BC_1,	IP2DT(7),	INPUT,	X),”&
”108	(BC_1,	IP2SOC,	INPUT,	X),”&
”109	(BC_1,	IP1DT(0),	INPUT,	X),”&
”110	(BC_1,	IP1DT(1),	INPUT,	X),”&
”111	(BC_1,	IP1DT(2),	INPUT,	X),”&
”112	(BC_1,	IP1DT(3),	INPUT,	X),”&
”113	(BC_1,	IP1DT(4),	INPUT,	X),”&
”114	(BC_1,	IP1DT(5),	INPUT,	X),”&
”115	(BC_1,	IP1DT(6),	INPUT,	X),”&
”116	(BC_1,	IP1DT(7),	INPUT,	X),”&
”117	(BC_1,	IP1SOC,	INPUT,	X),”&
”118	(BC_1,	OP4DT(0),	OUTPUT2,	X),”&
”119	(BC_1,	OP4DT(1),	OUTPUT2,	X),”&
”120	(BC_1,	OP4DT(2),	OUTPUT2,	X),”&
”121	(BC_1,	OP4DT(3),	OUTPUT2,	X),”&
”122	(BC_1,	OP4DT(4),	OUTPUT2,	X),”&
”123	(BC_1,	OP4DT(5),	OUTPUT5,	X),”&
”124	(BC_1,	OP4DT(6),	OUTPUT2,	X),”&
”125	(BC_1,	OP4DT(7),	OUTPUT2,	X),”&
”126	(BC_1,	OP4SOC,	OUTPUT2,	X),”&
”127	(BC_1,	OP3DT(0),	OUTPUT2,	X),”&
”128	(BC_1,	OP3DT(1),	OUTPUT2,	X),”&

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num	cell	port	function	safe
”129	(BC_1,	OP3DT(2),	OUTPUT2,	X),”&
”130	(BC_1,	OP3DT(3),	OUTPUT2,	X),”&
”131	(BC_1,	OP3DT(4),	OUTPUT2,	X),”&
”132	(BC_1,	OP3DT(5),	OUTPUT2,	X),”&
”133	(BC_1,	OP3DT(6),	OUTPUT2,	X),”&
”134	(BC_1,	OP3DT(7),	OUTPUT2,	X),”&
”135	(BC_1,	OP3SOC,	OUTPUT2,	X),”&
”136	(BC_1,	OP2DT(0),	OUTPUT2,	X),”&
”137	(BC_1,	OP2DT(1),	OUTPUT2,	X),”&
”138	(BC_1,	OP2DT(2),	OUTPUT2,	X),”&
”139	(BC_1,	OP2DT(3),	OUTPUT2,	X),”&
”140	(BC_1,	OP2DT(4),	OUTPUT2,	X),”&
”141	(BC_1,	OP2DT(5),	OUTPUT2,	X),”&
”142	(BC_1,	OP2DT(6),	OUTPUT2,	X),”&
”143	(BC_1,	OP2DT(7),	OUTPUT2,	X),”&
”144	(BC_1,	OP2SOC,	OUTPUT2,	X),”&
”145	(BC_1,	OP1DT(0),	OUTPUT2,	X),”&
”146	(BC_1,	OP1DT(1),	OUTPUT2,	X),”&
”147	(BC_1,	OP1DT(2),	OUTPUT2,	X),”&
”148	(BC_1,	OP1DT(3),	OUTPUT2,	X),”&
”149	(BC_1,	OP1DT(4),	OUTPUT2,	X),”&
”150	(BC_1,	OP1DT(5),	OUTPUT2,	X),”&
”151	(BC_1,	OP1DT(6),	OUTPUT2,	X),”&
”152	(BC_1,	OP1DT(7),	OUTPUT2,	X),”&
”153	(BC_1,	OP1SOC,	OUTPUT2,	X)”;

end mb86680b;

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D Pin Assignments

D.1 Pin Diagram

Pin Assignment below details the actual pin layout, whilst the table overleaf details the signals.

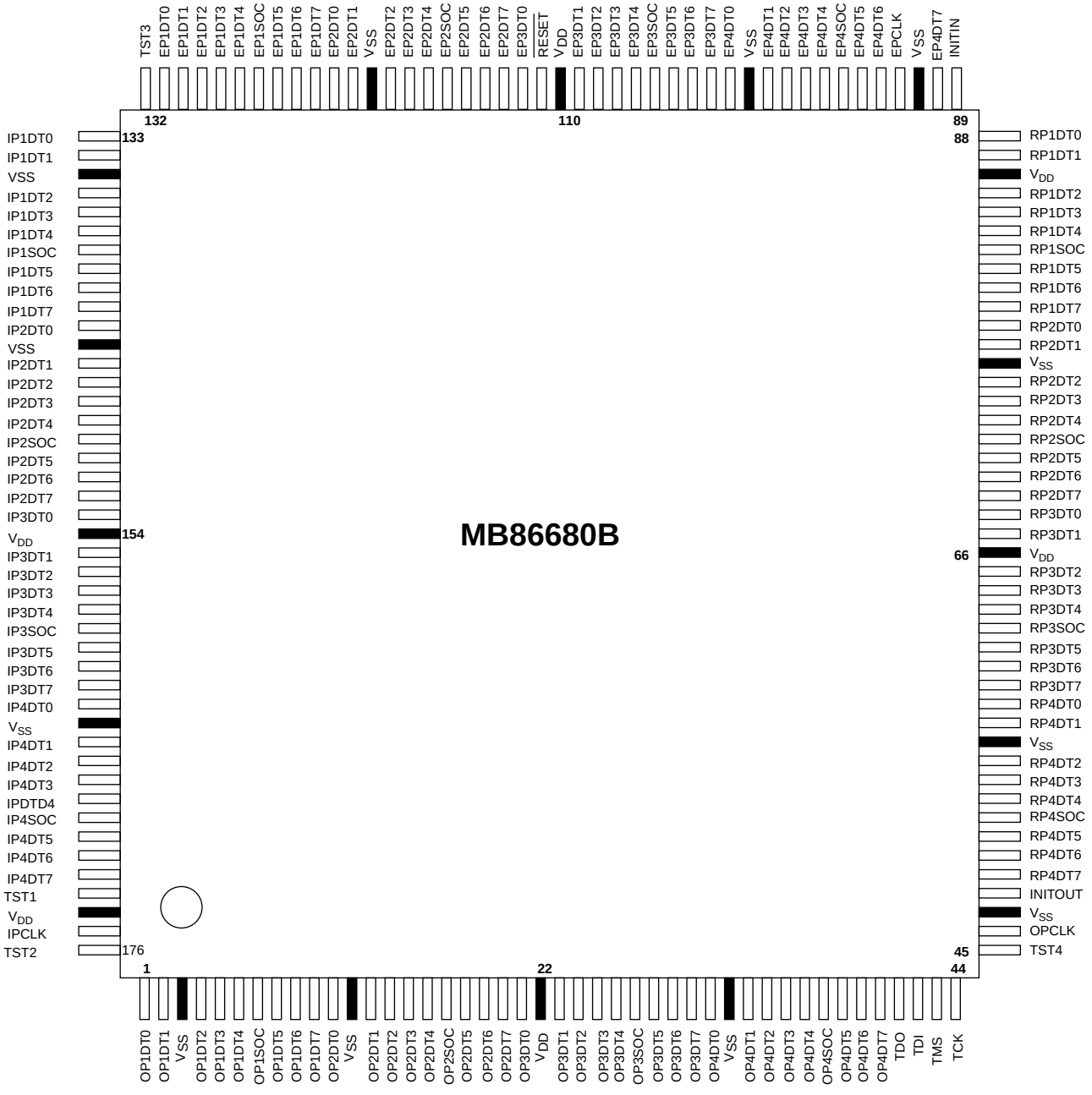

Figure 24 Pin Assignment

D.2 Pin Assignments

Pin No.	Pin Name	Type	Function
1	OP1DT0	O	Output Port1, bit D0 (LSB)
2	OP1DT1	O	Output Port1, bit D1
3	V_{SS}	-	
4	OP1DT2	O	Output Port1, bit D2
5	OP1DT3	O	Output Port1, bit D3
6	OP1DT4	O	Output Port1, bit D4
7	OP1SOC	O	Output Port1, Start of Cell Signal
8	OP1DT5	O	Output Port1, bit D5
9	OP1DT6	O	Output Port1, bit D6
10	OP1DY7	O	Output Port1, bit D7 (MSB)
11	OP2DT0	O	Output Port2, bit D0 (LSB)
12	V_{SS}	-	
13	OP2DT1	O	Output Port2, bit D1
14	OP2DT2	O	Output Port2, bit D2
15	OP2DT3	O	Output Port2, bit D3
16	OP2DT4	O	Output Port2, bit D4
17	OP2SOC	O	Output Port2, Start of Cell Signal
18	OP2DT5	O	Output Port2, bit D5
19	OP2DT6	O	Output Port2, bit D6
20	OP2DT7	O	Output Port2, bit D7 (MSB)
21	OP3DT0	O	Output Port3, bit D0 (LSB)
22	V_{DD}	-	
23	OP3DT1	O	Output Port3, bit D1
24	OP3DT2	O	Output port 3, bit D2
25	OP3DT3	O	Output port 3, bit D3
26	OP3DT4	O	Output port 3, bit D4
27	OP3SOC	O	Output port 3,Start of Cell Signal
28	OP3DT5	O	Output port 3, bit D5
29	OP3DT6	O	Output port 3, bit D6
30	OP3DT7	O	Output port 4, bit D7 (MSB)
31	OP4DT0	O	Output port 4, bit D0 (LSB)
32	V_{SS}	-	
33	OP4DT1	O	Output port 4, bit D1
34	OP4DT2	O	Output port 4, bit D2
35	OP4DT3	O	Output Port4, bit D3

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Pin No.	Pin Name	Type	Function
36	OP4DT4	O	Output Port4, bit D4
37	OP4SOC	O	Output Port4, Start of Cell Signal
38	OP4DT5	O	Output Port4, bit D5
39	OP4DT6	O	Output Port4, bit D6
40	OP4DT7	O	Output Port4, bit D7 (MSB)
41	TDO	O	JTAG Test Data Output
42	TDI	I	JTAG Test Data Input
43	TMS	I	JTAG Test Mode Select
44	TCK	I	JTAG Test Clock
45	TST4	O	Reserved Test Output pin
46	OPCLK	O	Output clock signal
47	V_{SS}	-	
48	INITOUT	O	Initialisation Output signal
49	RP4DT7	O	Regeneration port 4, bit D7 (MSB)
50	RP4DT6	O	Regeneration port 4, bit D6
51	RP4DT5	O	Regeneration port 4, bit D5
52	RP4SOC	O	Regeneration port 4, Start of Cell signal
53	RP4DT4	O	Regeneration port 4, bit D4
54	RP4DT3	O	Regeneration Port 4, bit D3
55	RP4DT2	O	Regeneration Port 4, bit D2
56	V_{SS}	-	
57	RP4DT1	O	Regeneration Port 4, bit D1
58	RP4DT0	O	Regeneration Port 4, bit D0 (LSB)
59	RP3DT7	O	Regeneration Port 3, bit D7 (MSB)
60	RP3DT6	O	Regeneration Port 3, bit D6
61	RP3DT5	O	Regeneration Port 3, bit D5
62	RP3SOC	O	Regeneration Port 3, Start of Cell signal
63	RP3DT4	O	Regeneration Port 3, bit D4
64	RP3DT	O	Regeneration Port 3, bit D3
65	RP3DT2	O	Regeneration Port 3, bit D2
66	V_{DD}	-	
67	RP3DT1	O	Regeneration Port 3, bit D1
68	RP3DT0	O	Regeneration Port 3, bit D0 (LSB)
69	RP2DT7	O	Regeneration Port 2, bit D7 (MSB)
70	RP2DT6	O	Regeneration Port 2, bit D6
71	RP2DT5	O	Regeneration Port 2, bit D5
72	RP2SOC	O	Regeneration Port 2, Start of Cell signal
73	RP2DT4	O	Regeneration Port 2, bit D4

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Pin No.	Pin Name	Type	Function
74	RP2DT3	O	Regeneration Port 2, bit D3
75	RP2DT2	O	Regeneration Port 2, bit D2
76	V_{SS}	-	
77	RP2DT1	O	Regeneration Port 2, bit D1
78	RP2DT0	O	Regeneration Port 2, bit D0 (LSB)
79	RP1DT7	O	Regeneration Port 1, bit D7 (MSB)
80	RP1DT6	O	Regeneration Port 1, bit D6
81	RP1DT5	O	Regeneration Port 1, bit D5
82	RP1SOC	O	Regeneration Port 1, Start of Cell signal
83	RP1DT4	O	Regeneration Port 1, bit D4
84	RP1DT3	O	Regeneration Port 1, bit D3
85	RP1DT2	O	Regeneration Port 1, bit D2
86	V_{DD}	-	
87	RP1DT1	O	Regeneration Port 1, bit D1
88	RP1DT0	O	Regeneration Port 1, bit D0 (LSB)
89	INITIN	I	Initialisation input signal
90	EP4DT7	I	Expansion port 4, bit D7 (MSB)
91	V_{SS}	-	
92	EPCLK	I	Expansion port clock signal
93	EP4DT6	I	Expansion port 4, bit D6
94	EP4DT5	I	Expansion port 4, bit D5
95	EP4SOC	I	Expansion port 4, Start of Cell signal
96	EP4DT4	I	Expansion port 4, bit D4
97	EP4DT3	I	Expansion port 4, bit D3
98	EP4DT2	I	Expansion port 4, bit D2
99	EP4DT1	I	Expansion port 4, bit D1
100	V_{SS}	-	
101	EP4DT0	I	Expansion port 4, bit D0 (LSB)
102	EP3DT7	I	Expansion port 3, bit D7 (MSB)
103	EP3DT6	I	Expansion port 3, bit D6
104	EP3DT5	I	Expansion port 3, bit D5
105	EP3SOC	I	Expansion port 3, Start of Cell signal
106	EP3DT4	I	Expansion port 3, bit D4
107	EP3DT3	I	Expansion port 3, bit D3
108	EP3DT2	I	Expansion port 3, bit D2
109	EP3DT1	I	Expansion port 3, bit D1
110	V_{DD}	-	
111	RESET	I	Reset

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Pin No.	Pin Name	Type	Function
112	EP3DT0	I	Expansion port 3, bit D0 (LSB)
113	EP2DT7	I	Expansion port 2, bit D7 (MSB)
114	EP2DT6	I	Expansion port 2, bit D6
115	EP2DT5	I	Expansion port 2, bit D5
116	EP2SOC	I	Expansion port 2, Start of Cell signal
117	EP2DT4	I	Expansion port 2, bit D4
118	EP2DT3	I	Expansion port 2, bit D3
119	EP2DT2	I	Expansion port 2, bit D2
120	V_{SS}	-	
121	EP2DT1	I	Expansion port 2, bit D1
122	EP2DT0	I	Expansion port 2, bit D0 (LSB)
123	EP1DT7	I	Expansion port 1, bit D7 (MSB)
124	EP1DT6	I	Expansion port 1, bit D6
125	EP1DT5	I	Expansion port 1, bit D5
126	EP1SOC	I	Expansion port 1, Start of Cell signal
127	EP1DT4	I	Expansion port 1, bit D4
128	EP1DT3	I	Expansion port 1, bit D3
129	EP1DT2	I	Expansion port 1, bit D2
130	EP1DT1	I	Expansion port 1, bit D1
131	EP1DT0	I	Expansion port 1, bit D0 (LSB)
132	TST3	I	Reserved Test Input pin-Connect to V_{SS}
133	IP1DT0	I	Input port 1, bit D0 (LSB)
134	IP1DT1	I	Input port 1, bit D1
135	V_{SS}	-	
136	IP1DT2	I	Input port 1, bit D2
137	IP1DT3	I	Input port 1, bit D3
138	IP1DT4	I	Input port 1, bit D4
139	IP1SOC	I	Input port1, Start of Cell signal
140	IP1DT5	I	Input port1, bit D5
141	IP1DT6	I	Input port1, bit D6
142	IP1DT7	I	Input port1, bit D7 (MSB)
143	IP2DT0	I	Input port2, bit D0 (LSB)
144	V_{SS}	-	
145	IP2DT1	I	Input port2, bit D1
146	IP1DT2	I	Input port2, bit D2
147	IP1DT3	I	Input port2, bit D3
148	IP1DT4	I	Input port2, bit D4
149	IP2SOC	I	Input port2, Start of Cell signal

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Pin No.	Pin Name	Type	Function
150	IP2DT5	I	Input port2, bit D5
151	IP2DT6	I	Input port2, bit D6
152	IP2DT7	I	Input port2, bit D7 (MSB)
153	IP3DT0	I	Input port3, bit D0 (LSB)
154	V_{DD}	-	
155	IP3DT1	I	Input port3, bit D1
156	IP3DT2	I	Input port3, bit D2
157	IP3DT3	I	Input port3, bit D3
158	IP3DT4	I	Input port3, bit D4
159	IP3SOC	I	Input port3, Start of Cell signal
160	IP3DT5	I	Input port3, bit D5
161	IP3DT6	I	Input port3, bit D6
162	IP3DT7	I	Input port3, bit D7 (MSB)
163	IP4DT0	I	Input port4, bit D0 (LSB)
164	V_{SS}	-	
165	IP4DT1	I	Input port4, bit D1
166	IP4DT2	I	Input port4, bit D2
167	IP4DT3	I	Input port4, bit D3
168	IP4DT4	I	Input port4, bit D4
169	IP4SOC	I	Input port4, Start of Cell signal
170	IP4DT5	I	Input port4, bit D5
171	IP4DT6	I	Input port4, bit D6
172	IP4DT7	I	Input port4, bit D7 (MSB)
173	TST1	I	Reserved Test Input pin-Connect to V_{SS}
174	V_{DD}	-	
175	IPCLK	I	Input clock signal
176	TST2	I	Reserved Test Input pin-Connect to V_{SS}

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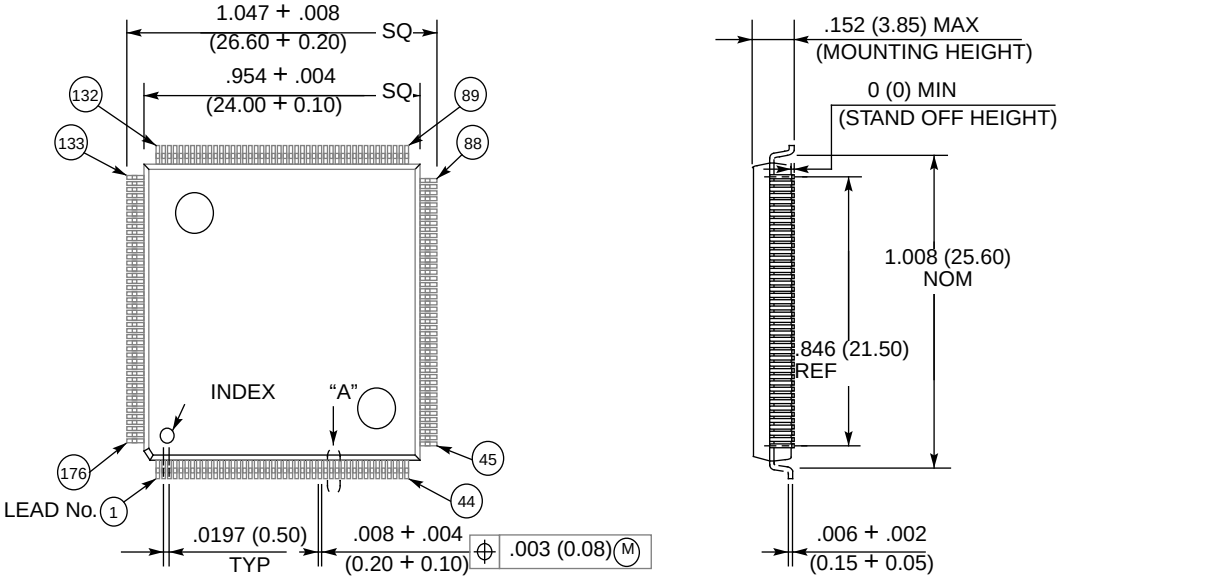
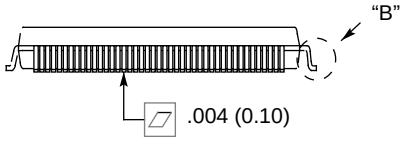
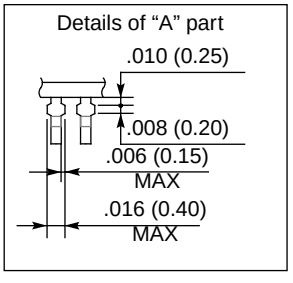
E Package Dimensions

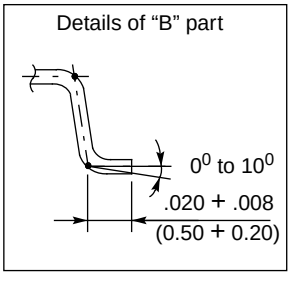
FPT-176P-M01

176-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-176P-M01)









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Dimensions in
inches (millimetres)

Revision Control

Revision Number	Date DD/MM/YY	Description of the Changes
4.2	11/09/96	Minor syntax corrections made to JTAG BSDL description in Appendix C. Correction to the Back page Revision Control Number.
4.25	06/01/97	Contact information updated

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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