TMS320F2808, TMS320F2806, TMS320F2801 Digital Signal Processors

Data Manual

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TEXAS INSTRUMENTS

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Revision History

This data sheet revision history highlights the technical changes made to the SPRS230A device-specific data sheet to make it an SPRS230B revision. The A revision was TI internal.

Scope: This document has been reviewed for technical accuracy; the technical content is up-to-date as of the specified release date with the following changes.

PAGE(S) NO.	ADDITIONS/CHANGES/DELETIONS
3−124	Added new information

Contents

List of Figures

Figure *Page*

List of Tables

1 Features

- High-Performance Static CMOS Technology
  - 100 MHz (10-ns Cycle Time)
  - Low-Power (1.8-V Core, 3.3-V I/O) Design
  - 3.3-V Flash Voltage
- JTAG Boundary Scan Support†
- High-Performance 32-Bit CPU (TMS320C28x)
  - 16 x 16 and 32 x 32 MAC Operations
  - 16 x 16 Dual MAC
  - Harvard Bus Architecture
  - Atomic Operations
  - Fast Interrupt Response and Processing
  - Unified Memory Programming Model
  - Code-Efficient (in C/C++ and Assembly)
- On-Chip Memory
  - F2808: 64K X 16 Flash, 18K X 16 SARAM
F2806: 32K X 16 Flash, 10K X 16 SARAM
F2801: 16K X 16 Flash, 6K X 16 SARAM
  - 1K x 16 OTP ROM
- Boot ROM (4K x 16)
  - With Software Boot Modes (via SCI, SPI, CAN, I^2C, and Parallel I/O)
  - Standard Math Tables
- Clock and System Control
  - Dynamic PLL Ratio Changes Supported
  - On-Chip Oscillator
  - Clock-Fail-Detect Mode
  - Watchdog Timer Module
- Any GPIO A Pin Can Be Connected to One of the Three External Core Interrupts
- Peripheral Interrupt Expansion (PIE) Block That Supports All 43 Peripheral Interrupts
- 128-Bit Security Key/Lock
  - Protects Flash/OTP/L0/L1 Blocks
  - Prevents Firmware Reverse Engineering
- Enhanced Control Peripherals
  - Up to 16 PWM Outputs
  - Up to Four Capture Inputs
  - Up to Two Quadrature Encoder Interfaces
  - Up to Six 32-bit Timers
  - Up to Six 16-bit Timers
- Serial Port Peripherals
  - Up to 4 Serial Peripheral Interface (SPI) Modules
  - Up to 2 Serial Communications Interface (SCI), Standard UART Modules
  - Up to 2 Enhanced Controller Area Network (eCAN) Modules
  - One Inter-Integrated-Circuit (I^2C) Bus
- 12-Bit ADC, 16 Channels
  - 2 x 8 Channel Input Multiplexer
  - Two Sample-and-Hold
  - Single/Simultaneous Conversions
  - Fast Conversion Rate: 160 ns/6.25 MSPS
  - Internal or External Reference
- Three 32-Bit CPU-Timers
- Up to 35 Individually Programmable, Multiplexed General-Purpose Input/Output (GPIO) Pins With Input Filtering
- Advanced Emulation Features
  - Analysis and Breakpoint Functions
  - Real-Time Debug via Hardware
- Development Tools Include
  - ANSI C/C++ Compiler/Assembler/Linker
  - Supports TMS320C24x™/240x Instructions
  - Code Composer Studio™ IDE
  - DSP/BIOS™
  - JTAG Scan Controllers†
[Texas Instruments (TI) or Third-Party]
  - Evaluation Modules
  - Broad Third-Party Digital Motor Control Support
- Low-Power Modes and Power Savings
  - IDLE, STANDBY, HALT Modes Supported
  - Disable Individual Peripheral Clocks
- Package Options
  - Thin Quad Flatpack (PZ)
(2808, 2806, 2801)
  - MicroStar BGA (GGM, ZGM)
(2808, 2806, 2801)
- Temperature Options:
  - A: −40°C to 85°C
  - S: −40°C to 125°C

PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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† IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

PRODUCT PREVIEW

2 Introduction

The TMS320F2808, TMS320F2806, and TMS320F2801 devices, members of the TMS320C28x™ DSP generation, are highly integrated, high-performance solutions for demanding control applications.

Throughout this document, TMS320F2808, TMS320F2806, and TMS320F2801 are abbreviated as F2808, F2806, and F2801, respectively. Throughout this document all three devices are collectively referred to as F280x.

Table 2−1 provides a summary of each device's features.

Table 2−1. Hardware Features

FEATURE		F2808	F2806	F2801
Instruction cycle (at 100 MHz)		10 ns	10 ns	10 ns
Single-access RAM (SARAM) (16-bit word)		18K (L0, L1, M0, M1, H0)	10K (L0, L1, M0, M1)	6K (L0, M0, M1)
3.3-V on-chip flash (16-bit word)		64K	32K	16K
Code security for on-chip flash/SARAM/OTP blocks		Yes	Yes	Yes
Boot ROM (4K X 16)		Yes	Yes	Yes
One-time programmable (OTP) ROM		Yes	Yes	Yes
External memory interface		No	No	No
Enhanced PWM outputs (six 16-bit timer-based modules with 2 PWM outputs/module)		ePWM1, ePWM2, ePWM3, ePWM4, ePWM5, ePWM6	ePWM1, ePWM2, ePWM3, ePWM4, ePWM5, ePWM6	ePWM1, ePWM2, ePWM3
Enhanced 32-bit CAPTURE inputs or auxiliary PWM outputs		eCAP1, eCAP2, eCAP3, eCAP4	eCAP1, eCAP2, eCAP3, eCAP4	eCAP1, eCAP2
Enhanced 32-bit QEP channels (four inputs/channel)		eQEP1, eQEP2	eQEP1, eQEP2	eQEP1
Watchdog timer		Yes	Yes	Yes
12-Bit ADC channels		16	16	16
32-Bit CPU timers		3	3	3
Serial Peripheral Interface (SPI)		SPI-A, SPI-B, SPI-C, SPI-D	SPI-A, SPI-B, SPI-C, SPI-D	SPI-A, SPI-B
Serial Communications Interface (SCI)		SCI-A, SCI-B	SCI-A, SCI-B	SCI-A
Enhanced Controller Area Network (eCAN)		eCAN-A, eCAN-B	eCAN-A	eCAN-A
Inter-Integrated Circuit (I^2C)		I2C-A	I2C-A	I2C-A
Digital I/O pins (shared)		35	35	35
External interrupts		3	3	3
Supply voltage		1.8-V Core, 3.3-V I/O	1.8-V Core, 3.3-V I/O	1.8-V Core, 3.3-V I/O
Packaging		100-Pin PZ 100-Ball GGM, ZGM	100-Pin PZ 100-Ball GGM, ZGM	100-Pin PZ 100-Ball GGM, ZGM
Temperature options	A: −40°C to 85°C	Yes	Yes	Yes
	S: −40°C to 125°C†	Yes	Yes	Yes
Product status		TMX‡	TMX‡	TMX‡

† The Q temperature version will be available once the S version is qualified for the Q100 automotive fault grading.
‡ See Section 5.1, Device and Development Support Nomenclature for descriptions of TMS and TMX stages.
TMX: Experimental device that is not necessarily representative of the final device's electrical specifications
TMP: Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
TMS: Fully qualified production device

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2.1 Pin Assignments

The TMS320F2808, TMS320F2806, and TMS320F2801 100-pin PZ low-profile quad flatpack (LQFP) pin assignments are shown in Figure 2−1, Figure 2−2, and Figure 2−3, respectively. See Table 2−2 for a description of each pin function. Figure 2−4 shows the ball assignments for the 100-ball GGM MicroStar BGA™ package.

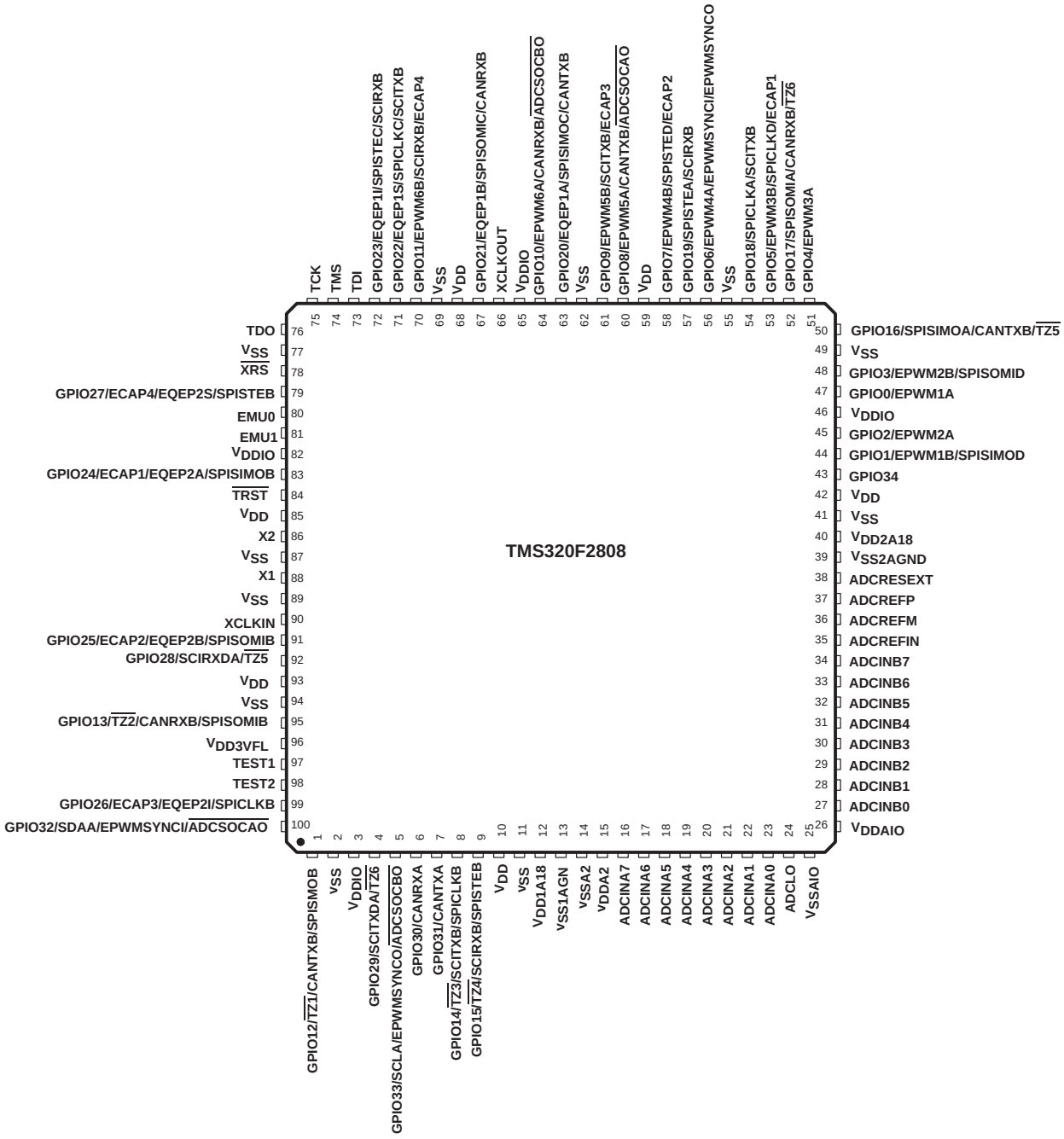

Figure 2−1. TMS320F2808 100-Pin PZ LQFP (Top View)

PRODUCT PREVIEW

PRODUCT PREVIEW

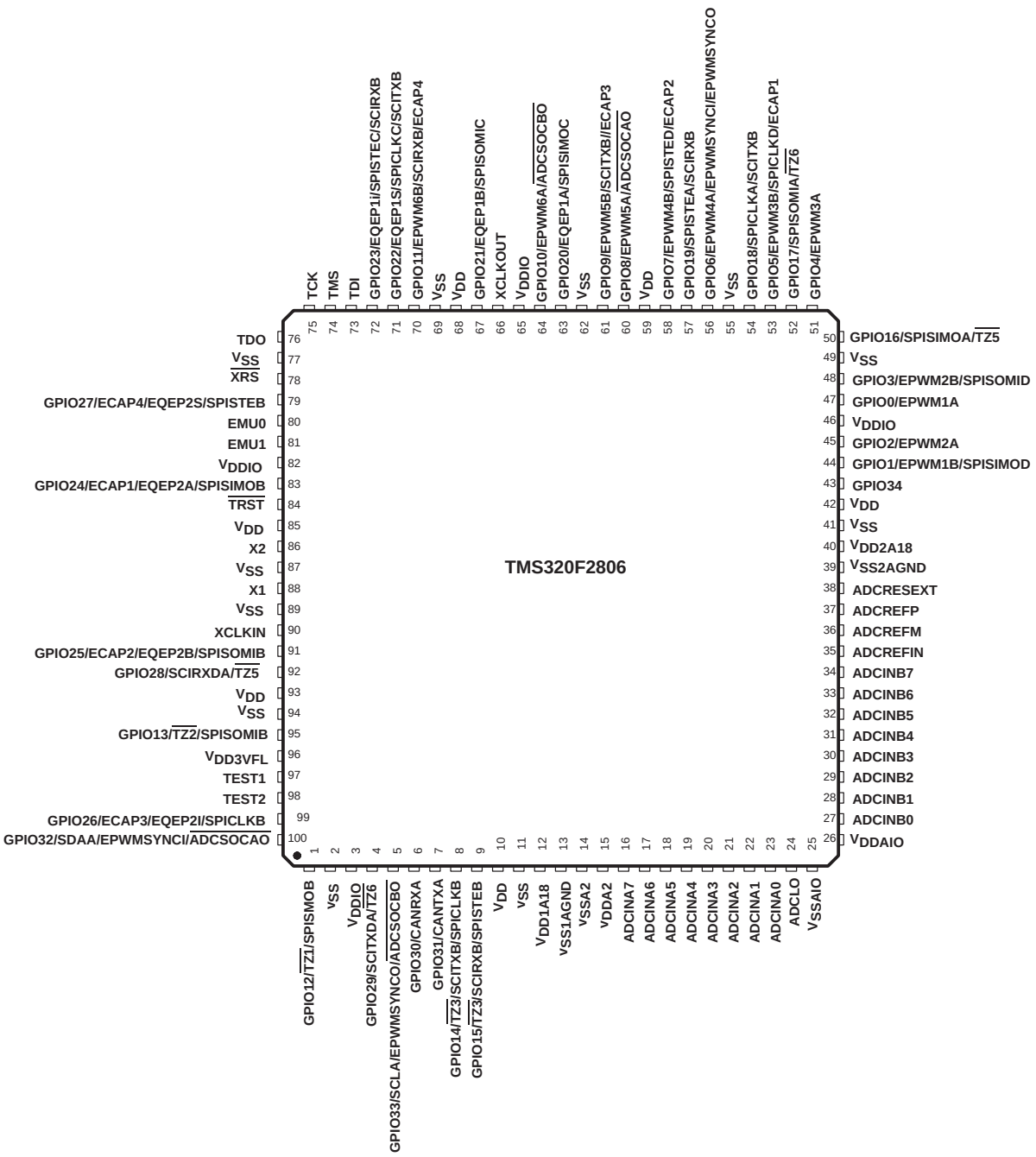

Figure 2−2. TMS320F2806 100-Pin PZ LQFP (Top View)

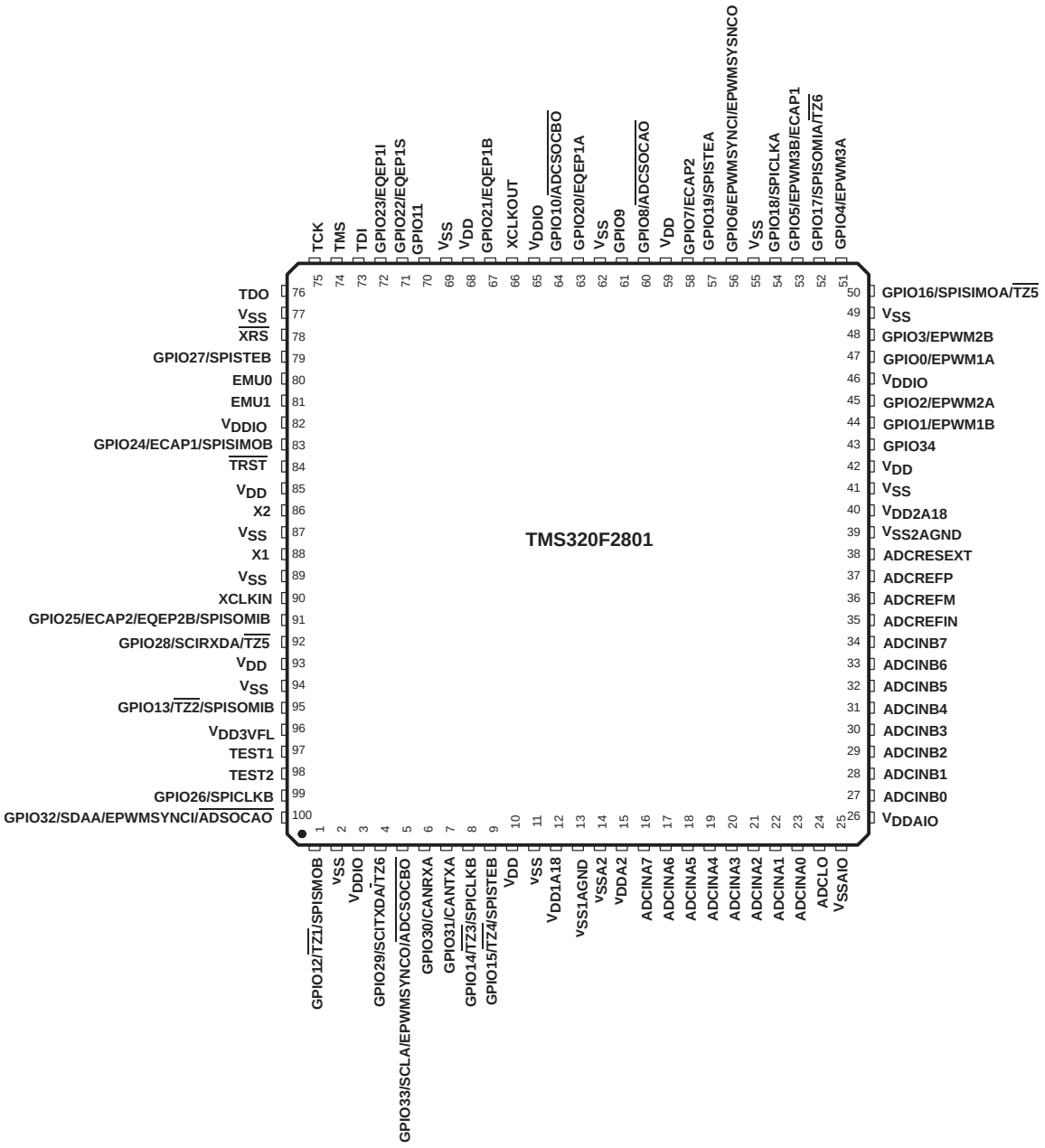

Figure 2−3. TMS320F2801 100-Pin PZ LQFP (Top View)

PRODUCT PREVIEW

PRODUCT PREVIEW

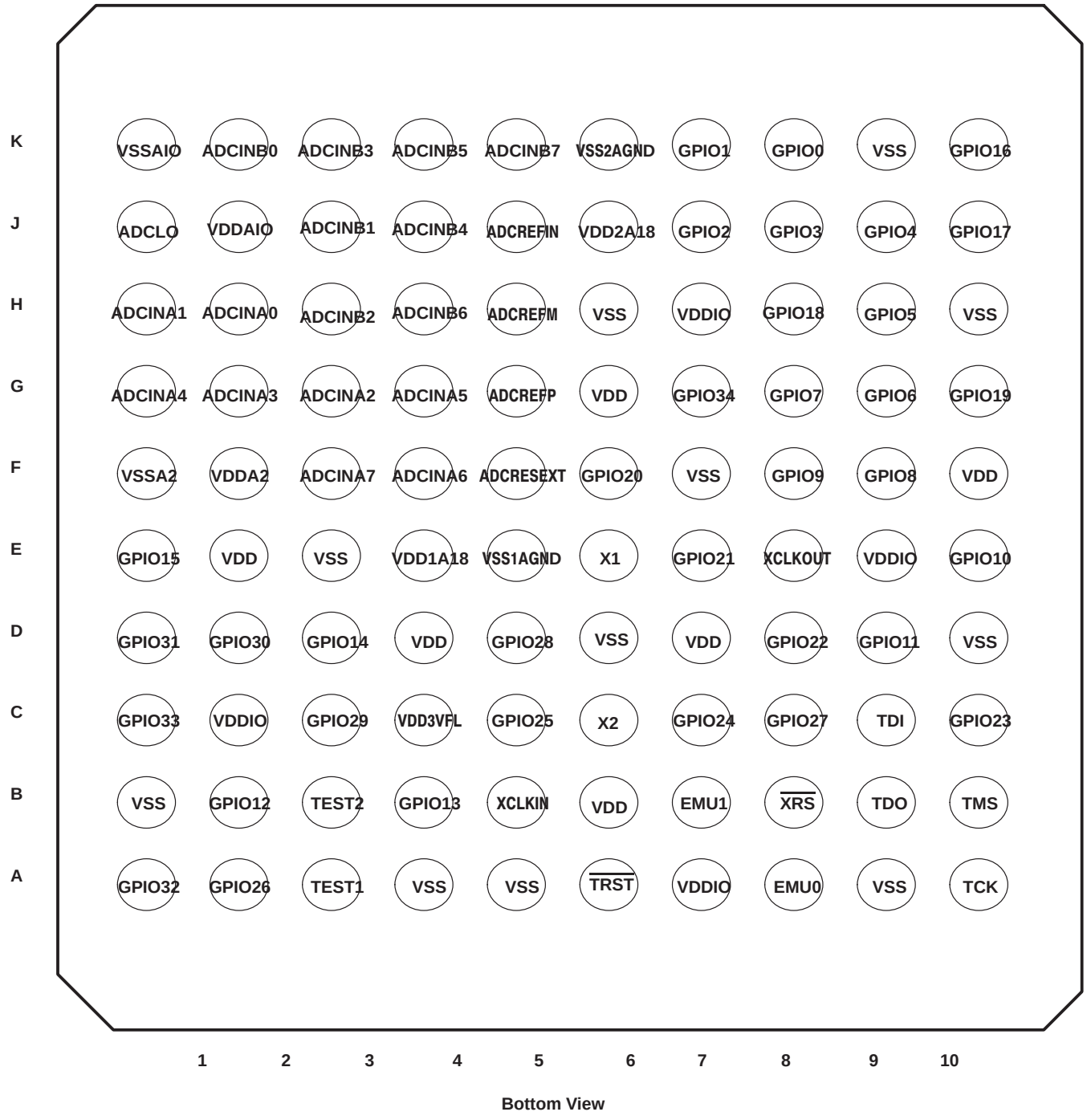

Figure 2−4. TMS320F280x 100-Ball GGM and ZGM MicroStar BGA™ (Bottom View)

2.2 Signal Descriptions

Table 2−2 describes the signals on the F280x devices. All digital inputs are TTL-compatible. All outputs are 3.3 V with CMOS levels. Inputs are not 5-V tolerant.

Table 2−2. Signal Descriptions

NAME	PZ PIN #	GGM BALL #	DESCRIPTION
JTAG			
$\overline{\text{TRST}}$	84	A6	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: Do not use pullup resistors on $\overline{\text{TRST}}$; it has an internal pulldown device. In a low-noise environment, $\overline{\text{TRST}}$ can be left floating. In a high-noise environment, an additional pulldown resistor may be needed. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Since this is application-specific, it is recommended that each target board is validated for proper operation of the debugger and the application. (I, ↓)
TCK	75	A10	JTAG test clock with internal pullup (I, ↑)
TMS	74	B10	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.(I, ↑)
TDI	73	C9	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (I, ↑)
TDO	76	B9	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) is shifted out of TDO on the falling edge of TCK. (O/Z, 8 mA drive)
EMU0	80	A8	Emulator pin 0. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. (I/O/Z, 8 mA drive, ↑)
EMU1	81	B7	Emulator pin 1. When $\overline{\text{TRST}}$ is driven high, EMU1 is used as an interrupt to or from the emulator system and is defined as input/output through the JTAG scan. (I/O/Z, 8 mA drive, ↑)
FLASH			
VDD3VFL	96	C4	3.3-V Flash Core Power Pin. This pin should be connected to 3.3 V at all times.
TEST1	97	A3	Test Pin. Reserved for TI. Must be left unconnected. (I/O)
TEST2	98	B3	Test Pin. Reserved for TI. Must be left unconnected. (I/O)
CLOCK			
XCLKOUT	66	E8	Output clock derived from SYSCLKOUT to be used as a general-purpose clock source. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. This is controlled by the bits 1,0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The status of the XCLKOUT pin may then be read through the XCLKOUTDAT bit in the XCLKOUT register. (I/O/Z, 8 mA drive)
XCLKIN	90	B5	External Oscillator Input. This pin is to feed clock from an external 3.3-V oscillator. If an external oscillator is not used, this pin must be tied to GND (I).
X1	88	E6	Internal Oscillator Input. A quartz crystal or a ceramic resonator may be connected across X1 and X2 (I). If an external oscillator is used, X1 must be tied to GND. The X1 pin is referenced to the 1.8-V core digital power supply. If a 3.3-V oscillator is to be used, connect it to XCLKIN and tie X1 to GND.

Legend: I/O/Z/OD: Input/Output/High Impedance/Open Drain
↑ Pullup
↓ Pulldown

† The pullups on the GPIO pins are disabled upon reset; they can be selectively enabled on a per-pin basis. This feature only applies to the GPIO pins.

‡ For pins with multiple functions, the function shown in Italicized bold face is the function upon reset.

§ In this section, all pins are I/O/Z, 4-mA drive typical (unless otherwise indicated), and have an internal pullup. The GPIO function is the default at reset. The peripheral signals that are listed under them are alternate functions.

PRODUCT PREVIEW

PRODUCT PREVIEW

Table 2−2. Signal Descriptions (continued)

NAME	PZ PIN #	GGM BALL #	DESCRIPTION
X2	86	C6	Internal Oscillator Output. A quartz crystal or a ceramic resonator may be connected across X1 and X2 (I). If X2 is not used it must be left unconnected.
RESET			
$\overline{\text{XRS}}$	78	B8	Device Reset (in) and Watchdog Reset (out). Device reset. $\overline{\text{XRS}}$ causes the device to terminate execution. The PC will point to the address contained at the location 0x3FFFC0. When $\overline{\text{XRS}}$ is brought to a high level, execution begins at the location pointed to by the PC. This pin is driven low by the DSP when a watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin (I/OD, ↑) is driven low for the watchdog reset duration of 512 XCLKIN cycles. (I/OD, ↑) The output buffer of this pin is an open-drain with an internal pullup (100 μA, typical). It is recommended that this pin be driven by an open-drain device.
ADC SIGNALS			
ADCINA7	16	F3	ADC Group A, Channel 7 Input (I)
ADCINA6	17	F4	ADC Group A, Channel 6 Input (I)
ADCINA5	18	G4	ADC Group A, Channel 5 Input (I)
ADCINA4	19	G1	ADC Group A, Channel 4 Input (I)
ADCINA3	20	G2	ADC Group A, Channel 3 Input (I)
ADCINA2	21	G3	ADC Group A, Channel 2 Input (I)
ADCINA1	22	H1	ADC Group A, Channel 1 Input (I)
ADCINA0	23	H2	ADC Group A, Channel 0 Input (I)
ADCINB7	34	K5	ADC Group B, Channel 7 Input (I)
ADCINB6	33	H4	ADC Group B, Channel 6 Input (I)
ADCINB5	32	K4	ADC Group B, Channel 5 Input (I)
ADCINB4	31	J4	ADC Group B, Channel 4 Input (I)
ADCINB3	30	K3	ADC Group B, Channel 3 Input (I)
ADCINB2	29	H3	ADC Group B, Channel 2 Input (I)
ADCINB1	28	J3	ADC Group B, Channel 1 Input (I)
ADCINB0	27	K2	ADC Group B, Channel 0 Input (I)
ADCLO	24	J1	Low Reference (connect to analog ground) (I)
ADCRESEXT	38	F5	External Current Bias Resistor. Connect a 22 kΩ resistor to analog ground.
ADCREFIN	35	J5	External Reference Input (I)
ADCREFP	37	G5	Internal Reference Positive Output (I/O)
ADCREFM	36	H5	Internal Reference Medium Output (I/O)
CPU AND I/O POWER PINS			
V_{DDA2}	15	F2	ADC Analog Power Pin (3.3 V)
V_{SSA2}	14	F1	ADC Analog Ground Pin
V_{DDAIO}	26	J2	ADC Analog I/O power pin (3.3 V)

Legend: I/O/Z/OD: Input/Output/High Impedance/Open Drain
↑ Pullup
↓ Pulldown

† The pullups on the GPIO pins are disabled upon reset; they can be selectively enabled on a per-pin basis. This feature only applies to the GPIO pins.

‡ For pins with multiple functions, the function shown in Italicized bold face is the function upon reset.

§ In this section, all pins are I/O/Z, 4-mA drive typical (unless otherwise indicated), and have an internal pullup. The GPIO function is the default at reset. The peripheral signals that are listed under them are alternate functions.

Table 2−2. Signal Descriptions (continued)

NAME	PZ PIN #	GGM BALL #	DESCRIPTION
V_{SSAIO}	25	K1	ADC Analog I/O ground pin
V_{DD1A18}	12	E4	ADC Analog Power Pin (1.8 V)
$V_{SS1AGND}$	13	E5	ADC Analog Ground Pin
V_{DD2A18}	40	J 6	ADC Analog Power Pin (1.8 V)
$V_{SS2AGND}$	39	K6	ADC Analog Ground Pin
V_{DD}	10	E2	CPU and Logic Digital Power Pins (1.8 V)
V_{DD}	42	G6	
V_{DD}	59	F10	
V_{DD}	68	D7	
V_{DD}	85	B6	
V_{DD}	93	D4	
V_{DDIO}	3	C2	Digital I/O Power Pin (3.3 V)
V_{DDIO}	46	H7	
V_{DDIO}	65	E9	
V_{DDIO}	82	A7	
V_{SS}	2	B1	Digital Ground Pins
V_{SS}	11	E3	
V_{SS}	41	H6	
V_{SS}	49	K9	
V_{SS}	55	H10	
V_{SS}	62	F7	
V_{SS}	69	D10	
V_{SS}	77	A9	
V_{SS}	87	D6	
V_{SS}	89	A5	
V_{SS}	94	A4	
GPIO AND PERIPHERAL PINS§			
GPIO0 EPWM1A (O) – –	47	K8	General Purpose Input/Output 0 Enhanced PWM1 output A (O)
GPIO1 EPWM1B (O) SPISIMOD (I/O) –	44	K7	General Purpose Input/Output 1 Enhanced PWM1 output B (O) SPI-D slave in, master out (I/O) (not available on F2801)
GPIO2 EPWM2A (O) – –	45	J7	General Purpose Input/Output 2 Enhanced PWM2 output A (O)

Legend: I/O/Z/OD: Input/Output/High Impedance/Open Drain
↑ Pullup
↓ Pulldown

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‡ For pins with multiple functions, the function shown in Italicized bold face is the function upon reset.

§ In this section, all pins are I/O/Z, 4-mA drive typical (unless otherwise indicated), and have an internal pullup. The GPIO function is the default at reset. The peripheral signals that are listed under them are alternate functions.

PRODUCT PREVIEW

PRODUCT PREVIEW

Table 2−2. Signal Descriptions (continued)

NAME	PZ PIN #	GGM BALL #	DESCRIPTION
GPIO3 EPWM2B (O) SPISOMID (I/O) –	48	J8	General Purpose Input/Output 3 Enhanced PWM2 output B (O) SPI-D slave out, master in (I/O) (not available on F2801)
GPIO4 EPWM3A (O) – –	51	J9	General Purpose Input/Output 4 Enhanced PWM3 output A (O)
GPIO5 EPWM3B (O) SPICLKD (I/O) ECAP1 (I/O)	53	H9	General Purpose Input/Output 5 Enhanced PWM3 output B (O) SPI-D clock (I/O) (not available on F2801) Enhanced capture input/output 1 (I/O)
GPIO6 EPWM4A (O) EPWMSYNCI (I) EPWMSYNCO (O)	56	G9	General Purpose Input/Output 6 Enhanced PWM4 output A(O) (not available on F2801) External ePWM synch pulse input (I) External ePWM synch pulse output (O)
GPIO7 EPWM4B (O) SPISTED (I/O) ECAP2 (I/O)	58	G8	General Purpose Input/Output 7 Enhanced PWM4 output B (O) (not available on F2801) SPI-D slave transmit enable (I/O) (not available on F2801) Enhanced capture input/output 2 (I/O)
GPIO8 EPWM5A (O) $\overline{\text{CANTXB}}$ (O) $\overline{\text{ADCSOCAO}}$ (O)	60	F9	General Purpose Input/Output 8 Enhanced PWM5 output A (O) (not available on F2801) ECAN-B transmit (O) (not available on F2806 or F2801) ADC start-of-conversion A (O)
GPIO9 EPWM5B SCITXB ECAP3	61	F8	General-Purpose Input/Output 9 Enhanced PWM5 output B (O) (not available on F2801) SCI-B transmit data (O) Enhanced capture input/output 3 (I/O) (not available on F2801)
GPIO10 EPWM6A $\overline{\text{CANRXB}}$ $\overline{\text{ADCSOCBO}}$	64	E10	General-Purpose Input/Output 10 Enhanced PWM6 output A (O) (not available on F2801) CAN-B receive data (I) (not available on F2806 or F2801) ADC start of conversion B (O)
GPIO11 EPWM6B SCIRXB ECAP4	70	D9	General-Purpose Input/Output 11 Enhanced PWM6 output B (O) (not available on F2801) SCI-B receive data (I) (not available on F2801) Enhanced CAP input/output 4 (I/O) (not available on F2801)
GPIO12 $\overline{\text{TZ1}}$ CANTXB SPISIMOB	1	B2	General-Purpose Input/Output 12 Trip zone input 1 (I) CAN-B transmit (O) (not available on F2806 or F2801) SPI-B slave in, master out (I/O)

Legend: I/O/Z/OD: Input/Output/High Impedance/Open Drain
↑ Pullup
↓ Pulldown

† The pullups on the GPIO pins are disabled upon reset; they can be selectively enabled on a per-pin basis. This feature only applies to the GPIO pins.

‡ For pins with multiple functions, the function shown in Italicized bold face is the function upon reset.

§ In this section, all pins are I/O/Z, 4-mA drive typical (unless otherwise indicated), and have an internal pullup. The GPIO function is the default at reset. The peripheral signals that are listed under them are alternate functions.

Table 2−2. Signal Descriptions (continued)

NAME	PZ PIN #	GGM BALL #	DESCRIPTION
GPIO13 $\overline{\text{TZ2}}$ CANRXB SPISOMIB	95	B4	General-Purpose Input/Output 13 Trip zone input 2 (I) CAN-B receive (I) (not available on F2806 or F2801) SPI-B slave out, master in (I/O)
GPIO14 $\overline{\text{TZ3}}$ SCITXB SPICLKB	8	D3	General-Purpose Input/Output 14 Trip zone input 3 (I) SCI-B transmit (O) (not available on F2801) SPI-B clock input/output (I/O)
GPIO15 $\overline{\text{TZ4}}$ SCIRXB SPISTEB	9	E1	General-Purpose Input/Output 15 Trip zone input (I) SCI-B receive (I) (not available on F2801) SPI-B slave transmit enable (I/O)
GPIO16 SPISIMOA CANTXB $\overline{\text{TZ5}}$	50	K10	General-Purpose Input/Output 16 SPI-A slave in, master out (I/O) CAN-B transmit (O) Trip zone input 5 (I)
GPIO17 SPISOMIA CANRXB $\overline{\text{TZ6}}$	52	J10	General-Purpose Input/Output 17 SPI-A slave out, master in (I/O) CAN-B receive (I) (not available on F2801) Trip zone input 6 (I)
GPIO18 SPICLKA SCITXB –	54	H8	General-Purpose Input/Output 18 SPI-A clock input/output (I/O) SCI-B transmit (O)
GPIO19 SPISTEA SCIRXB –	57	G10	General-Purpose Input/Output 19 SPI-A slave transmit enable input/output (I/O) SCI-B receive (I) (not available on F2801)
GPIO20 EQEP1A SPISIMOC CANTXB	63	F6	General-Purpose Input/Output 20 Enhanced QEP1 input A (I) SPI-C slave in, master out (I/O) (not available on F2801) CAN-B transmit (O) (not available on F2801 or F2806)
GPIO21 EQEP1B SPISOMIC CANRXB	67	E7	General-Purpose Input/Output 21 Enhanced QEP1 input B (I) SPI-C master in, slave out (I/O) (not available on F2801) CAN-B receive (I) (not available on F2801 or F2806)
GPIO22 EQEP1S SPICLKC SCITXB	71	D8	General-Purpose Input/Output 22 Enhanced QEP1 strobe (I/O) SPI-C clock (I/O) (not available on F2801) SCI-B transmit (O)

Legend: I/O/Z/OD: Input/Output/High Impedance/Open Drain
↑ Pullup
↓ Pulldown

† The pullups on the GPIO pins are disabled upon reset; they can be selectively enabled on a per-pin basis. This feature only applies to the GPIO pins.

‡ For pins with multiple functions, the function shown in Italicized bold face is the function upon reset.

§ In this section, all pins are I/O/Z, 4-mA drive typical (unless otherwise indicated), and have an internal pullup. The GPIO function is the default at reset. The peripheral signals that are listed under them are alternate functions.

PRODUCT PREVIEW

PRODUCT PREVIEW

Table 2−2. Signal Descriptions (continued)

NAME	PZ PIN #	GGM BALL #	DESCRIPTION
GPIO23 EQEP1I SPISTEC SCIRXB	72	C10	General-Purpose Input/Output 23 Enhanced QEP1 Index (I/O) SPI-C slave transmit enable (I/O) (not available on F2801) SCI-B receive (I) (not available on F2801)
GPIO24 ECAP1 EQEP2A SPISIMOB	83	C7	General-Purpose Input/Output 24 Enhanced capture 1 (I/O) Enhanced QEP2-input A (I) (not available on F2801) SPI-B slave in, master out (I/O)
GPIO25 ECAP2 EQEP2B SPISOMIB	91	C5	General-Purpose Input/Output 25 Enhanced capture 2 (I/O) Enhanced QEP2 input-B (I) (not available on F2801) SPI-B master in, slave out (I/O)
GPIO26 ECAP3 EQEP2I SPICLKB	99	A2	General-Purpose Input/Output 26 Enhanced capture 3 (I/O) (not available on F2801) Enhanced QEP 2 index (I/O) (not available on F2801) SPI-B clock (I/O)
GPIO27 ECAP4 EQEP2S SPISTEB	79	C8	General-Purpose Input/Output 27 Enhanced CAP 4 (I/O) (not available on F2801) Enhanced QEP2 strobe (I/O) (not available on F2801) SPI-B slave transmit enable (I/O)
GPIO28 SCIRXDA – $\overline{\text{TZ5}}$	92	D5	General-Purpose Input/Output 28. This pin has an 8-mA (typical) output buffer. SCI receive data (I) Trip zone 5 (I)
GPIO29 SCITXDA – $\overline{\text{TZ6}}$	4	C3	General-Purpose Input/Output 29. This pin has an 8-mA (typical) output buffer. SCI transmit data (O) Trip zone 6 (I)
GPIO30 CANRXA – –	6	D2	General-Purpose Input/Output 30. This pin has an 8-mA (typical) output buffer. CAN-A receive data (I)
GPIO31 CANTXA – –	7	D1	General-Purpose Input/Output 31. This pin has an 8-mA (typical) output buffer. CAN-A transmit data (O)
GPIO32 SDAA $\overline{\text{EPWMSYNCI}}$ $\overline{\text{ADCSOCAO}}$	100	A1	General-Purpose Input/Output 32 I^2C data open-drain bidirectional port (I/OD) Enhanced PWM external synch pulse input (I) ADC start-of-conversion (O)

Legend: I/O/Z/OD: Input/Output/High Impedance/Open Drain
↑ Pullup
↓ Pulldown

† The pullups on the GPIO pins are disabled upon reset; they can be selectively enabled on a per-pin basis. This feature only applies to the GPIO pins.

‡ For pins with multiple functions, the function shown in Italicized bold face is the function upon reset.

§ In this section, all pins are I/O/Z, 4-mA drive typical (unless otherwise indicated), and have an internal pullup. The GPIO function is the default at reset. The peripheral signals that are listed under them are alternate functions.

Table 2−2. Signal Descriptions (continued)

NAME	PZ PIN #	GGM BALL #	DESCRIPTION
GPIO33 SCLA (I/OC) EPWMSYNCO ADCSOCBO	5	C1	General-Purpose Input/Output 33 I^2C clock open-drain bidirectional port (I/OD) Enhanced PWM external synch pulse output (O) ADC start-of-conversion (O)
GPIO34 – – –	43	G7	General-Purpose Input/Output 34

Legend: I/O/Z/OD: Input/Output/High Impedance/Open Drain
↑ Pullup
↓ Pulldown

† The pullups on the GPIO pins are disabled upon reset; they can be selectively enabled on a per-pin basis. This feature only applies to the GPIO pins.

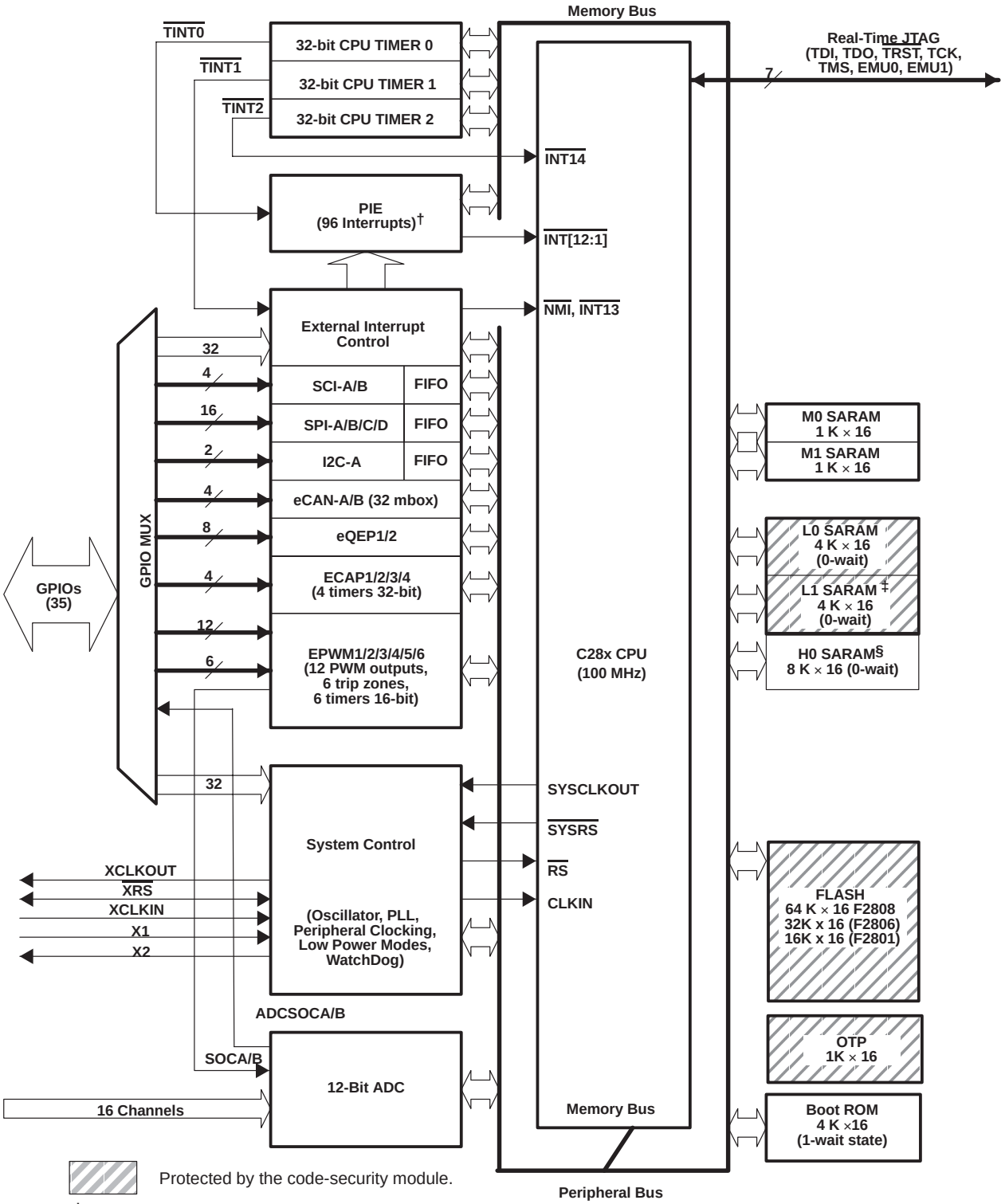
‡ For pins with multiple functions, the function shown in Italicized bold face is the function upon reset.

§ In this section, all pins are I/O/Z, 4-mA drive typical (unless otherwise indicated), and have an internal pullup. The GPIO function is the default at reset. The peripheral signals that are listed under them are alternate functions.

PRODUCT PREVIEW

PRODUCT PREVIEW

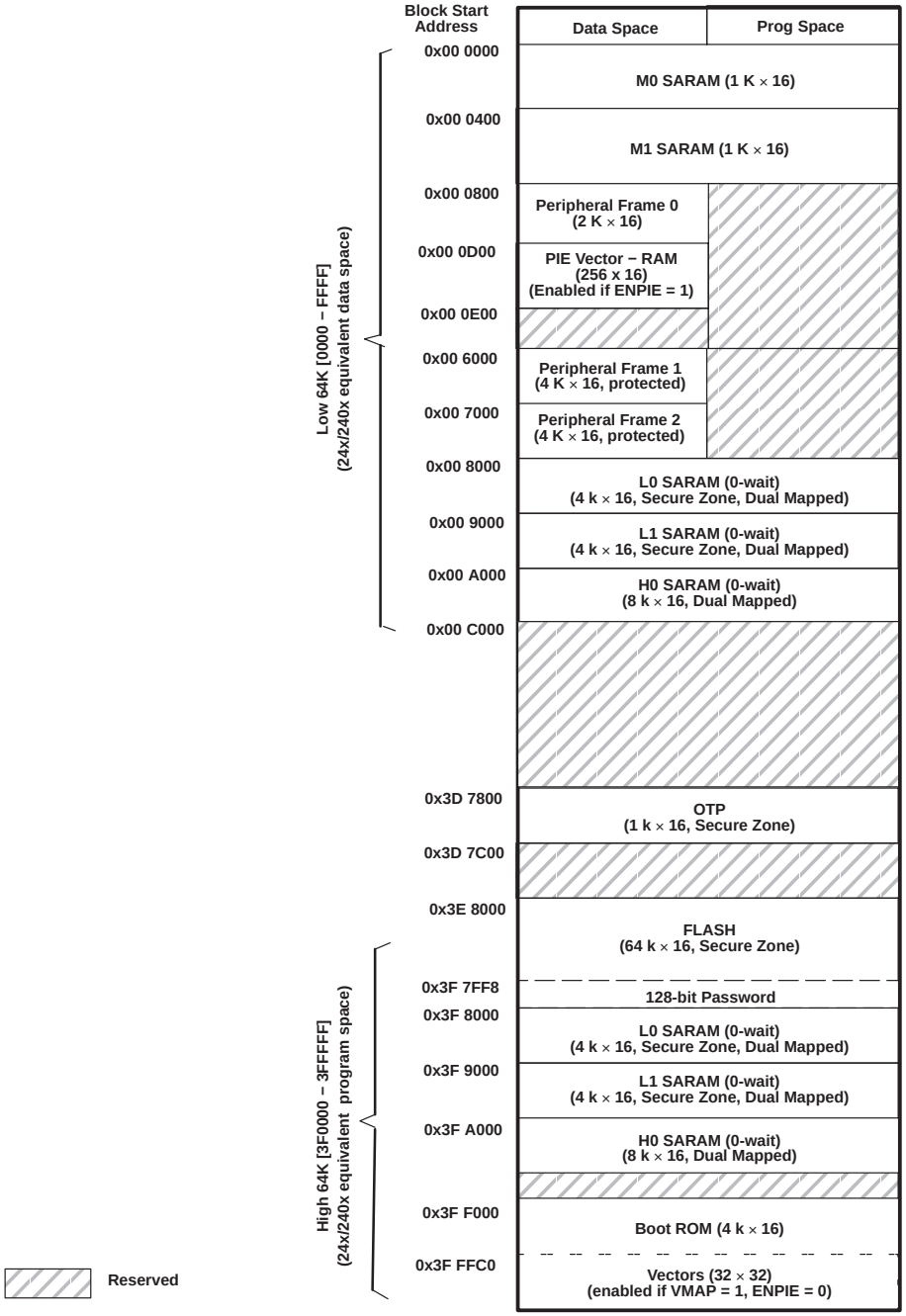
3 Functional Overview



† 43 of the possible 96 interrupts are used on the devices.
‡ Not available in 2801
§ Not available in 2806 or 2801

Figure 3−1. Functional Block Diagram

3.1 Memory Maps

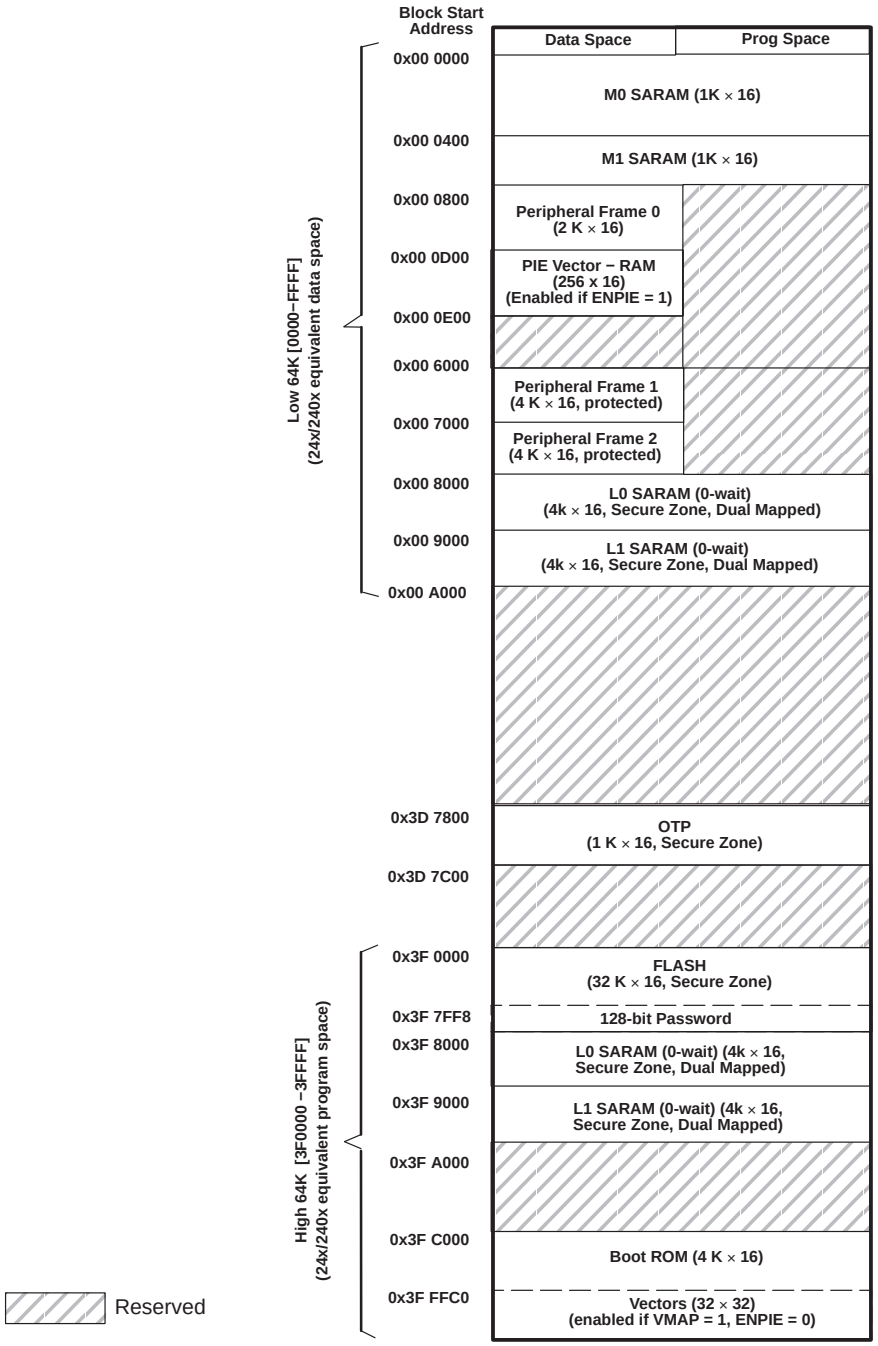


NOTES: A. Memory blocks are not to scale.
B. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.
C. “Protected” means the order of Write followed by Read operations is preserved rather than the pipeline order.
D. Certain memory ranges are EALLOW protected against spurious writes after configuration.

Figure 3−2. 2808 Memory Map

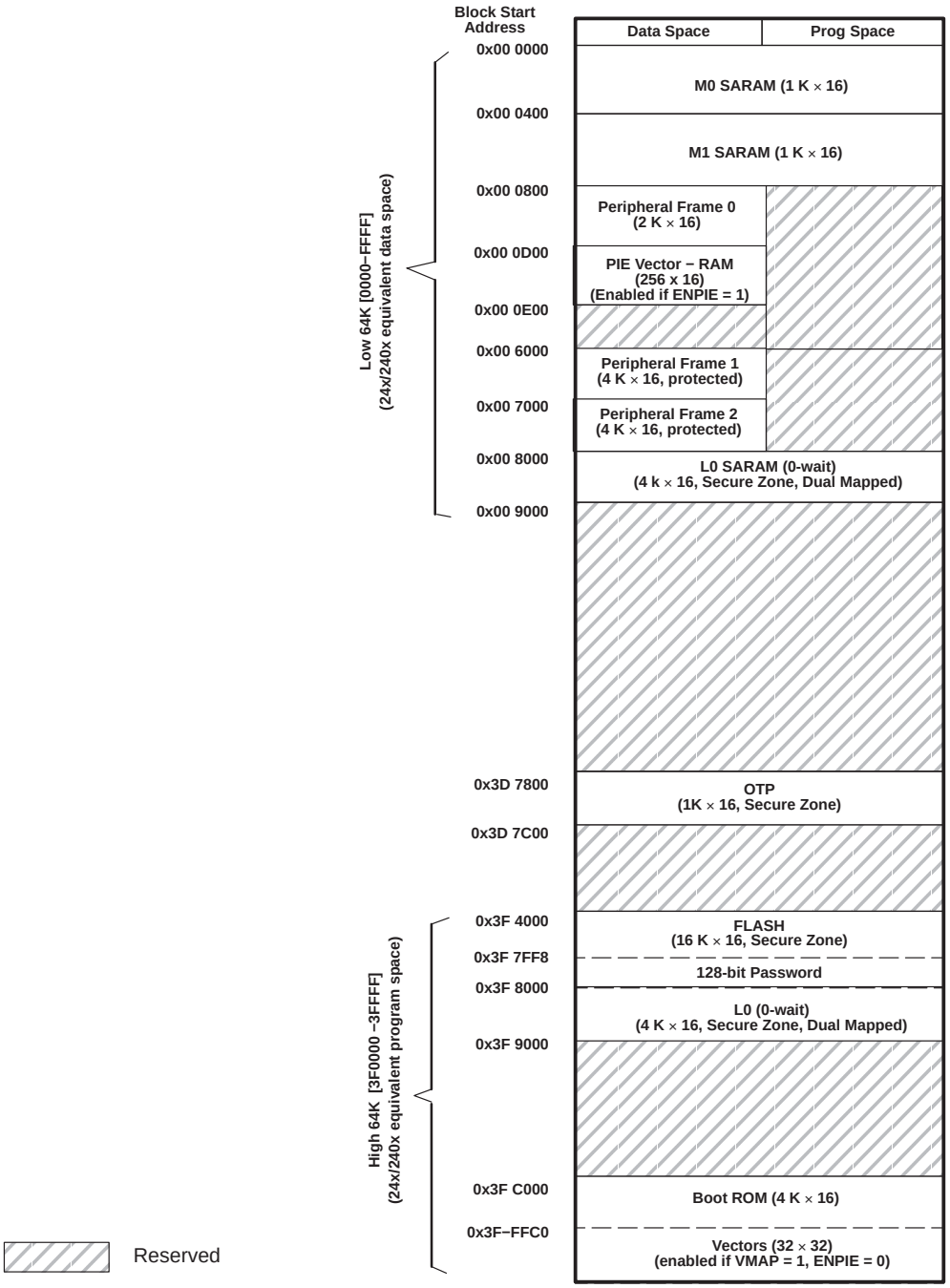
PRODUCT PREVIEW

PRODUCT PREVIEW



NOTES: A. Memory blocks are not to scale.
B. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.
C. “Protected” means the order of Write followed by Read operations is preserved rather than the pipeline order.
D. Certain memory ranges are EALLOW protected against spurious writes after configuration.

Figure 3−3. 2806 Memory Map



NOTES: A. Memory blocks are not to scale.
B. Peripheral Frame 0, Peripheral Frame 1, and Peripheral Frame 2 memory maps are restricted to data memory only. User program cannot access these memory maps in program space.
C. “Protected” means the order of Write followed by Read operations is preserved rather than the pipeline order.
D. Certain memory ranges are EALLOW protected against spurious writes after configuration.

Figure 3−4. 2801 Memory Map

PRODUCT PREVIEW

PRODUCT PREVIEW

Table 3−1. Addresses of Flash Sectors in F2808

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3E 8000 0x3E BFFF	Sector D (16K x 16)
0x3E C000 0x3E FFFF	Sector C (16K x 16)
0x3F 0000 0x3F 3FFF	Sector B (16K x 16)
0x3F 4000 0x3F 7F7F	Sector A (16K x 16)
0x3F 7F80 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

Table 3−2. Addresses of Flash Sectors in F2806

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3F 0000 0x3F 1FFF	Sector D (8K x 16)
0x3F 2000 0x3F 3FFF	Sector C (8K x 16)
0x3F 4000 0x3F 5FFF	Sector B (8K x 16)
0x3F 6000 0x3F 7F7F	Sector A (8K x 16)
0x3F 7F80 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

Table 3−3. Addresses of Flash Sectors in F2801

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3F 4000 0x3F 4FFF	Sector D (4K x 16)
0x3F 5000 0x3F 5FFF	Sector C (4K x 16)
0x3F 6000 0x3F 6FFF	Sector B (4K x 16)
0x3F 7000 0x3F 7F7F	Sector A (4K x 16)
0x3F 7F80 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

Peripheral Frame 1 and Peripheral Frame 2 are grouped together so as to enable these blocks to be “write/read peripheral block protected”. The protected mode ensures that all accesses to these blocks happen as written. Because of the C28x pipeline, a write immediately followed by a read, to different memory locations, will appear in reverse order on the memory bus of the CPU. This can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The C28x CPU supports a block protection mode where a region of memory can be protected so as to make sure that operations occur as written (the penalty is extra cycles are added to align the operations). This mode is programmable and by default, it will protect the selected zones.

The wait states for the various spaces in the memory map area are listed in Table 3−4.

Table 3−4. Wait States

AREA	WAIT-STATES	COMMENTS
M0 and M1 SARAMs	0-wait	Fixed
Peripheral Frame 0	0-wait	Fixed
Peripheral Frame 1	0-wait (writes) 2-wait (reads)	Fixed
Peripheral Frame 2	0-wait (writes) 2-wait (reads)	Fixed
L0 and L1 SARAMs	0-wait	
OTP	Programmable, 1-wait minimum	Programmed via the Flash registers. 1-wait-state operation is possible at a reduced CPU frequency. See Section 3.2.5 for more information.
Flash	Programmable, 0-wait minimum	Programmed via the Flash registers. 0-wait-state operation is possible at reduced CPU frequency. The CSM password locations are hardwired for 16 wait-states. See Section 3.2.5 for more information.
H0 SARAM	0-wait	Fixed
Boot-ROM	1-wait	Fixed

3.2 Brief Descriptions

3.2.1 C28x CPU

The C28x™ DSP generation is the newest member of the TMS320C2000™ DSP platform. The C28x is a very efficient C/C++ engine, enabling users to develop not only their system control software in a high-level language, but also enables math algorithms to be developed using C/C++. The C28x is as efficient in DSP math tasks as it is in system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC capabilities of the C28x and its 64-bit processing capabilities, enable the C28x to efficiently handle higher numerical resolution problems that would otherwise demand a more expensive floating-point processor solution. Add to this the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The C28x has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables the C28x to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

3.2.2 Memory Bus (Harvard Bus Architecture)

As with many DSP type devices, multiple busses are used to move data between the memories and peripherals and the CPU. The C28x memory bus architecture contains a program read bus, data read bus and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write busses consist of 32 address lines and 32 data lines each. The 32-bit-wide data busses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed “Harvard Bus”, enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories

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PRODUCT PREVIEW

attached to the memory bus will prioritize memory accesses. Generally, the priority of Memory Bus accesses can be summarized as follows:

Highest:	Data Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Program Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Data Reads	
	Program Reads	(Simultaneous program reads and fetches cannot occur on the memory bus.)
Lowest:	Fetches	(Simultaneous program reads and fetches cannot occur on the memory bus.)

3.2.3 Peripheral Bus

To enable migration of peripherals between various Texas Instruments (TI) DSP family of devices, the 280x adopt a peripheral bus standard for peripheral interconnect. The peripheral bus bridge multiplexes the various busses that make up the processor “Memory Bus” into a single bus consisting of 16 address lines and 16 or 32 data lines and associated control signals. Two versions of the peripheral bus are supported on the 280x. One version only supports 16-bit accesses (called peripheral frame 2). The other version supports both 16- and 32-bit accesses (called peripheral frame 1).

3.2.4 Real-Time JTAG and Analysis

The 280x implements the standard IEEE 1149.1 JTAG interface. Additionally, the 280x supports real-time mode of operation whereby the contents of memory, peripheral and register locations can be modified while the processor is running and executing code and servicing interrupts. The user can also single step through non-time critical code while enabling time-critical interrupts to be serviced without interference. The 280x implements the real-time mode in hardware within the CPU. This is a unique feature to the 280x, no software monitor is required. Additionally, special analysis hardware is provided which allows the user to set hardware breakpoint or data/address watch-points and generate various user-selectable break events when a match occurs.

3.2.5 Flash

The F2808 contains 64K x 16 of embedded flash memory, segregated into four 16K X 16 sectors. The F2806 has 32K X 16 of embedded flash, segregated into four 8K X 16 sectors. The F2801 contains 16K X 16 of embedded Flash (four 4K X 16 sectors). All three devices also contain a single 1K x 16 of OTP memory at address range 0x3D 7800 − 0x3D 7BFF. The user can individually erase, program, and validate a flash sector while leaving other sectors untouched. However, it is not possible to use one sector of the flash or the OTP to execute flash algorithms that erase/program other sectors. Special memory pipelining is provided to enable the flash module to achieve higher performance. The flash/OTP is mapped to both program and data space; therefore, it can be used to execute code or store data information.

NOTE:

The F2808/F2806/F2801 Flash and OTP wait states can be configured by the application. This allows applications running at slower frequencies to configure the flash to use fewer wait states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent. The pipeline mode is not available for the OTP block.

For more information on the Flash options, Flash wait-state, and OTP wait-state registers, see the *TMS320x280x System Control and Interrupts Reference Guide* (literature number SPRU712).

PRODUCT PREVIEW

3.2.6 M0, M1 SARAMs

All 280x devices contain these two blocks of single access memory, each 1K x 16 in size. The stack pointer points to the beginning of block M1 on reset. The M0 and M1 blocks, like all other memory blocks on C28x devices, are mapped to both program and data space. Hence, the user can use M0 and M1 to execute code or for data variables. The partitioning is performed within the linker. The C28x device presents a unified memory map to the programmer. This makes for easier programming in high-level languages.

3.2.7 L0, L1, H0 SARAMs

The F2808 contains an additional 16K x 16 of single-access RAM, divided into 3 blocks (L0−4K, L1−4K, H0−8K). The F2806 contains an additional 8K x 16 of single-access RAM, divided into 2 blocks (L0−4K, L1−4K). The F2801 contains an additional 4K x 16 of single-access RAM (L0−4K). Each block can be independently accessed to minimize CPU pipeline stalls. Each block is mapped to both program and data space.

3.2.8 Boot ROM

The Boot ROM is factory-programmed with boot-loading software. Boot-mode signals are provided to tell the bootloader software what boot mode to use on power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash. Table 3−5 shows the boot mode selection data. The Boot ROM will also contain standard tables, such as SIN/COS waveforms, for use in math related algorithms.

Table 3−5. Boot Mode Selection

MODE	DESCRIPTION	GPIO18 SPICLKA SCITXB	GPIO29 SCITXA	GPIO34
Boot to Flash	Jump to Flash address 0x3F 7FF6 You must have programmed a branch instruction here prior to reset to redirect code execution as desired.	1	1	1
SCI−A Boot	Load a data stream from SCI−A.	1	1	0
SPI−A Boot	Load from an external serial SPI EEPROM on SPI−A.	1	0	1
I2C Boot	Load data from an external EEPROM at address 0x50 on the I2C bus.	1	0	0
eCAN−A Boot	Call CAN_Boot to load from eCAN−A mailbox 1.	0	1	1
Boot to M0 SARAM	Jump to M0 SARAM address 0x00 0000.	0	1	0
Boot to OTP	Jump to OTP address 0x3D 7800.	0	0	1
Parallel I/O Boot	Load data from GPIO0 - GPIO15.	0	0	0

3.2.9 Security

The 280x support high levels of security to protect the user firmware from being reversed engineered. The security features a 128-bit password (hardcoded for 16 wait states), which the user programs into the flash. One code security module (CSM) is used to protect the flash/OTP and the L0/L1 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents via the JTAG port, executing code from external memory or trying to boot-load some undesirable software that would export the secure memory contents. To enable access to the secure blocks, the user must write the correct 128-bit ”KEY” value, which matches the value stored in the password locations within the Flash.

PRODUCT PREVIEW

NOTE:

For code security operation, all addresses between 0x3F7F80 and 0x3F7FF5 cannot be used as program code or data, but must be programmed to 0x0000 when the Code Security Passwords are programmed. If security is not a concern, then these addresses may be used for code or data.

The 128-bit password (at 0x3F 7FF8 − 0x3F 7FFF) must *not* be programmed to zeros. Doing so would permanently lock the device.

Code Security Module Disclaimer

The Code Security Module (“CSM”) included on this device was designed to password protect the data stored in the associated memory and is warranted by Texas Instruments (TI), in accordance with its standard terms and conditions, to conform to TI’s published specifications for the warranty period applicable for this device.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

PRODUCT PREVIEW

3.2.10 Peripheral Interrupt Expansion (PIE) Block

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the 280x, 43 of the possible 96 interrupts are used by peripherals. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12 CPU interrupt lines ($\overline{\text{INT1}}$ to $\overline{\text{INT12}}$). Each of the 96 interrupts is, supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is, automatically fetched by the CPU on servicing the interrupt. It takes 8 CPU clock cycles to fetch the vector and save critical CPU registers. Hence the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the PIE block.

3.2.11 External Interrupts ($\overline{\text{XINT1}}$, $\overline{\text{XINT2}}$, $\overline{\text{XINT13}}$, $\overline{\text{XNMI}}$)

The 280x supports three masked external interrupts ($\overline{\text{XINT1}}$, $\overline{\text{XINT2}}$, $\overline{\text{XINT13}}$). $\overline{\text{XINT13}}$ is combined with one non-masked external interrupt ($\overline{\text{XNMI}}$). The combined signal name is XNMI_XINT13. Each of the interrupts can be selected for negative or positive edge triggering and can also be enabled/disabled (including the $\overline{\text{XNMI}}$). The masked interrupts also contain a 16-bit free running up counter, which is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time stamp the interrupt. Unlike the 281x devices, there are no dedicated pins for the external interrupts. Rather, any Port A GPIO pin can be configured to trigger any external interrupt.

3.2.12 Oscillator and PLL

The 280x can be clocked by an external oscillator or by a crystal attached to the on-chip oscillator circuit. A PLL is provided supporting up to 10-input clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired. See the Electrical Specification section for timing details. The PLL block can be set in bypass mode.

3.2.13 Watchdog

The 280x devices contain a watchdog timer. The user software must regularly reset the watchdog counter within a certain time frame; otherwise, the watchdog will generate a reset to the processor. The watchdog can be disabled if necessary.

3.2.14 Peripheral Clocking

The clocks to each individual peripheral can be enabled/disabled so as to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except eCAN) and the ADC blocks can be scaled relative to the CPU clock. This enables the timing of peripherals to be decoupled from increasing CPU clock speeds.

3.2.15 Low-Power Modes

The 280x devices are full static CMOS devices. Three low-power modes are provided:

IDLE:	Place CPU into low-power mode. Peripheral clocks may be turned off selectively and only those peripherals that need to function during IDLE are left operating. An enabled interrupt from an active peripheral or the watchdog timer will wake the processor from IDLE mode.
STANDBY:	Turn off clock to CPU and peripherals. This mode leaves the oscillator and PLL functional. An external interrupt event or the watchdog timer will wake the processor and the peripherals. Execution begins on the next valid cycle after detection of the interrupt event.
HALT:	Turn off oscillator. This mode basically shuts down the device and places it in the lowest possible power consumption mode. A reset or external signal can wake the device from this mode.

3.2.16 Peripheral Frames 0, 1, 2 (PFn)

The 280x segregate peripherals into three sections. The mapping of peripherals is as follows:

PF0:	PIE:	PIE Interrupt Enable and Control Registers Plus PIE Vector Table
	Flash:	Flash Control, Programming, Erase, Verify Registers
	Timers:	CPU-Timers 0, 1, 2 Registers
	CSM:	Code Security Module KEY Registers
	ADC:	12-bit ADC Result Registers
PF1:	eCAN:	eCAN Mailbox and Control Registers
	GPIO:	GPIO Mux Configuration and Control Registers
	ePWM:	Enhanced Pulse Width Modulator Module and Registers
	eCAP:	Enhanced Capture Module and Registers
	eQEP:	Enhanced Quadrature Encoder Pulse Module and Registers
PF2:	SYS:	System Control Registers
	SCI:	Serial Communications Interface (SCI) Control and RX/TX Registers
	SPI:	Serial Port Interface (SPI) Control and RX/TX Registers
	ADC:	ADC Status, Control, and Result Registers
	I^2C:	Inter-Integrated Circuit Module and Registers

3.2.17 General-Purpose Input/Output (GPIO) Multiplexer

Most of the peripheral signals are multiplexed with general-purpose I/O (GPIO) signals. This enables the user to use a pin as GPIO if the peripheral signal or function is not used. On reset, GPIO pins are configured as inputs. The user can then individually program each pin for GPIO mode or Peripheral Signal mode. For specific inputs, the user can also select the number of input qualification cycles. This is to filter unwanted noise glitches. The GPIO signals can also be used to bring the device out of specific low−power modes.

PRODUCT PREVIEW

3.2.18 32-Bit CPU-Timers (0, 1, 2)

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value. CPU-Timer 2 is reserved for Real-Time OS (RTOS)/BIOS applications. CPU-Timer 1 is also reserved for TI system functions. CPU-Timer 2 is connected to INT14 of the CPU. CPU-Timer 1 can be connected to INT13 of the CPU. CPU-Timer 0 is for general use and is connected to the PIE block.

3.2.19 Control Peripherals

The 280x supports the following peripherals for embedded control applications:

ePWM: The enhanced PWM peripheral supports independent/complementary PWM generation, adjustable dead-band generation for leading/trailing edges, latched/cycle-by-cycle trip mechanism.

eCAP: The enhanced capture peripheral uses a 32-bit time base and registers up to four programmable events in continuous/one-shot capture modes.

This peripheral can also be configured to generate an auxiliary PWM signal.

eQEP: The enhanced QEP peripheral uses a 32-bit position counter, supports low-speed measurement using capture unit and high-speed measurement using a 32-bit unit timer.

This peripheral has a watchdog timer to detect motor stall and input error detection logic to identify simultaneous edge transition in QEP signals.

ADC: The ADC block is a 12-bit converter, single ended, 16-channels. It contains two sample-and-hold units for simultaneous sampling.

3.2.20 Serial Port Peripherals

The 280x support the following serial communication peripherals:

eCAN: This is the enhanced version of the CAN peripheral. It supports 32 mailboxes, time stamping of messages, and is CAN 2.0B-compliant.

SPI: The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. On the 280x, the SPI contains a 16-level receive and transmit FIFO for reducing interrupt servicing overhead.

SCI: The serial communications interface is a two-wire asynchronous serial port, commonly known as UART. On the 280x, the SCI contains a 16-level receive and transmit FIFO for reducing interrupt servicing overhead.

I^2C The inter-integrated circuit (I^2C) module provides an interface between a DSP and other devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus) specification version 2.1 and connected by way of an I^2C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the DSP through the I^2C module. On the 280x, the I^2C contains a 16-level receive and transmit FIFO for reducing interrupt servicing overhead.

PRODUCT PREVIEW

3.3 Register Map

The 280x devices contain three peripheral register spaces. The spaces are categorized as follows:

Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See Table 3−6.

Peripheral Frame 1: These are peripherals that are mapped to the 32-bit peripheral bus. See Table 3−7.

Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See Table 3−8.

Table 3−6. Peripheral Frame 0 Registers†‡

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE§
Device Emulation Registers	0x0880 0x09FF	384	EALLOW protected
FLASH Registers¶	0x0A80 0x0ADF	96	EALLOW protected CSM Protected
Code Security Module Registers	0x0AE0 0x0AEF	16	EALLOW protected
CPU-TIMER0/1/2 Registers	0x0C00 0x0C3F	64	Not EALLOW protected
PIE Registers	0x0CE0 0x0CFF	32	Not EALLOW protected
PIE Vector Table	0x0D00 0x0DFF	256	EALLOW protected

† Registers in Frame 0 support 16-bit and 32-bit accesses.
‡ Missing segments of memory space are reserved and should not be used in applications.
§ If registers are EALLOW protected, then writes cannot be performed until the user executes the EALLOW instruction. The EDIS instruction disables writes. This prevents stray code or pointers from corrupting register contents.
¶ The Flash Registers are also protected by the Code Security Module (CSM).

Table 3−7. Peripheral Frame 1 Registers†‡

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE
eCANA Registers	0x6000 0x60FF	256 (128 x 32)	Some eCAN control registers (and selected bits in other eCAN control registers) are EALLOW-protected.
eCANA Mailbox RAM	0x6100 0x61FF	256 (128 x 32)	Not EALLOW-protected
eCANB Registers	0x6200 0x62FF	256 (128 x 32)	Some eCAN control registers (and selected bits in other eCAN control registers) are EALLOW-protected.
eCANB Mailbox RAM	0x6300 0x63FF	256 (128 x 32)	Not EALLOW-protected
ePWM1 Registers	0x6800 0x683F	64 (32 x 32)	Some ePWM registers are EALLOW protected. See Table 4−2.
ePWM2 Registers	0x6840 0x687F	64 (32 x 32)	Some ePWM registers are EALLOW protected. See Table 4−2.
ePWM3 Registers	0x6880 0x68BF	64 (32 x 32)	Some ePWM registers are EALLOW protected. See Table 4−2.
ePWM4 Registers	0x68C0 0x68FF	64 (32 x 32)	Some ePWM registers are EALLOW protected. See Table 4−2.
ePWM5 Registers	0x6900 0x693F	64 (32 x 32)	Some ePWM registers are EALLOW protected. See Table 4−2.
ePWM6 Registers	0x6940 0x697F	64 (32 x 32)	Some ePWM registers are EALLOW protected. See Table 4−2.
eCAP1 Registers	0x6A00 0x6A1F	32 (16 x 32)	Not EALLOW protected

PRODUCT PREVIEW

Table 3−7. Peripheral Frame 1 Registers†‡ (Continued)

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE
eCAP2 Registers	0x6A20 0x6A3F	32 (16 x 32)	Not EALLOW protected
eCAP3 Registers	0x6A40 0x6A5F	32 (16 x 32)	Not EALLOW protected
eCAP4 Registers	0x6A60 0x6A7F	32 (16 x 32)	Not EALLOW protected
eQEP1 Registers	0x6B00 0x6B3F	64 (32 x 32)	Not EALLOW protected
eQEP2 Registers	0x6B40 0x6B7F	64 (32 x 32)	Not EALLOW protected
GPIO Control Registers	0x6F80 0x6FBF	128 (64 x 32)	EALLOW protected
GPIO Data Registers	0x6FC0 0x6FDF	32 (16 x 32)	Not EALLOW protected
GPIO Interrupt and LPM Select Registers	0x6FE0 0x6FFF	32 (16 x 32)	EALLOW protected

† The eCAN control registers only support 32-bit read/write operations. All 32-bit accesses are aligned to even address boundaries.
‡ Missing segments of memory space are reserved and should not be used in applications.

Table 3−8. Peripheral Frame 2 Registers§ ¶

NAME	ADDRESS RANGE	SIZE (x16)	ACCESS TYPE
System Control Registers	0x7010 0x702F	32	EALLOW Protected
SPI-A Registers	0x7040 0x704F	16	Not EALLOW Protected
SCI-A Registers	0x7050 0x705F	16	Not EALLOW Protected
External Interrupt Registers	0x7070 0x707F	16	Not EALLOW Protected
ADC Registers	0x7100 0x711F	32	Not EALLOW Protected
SPI-B Registers	0x7740 0x774F	16	Not EALLOW Protected
SCI-B Registers	0x7750 0x775F	16	Not EALLOW Protected
SPI-C Registers	0x7760 0x776F	16	Not EALLOW Protected
SPI-D Registers	0x7780 0x778F	16	Not EALLOW Protected
I^2C Registers	0x7900 0x792F	48	Not EALLOW Protected

§ Peripheral Frame 2 only allows 16-bit accesses. All 32-bit accesses are ignored (invalid data may be returned or written).
¶ Missing segments of memory space are reserved and should not be used in applications.

3.4 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 3−9.

PRODUCT PREVIEW

Table 3−9. Device Emulation Registers

NAME	ADDRESS RANGE	SIZE (x16)	DESCRIPTION
DEVICECNF	0x0880 0x0881	2	Device Configuration Register
DEVICEID	0x0883	1	Device ID Register (0x0001 − Silicon − Rev. 0)
PROTSTART	0x0884	1	Block Protection Start Address Register
PROTRANGE	0x0885	1	Block Protection Range Address Register

PRODUCT PREVIEW

3.5 Interrupts

Figure 3−5 shows how the various interrupt sources are multiplexed within the 280x devices.

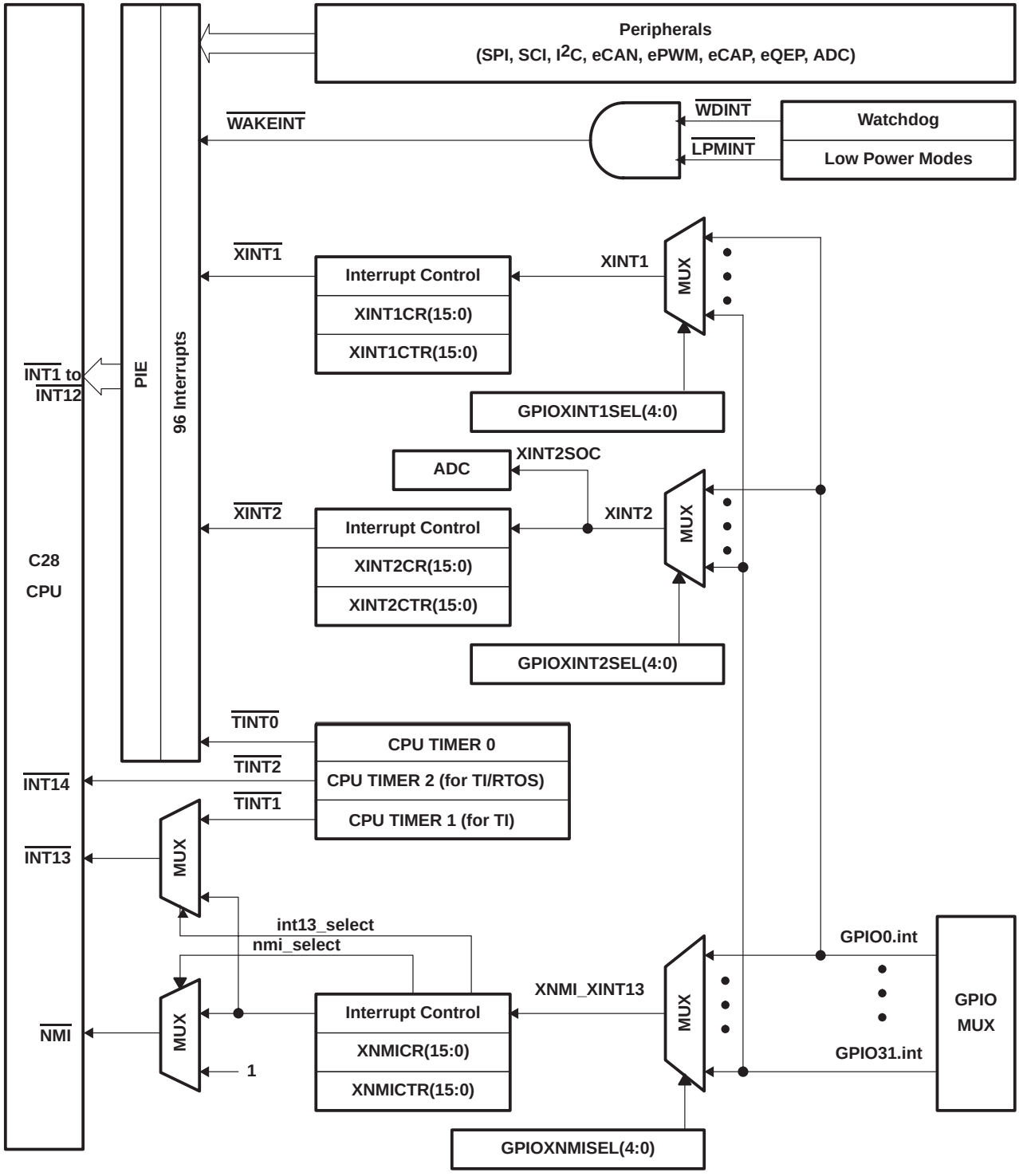


Figure 3−5. External and PIE Interrupt Sources

PRODUCT PREVIEW

Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. On the 280x, 43 of these are used by peripherals as shown in Table 3−10.

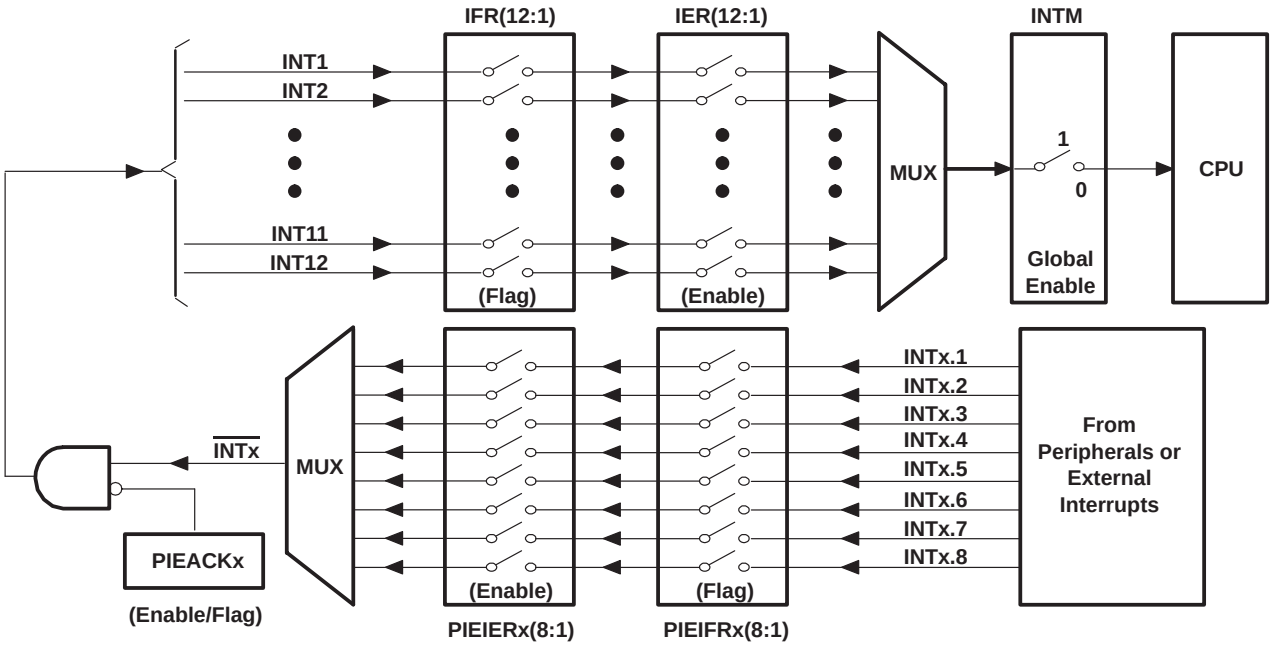


Figure 3−6. Multiplexing of Interrupts Using the PIE Block

Table 3−10. PIE Peripheral Interrupts†

CPU INTER-RUPTS	PIE INTERRUPTS							
	INTX.8	INTX.7	INTX.6	INTX.5	INTX.4	INTX.3	INTX.2	INTX.1
INT1	WAKEINT (LPM/WD)	TINT0 (TIMER 0)	ADCINT (ADC)	XINT2	XINT1	Reserved	SEQ2INT (ADC)	SEQ1INT (ADC)
INT2	Reserved	Reserved	EPWM6_TZINT (ePWM6)	EPWM5_TZINT (ePWM5)	EPWM4_TZINT (ePWM4)	EPWM3_TZINT (ePWM3)	EPWM2_TZINT (ePWM2)	EPWM1_TZINT (ePWM1)
INT3	Reserved	Reserved	EPWM6_INT (ePWM6)	EPWM5_INT (ePWM5)	EPWM4_INT (ePWM4)	EPWM3_INT (ePWM3)	EPWM2_INT (ePWM2)	EPWM1_INT (ePWM1)
INT4	Reserved	Reserved	Reserved	Reserved	ECAP4_INT (eCAP4)	ECAP3_INT (eCAP3)	ECAP2_INT (eCAP2)	ECAP1_INT (eCAP1)
INT5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EQEP2_INT (eQEP2)	EQEP1_INT (eQEP1)
INT6	SPITXINTD (SPI-D)	SPIRXINTD (SPI-D)	SPITXINTC (SPI-C)	SPIRXINTC (SPI-C)	SPITXINTB (SPI-B)	SPIRXINTB (SPI-B)	SPITXINTA (SPI-A)	SPIRXINTA (SPI-A)
INT7	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INT8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	I2CINT2A (I2C-A)	I2CINT1A (I2C-A)
INT9	ECAN1_INTB (CAN-B)	ECAN0_INTB (CAN-B)	ECAN1_INTA (CAN-A)	ECAN0_INTA (CAN-A)	SCITXINTB (SCI-B)	SCIRXINTB (SCI-B)	SCITXINTA (SCI-A)	SCIRXINTA (SCI-A)
INT10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INT11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
INT12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

† Out of the 96 possible interrupts, 43 interrupts are currently used. the remaining interrupts are reserved for future devices. However, these interrupts can be used as software interrupts if they are enabled at the PIEIFRx level.

PRODUCT PREVIEW

PRODUCT PREVIEW

Table 3−11. PIE Configuration and Control Registers

NAME	ADDRESS	Size (x16)	DESCRIPTION
PIECTRL	0x0CE0	1	PIE, Control Register
PIEACK	0x0CE1	1	PIE, Acknowledge Register
PIEIER1	0x0CE2	1	PIE, INT1 Group Enable Register
PIEIFR1	0x0CE3	1	PIE, INT1 Group Flag Register
PIEIER2	0x0CE4	1	PIE, INT2 Group Enable Register
PIEIFR2	0x0CE5	1	PIE, INT2 Group Flag Register
PIEIER3	0x0CE6	1	PIE, INT3 Group Enable Register
PIEIFR3	0x0CE7	1	PIE, INT3 Group Flag Register
PIEIER4	0x0CE8	1	PIE, INT4 Group Enable Register
PIEIFR4	0x0CE9	1	PIE, INT4 Group Flag Register
PIEIER5	0x0CEA	1	PIE, INT5 Group Enable Register
PIEIFR5	0x0CEB	1	PIE, INT5 Group Flag Register
PIEIER6	0x0CEC	1	PIE, INT6 Group Enable Register
PIEIFR6	0x0CED	1	PIE, INT6 Group Flag Register
PIEIER7	0x0CEE	1	PIE, INT7 Group Enable Register
PIEIFR7	0x0CEF	1	PIE, INT7 Group Flag Register
PIEIER8	0x0CF0	1	PIE, INT8 Group Enable Register
PIEIFR8	0x0CF1	1	PIE, INT8 Group Flag Register
PIEIER9	0x0CF2	1	PIE, INT9 Group Enable Register
PIEIFR9	0x0CF3	1	PIE, INT9 Group Flag Register
PIEIER10	0x0CF4	1	PIE, INT10 Group Enable Register
PIEIFR10	0x0CF5	1	PIE, INT10 Group Flag Register
PIEIER11	0x0CF6	1	PIE, INT11 Group Enable Register
PIEIFR11	0x0CF7	1	PIE, INT11 Group Flag Register
PIEIER12	0x0CF8	1	PIE, INT12 Group Enable Register
PIEIFR12	0x0CF9	1	PIE, INT12 Group Flag Register
Reserved	0x0CFA 0x0CFF	6	Reserved

Note: The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

3.5.1 External Interrupts

Table 3−12. External Interrupt Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XINT1CR	0x7070	1	XINT1 control register
XINT2CR	0x7071	1	XINT2 control register
reserved	0x7072 0x7076	5	
XNMICR	0x7077	1	XNMI control register
XINT1CTR	0x7078	1	XINT1 counter register
XINT2CTR	0x7079	1	XINT2 counter register
reserved	0x707A 0x707E	5	
XNMICTR	0x707F	1	XNMI counter register

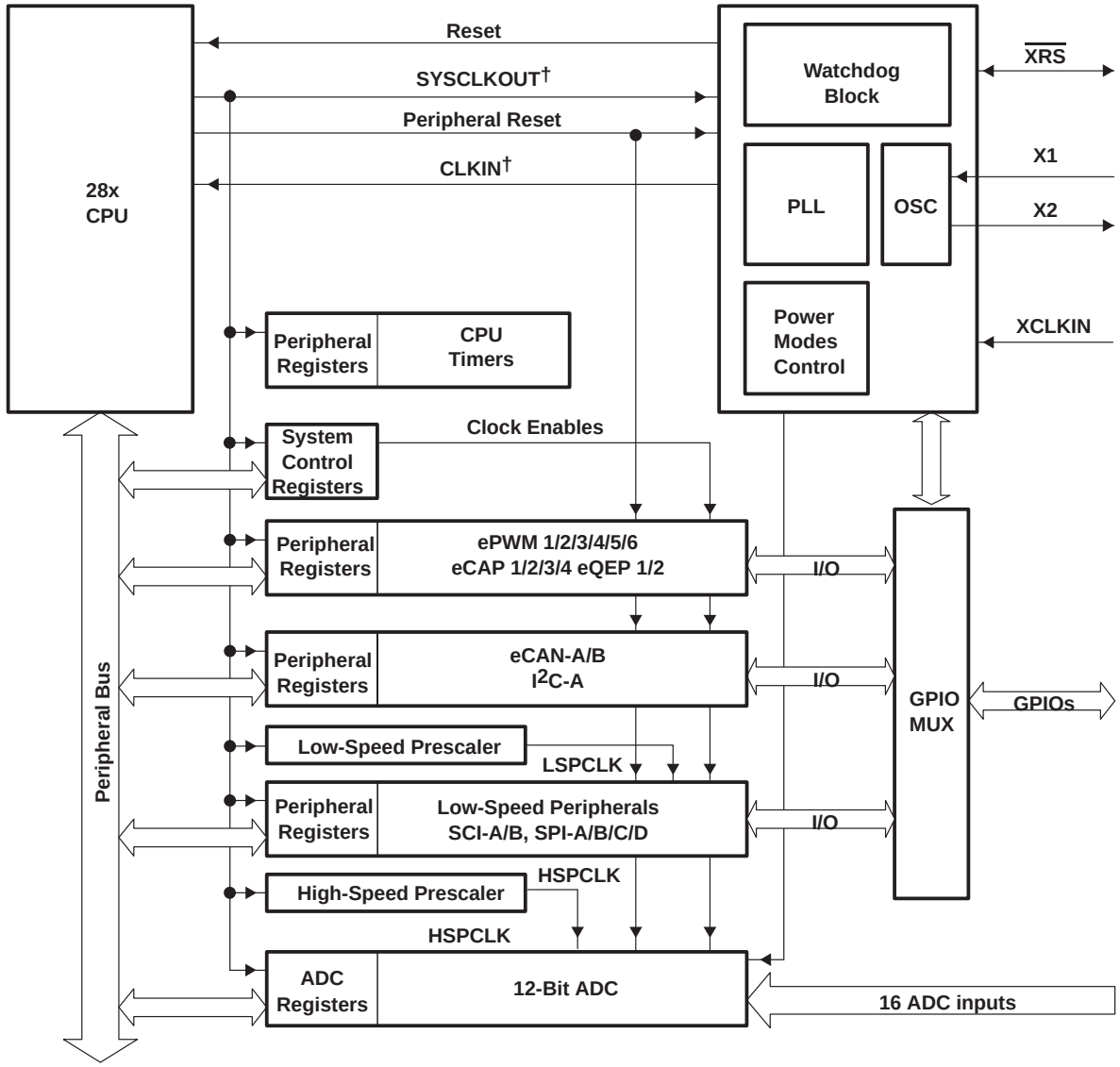
Each external interrupt can be enabled/disabled or qualified using positive, negative, or both positive and negative going edge. For more information, see the *TMS320x280x System Control and Interrupts Reference Guide* (literature number SPRU712).

3.6 System Control

This section describes the 280x oscillator, PLL and clocking mechanisms, the watchdog function and the low power modes. Figure 3−7 shows the various clock and reset domains in the 280x devices that will be discussed.

PRODUCT PREVIEW

PRODUCT PREVIEW



† CLKIN is the clock into the CPU. It is passed out of the CPU as SYSCLKOUT (that is, CLKIN is the same frequency as SYSCLKOUT).

Figure 3−7. Clock and Reset Domains

The PLL, clocking, watchdog and low-power modes, are controlled by the registers listed in Table 3−13.

Table 3−13. PLL, Clocking, Watchdog, and Low-Power Mode Registers†

NAME	ADDRESS	SIZE (X16)	DESCRIPTION
XCLK	0x7010	1	XCLKOUT Pin Control and X1/XCLKIN Status Register
PLLSTS	0x7011	1	PLL Status Register
Reserved	0x7012 0x7019	8	
HISPCP	0x701A	1	High-Speed Peripheral Clock Prescaler Register
LOSPCP	0x701B	1	Low-Speed Peripheral Clock Prescaler Register
PCLKCR0	0x701C	1	Peripheral Clock Control Register 0
PCLKCR1	0x701D	1	Peripheral Clock Control Register 1
LPMCR0	0x701E	1	Low Power Mode Control Register 0
Reserved	0x701F 0x7020	1	
PLLCR	0x7021	1	PLL Control Register
SCSR	0x7022	1	System Control and Status Register
WDCNTR	0x7023	1	Watchdog Counter Register
Reserved	0x7024	1	
WDKEY	0x7025	1	Watchdog Reset Key Register
Reserved	0x7026 0x7028	3	
WDCR	0x7029	1	Watchdog Control Register
Reserved	0x702A 0x702F	6	

† All of the registers in this table are EALLOW protected.

3.6.1 OSC and PLL Block

Figure 3−8 shows the OSC and PLL block on the 280x.

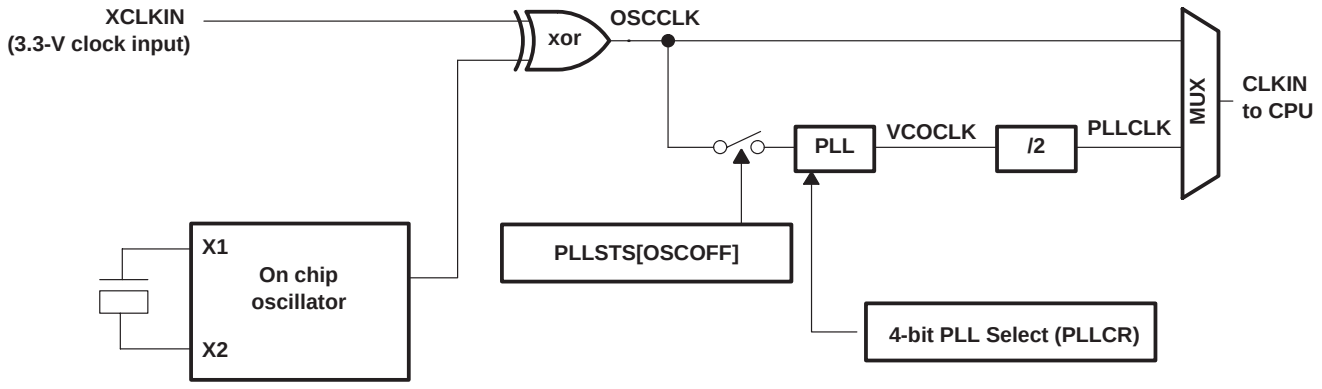


Figure 3−8. OSC and PLL Block Diagram

The on-chip oscillator circuit enables a crystal to be attached to the 280x devices using the X1 and X2 pins. If a crystal is not used, an external oscillator can be directly connected to the XCLKIN pin, the X2 pin is left unconnected, and X1 is tied low. The logic-high level in this case should not exceed V_{DDIO}. The PLLCR bits [3:0] set the clocking ratio.

PRODUCT PREVIEW

Table 3−14. PLLCR Register Bit Definitions

Value	Description
0000 (PLL bypass)	CLKIN = OSCCLK/2
0001	CLKIN = (OSCCLK*1)/2
0010	CLKIN = (OSCCLK*2)/2
0011	CLKIN = (OSCCLK*3)/2
0100	CLKIN = (OSCCLK*4)/2
0101	CLKIN = (OSCCLK*5)/2
0110	CLKIN = (OSCCLK*6)/2
0111	CLKIN = (OSCCLK*7)/2
1000	CLKIN = (OSCCLK*8)/2
1001	CLKIN = (OSCCLK*9)/2
1010	CLKIN = (OSCCLK*10)/2
1011 – 1111	reserved

PRODUCT PREVIEW

3.6.1.1 Loss of Input Clock

In PLL enabled mode, if the input clock XCLKIN or the oscillator clock is removed or absent, the PLL will still issue a “limp-mode” clock. The limp-mode clock will continue to clock the CPU and peripherals at a typical frequency of 1−4 MHz. The device must first receive a clock to reset the PLL and then it will go into limp mode if the clock is removed. The limp mode will not work at power-up.

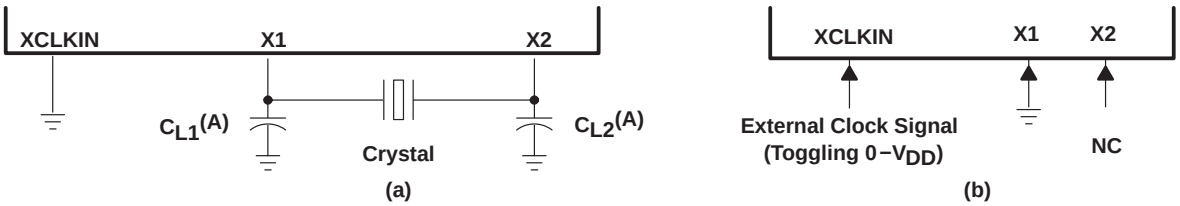
Normally, when the input clocks are present, the watchdog counter decrements to initiate a watchdog reset or WDINT interrupt. However, when the external input clock fails, the watchdog counter stops decrementing (i.e., the watchdog counter does not change with the limp-mode clock). This condition could be used by the application firmware to detect the input clock failure and initiate necessary shut-down procedures for the system.

3.6.1.2 PLL-Based Clock Module

The 280x devices have an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 4-bit ratio control to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. It can be re-enabled (if need be) after the PLL module has stabilized, which takes 131072 XCLKIN cycles.

The PLL-based clock module provides two modes of operation:

- Crystal-operation
  This mode allows the use of an external crystal/resonator to provide the time base to the device.
- External clock source operation
  This mode allows the internal oscillator to be bypassed. The device clocks are generated from an external clock source input on the XCLKIN pin.



(A) TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the DSP chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will ensure start-up and stability over the entire operating range.

Figure 3−9. Recommended Crystal/Clock Connection

Table 3−15. Possible PLL Configuration Modes

PLL MODE	REMARKS	SYSCLKOUT
PLL Off	Invoked by the user setting the PLLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. This can be useful to reduce system noise and for low power operation. The PLLCR register must be set to 0x0000 before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2 or XCLKIN.	OSCCLK
PLL Bypass	The default PLL configuration upon power-up. The PLL itself is bypassed.	OSCCLK/2
PLL Enabled	Achieved by writing a non-zero value into the PLLCR register.	OSCCLK*n/2

3.6.2 External Reference Oscillator Clock Option

The typical specifications for the external quartz crystal for a frequency of 20 MHz are listed below:

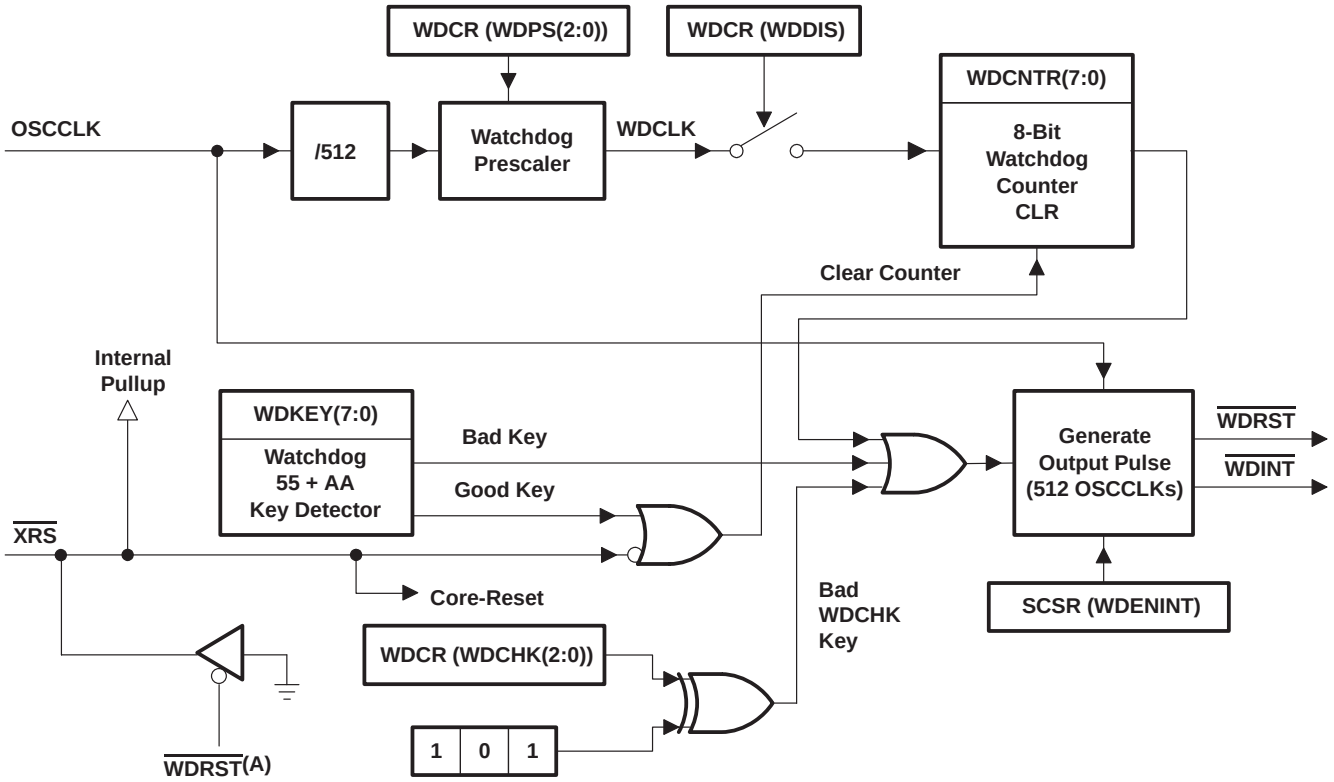
- Fundamental mode, parallel resonant
- C_L (load capacitance) = 12 pF
- $C_{L1} = C_{L2}$ = 24 pF
- C_{shunt} = 6 pF
- ESR range = 30 to 60 Ω

3.6.3 Watchdog Block

The watchdog block on the 280x is similar to the one used on the 240x and 281x devices. The watchdog module generates an output pulse, 512 oscillator clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this, the user disables the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register which will reset the watchdog counter. Figure 3−10 shows the various functional blocks within the watchdog module.

PRODUCT PREVIEW

PRODUCT PREVIEW



(A) The $\overline{\text{WDRST}}$ signal is driven low for 512 OSCCLK cycles.

Figure 3−10. Watchdog Module

The $\overline{\text{WDINT}}$ signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode timer.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the watchdog. The watchdog module will run off the oscillator clock. The $\overline{\text{WDINT}}$ signal is fed to the LPM block so that it can wake the device from STANDBY (if enabled). See Section 3.7, Low-Power Modes Block, for more details.

In IDLE mode, the $\overline{\text{WDINT}}$ signal can generate an interrupt to the CPU, via the PIE, to take the CPU out of IDLE mode.

In HALT mode, this feature cannot be used because the oscillator (and PLL) are turned off and hence so is the watchdog.

3.7 Low-Power Modes Block

The low-power modes on the 280x are similar to the 240x devices. Table 3−16 summarizes the various modes.

Table 3−16. 280x Low-Power Modes

MODE	LPMCR0[1:0]	OSCCLK	CLKIN	SYSCLKOUT	Exit†
IDLE	00	On	On	On‡	$\overline{\text{XRS}}$, Watchdog interrupt, Any enabled interrupt, XNMI
STANDBY	01	On (watchdog still running)	Off	Off	$\overline{\text{XRS}}$, Watchdog interrupt, GPIO Port A signal, Debugger§ XNMI
HALT	1X	Off (oscillator and PLL turned off, watchdog not functional)	Off	Off	$\overline{\text{XRS}}$, GPIO Port A Signal, Debugger§ XNMI

† The Exit column lists which signals or under what conditions the low power mode is exited. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise the IDLE mode is not exited and the device goes back into the indicated low power mode.
‡ The IDLE mode on the 28x behaves differently than on the 24x/240x. On the 28x, the clock output from the CPU (SYSCLKOUT) is still functional while on the 24x/240x the clock is turned off.
§ On the 28x, the JTAG port can still function even if the clock to the CPU (CLKIN) is turned off.

The various low-power modes operate as follows:

IDLE Mode: This mode is exited by any enabled interrupt or an $\overline{\text{XNMI}}$ that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.

STANDBY Mode: Any GPIO port A signal (GPIO[31:0]) can wake the device from STANDBY mode. The user must select which signal(s) will wake the device in the GPIOLPMSEL register. The selected signal(s) are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register.

HALT Mode: $\overline{\text{XRS}}$ and any GPIO port A signal (GPIO[31:0]) can wake the device from HALT mode. The user selects the signal in the GPIOLPMSEL register.

NOTE: The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them in when the IDLE instruction was executed.
See the *TMS320x280x System Control and Interrupts Reference Guide* (literature number SPRU712) for more details.

PRODUCT PREVIEW

4 Peripherals

The integrated peripherals of the 280x are described in the following subsections:

- Three 32-bit CPU-Timers
- Up to six enhanced PWM modules (ePWM1, ePWM2, ePWM3, ePWM4, ePWM5, ePWM6)
- Up to four enhanced capture modules (eCAP1, eCAP2, eCAP3, eCAP4)
- Up to two enhanced QEP modules (eQEP1, eQEP2)
- Enhanced analog-to-digital converter (ADC) module
- Up to two enhanced controller area network (eCAN) modules (eCAN-A, eCAN-B)
- Up to two serial communications interface modules (SCI-A, SCI-B)
- Up to four serial peripheral interface (SPI) modules (SPI-A, SPI-B, SPI-C, SPI-D)
- Inter-integrated circuit module (I^2C)
- Digital I/O and shared pin functions

4.1 32-Bit CPU-Timers 0/1/2

There are three 32-bit CPU-timers on the 280x devices (CPU-TIMER0/1/2).

CPU-Timer 1 is reserved for TI system functions and Timer 2 is reserved for DSP/BIOS. CPU-Timer 0 can be used in user applications. These timers are different from the timers that are present in the ePWM modules.

NOTE: If the application is not using DSP/BIOS, then CPU-Timer 2 can be used in the application.

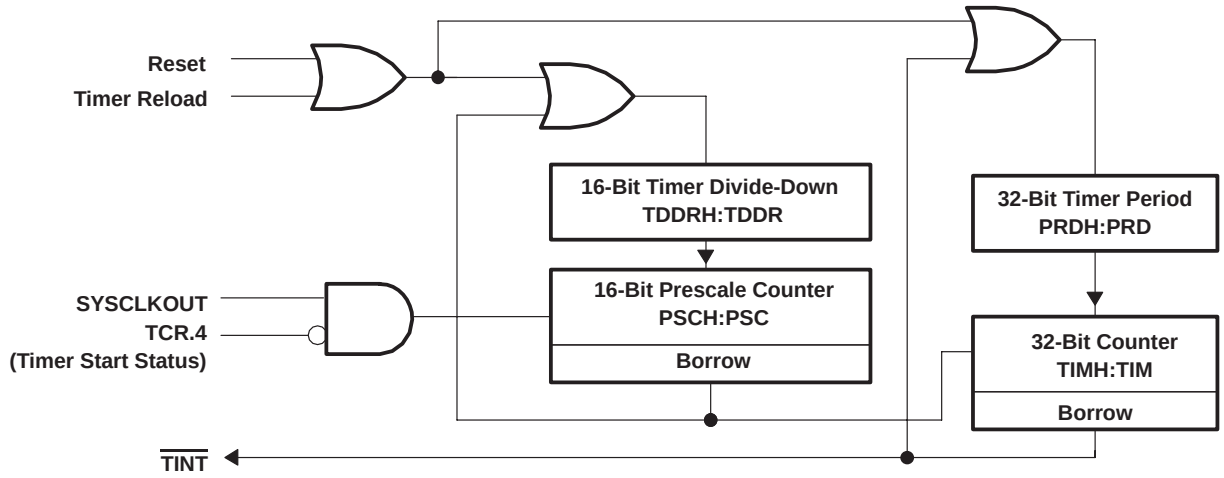
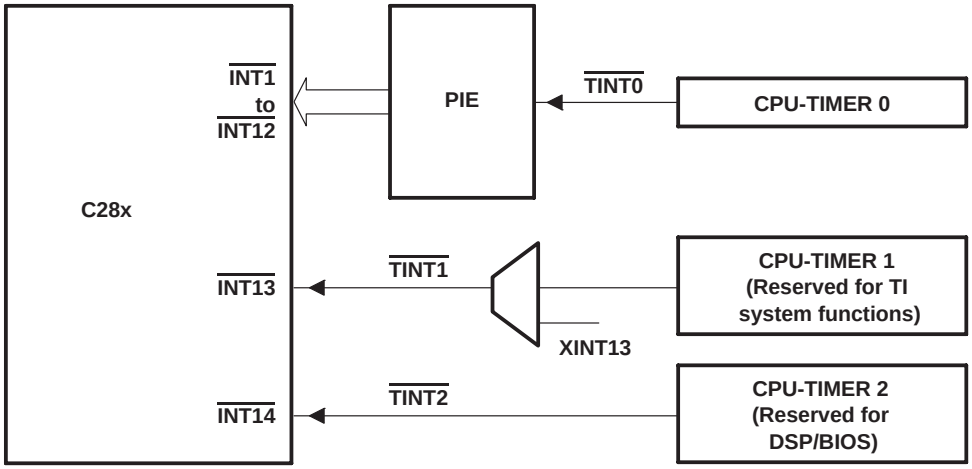


Figure 4−1. CPU-Timers

PRODUCT PREVIEW

In the 280x devices, the timer interrupt signals ($\overline{\text{TINT0}}$, $\overline{\text{TINT1}}$, $\overline{\text{TINT2}}$) are connected as shown in Figure 4−2.



(A) The timer registers are connected to the Memory Bus of the C28x processor.
(B) The timing of the timers is synchronized to SYSCLKOUT of the processor clock.

Figure 4−2. CPU-Timer Interrupts Signals and Output Signal

The general operation of the timer is as follows: The 32-bit counter register “TIMH:TIM” is loaded with the value in the period register “PRDH:PRD”. The counter register, decrements at the SYSCLKOUT rate of the C28x. When the counter reaches 0, a timer interrupt output signal generates an interrupt pulse. The registers listed in Table 4−1 are used to configure the timers. For more information, see the *TMS320x280x System Control and Interrupts Reference Guide* (literature number SPRU712).

PRODUCT PREVIEW

PRODUCT PREVIEW

Table 4−1. CPU-Timers 0, 1, 2 Configuration and Control Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
TIMER0TIM	0x0C00	1	CPU-Timer 0, Counter Register
TIMER0TIMH	0x0C01	1	CPU-Timer 0, Counter Register High
TIMER0PRD	0x0C02	1	CPU-Timer 0, Period Register
TIMER0PRDH	0x0C03	1	CPU-Timer 0, Period Register High
TIMER0TCR	0x0C04	1	CPU-Timer 0, Control Register
reserved	0x0C05	1	
TIMER0TPR	0x0C06	1	CPU-Timer 0, Prescale Register
TIMER0TPRH	0x0C07	1	CPU-Timer 0, Prescale Register High
TIMER1TIM	0x0C08	1	CPU-Timer 1, Counter Register
TIMER1TIMH	0x0C09	1	CPU-Timer 1, Counter Register High
TIMER1PRD	0x0C0A	1	CPU-Timer 1, Period Register
TIMER1PRDH	0x0C0B	1	CPU-Timer 1, Period Register High
TIMER1TCR	0x0C0C	1	CPU-Timer 1, Control Register
reserved	0x0C0D	1	
TIMER1TPR	0x0C0E	1	CPU-Timer 1, Prescale Register
TIMER1TPRH	0x0C0F	1	CPU-Timer 1, Prescale Register High
TIMER2TIM	0x0C10	1	CPU-Timer 2, Counter Register
TIMER2TIMH	0x0C11	1	CPU-Timer 2, Counter Register High
TIMER2PRD	0x0C12	1	CPU-Timer 2, Period Register
TIMER2PRDH	0x0C13	1	CPU-Timer 2, Period Register High
TIMER2TCR	0x0C14	1	CPU-Timer 2, Control Register
reserved	0x0C15	1	
TIMER2TPR	0x0C16	1	CPU-Timer 2, Prescale Register
TIMER2TPRH	0x0C17	1	CPU-Timer 2, Prescale Register High
reserved	0x0C18 0x0C3F	40	

4.2 Enhanced PWM Modules (ePWM1/2/3/4/5/6)

The 280x device contains up to six enhanced PWM Modules (ePWM). Figure 4−3 shows a block diagram of multiple PWM modules Figure 4−4 shows the signal interconnections with the ePWM. See the *TMS320x280x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* (literature number SPRU791) for more details.

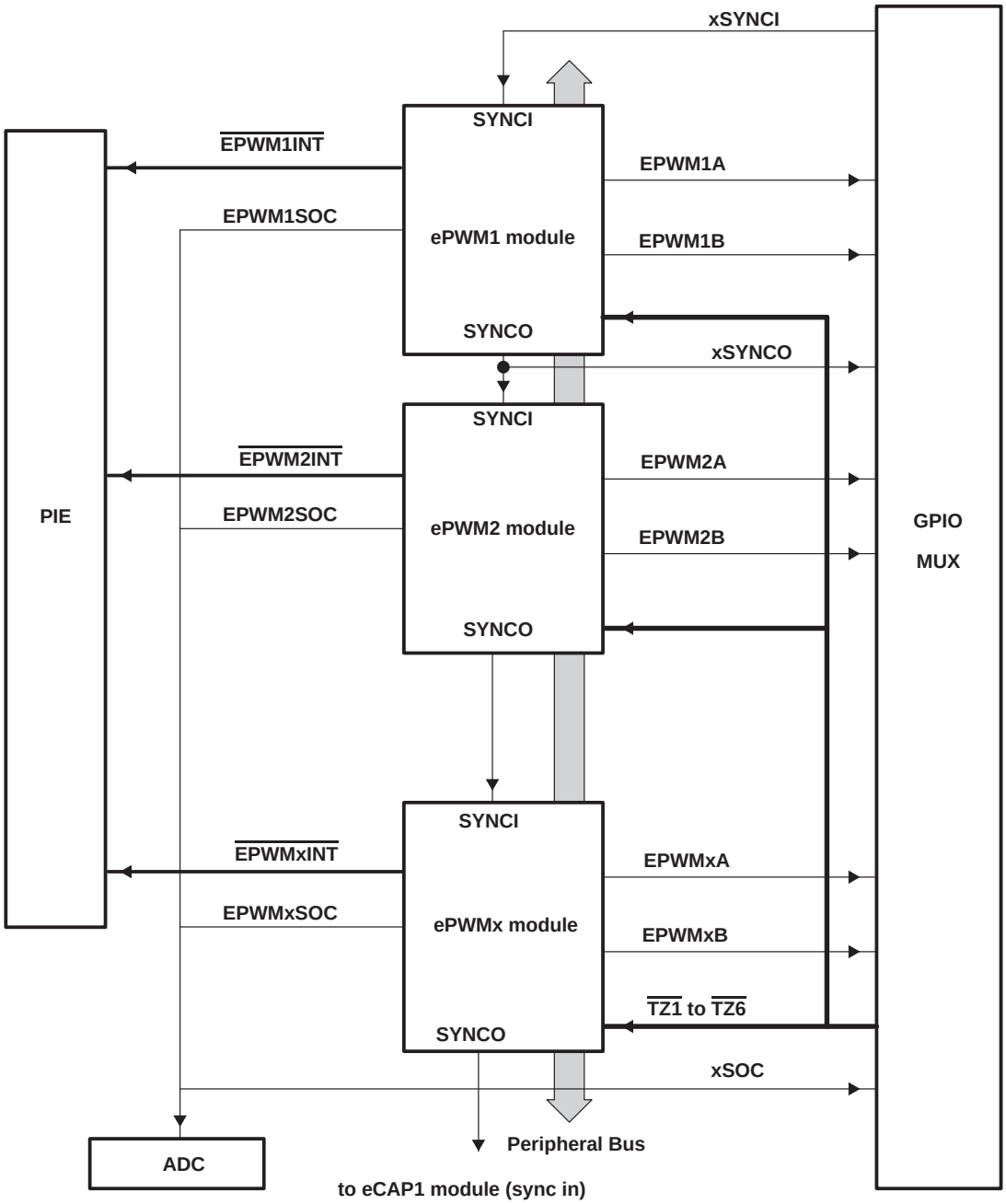


Figure 4−3. Multiple PWM Modules in a 280x System

Table 4−2 shows the complete ePWM register set per module.

PRODUCT PREVIEW

Table 4−2. ePWM Control and Status Registers

NAME	EPWM1	EPWM2	EPWM3	EPWM4	EPWM5	EPWM6	SIZE (X16) / #SHADOW	DESCRIPTION
TBCTL	0x6800	0x6840	0x6880	0x68C0	0x6900	0x6940	1 / 0	Time Base Control Register
TBSTS	0x6801	0x6841	0x6881	0x68C1	0x6901	0x6941	1 / 0	Time Base Status Register
TBPHS	0x6803	0x6843	0x6883	0x68C3	0x6903	0x6943	1 / 0	Time Base Phase Register
TBCNT	0x6804	0x6844	0x6884	0x68C4	0x6904	0x6944	1 / 0	Time Base Counter Register
TBPRD	0x6805	0x6845	0x6885	0x68C5	0x6905	0x6945	1 / **1**	Time Base Period Register Set
CMPCTL	0x6807	0x6847	0x6887	0x68C7	0x6907	0x6947	1 / 0	Counter Compare Control Register
CMPA	0x6809	0x6849	0x6889	0x68C9	0x6909	0x6949	1 / **1**	Counter Compare A Register Set
CMPB	0x680A	0x684A	0x688A	0x68CA	0x690A	0x694A	1 / **1**	Counter Compare B Register Set
AQCTLA	0x680B	0x684B	0x688B	0x68CB	0x690B	0x694B	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x680C	0x684C	0x688C	0x68CC	0x690C	0x694C	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x680D	0x684D	0x688D	0x68CD	0x690D	0x694D	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x680E	0x684E	0x688E	0x68CE	0x690E	0x694E	1 / **1**	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x680F	0x684F	0x688F	0x68CF	0x690F	0x694F	1 / 0	Dead-Band Generator Control Register
DBRED	0x6810	0x6850	0x6890	0x68D0	0x6910	0x6950	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6811	0x6851	0x6891	0x68D1	0x6911	0x6951	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6812	0x6852	0x6892	0x68D2	0x6912	0x6952	1 / 0	Trip Zone Select Register†
TZCTL	0x6814	0x6854	0x6894	0x68D4	0x6914	0x6954	1 / 0	Trip Zone Control Register†
TZEINT	0x6815	0x6855	0x6895	0x68D5	0x6915	0x6955	1 / 0	Trip Zone Enable Interrupt Register†
TZFLG	0x6816	0x6856	0x6896	0x68D6	0x6916	0x6956	1 / 0	Trip Zone Flag Register
TZCLR	0x6817	0x6857	0x6897	0x68D7	0x6917	0x6957	1 / 0	Trip Zone Clear Register†
TZFRC	0x6818	0x6858	0x6898	0x68D8	0x6918	0x6958	1 / 0	Trip Zone Force Register†
ETSEL	0x6819	0x6859	0x6899	0x68D9	0x6919	0x6959	1 / 0	Event Trigger Selection Register
ETPS	0x681A	0x685A	0x689A	0x68DA	0x691A	0x695A	1 / 0	Event Trigger Prescale Register
ETFLG	0x681B	0x685B	0x689B	0x68DB	0x691B	0x695B	1 / 0	Event Trigger Flag Register
ETCLR	0x681C	0x685C	0x689C	0x68DC	0x691C	0x695C	1 / 0	Event Trigger Clear Register
ETFRC	0x681D	0x685D	0x689D	0x68DD	0x691D	0x695D	1 / 0	Event Trigger Force Register
PCCTL	0x681E	0x685E	0x689E	0x68DE	0x691E	0x695E	1 / 0	PWM Chopper Control Register

† Registers that are EALLOW protected.

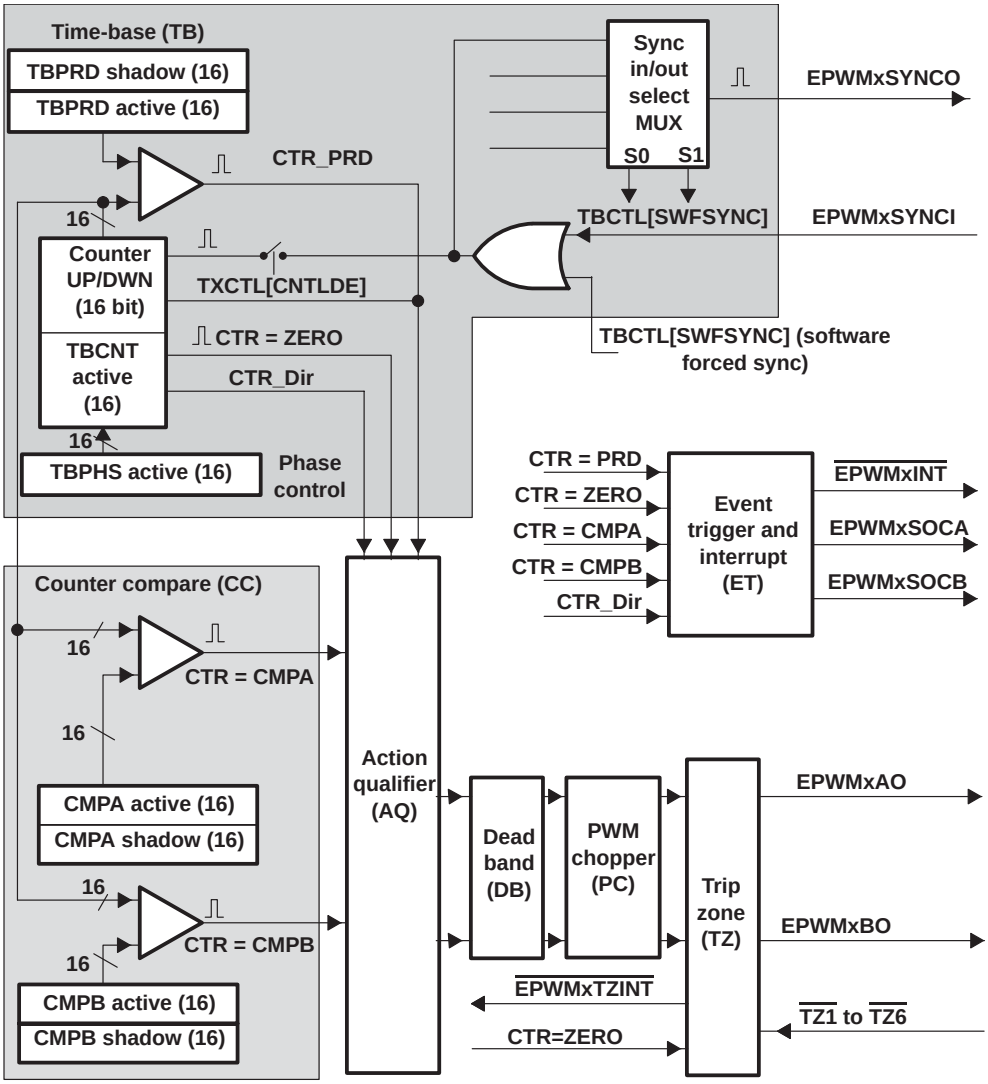


Figure 4−4. ePWM Sub-Modules Showing Critical Internal Signal Interconnects

4.3 Enhanced CAP Modules (eCAP1/2/3/4)

The 280x device contains up to four enhanced capture (eCAP) modules. Figure 4−5 shows a functional block diagram of a module. See the *TMS320x280x Enhanced Capture (eCAP) Module Reference Guide* (literature number SPRU807) for more details.

The eCAP modules are clocked at the SYSCLKOUT rate.

The clock enable bits (ECAP1/2/3/4ENCLK) in the PCLKCR1 register are used to turn off the eCAP modules individually (for low power operation). Upon reset, ECAP1ENCLK, ECAP2ENCLK, ECAP3ENCLK, and ECAP4ENCLK are set to low, indicating that the peripheral clock is off.

PRODUCT PREVIEW

The eCAP module control and status register set is given in Table 4−3.

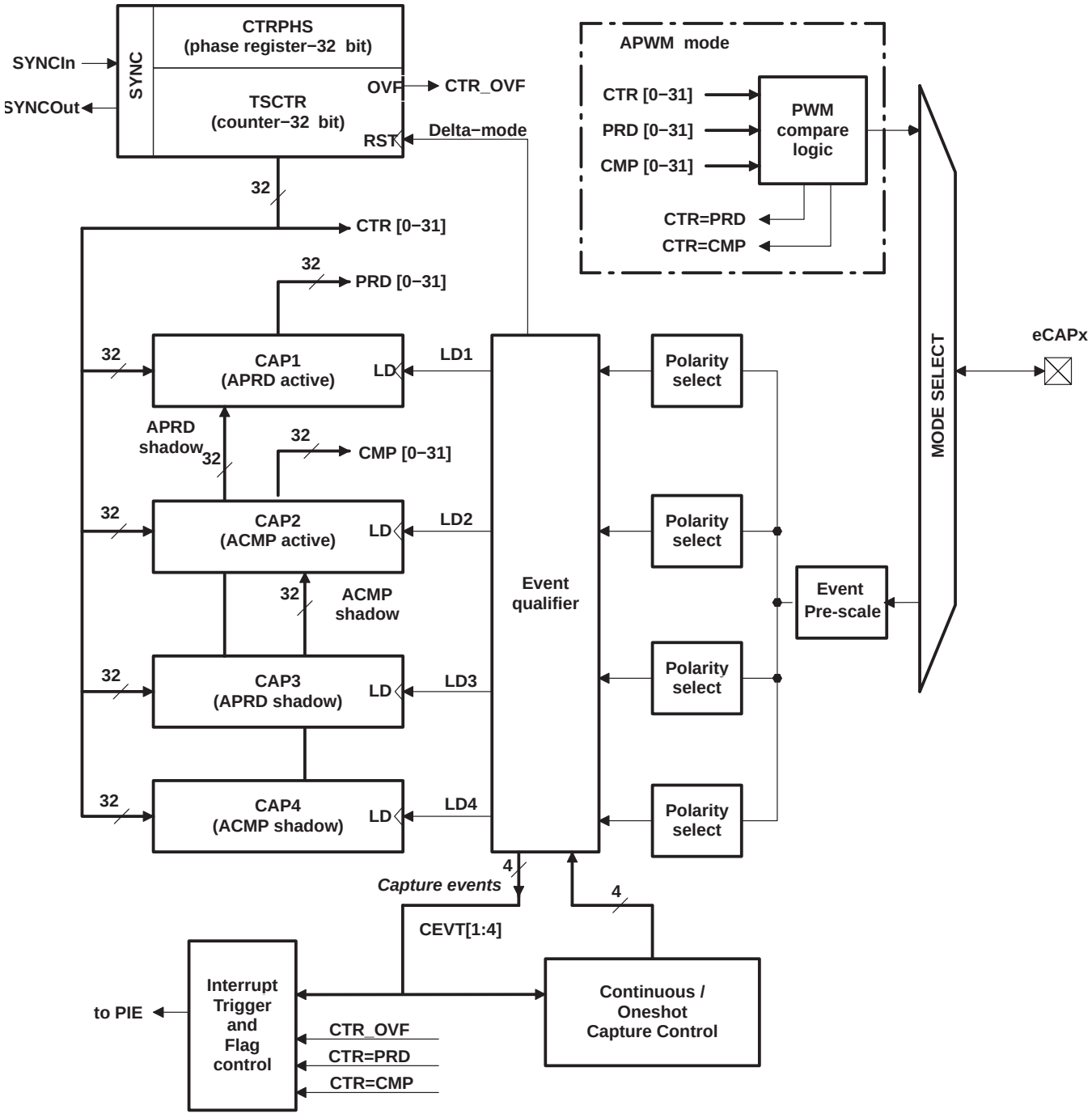


Figure 4−5. eCAP Functional Block Diagram

PRODUCT PREVIEW

Table 4−3. eCAP Control and Status Registers

NAME	ECAP1	ECAP2	ECAP3	ECAP4	SIZE (X16)	DESCRIPTION
TIME BASE MODULE REGISTERS						
TSCTR	0x6A00	0x6A20	0x6A40	0x6A60	2	Time-Stamp Counter
CTRPHS	0x6A02	0x6A22	0x6A42	0x6A62	2	Counter Phase Offset Value Register
CAP1	0x6A04	0x6A24	0x6A44	6A64	2	Capture 1 Register
CAP2	0x6A06	0x6A26	0x6A46	0x6A66	2	Capture 2 Register
CAP3	0x6A08	0x6A28	0x6A48	0x6A68	2	Capture 3 Register
CAP4	0x6A0A	0x6A2A	0x6A4A	0x6A6A	2	Capture 4 Register
Reserved	0x6A0C−0x6A12	0x6A2C−0x6A32	0x6A4C−0x6A52	0x6A6C−0x6A72	8	
ECCTL1	0x6A14	0x6A34	0x6A54	0x6A74	1	Capture Control Register 1
ECCTL2	0x6A15	0x6A35	0x6A55	0x6A75	1	Capture Control Register 2
ECEINT	0x6A16	0x6A36	0x6A56	0x6A76	1	Capture Interrupt Enable Register
ECFLG	0x6A17	0x6A37	0x6A57	0x6A77	1	Capture Interrupt Flag Register
ECCLR	0x6A18	0x6A38	0x6A58	0x6A78	1	Capture Interrupt Clear Register
ECFRC	0x6A19	0x6A39	0x6A59	0x6A79	1	Capture Interrupt Force Register
Reserved	0x6A1A−0x6A1F	0x6A3A−0x6A3F	0x6A5A−0x6A5F	0x6A7A−0x6A7F	6	

PRODUCT PREVIEW

PRODUCT PREVIEW

4.4 Enhanced QEP Modules (eQEP1/1)

The F2808 device contains four enhanced quadrature encoder (eQEP) modules. See the *TMS320x280x Enhanced Quadrature Encoder (eQEP) Module Reference Guide* (literature number SPRU790) for more details.

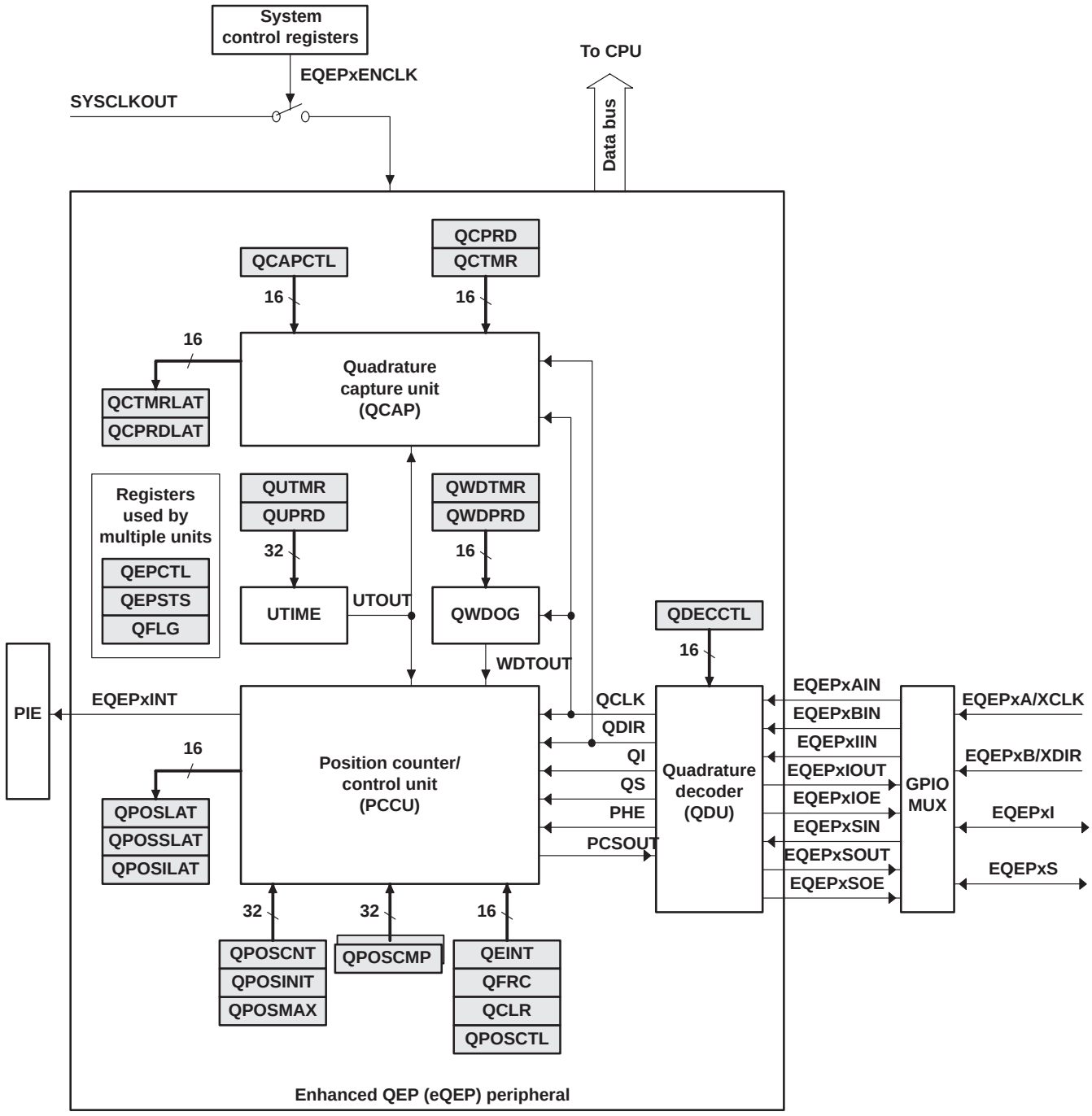


Figure 4−6. eQEP Functional Block Diagram

Table 4−4. eQEP Control and Status Registers

Name	EQEP1 ADDRESS	EQEP2 ADDRESS	EQEP1 SIZE(X16)/ #SHADOW	Register Description
QPOSCNT	0x6B00	0x6B40	2/0	eQEP Position Counter
QPOSINIT	0x6B02	0x6B42	2/0	eQEP Initialization Position Count
QPOSMAX	0x6B04	0x6B44	2/0	eQEP Maximum Position Count
QPOSCMP	0x6B06	0x6B46	2/1	eQEP Position-compare
QPOSILAT	0x6B08	0x6B48	2/0	eQEP Index Position Latch
QPOSSLAT	0x6B0A	0x6B4A	2/0	eQEP Strobe Position Latch
QPOSLAT	0x6B0C	0x6B4C	2/0	eQEP Position Latch
QUTMR	0x6B0E	0x6B4E	2/0	QEP Unit Timer
QUPRD	0x6B10	0x6B50	2/0	eQEP Unit Period Register
QWDTMR	0x6B12	0x6B52	1/0	eQEP Watchdog Timer
QWDPRD	0x6B13	0x6B53	1/0	eQEP Watchdog Period Register
QDECCTL	0x6B14	0x6B54	1/0	eQEP Decoder Control Register
QEPCTL	0x6B15	0x6B55	1/0	eQEP Control Register
QCAPCTL	0x6B16	0x6B56	1/0	eQEP Capture Control Register
QPOSCTL	0x6B17	0x6B57	1/0	eQEP Position-compare Control Register
QEINT	0x6B18	0x6B58	1/0	eQEP Interrupt Enable Register
QFLG	0x6B19	0x6B59	1/0	eQEP Interrupt Flag Register
QCLR	0x6B1A	0x6B5A	1/0	eQEP Interrupt Clear Register
QFRC	0x6B1B	0x6B5B	1/0	eQEP Interrupt Force Register
QEPSTS	0x6B1C	0x6B5C	1/0	eQEP Status Register
QCTMR	0x6B1D	0x6B5D	1/0	eQEP Capture Timer
QCPRD	0x6B1E	0x6B5E	1/0	eQEP Capture Period Register
QCTMRLAT	0x6B1F	0x6B5F	1/0	eQEP Capture Timer Latch
QCPRDLAT	0x6B20	0x6B60	1/0	eQEP Capture Period Latch
Reserved	0x6B21−0x6B3F	0x6B61−0x6B7F	31/0	

PRODUCT PREVIEW

PRODUCT PREVIEW

4.5 Enhanced Analog-to-Digital Converter (ADC) Module

A simplified functional block diagram of the ADC module is shown in Figure 4−7. The ADC module consists of a 12-bit ADC with a built-in sample-and-hold (S/H) circuit. Functions of the ADC module include:

- 12-bit ADC core with built-in S/H
- Analog input: 0.0 V to 3.0 V (Voltages above 3.0 V produce full-scale conversion results.)
- Fast conversion rate: 160 ns at 12.5-MHz ADC clock, 6.25 MSPS
- 16-channel, MUXed inputs
- Autosequencing capability provides up to 16 “autoconversions” in a single session. Each conversion can be programmed to select any 1 of 16 input channels
- Sequencer can be operated as two independent 8-state sequencers or as one large 16-state sequencer (i.e., two cascaded 8-state sequencers)
- Sixteen result registers (individually addressable) to store conversion values
  - The digital value of the input analog voltage is derived by:

$$\text{Digital Value} = 0, \quad \text{when input} \le 0\ \text{V}$$

$$\text{Digital Value} = 4096 \times \frac{\text{Input Analog Voltage} - \text{ADCLO}}{3}, \quad \text{when } 0\ \text{V} < \text{input} < 3\ \text{V}$$

$$\text{Digital Value} = 4095, \quad \text{when input} \ge 3\ \text{V}$$

Note: All fractional values are truncated.

- Multiple triggers as sources for the start-of-conversion (SOC) sequence
  - S/W − software immediate start
  - ePWM start of conversion
  - XINT2 ADC start of conversion
- Flexible interrupt control allows interrupt request on every end-of-sequence (EOS) or every other EOS
- Sequencer can operate in “start/stop” mode, allowing multiple “time-sequenced triggers” to synchronize conversions
- SOCA and SOCB triggers can operate independently in dual-sequencer mode
- Sample-and-hold (S/H) acquisition time window has separate prescale control

The ADC module in the 280x has been enhanced to provide flexible interface to ePWM peripherals. The ADC interface is built around a fast, 12-bit ADC module with a fast conversion rate of 160 ns at 12.5-MHz ADC clock. The ADC module has 16 channels, configurable as two independent 8-channel modules. The two independent 8-channel modules can be cascaded to form a 16-channel module. Although there are multiple input channels and two sequencers, there is only one converter in the ADC module. Figure 4−7 shows the block diagram of the 280x ADC module.

The two 8-channel modules have the capability to autosequence a series of conversions, each module has the choice of selecting any one of the respective eight channels available through an analog MUX. In the cascaded mode, the autosequencer functions as a single 16-channel sequencer. On each sequencer, once the conversion is complete, the selected channel value is stored in its respective RESULT register. Autosequencing allows the system to convert the same channel multiple times, allowing the user to perform oversampling algorithms. This gives increased resolution over traditional single-sampled conversion results.

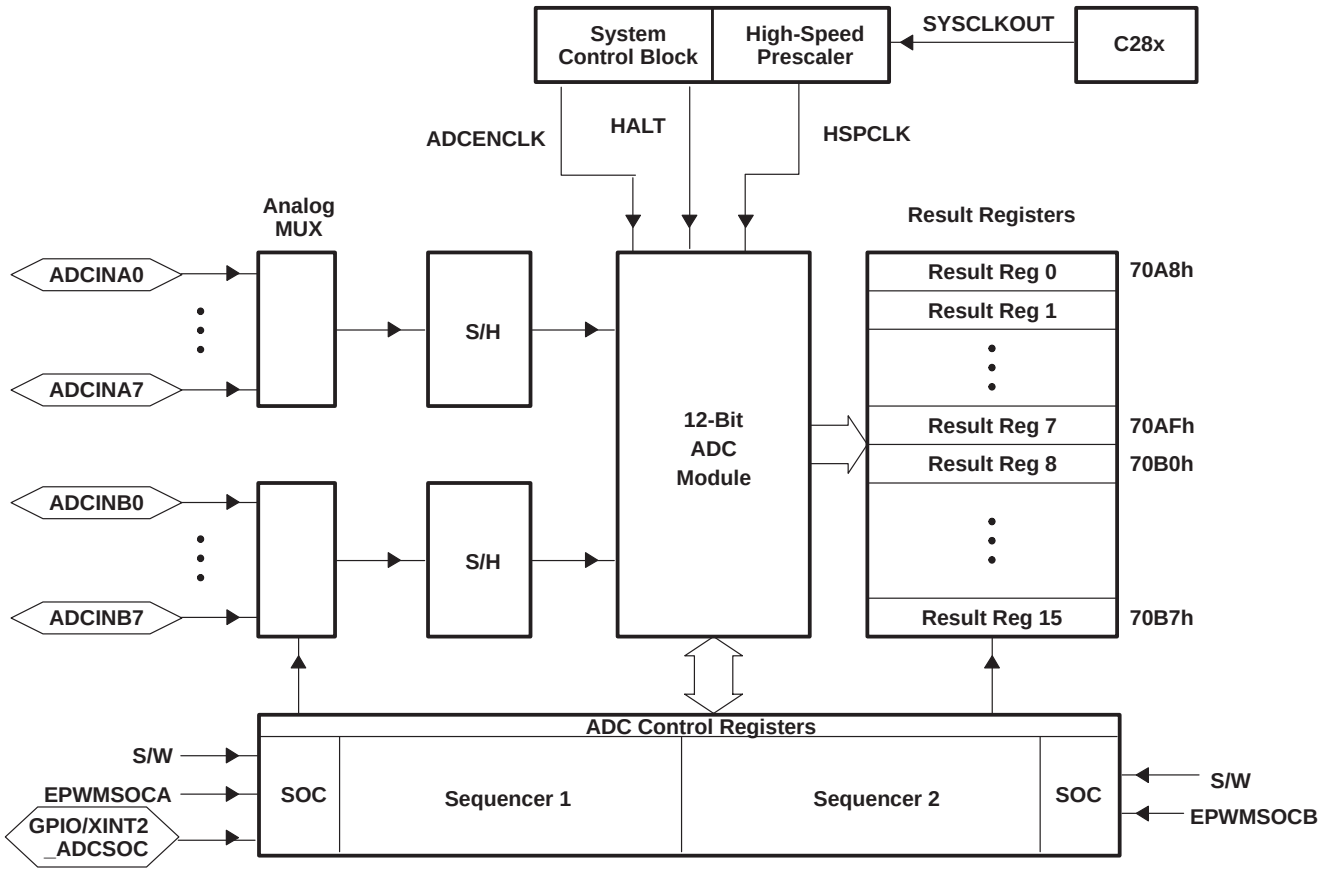


Figure 4−7. Block Diagram of the F280x ADC Module

To obtain the specified accuracy of the ADC, proper board layout is very critical. To the best extent possible, traces leading to the ADCIN pins should not run in close proximity to the digital signal paths. This is to minimize switching noise on the digital lines from getting coupled to the ADC inputs. Furthermore, proper isolation techniques must be used to isolate the ADC module power pins (V_{DDIA18}, V_{DD2A18}, V_{DDA2}, V_{DDAIO}) from the digital supply. Figure 4−8 shows the ADC pin connections for the 280x devices.

1. The ADC registers are accessed at the SYSCLKOUT rate. The internal timing of the ADC module is controlled by the high-speed peripheral clock (HSPCLK).

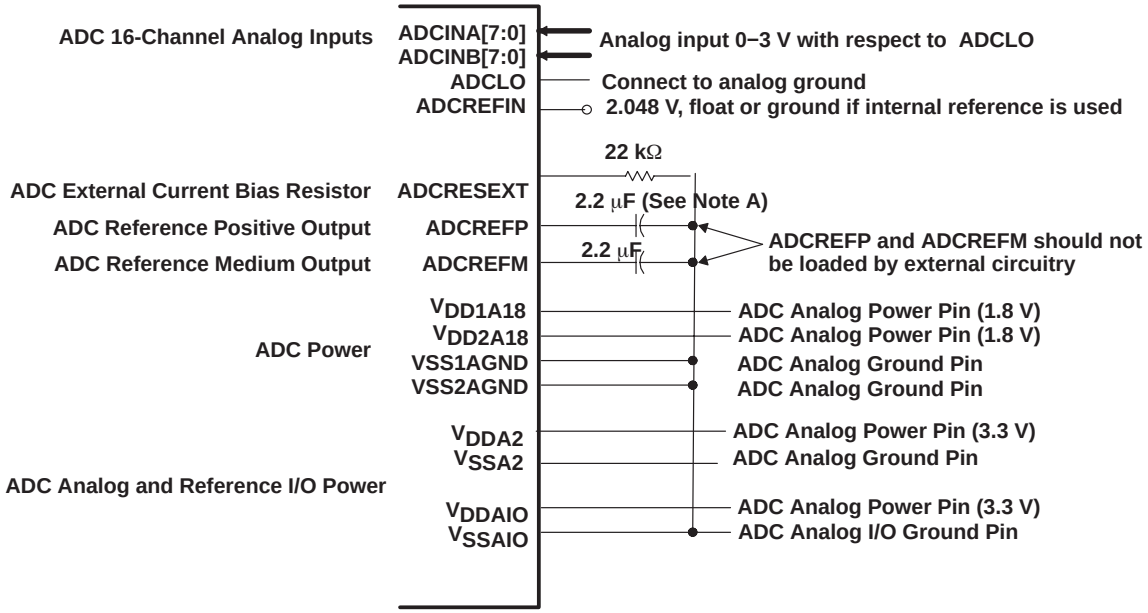
2. The behavior of the ADC module based on the state of the ADCENCLK signal and HALT mode is as follows:

ADCENCLK: On reset, this signal will be low. While reset is active-low ($\overline{XRS}$) the clock to the register will still function. This is necessary to make sure all registers and modes go into their default reset state. The analog module, however, will be in a low-power inactive state. As soon as reset goes high, then the clock to the registers will be disabled. When the user sets the ADCENCLK signal high, then the clocks to the registers will be enabled and the analog module will be enabled. There will be a certain time delay (ms range) before the ADC is stable and can be used.

HALT Mode: This mode only affects the analog module. It does not affect the registers. In this mode, the ADC module goes into low-power mode. This mode also will stop the clock to the CPU, which will stop the HSPCLK; therefore, the ADC register logic will be turned off indirectly.

PRODUCT PREVIEW

Figure 4−8 shows the ADC pin-biasing for internal reference and Figure 4−9 shows the ADC pin-biasing for external reference.



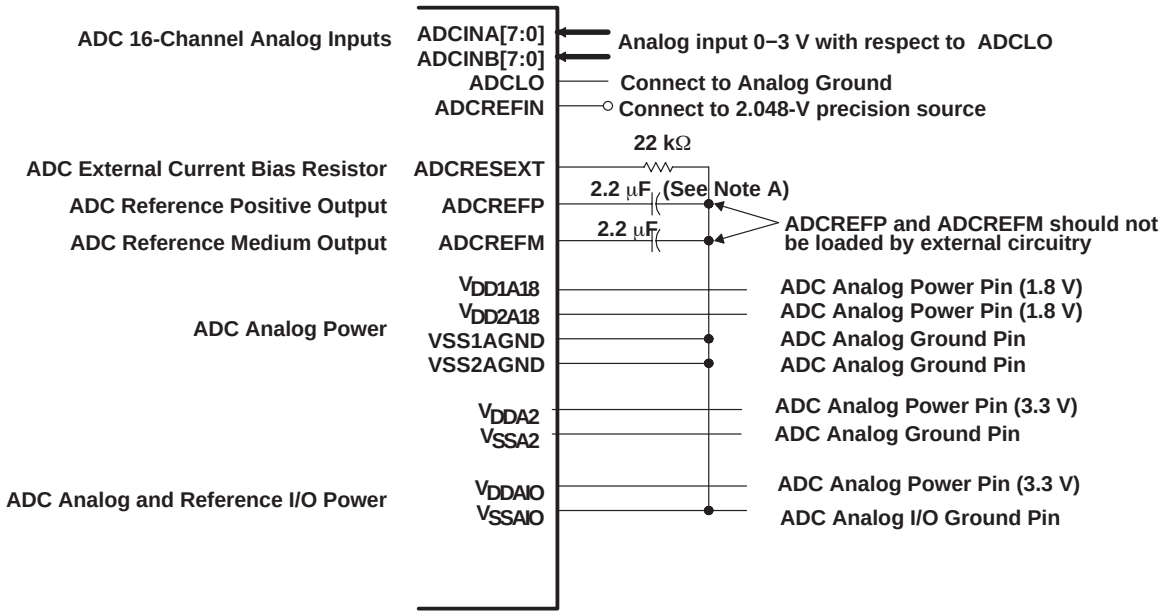
NOTES: A. TAIYO YUDEN LMK212BJ225MG−T or equivalent
B. External decoupling capacitors are recommended on all power pins.
C. Analog inputs must be driven from an operational amplifier that does not degrade the ADC performance.

Figure 4−8. ADC Pin Connections With Internal Reference

NOTE:

The temperature rating of any recommended component must match the rating of the end product.

PRODUCT PREVIEW



NOTES: A. TAIYO YUDEN LMK212BJ225MG−T or equivalent
B. External decoupling capacitors are recommended on all power pins.
C. Analog inputs must be driven from an operational amplifier that does not degrade the ADC performance.
D. External voltage on ADCREFIN is enabled by changing bits 15:14 in the ADC Reference Select register depending on the voltage used on this pin. TI recommends TI part REF3020 or equivalent for 2.048 V generation. Overall gain accuracy will be determined by accuracy of this voltage source.

Figure 4−9. ADC Pin Connections With External Reference

The ADC operation is configured, controlled, and monitored by the registers listed in Table 4−5.

PRODUCT PREVIEW

PRODUCT PREVIEW

Table 4−5. ADC Registers

NAME	ADDRESS†	ADDRESS‡	SIZE (x16)	DESCRIPTION
ADCTRL1	0x7100		1	ADC Control Register 1
ADCTRL2	0x7101		1	ADC Control Register 2
ADCMAXCONV	0x7102		1	ADC Maximum Conversion Channels Register
ADCCHSELSEQ1	0x7103		1	ADC Channel Select Sequencing Control Register 1
ADCCHSELSEQ2	0x7104		1	ADC Channel Select Sequencing Control Register 2
ADCCHSELSEQ3	0x7105		1	ADC Channel Select Sequencing Control Register 3
ADCCHSELSEQ4	0x7106		1	ADC Channel Select Sequencing Control Register 4
ADCASEQSR	0x7107		1	ADC Auto-Sequence Status Register
ADCRESULT0	0x7108	0x0B00	1	ADC Conversion Result Buffer Register 0
ADCRESULT1	0x7109	0x0B01	1	ADC Conversion Result Buffer Register 1
ADCRESULT2	0x710A	0x0B02	1	ADC Conversion Result Buffer Register 2
ADCRESULT3	0x710B	0x0B03	1	ADC Conversion Result Buffer Register 3
ADCRESULT4	0x710C	0x0B04	1	ADC Conversion Result Buffer Register 4
ADCRESULT5	0x710D	0x0B05	1	ADC Conversion Result Buffer Register 5
ADCRESULT6	0x710E	0x0B06	1	ADC Conversion Result Buffer Register 6
ADCRESULT7	0x710F	0x0B07	1	ADC Conversion Result Buffer Register 7
ADCRESULT8	0x7110	0x0B00	1	ADC Conversion Result Buffer Register 8
ADCRESULT9	0x7111	0x0B09	1	ADC Conversion Result Buffer Register 9
ADCRESULT10	0x7112	0x0B0A	1	ADC Conversion Result Buffer Register 10
ADCRESULT11	0x7113	0x0B0B	1	ADC Conversion Result Buffer Register 11
ADCRESULT12	0x7114	0x0B0C	1	ADC Conversion Result Buffer Register 12
ADCRESULT13	0x7115	0x0B0D	1	ADC Conversion Result Buffer Register 13
ADCRESULT14	0x7116	0x0B0E	1	ADC Conversion Result Buffer Register 14
ADCRESULT15	0x7117	0x0B0F	1	ADC Conversion Result Buffer Register 15
ADCTRL3	0x7118		1	ADC Control Register 3
ADCST	0x7119		1	ADC Status Register
reserved	0x711A 0x711B		2	
ADCREFSEL	0x711C		1	ADC Reference Select Register
ADCOFFTRIM	0x711D		1	ADC Offset Trim Register
Reserved	0x711E ox711F		2	ADC Status Register

† The registers in this column are Peripheral Frame 2 Registers.

‡ The ADC result registers are dual mapped in the F280x DSP. Locations in Peripheral Frame 2 (0x7108−0x7117) are 2 wait states and left justified. Locations in Peripheral Frame 0 space (0x0B00−0x0B0F) are 0 wait states and right justified. During high speed/continuous conversion use of the ADC, use the 0 wait state locations for fast transfer of ADC results to user memory.

4.6 Enhanced Controller Area Network (eCAN) Modules (eCAN-A and eCAN-B)

Each CAN module has the following features:

- Fully compliant with CAN protocol, version 2.0B
- Supports data rates up to 1 Mbps
- Thirty-two mailboxes, each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Has a programmable receive mask
  - Supports data and remote frame
  - Composed of 0 to 8 bytes of data
  - Uses a 32-bit time stamp on receive and transmit message
  - Protects against reception of new message
  - Holds the dynamically programmable priority of transmit message
  - Employs a programmable interrupt scheme with two interrupt levels
  - Employs a programmable alarm on transmission or reception time-out
- Low-power mode
- Programmable wake-up on bus activity
- Automatic reply to a remote request message
- Automatic retransmission of a frame in case of loss of arbitration or error
- 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
- Self-test mode
  - Operates in a loopback mode receiving its own message. A “dummy” acknowledge is provided, thereby eliminating the need for another node to provide the acknowledge bit.

NOTE: For a SYSCLKOUT of 100 MHz, the smallest bit rate possible is 15.6 kbps.

PRODUCT PREVIEW

PRODUCT PREVIEW

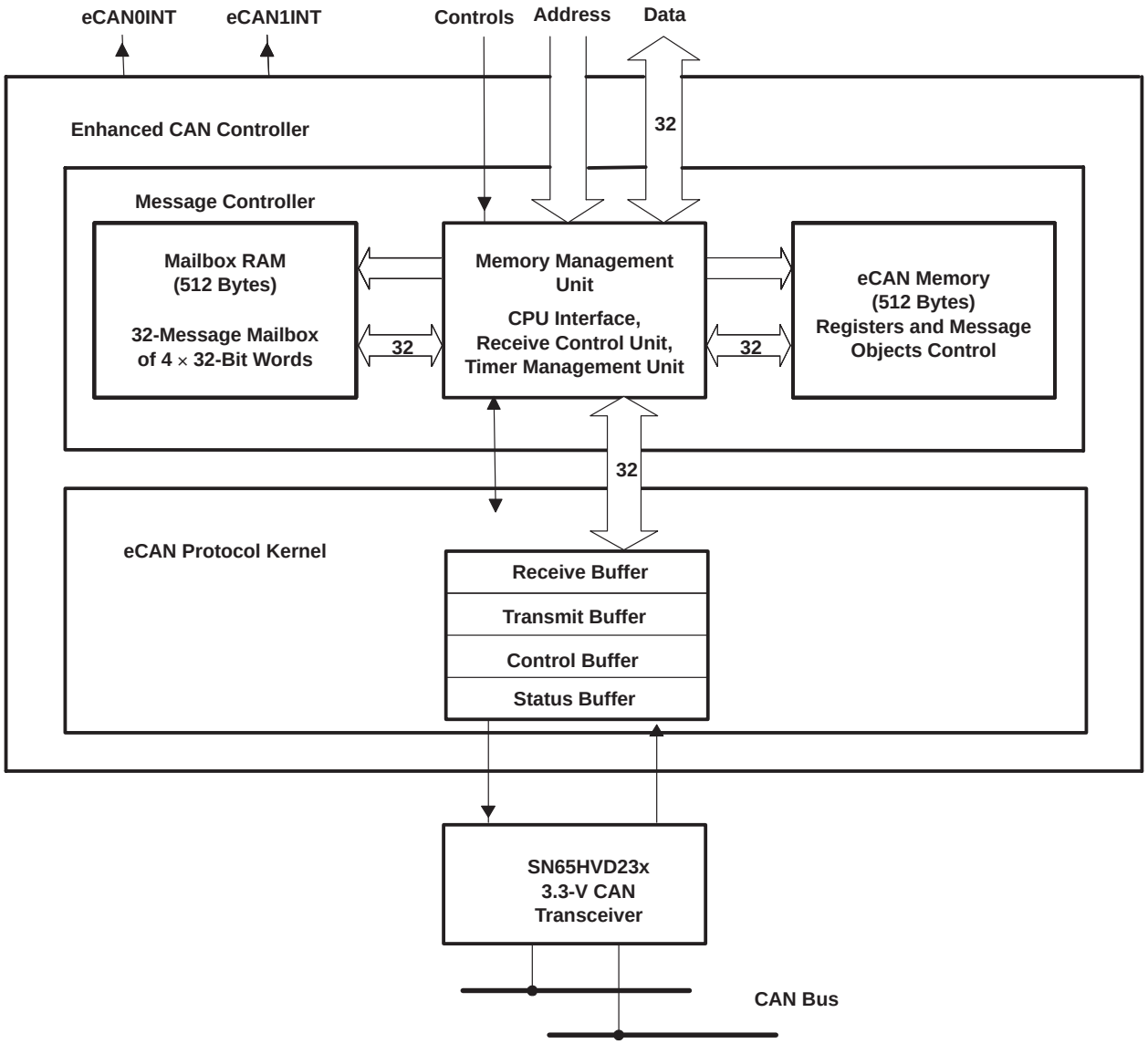


Figure 4−10. eCAN-A Block Diagram and Interface Circuit

Table 4−6. 3.3-V eCAN Transceivers for the TMS320F280x DSPs

Part Number	Supply Voltage	Low-Power Mode	Slope Control	Vref	Other	T_A
SN65HVD230	3.3 V	Standby	Adjustable	Yes	−−	−40°C to 85°C
SN65HVD230Q	3.3 V	Standby	Adjustable	Yes	−−	−40°C to 125°C
SN65HVD231	3.3 V	Sleep	Adjustable	Yes	−−	−40°C to 85°C
SN65HVD231Q	3.3 V	Sleep	Adjustable	Yes	−−	−40°C to 125°C
SN65HVD232	3.3 V	None	None	None	−−	−40°C to 85°C
SN65HVD232Q	3.3 V	None	None	None	−−	−40°C to 125°C
SN65HVD233	3.3 V	Standby	Adjustable	None	Diagnostic Loopback	−40°C to 125°C
SN65HVD234	3.3 V	Standby and Sleep	Adjustable	None	−−	−40°C to 125°C
SN65HVD235	3.3 V	Standby	Adjustable	None	Autobaud Loopback	−40°C to 125°C

PRODUCT PREVIEW

PRODUCT PREVIEW

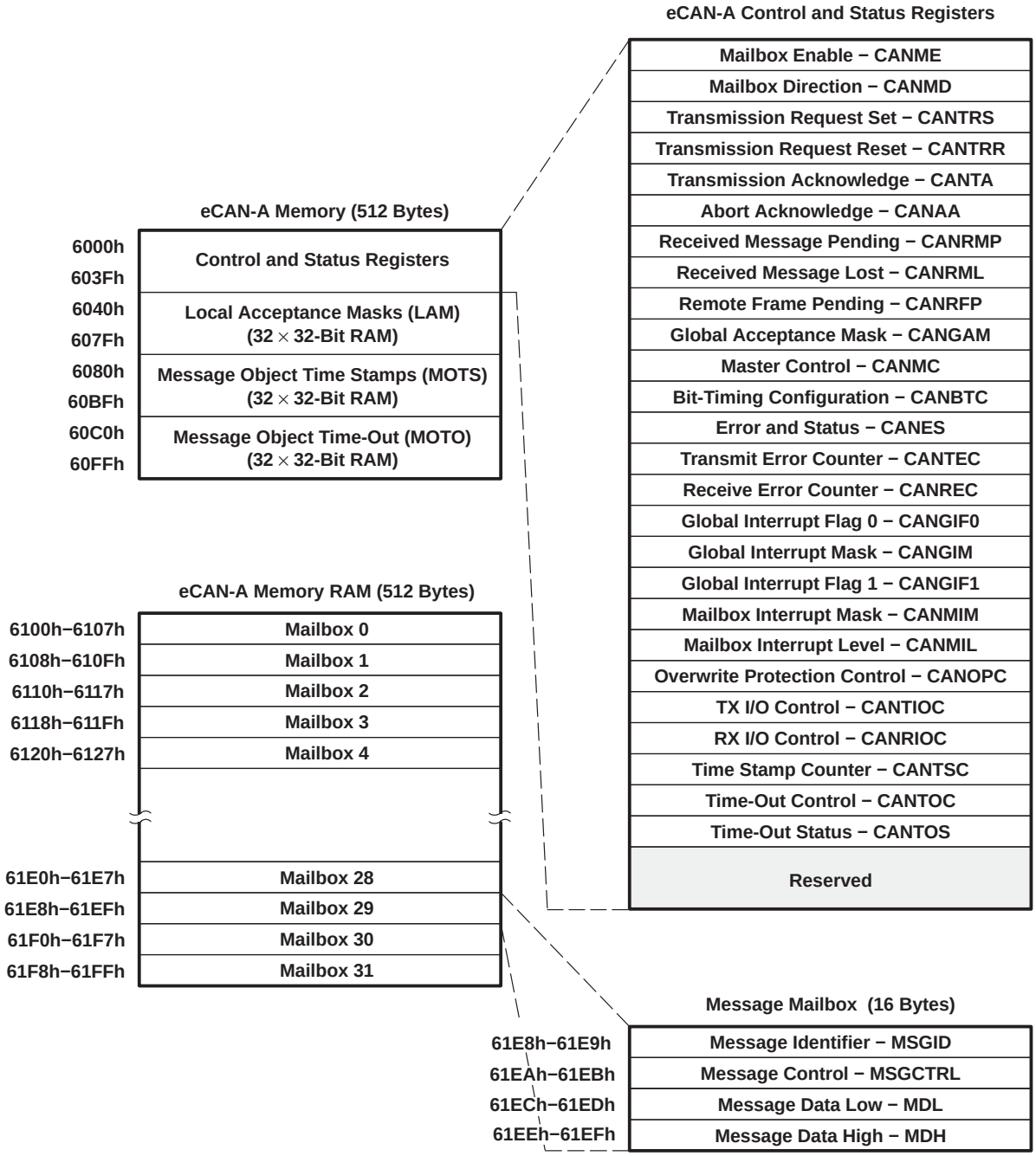


Figure 4−11. eCAN-A Memory Map

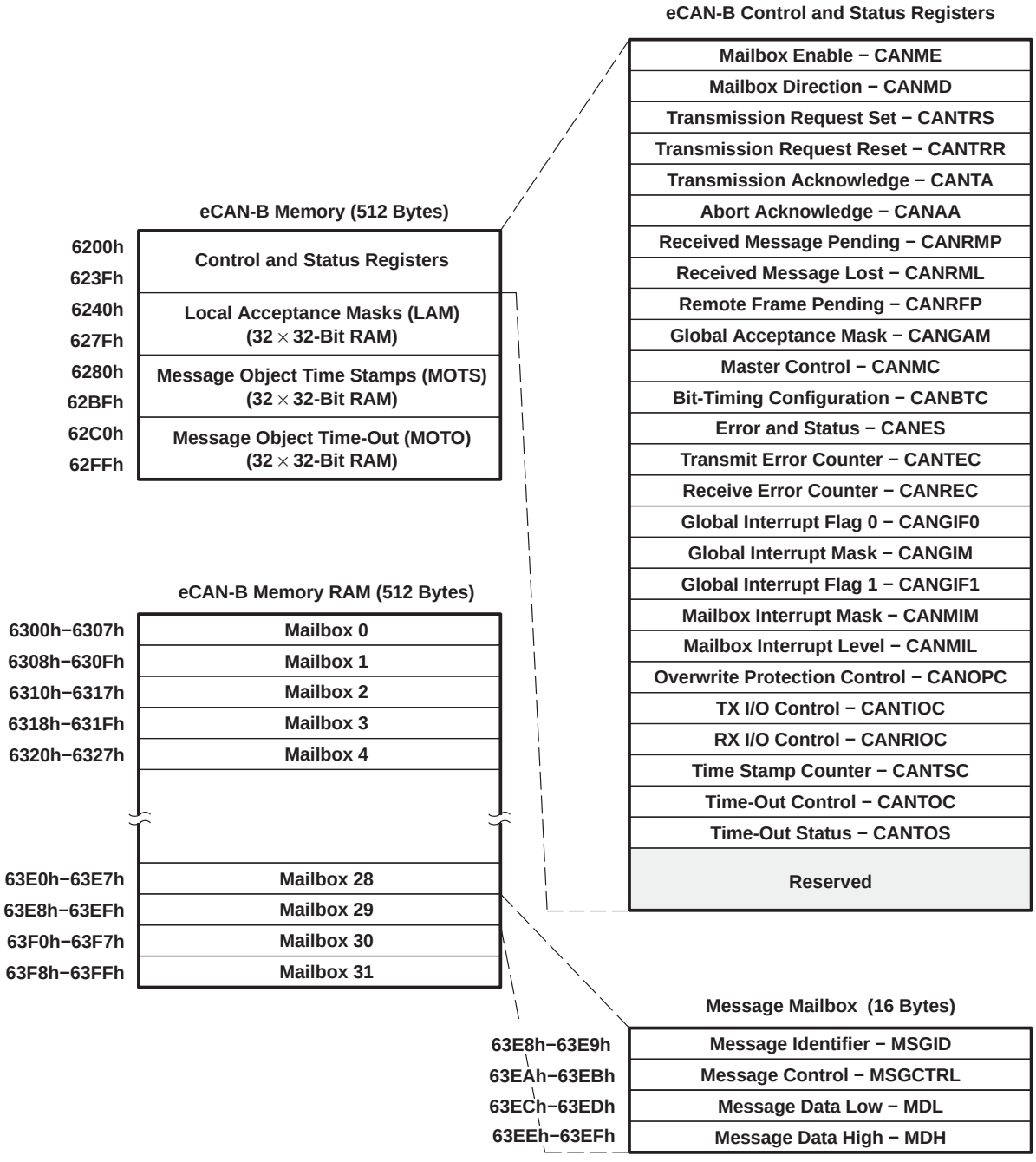


Figure 4−12. eCAN-B Memory Map

PRODUCT PREVIEW

The CAN registers listed in Table 4−7 are used by the CPU to configure and control the CAN controller and the message objects. eCAN control registers only support 32-bit read/write operations. Mailbox RAM can be accessed as 16 bits or 32 bits. 32-bit accesses are aligned to an even boundary.

Table 4−7. CAN Register Map†

REGISTER NAME	ECAN-A ADDRESS	ECAN-B ADDRESS	SIZE (x32)	DESCRIPTION
CANME	0x6000	0x6200	1	Mailbox enable
CANMD	0x6002	0x6202	1	Mailbox direction
CANTRS	0x6004	0x6204	1	Transmit request set
CANTRR	0x6006	0x6206	1	Transmit request reset
CANTA	0x6008	0x6208	1	Transmission acknowledge
CANAA	0x600A	0x620A	1	Abort acknowledge
CANRMP	0x600C	0x620C	1	Receive message pending
CANRML	0x600E	0x620E	1	Receive message lost
CANRFP	0x6010	0x6210	1	Remote frame pending
CANGAM	0x6012	0x6212	1	Global acceptance mask
CANMC	0x6014	0x6214	1	Master control
CANBTC	0x6016	0x6216	1	Bit-timing configuration
CANES	0x6018	0x6218	1	Error and status
CANTEC	0x601A	0x621A	1	Transmit error counter
CANREC	0x601C	0x621C	1	Receive error counter
CANGIF0	0x601E	0x621E	1	Global interrupt flag 0
CANGIM	0x6020	0x6220	1	Global interrupt mask
CANGIF1	0x6022	0x6222	1	Global interrupt flag 1
CANMIM	0x6024	0x6224	1	Mailbox interrupt mask
CANMIL	0x6026	0x6226	1	Mailbox interrupt level
CANOPC	0x6028	0x6228	1	Overwrite protection control
CANTIOC	0x602A	0x622A	1	TX I/O control
CANRIOC	0x602C	0x622C	1	RX I/O control
CANTSC	0x602E	0x622E	1	Time stamp counter (Reserved in SCC mode)
CANTOC	0x6030	0x6230	1	Time-out control (Reserved in SCC mode)
CANTOS	0x6032	0x6232	1	Time-out status (Reserved in SCC mode)

† These registers are mapped to Peripheral Frame 1.

PRODUCT PREVIEW

4.7 Serial Communications Interface Modules (SCI-A, SCI-B)

The 280x devices include up to two serial communications interface (SCI) modules. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

  NOTE: Both pins can be used as GPIO if not used for SCI.
- Baud rate programmable to 64K different rates
  - Baud rate $= \frac{\text{LSPCLK}}{(\text{BRR} + 1) * 8}$, when BRR $\neq 0$

    $= \frac{\text{LSPCLK}}{16}$, when BRR = 0

    SPI performance is limited by I/O buffer switching speed. Internal prescalers must be adjusted such that the peripheral speed is less than the I/O buffer speed limit—20 MHz maximum.
- Data-word format
  - One start bit
  - Data-word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- Max bit rate $= \frac{100 \text{ MHz}}{2 \times 8} = 6.25 \times 10^6$ b/s

PRODUCT PREVIEW

PRODUCT PREVIEW

- NRZ (non-return-to-zero) format
- Ten SCI module control registers located in the control register frame beginning at address 7050h

  NOTE: All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7−0), and the upper byte (15−8) is read as zeros. Writing to the upper byte has no effect.

- Enhanced features:
  − Auto baud-detect hardware logic
  − 16-level transmit/receive FIFO

The SCI port operation is configured and controlled by the registers listed in Table 4−8 and Table 4−9.

Table 4−8. SCI-A Registers†‡

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCICCRA	0x7050	1	SCI-A Communications Control Register
SCICTL1A	0x7051	1	SCI-A Control Register 1
SCIHBAUDA	0x7052	1	SCI-A Baud Register, High Bits
SCILBAUDA	0x7053	1	SCI-A Baud Register, Low Bits
SCICTL2A	0x7054	1	SCI-A Control Register 2
SCIRXSTA	0x7055	1	SCI-A Receive Status Register
SCIRXEMUA	0x7056	1	SCI-A Receive Emulation Data Buffer Register
SCIRXBUFA	0x7057	1	SCI-A Receive Data Buffer Register
SCITXBUFA	0x7059	1	SCI-A Transmit Data Buffer Register
SCIFFTXA	0x705A	1	SCI-A FIFO Transmit Register
SCIFFRXA	0x705B	1	SCI-A FIFO Receive Register
SCIFFCTA	0x705C	1	SCI-A FIFO Control Register
SCIPRIA	0x705F	1	SCI-A Priority Control Register

† Shaded registers are registers for the FIFO mode.
‡ Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Table 4−9. SCI-B Registers†‡

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SCICCRB	0x7750	1	SCI-B Communications Control Register
SCICTL1B	0x7751	1	SCI-B Control Register 1
SCIHBAUDB	0x7752	1	SCI-B Baud Register, High Bits
SCILBAUDB	0x7753	1	SCI-B Baud Register, Low Bits
SCICTL2B	0x7754	1	SCI-B Control Register 2
SCIRXSTB	0x7755	1	SCI-B Receive Status Register
SCIRXEMUB	0x7756	1	SCI-B Receive Emulation Data Buffer Register
SCIRXBUFB	0x7757	1	SCI-B Receive Data Buffer Register
SCITXBUFB	0x7759	1	SCI-B Transmit Data Buffer Register
SCIFFTXB	0x775A	1	SCI-B FIFO Transmit Register
SCIFFRXB	0x775B	1	SCI-B FIFO Receive Register
SCIFFCTB	0x775C	1	SCI-B FIFO Control Register
SCIPRIB	0x775F	1	SCI-B Priority Control Register

† Shaded registers are new registers for the FIFO mode.
‡ Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Figure 4−13 shows the SCI module block diagram.

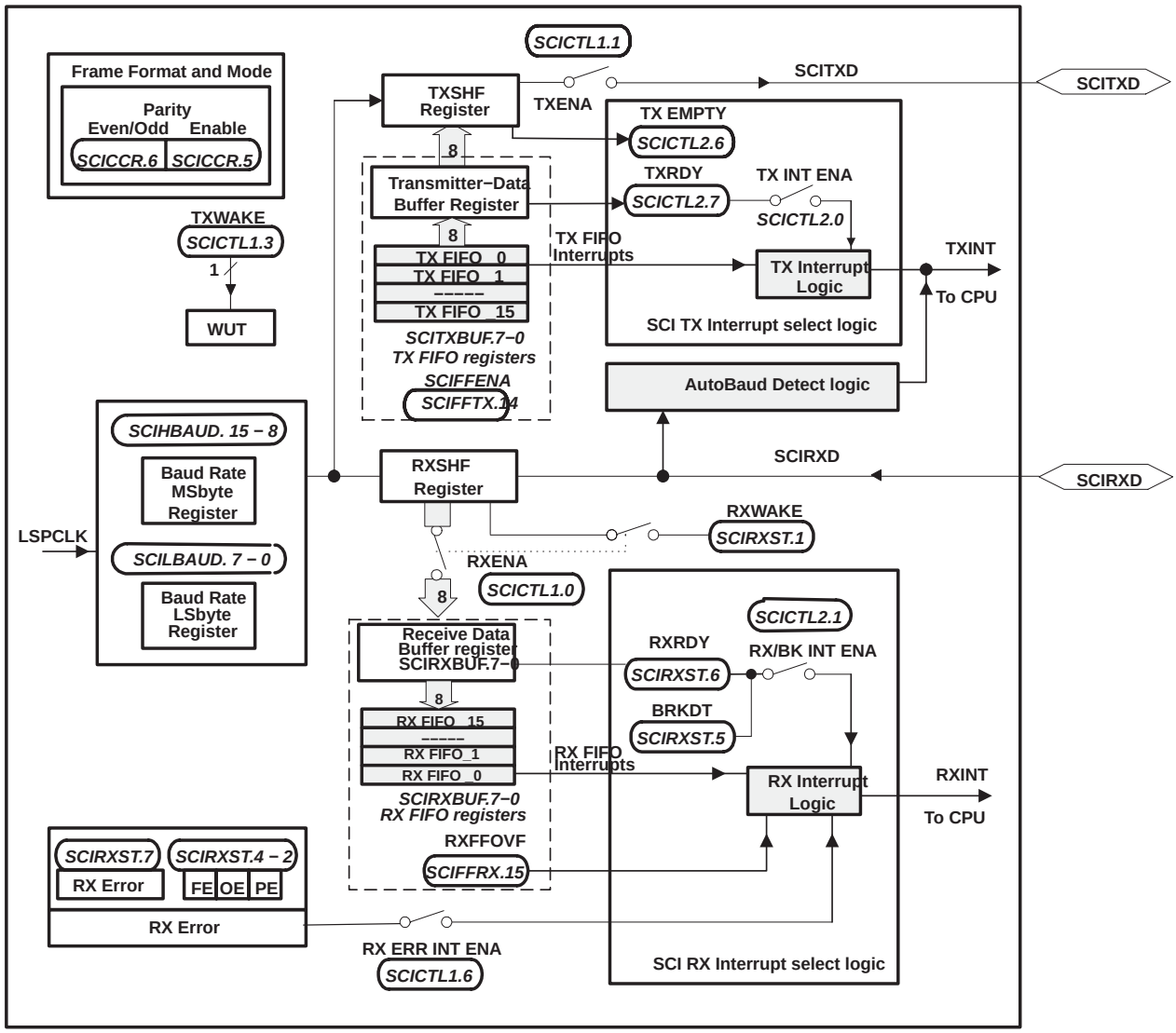


Figure 4−13. Serial Communications Interface (SCI) Module Block Diagram

PRODUCT PREVIEW

PRODUCT PREVIEW

4.8 Serial Peripheral Interface Modules (SPI-A, SPI-B, SPI-C, SPI-D)

The 280x devices include the four-pin serial peripheral interface (SPI) module. Up to four SPI modules (SPI-A, SPI-B, SPI-C, and SPI-D) are available. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the DSP controller and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
  - SPISOMI: SPI slave-output/master-input pin
  - SPISIMO: SPI slave-input/master-output pin
  - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
  - SPICLK: SPI serial-clock pin

NOTE: All four pins can be used as GPIO, if the SPI module is not used.

- Two operational modes: master and slave
- Baud rate: 125 different programmable rates
  - Baud rate $= \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)}$, when BRR $\neq 0$
    $= \frac{\text{LSPCLK}}{4}$, when BRR = 0, 1, 2, 3

    SPI performance is limited by I/O buffer switching speed. Internal prescalers must be adjusted such that the peripheral speed is less than the I/O buffer speed limit—20 MHz maximum.
- Data word length: one to sixteen data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: Located in control register frame beginning at address 7040h.

  NOTE: All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7−0), and the upper byte (15−8) is read as zeros. Writing to the upper byte has no effect.

Enhanced feature:

- 16-level transmit/receive FIFO
- Delayed transmit control

The SPI port operation is configured and controlled by the registers listed in Table 4−10.

Table 4−10. SPI-A Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
SPICCR	0x7040	1	SPI-A Configuration Control Register
SPICTL	0x7041	1	SPI-A Operation Control Register
SPISTS	0x7042	1	SPI-A Status Register
SPIBRR	0x7044	1	SPI-A Baud Rate Register
SPIRXEMU	0x7046	1	SPI-A Receive Emulation Buffer Register
SPIRXBUF	0x7047	1	SPI-A Serial Input Buffer Register
SPITXBUF	0x7048	1	SPI-A Serial Output Buffer Register
SPIDAT	0x7049	1	SPI-A Serial Data Register
SPIFFTX	0x704A	1	SPI-A FIFO Transmit Register
SPIFFRX	0x704B	1	SPI-A FIFO Receive Register
SPIFFCT	0x704C	1	SPI-A FIFO Control Register
SPIPRI	0x704F	1	SPI-A Priority Control Register

NOTE: Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Table 4−11. SPI-B Registers

NAME	ADDRESS RANGE	SIZE (X16)	DESCRIPTION
SPICCR	0x7740	1	SPI-B Configuration Control Register
SPICTL	0x7741	1	SPI-B Operation Control Register
SPISTS	0x7742	1	SPI-B Status Register
SPIBRR	0x7744	1	SPI-B Baud Rate Register
SPIEMU	0x7746	1	SPI-B Emulation Buffer Register
SPIRXBUF	0x7747	1	SPI-B Serial Input Buffer Register
SPITXBUF	0x7748	1	SPI-B Serial Output Buffer Register
SPIDAT	0x7749	1	SPI-B Serial Data Register
SPIFFTX	0x774A	1	SPI-B FIFO Transmit Register
SPIFFRX	0x774B	1	SPI-B FIFO Receive Register
SPIFFCT	0x774C	1	SPI-B FIFO Control Register
SPIPRI	0x774F	1	SPI-B Priority Control Register

NOTE: Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

PRODUCT PREVIEW

Table 4−12. SPI-C Registers

NAME	ADDRESS RANGE	SIZE (X16)	DESCRIPTION
SPICCR	0x7760	1	SPI−C Configuration Control Register
SPICTL	0x7761	1	SPI−C Operation Control Register
SPISTS	0x7762	1	SPI−C Status Register
SPIBRR	0x7764	1	SPI−C Baud Rate Register
SPIRXEMU	0x7766	1	SPI−C Emulation Buffer Register
SPIRXBUF	0x7767	1	SPI−C Serial Input Buffer Register
SPITXBUF	0x7768	1	SPI−C Serial Output Buffer Register
SPIDAT	0x7769	1	SPI−C Serial Data Register
SPIFFTX	0x776A	1	SPI−C FIFO Transmit Register
SPIFFRX	0x776B	1	SPI−C FIFO Receive Register
SPIFFCT	0x776C	1	SPI−C FIFO Control Register
SPIPRI	0x776F	1	SPI−C Priority Control Register

NOTE: Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

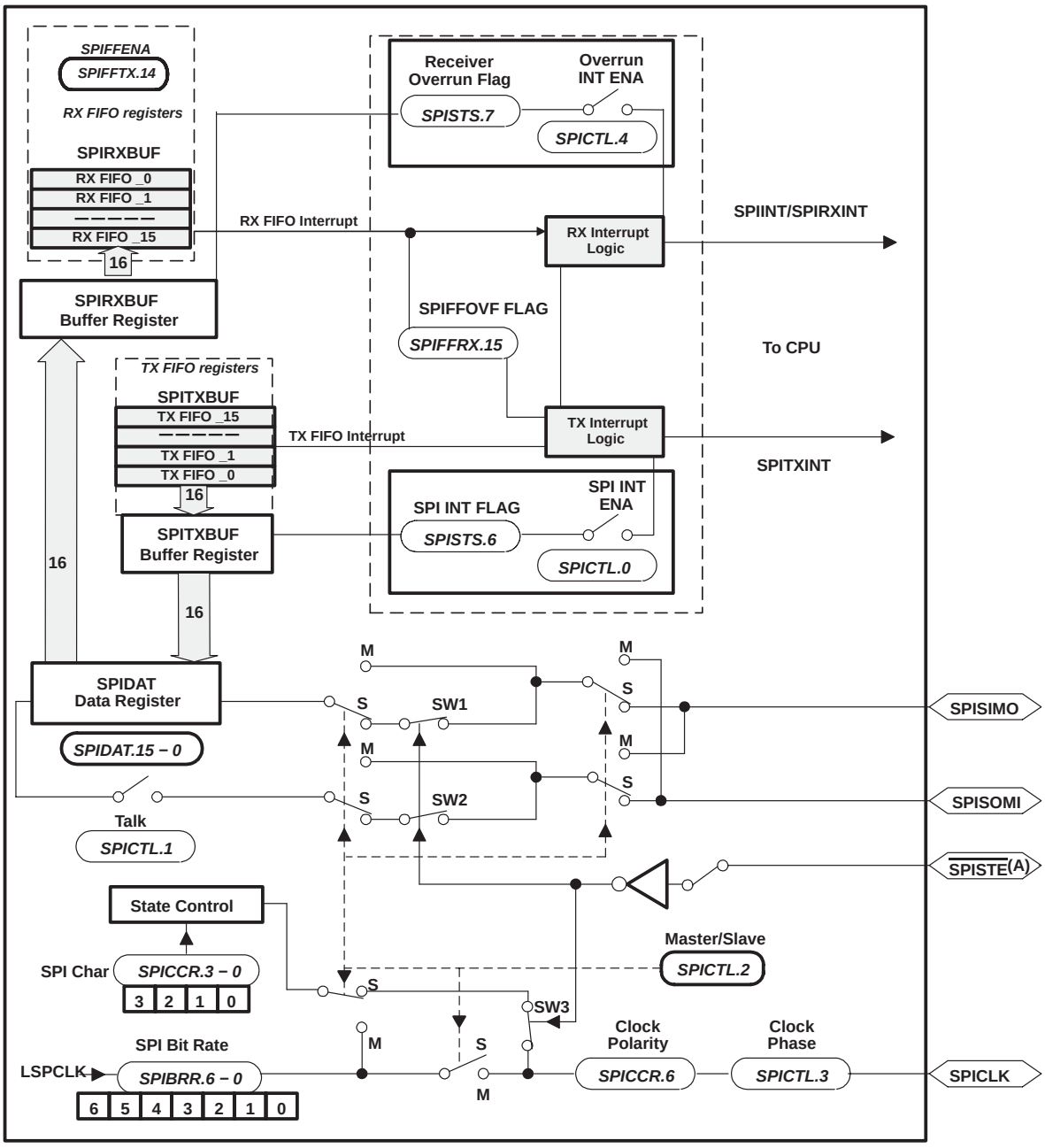
Table 4−13. SPI-D Registers

NAME	ADDRESS RANGE	SIZE (X16)	DESCRIPTION
SPICCR	0x7780	1	SPI−D Configuration Control Register
SPICTL	0x7781	1	SPI−D Operation Control Register
SPISTS	0x7782	1	SPI−D Status Register
SPIBRR	0x7784	1	SPI−D Baud Rate Register
SPIRXEMU	0x7786	1	SPI−D Emulation Buffer Register
SPIRXBUF	0x7787	1	SPI−D Serial Input Buffer Register
SPITXBUF	0x7788	1	SPI−D Serial Output Buffer Register
SPIDAT	0x7789	1	SPI−D Serial Data Register
SPIFFTX	0x778A	1	SPI−D FIFO Transmit Register
SPIFFRX	0x778B	1	SPI−D FIFO Receive Register
SPIFFCT	0x778C	1	SPI−D FIFO Control Register
SPIPRI	0x778F	1	SPI−D Priority Control Register

NOTE: Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

PRODUCT PREVIEW

Figure 4−14 is a block diagram of the SPI in slave mode.



(A) $\overline{\text{SPISTE}}$ is driven low by the master for a slave device.

Figure 4−14. Serial Peripheral Interface Module Block Diagram (Slave Mode)

PRODUCT PREVIEW

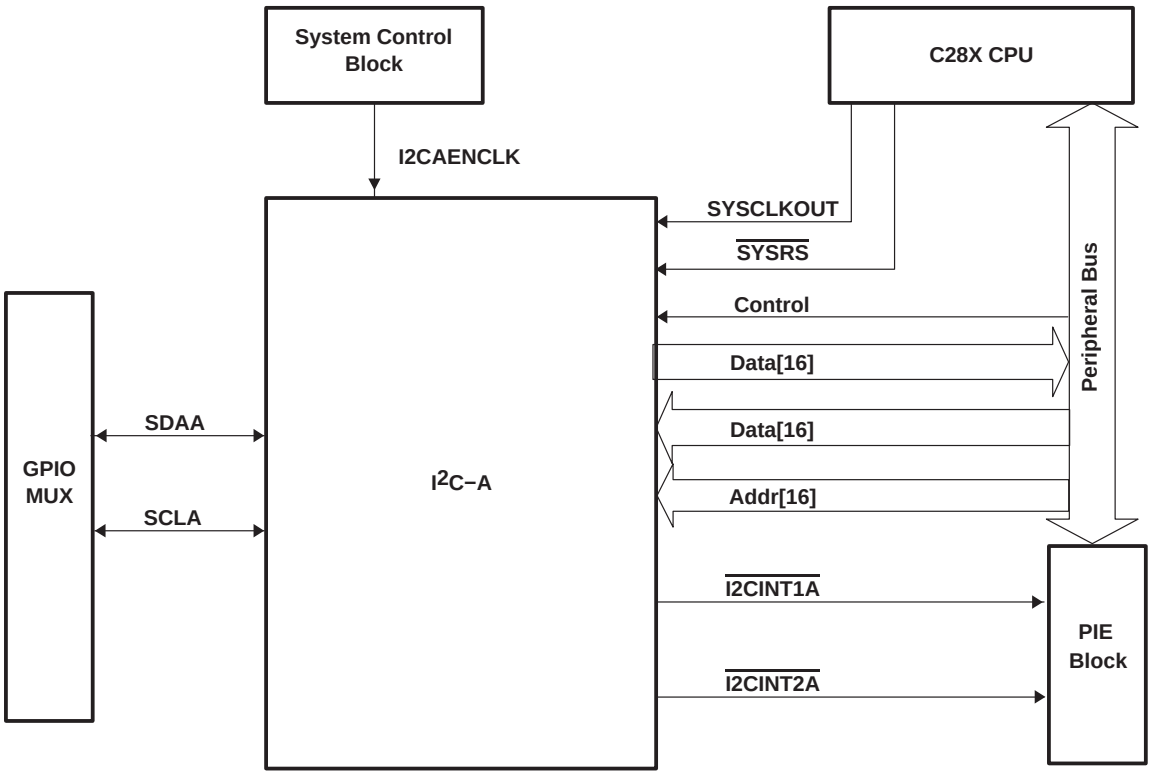
4.9 Inter-Integrated Circuit (I^2C)

The 280x device contains one I^2C Serial Port. Figure 4−15 shows how the I^2C peripheral module interfaces within the 280x device.

The I^2C module has the following features:

- Compliance with the Philips Semiconductors I^2C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (Philips Fast-mode rate)
- One 16-bit receive FIFO and one 16-bit transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgement received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode

PRODUCT PREVIEW



NOTES: A. The I2C registers are accessed at the SYSCLKOUT rate. The internal timing, and signal waveforms of the I2C port, is also at the SYSCLKOUT rate.
B. The clock enable bit (I2CAENCLK) in the PCLKCRO register turns off the clock to the I2C port for low power operation. Upon reset, I2CAENCLK is clear, which indicates the peripheral internal clocks are off.

Figure 4−15. I2C Peripheral Module Interfaces

The I2C port operation is configured and controlled by the registers in Table 4−14.

Table 4−14. I2C−A Registers

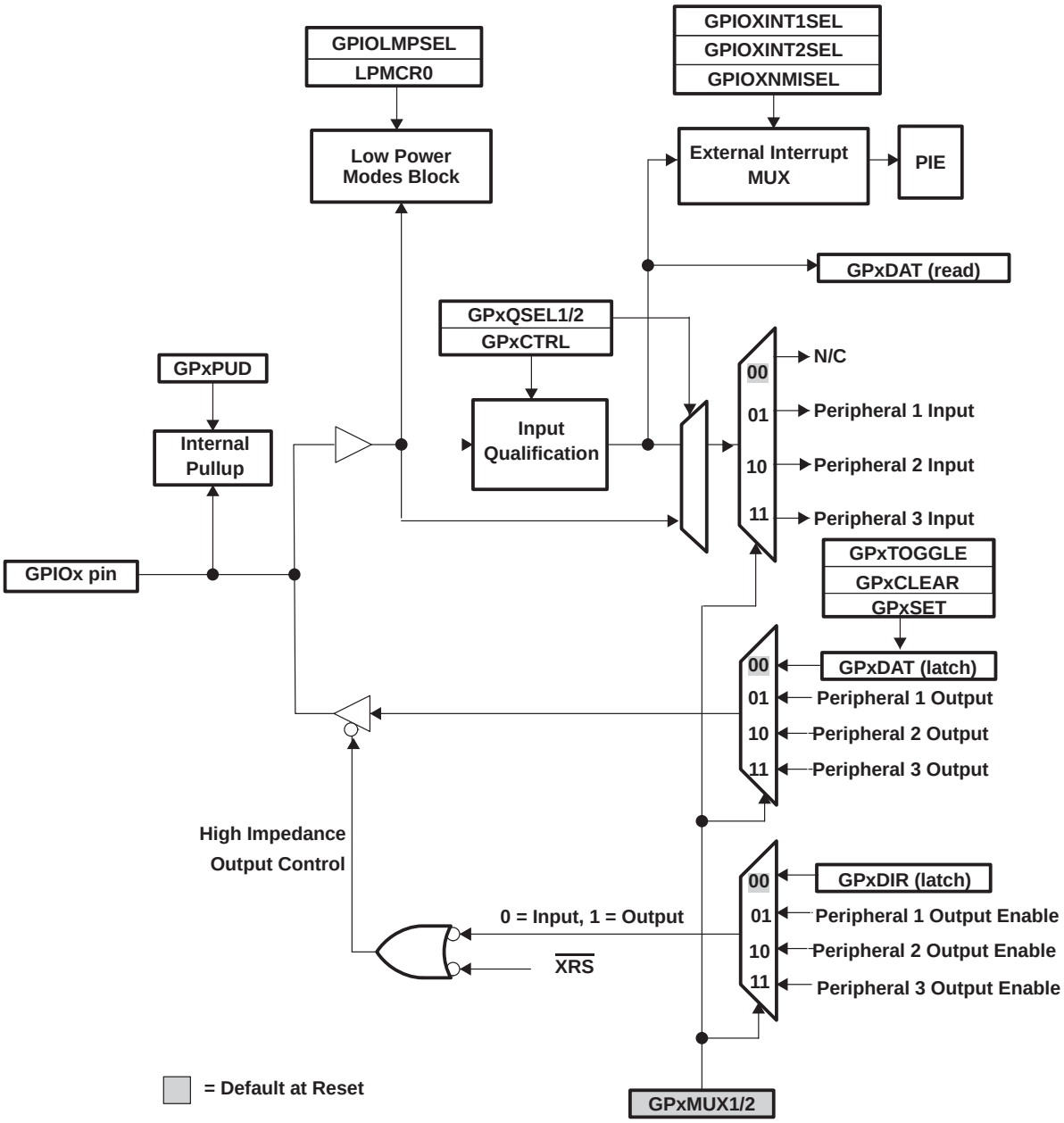
NAME	ADDRESS	DESCRIPTION
I2COAR	0x7900	I2C own address register
I2CIER	0x7901	I2C interrupt enable register
I2CSTR	0x7902	I2C status register
I2CCLKL	0x7903	I2C clock low-time divider register
I2CCLKH	0x7904	I2C clock high-time divider register
I2CCNT	0x7905	I2C data count register
I2CDRR	0x7906	I2C data receive register
I2CSAR	0x7907	I2C slave address register
I2CDXR	0x7908	I2C data transmit register
I2CMDR	0x7909	I2C mode register
I2CISRC	0x790A	I2C interrupt source register
I2CPSC	0x790C	I2C prescaler register
I2CFFTX	0x7920	I2C FIFO transmit register
I2CFFRX	0x7921	I2C FIFO receive register
I2CRSR	−	I2C receive shift register (not accessible to the CPU)
I2CXSR	−	I2C transmit shift register (not accessible to the CPU)

PRODUCT PREVIEW

PRODUCT PREVIEW

4.10 GPIO MUX

On the 280x, the GPIO MUX can multiplex up to three independent peripheral signals on a single GPIO pin in addition to providing individual pin bit-banging IO capability. The GPIO MUX block diagram per pin is shown in Figure 4−16. Because of the open drain capabilities of the I^2C pins, the GPIO MUX block diagram for these pins differ. See the *TMS320x280x System Control and Interrupts Reference Guide* (literature number SPRU712) for details.



x stands for the port, either A or B. For example, GPxDIR refers to either the GPADIR and GPBDIR register depending on the particular GPIO pin selected

GPxDAT latch/read are accessed at the same memory location.

Figure 4−16. GPIO MUX Block Diagram

The 280x supports 34 GPIO pins. The GPIO control and data registers are mapped to Peripheral Frame 1 to enable 32-bit operations on the registers (along with 16-bit operations). Table 4−15 shows the GPIO register mapping.

Table 4−15. GPIO Registers

NAME	ADDRESS	SIZE (X16)	Register Description
GPIO CONTROL REGISTERS (EALLOW PROTECTED)			
GPACTRL	0x6F80	2	GPIO A Control Register (GPIO0 to 31)
GPAQSEL1	0x6F82	2	GPIO A Qualifier Select 1 Register (GPIO0 to 15)
GPAQSEL2	0x6F84	2	GPIO A Qualifier Select 2 Register (GPIO16 to 31)
GPAMUX1	0x6F86	2	GPIO A MUX 1 Register (GPIO0 to 15)
GPAMUX2	0x6F88	2	GPIO A MUX 2 Register (GPIO16 to 31)
GPADIR	0x6F8A	2	GPIO A Direction Register (GPIO0 to 31)
GPAPUD	0x6F8C	2	GPIO A Pull Up Disable Register (GPIO0 to 31)
reserved	0x6F8E 0x6F8F	2	
GPBCTRL	0x6F90	2	GPIO B Control Register (GPIO32 to 35)
GPBQSEL1	0x6F92	2	GPIO B Qualifier Select 1 Register (GPIO32 to 35)
GPBQSEL2	0x6F94	2	reserved
GPBMUX1	0x6F96	2	GPIO B MUX 1 Register (GPIO32 to 35)
GPBMUX2	0x6F98	2	reserved
GPBDIR	0x6F9A	2	GPIO B Direction Register (GPIO32 to 35)
GPBPUD	0x6F9C	2	GPIO B Pull Up Disable Register (GPIO32 to 35)
reserved	0x6F9E 0x6F9F	2	
reserved	0x6FA0 0x6FBF	32	
GPIO DATA REGISTERS (NOT EALLOW PROTECTED)			
GPADAT	0x6FC0	2	GPIO Data Register (GPIO0 to 31)
GPASET	0x6FC2	2	GPIO Data Set Register (GPIO0 to 31)
GPACLEAR	0x6FC4	2	GPIO Data Clear Register (GPIO0 to 31)
GPATOGGLE	0x6FC6	2	GPIO Data Toggle Register (GPIO0 to 31)
GPBDAT	0x6FC8	2	GPIO Data Register (GPIO32 to 35)
GPBSET	0x6FCA	2	GPIO Data Set Register (GPIO32 to 35)
GPBCLEAR	0x6FCC	2	GPIO Data Clear Register (GPIO32 to 35)
GPBTOGGLE	0x6FCE	2	GPIO Data Toggle Register (GPIO32 to 35)
reserved	0x6FD0 0x6FDF	16	
GPIO INTERRUPT AND LOW POWER MODES SELECT REGISTERS (EALLOW PROTECTED)			
GPIOXINT1SEL	0x6FE0	1	XINT1 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT2SEL	0x6FE1	1	XINT2 GPIO Input Select Register (GPIO0 to 31)
GPIOXNMISEL	0x6FE2	1	XNMI GPIO Input Select Register (GPIO0 to 31)
reserved	0x6FE3 0x6FE7	5	
GPIOLPMSEL	0x6FE8	2	LPM GPIO Select Register (GPIO0 to 31)
reserved	0x6FEA 0x6FFF	22	

PRODUCT PREVIEW

The user can select the type of input qualification for each GPIO pin via the GPxQSEL1/2 registers from four choices:

- Synchronization To SYSCLKOUT Only (GPxQSEL1/2=0,0): This is the default mode of all GPIO pins at reset and it simply synchronizes the input signal to the system clock (SYSCLKOUT).
- Qualification Using Sampling Window (GPxQSEL1/2=0,1 and 1,0): In this mode the input signal, after synchronization to the system clock (SYSCLKOUT), is qualified by a specified number of cycles before the input is allowed to change.

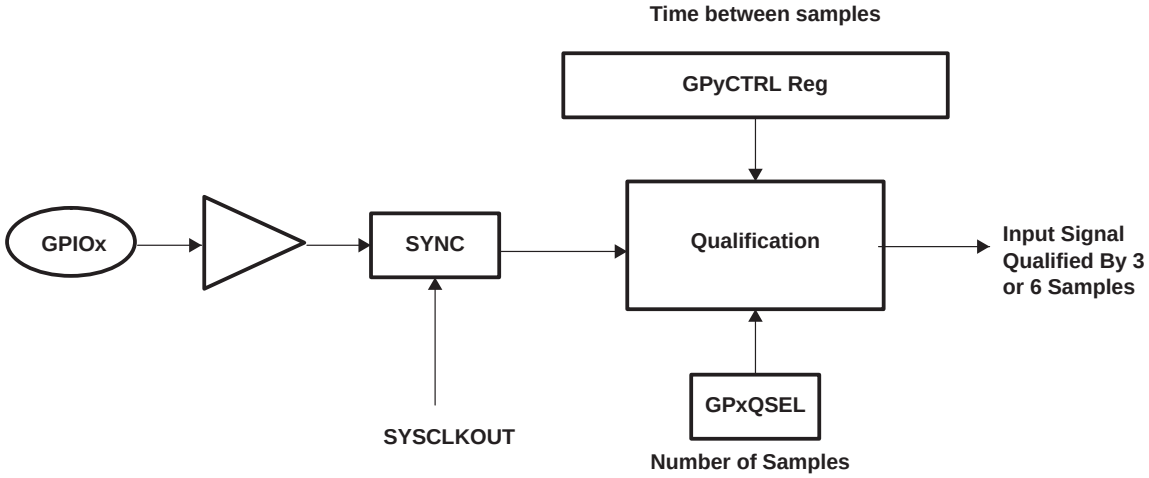
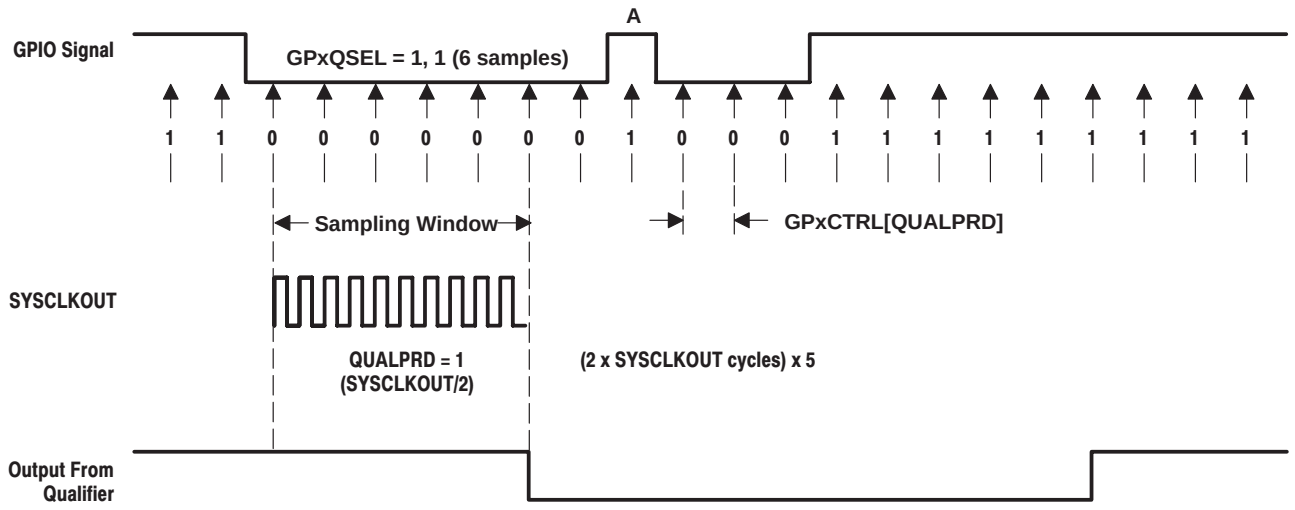


Figure 4−17. Qualification Using Sampling Window

- The sampling period is specified by the QUALPRD bits in the GPxCTRL register and is configurable in groups of 8 signals. It specifies a multiple of SYSCLKOUT cycles for sampling the input signal. The sampling window is either 3-samples or 6-samples wide and the output is only changed when ALL samples are the same (all 0s or all 1s) as shown in Figure 4−18 (for 6 sample mode).

PRODUCT PREVIEW



NOTES: A. The qualification block generates both the 3 and 6 sample signals. A MUX is then used to select which sample mode is used.
B. The qualification period selected via the GPxCTRL register applies to groups of 8 GPIO pins.

Figure 4−18. Sampling Mode

- No Synchronization (GPxQSEL1/2=1,1): This mode is used for peripherals where synchronization is not required (synchronization is performed within the peripheral).

Due to the multi-level multiplexing that is required on the 280x device, there may be cases where a peripheral input signal can be mapped to more then one GPIO pin. Also, when an input signal is not selected, the input signal will default to either a 0 or 1 state, depending on the peripheral.

PRODUCT PREVIEW

5 Device Support

Texas Instruments (TI) offers an extensive line of development tools for the C28x™ generation of DSPs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of 280x-based applications:

Software Development Tools

- Code Composer Studio™ Integrated Development Environment (IDE)
  - C/C++ Compiler
  - Code generation tools
  - Assembler/Linker
  - Cycle Accurate Simulator
- Application algorithms
- Sample applications code

Hardware Development Tools

- 2808 eZdsp
- JTAG-based emulators − SPI515, XDS510PP, XDS510PP Plus, XDS510 USB
- Universal 5-V dc power supply
- Documentation and cables

PRODUCT PREVIEW

5.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP devices and support tools. Each TMS320™ DSP commercial family member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TMS320 is a trademark of Texas Instruments.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PBK) and temperature range (for example, A). Figure 5−1 provides a legend for reading the complete device name for any TMS320x280x family member.

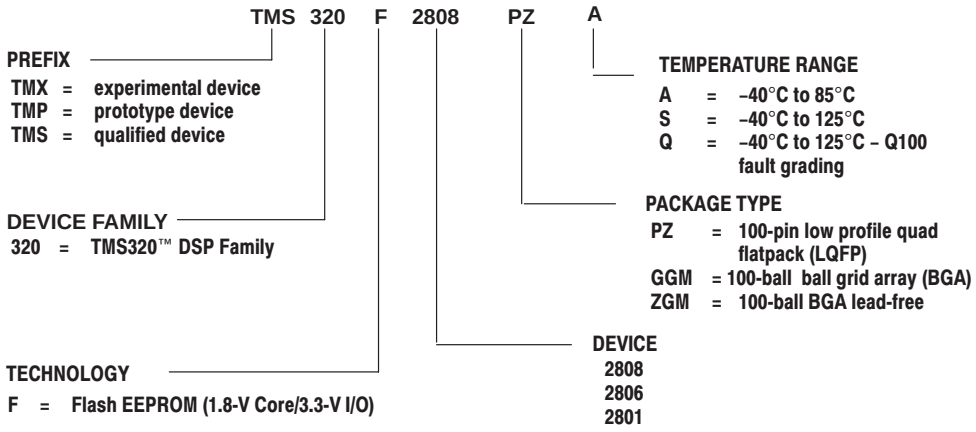


Figure 5−1. TMS320x28x Device Nomenclature

5.2 Documentation Support

Extensive documentation supports all of the TMS320™ DSP family generations of devices from product announcement through applications development. The types of documentation available include: data sheets and data manuals, with design specifications; and hardware and software applications. Useful reference documentation includes:

TMS320C28x DSP CPU and Instruction Set Reference Guide (literature number SPRU430) describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x™ fixed-point digital signal processors (DSPs). It also describes emulation features available on these DSPs.

TMS320x280x Analog-to-Digital Converter (ADC) Reference Guide (literature number SPRU716) describes the ADC module. The module is a 12−bit pipelined ADC. The analog circuits of this converter, referred to as the core in this document, include the front-end analog multiplexers (MUXs), sample−and−hold (S/H) circuits, the conversion core, voltage regulators, and other analog supporting circuits. Digital circuits, referred to as the wrapper in this document, include programmable conversion sequencer, result registers, interface to analog circuits, interface to device peripheral bus, and interface to other on-chip modules.

TMS320x280x Boot ROM Reference Guide (literature number SPRU722) describes the purpose and features of the bootloader (factory-programmed boot-loading software). It also describes other contents of the device on-chip boot ROM and identifies where all of the information is located within that memory.

TMS320x280x Enhanced Capture (eCAP) Module Reference Guide (literature number SPRU807) describes the enhanced Capture Module. It includes the module description and registers.

TMS320x281x, 280x Enhanced Controller Area Network (eCAN) Reference Guide (literature number SPRU074) describes the eCAN that uses established protocol to communicate serially with other controllers in electrically noisy environments. With 32 fully configurable mailboxes and time-stamping feature, the eCAN module provides a versatile and robust serial communication interface. The eCAN module implemented in the C28x DSP is compatible with the CAN 2.0B standard (active).

TMS320x280x Enhanced Quadrature Encoder Pulse (eQEP) Reference Guide (literature number SPRU790) describes the eQEP module, which is used for interfacing with a linear or rotary incremental encoder to get position, direction, and speed information from a rotating machine in high performance motion and position control systems. It includes the module description and registers.

PRODUCT PREVIEW

TMS320x280x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide (literature number SPRU791). The PWM peripheral is an essential part of controlling many of the power related systems found in both commercial and industrial equipments. This guide describes the main areas that include digital motor control, switch mode power supply control, UPS (uninterruptable power supplies), and other forms of power conversion. The PWM peripheral can be considered as performing a DAC function, where the duty cycle is equivalent to a DAC analog value, it is sometimes referred to as a Power DAC.

TMS320x280x Inter-Integrated Circuit (I^2C) Reference Guide (literature number SPRU721) describes the features and operation of the inter-integrated circuit (I^2C) module that is available on the TMS320x280x digital signal processor (DSP). The I^2C module provides an interface between one of these DSPs and devices compliant with Philips Semiconductors Inter-IC bus (I^2C-bus) specification version 2.1 and connected by way of an I^2C-bus.

TMS320x281x, 280x Serial Communication Interface (SCI) Reference Guide (literature number SPRU051) describes the SCI that is a two-wire asynchronous serial port, commonly known as a UART. The SCI modules support digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format.

TMS320x281x, 280x Serial Peripheral Interface (SPI) Reference Guide (literature number SPRU059) describes the SPI − a high-speed synchronous serial input/output (I/O) port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmed bit−transfer rate. The SPI is used for communications between the DSP controller and external peripherals or another controller.

TMS320x280x System Control and Interrupts Reference Guide (literature number SPRU712) describes the various interrupts and system control features of the 280x digital signal processors (DSPs).

TMS320x281x, 280x Peripheral Reference Guide (literature number SPRU566) describes the peripheral reference guides of the 28x digital signal processors (DSPs).

3.3 V DSP for Digital Motor Control Application Report (literature number SPRA550). New generations of motor control digital signal processors (DSPs) lower their supply voltages from 5 V to 3.3 V to offer higher performance at lower cost. Replacing traditional 5-V digital control circuitry by 3.3-V designs introduce no additional system cost and no significant complication in interfacing with TTL and CMOS compatible components, as well as with mixed voltage ICs such as power transistor gate drivers. Just like 5-V based designs, good engineering practice should be exercised to minimize noise and EMI effects by proper component layout and PCB design when 3.3-V DSP, ADC, and digital circuitry are used in a mixed signal environment, with high and low voltage analog and switching signals, such as a motor control system. In addition, software techniques such as Random PWM method can be used by special features of the Texas Instruments (TI) TMS320x24xx DSP controllers to significantly reduce noise effects caused by EMI radiation.

This application report reviews designs of 3.3-V DSP versus 5-V DSP for low HP motor control applications. The application report first describes a scenario of a 3.3-V-only motor controller indicating that for most applications, no significant issue of interfacing between 3.3 V and 5 V exists. Cost-effective 3.3-V − 5-V interfacing techniques are then discussed for the situations where such interfacing is needed. On-chip 3.3-V ADC versus 5-V ADC is also discussed. Sensitivity and noise effects in 3.3-V and 5-V ADC conversions are addressed. Guidelines for component layout and printed circuit board (PCB) design that can reduce system's noise and EMI effects are summarized in the last section.

The TMS320C28x Instruction Set Simulator Technical Overview (literature number SPRU608) describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x core.

TMS320C28x DSP/BIOS Application Programming Interface (API) Reference Guide (literature number SPRU625) describes development using DSP/BIOS.

TMS320C28x Assembly Language Tools User's Guide (literature number SPRU513) describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x™ device.

PRODUCT PREVIEW

TMS320C28x Optimizing C Compiler User's Guide (literature number SPRU514) describes the TMS320C28x™ C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320™ DSP assembly language source code for the TMS320C28x device.

A series of DSP textbooks is published by Prentice-Hall and John Wiley and Sons to support digital signal processing research and education. The TMS320™ DSP newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320™ DSP customers on product information.

Updated information on the TMS320™ DSP controllers can be found on the worldwide web at: **http://www.ti.com**.

To send comments regarding this TMS320F280x data manual (literature number SPRS230), use the *comments@books.sc.ti.com* email address, which is a repository for feedback. For questions and support, contact the Product Information Center listed at the **http://www.ti.com/sc/docs/pic/home.htm** site.

PRODUCT PREVIEW

6 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the TMS320F280x DSPs.

6.1 Absolute Maximum Ratings

Unless otherwise noted, the list of absolute maximum ratings are specified over operating temperature ranges. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 6.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to V_{SS}.

Supply voltage range, V_{DDIO}, V_{DDA2}, V_{DDAIO} . . . . . − 0.3 V to 4.6 V
Supply voltage range, V_{DD}, V_{DD1A18}, V_{DD2A18}, ... − 0.5 V to 2.5 V
V_{DD3VFL} range . . . . . − 0.3 V to 4.6 V
Input voltage range, V_{IN} . . . . . − 0.3 V to 4.6 V
Output voltage range, V_O . . . . . − 0.3 V to 4.6 V
Input clamp current, I_{IK} (V_{IN} < 0 or V_{IN} > V_{DDIO})† . . . . . ± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDIO}) . . . . . ± 20 mA
Operating ambient temperature ranges, T_A: A version (GGM, PZ)‡ . . . . . − 40°C to 85°C
T_A: S version (GGM, PZ)‡§ . . . . . − 40°C to 125°C
T_A: Q version (GGM, PZ)‡ . . . . . − 40°C to 125°C
Storage temperature range, T_{stg}† . . . . . − 65°C to 150°C

† Continuous clamp current per pin is± 2 mA
‡ Long-term high-temperature storage and/or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *IC Package Thermal Metrics Application Report* (literature number SPRA953) and *Reliability Data for TMS320LF24x and TMS320F281x Devices Application Repor*t (literature number SPRA963).

PRODUCT PREVIEW

6.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DDIO}	Device supply voltage, I/O		3.14	3.3	3.47	V
V_{DD}	Device supply voltage, CPU	1.8 V	1.71	1.8	1.89	V
V_{SS}	Supply ground			0		V
V_{DDA2}, V_{DDAIO}	ADC supply voltage (3.3 V)		3.14	3.3	3.47	V
V_{DD1A18}, V_{DD2A18}	ADC supply voltage (1.8 V)		1.71	1.8	1.89	V
V_{DD3VFL}	Flash programming supply voltage		3.14	3.3	3.47	V
$f_{SYSCLKOUT}$	Device clock frequency (system clock)	V_{DD} = 1.8 V ± 5%	2		100	MHz
V_{IH}	High-level input voltage		2		V_{DDIO}	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output source current, V_{OH} = 2.4 V	All I/Os except Group 2			− 4	mA
		Group 2†			− 8	
I_{OL}	Low-level output sink current, V_{OL} = V_{OL} MAX	All I/Os except Group 2			4	mA
		Group 2†			8	
T_A	Ambient temperature, A version		− 40		85	°C
	Ambient temperature, S version		− 40		125	°C

† Group 2 pins are as follows: GPIO28, GPIO29, GPIO30, GPIO31, TDO, XCLKOUT, EMU0, and EMU1.

6.3 Electrical Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = I_{OH}MAX		2.4			V
			I_{OH} = 50 µA		V_{DDIO} − 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL}MAX				0.4	V
I_{IL}	Input current (low level)	With pullup	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All I/Os (including $\overline{XRS}$)		−100		µA
		With pulldown	V_{DDIO} = 3.3 V, V_{IN} = 0 V				±2	
I_{IH}	Input current (high level)	With pullup	V_{DDIO} = 3.3 V, V_{IN} = V_{DD}				±2	µA
		With pulldown	V_{DDIO} = 3.3 V, V_{IN} = V_{DD}			50		
I_{OZ}	Output current, high-impedance state (off-state)		V_O = V_{DDIO} or 0 V				±2	µA
C_i	Input capacitance					2		pF
C_o	Output capacitance					3		pF

PRODUCT PREVIEW

7 Mechanical Data

The following mechanical package diagram(s) reflect the most current released mechanical data available for the designated device(s).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TMS320F2801GGMA	ACTIVE	BGA	GGM	100		None	Call TI	Call TI
TMS320F2801GGMQ	ACTIVE	BGA	GGM	100		None	Call TI	Call TI
TMS320F2801PZA	ACTIVE	LQFP	PZ	100		None	Call TI	Call TI
TMS320F2801PZQ	ACTIVE	LQFP	PZ	100		None	Call TI	Call TI
TMS320F2801ZGMA	ACTIVE	BGA MICROSTAR	ZGM	100		None	Call TI	Call TI
TMS320F2801ZGMQ	ACTIVE	BGA MICROSTAR	ZGM	100		None	Call TI	Call TI
TMS320F2806GGMA	ACTIVE	BGA	GGM	100		None	Call TI	Call TI
TMS320F2806GGMQ	ACTIVE	BGA	GGM	100		None	Call TI	Call TI
TMS320F2806PZA	ACTIVE	LQFP	PZ	100		None	Call TI	Call TI
TMS320F2806PZQ	ACTIVE	LQFP	PZ	100		None	Call TI	Call TI
TMS320F2806ZGMA	ACTIVE	BGA MICROSTAR	ZGM	100		None	Call TI	Call TI
TMS320F2806ZGMQ	ACTIVE	BGA MICROSTAR	ZGM	100		None	Call TI	Call TI
TMS320F2808GGMA	ACTIVE	BGA	GGM	100		None	Call TI	Call TI
TMS320F2808GGMQ	ACTIVE	BGA	GGM	100		None	Call TI	Call TI
TMS320F2808ZGMA	ACTIVE	BGA MICROSTAR	ZGM	100		None	Call TI	Call TI
TMS320F2808ZGMQ	ACTIVE	BGA MICROSTAR	ZGM	100		None	Call TI	Call TI
TMX320F2801GGMA	ACTIVE	BGA	GGM	100	1	None	Call TI	Call TI
TMX320F2801PZA	ACTIVE	LQFP	PZ	100	1	None	Call TI	Call TI
TMX320F2806GGMA	ACTIVE	BGA	GGM	100	1	None	Call TI	Call TI
TMX320F2806PZA	ACTIVE	LQFP	PZ	100	1	None	Call TI	Call TI
TMX320F2808GGMA	ACTIVE	BGA	GGM	100	1	None	Call TI	Call TI
TMX320F2808PZA	ACTIVE	LQFP	PZ	100	1	None	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens,

including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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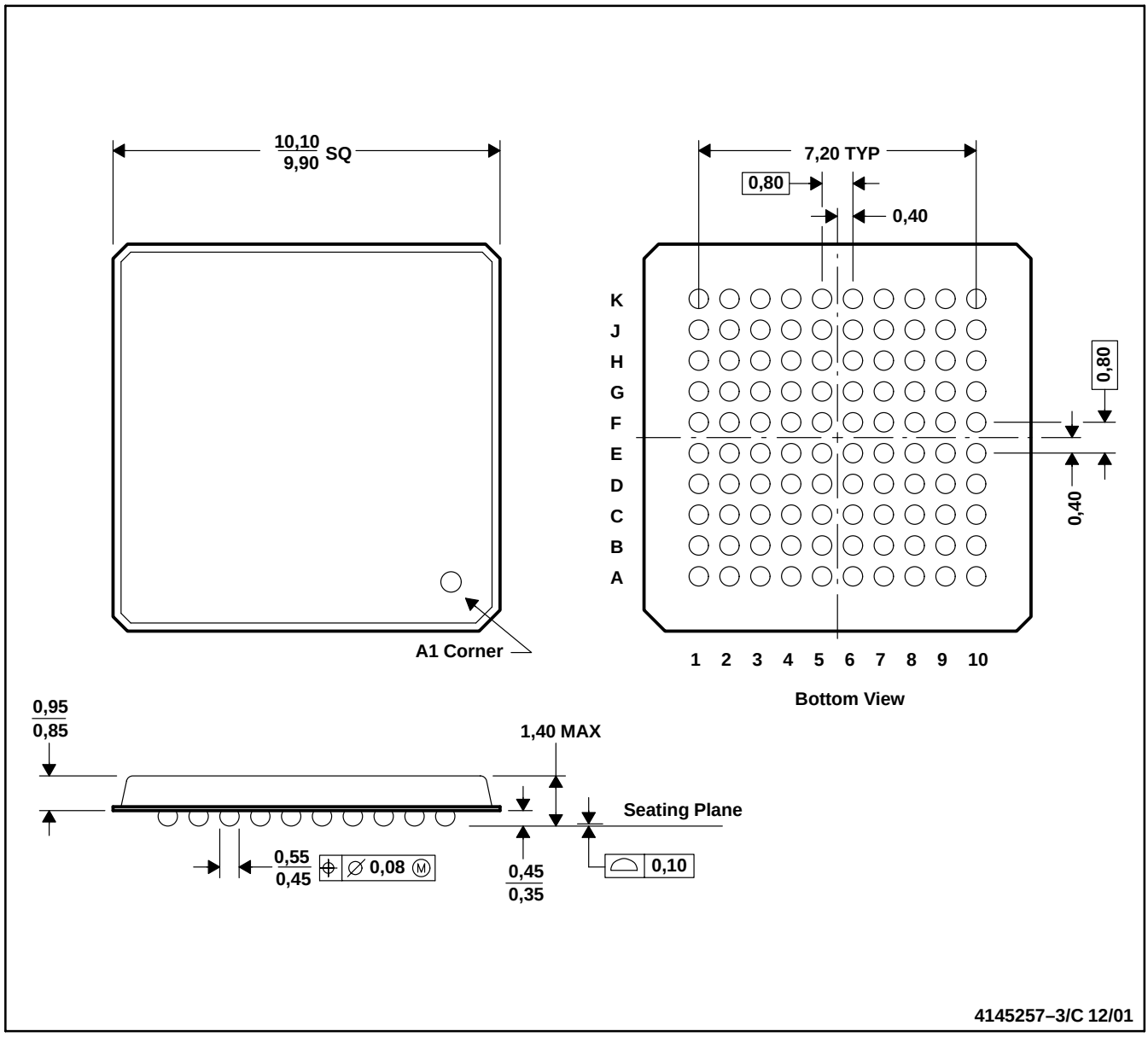
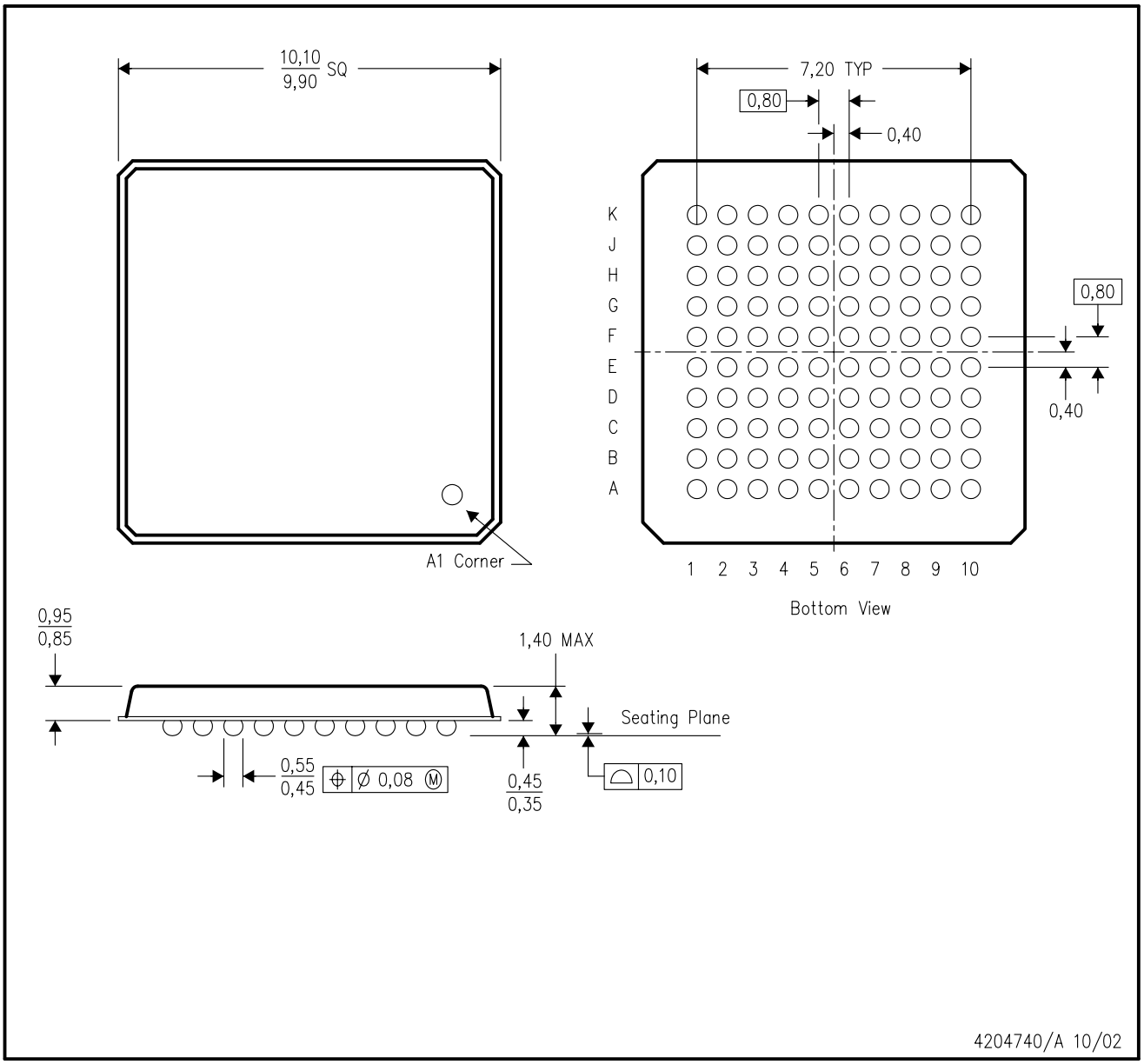
GGM (S–PBGA–N100) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice
C. MicroStar BGA configuration.

ZGM (S–PBGA–N100) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration.
D. This package is lead–free.

MicroStar BGA is a trademark of Texas Instruments.

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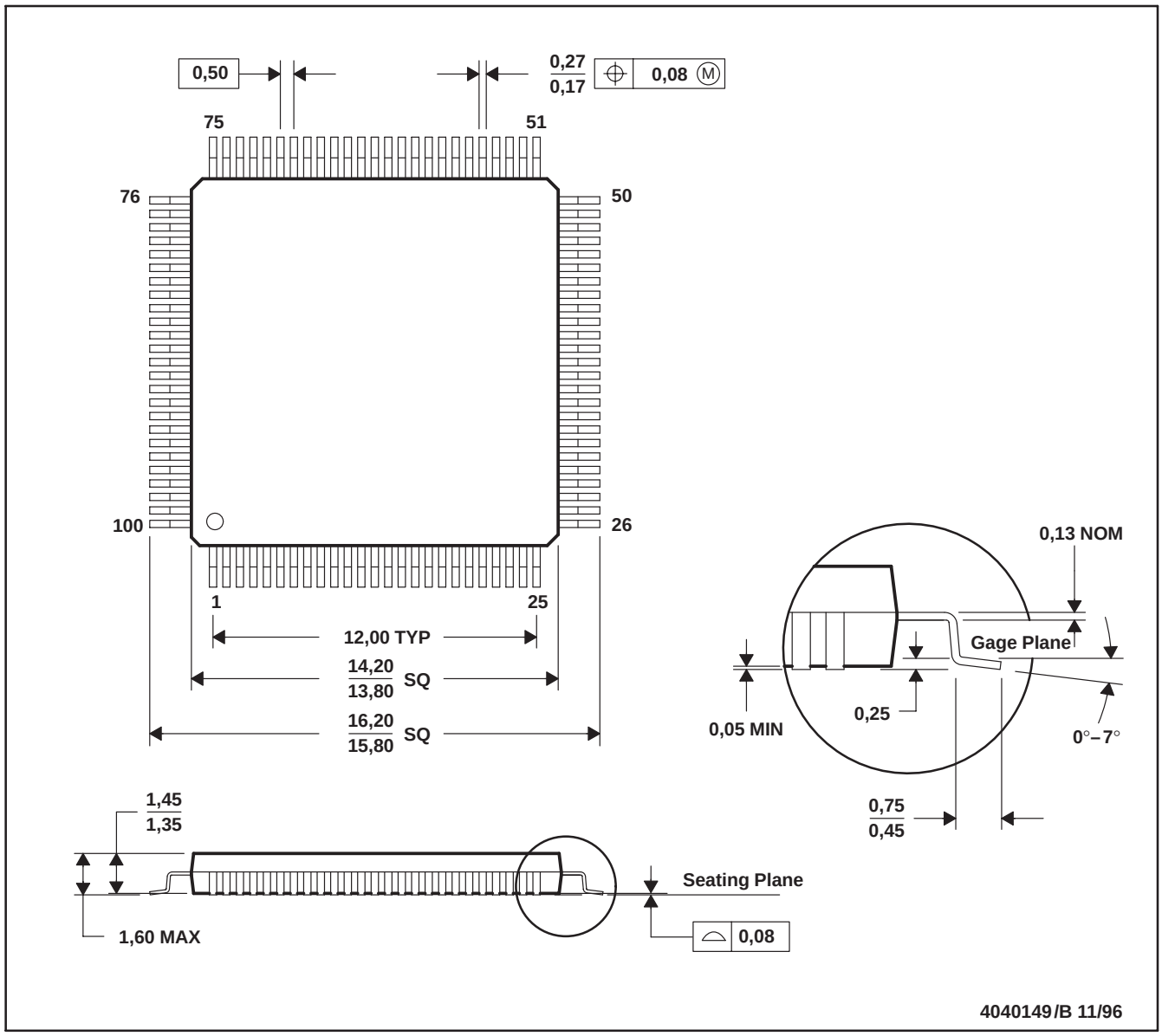
PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026