TPD4E002 Quad Low-Capacitance Array with ±15-kV ESD Protection

1 Features

- IEC 61000-4-2 ESD Protection
  - ±15-kV IEC 61000-4-2 Contact Discharge
- IEC 61000-4-5 Surge Protection
  - 2.5-A Peak Pulse Current (8/20-µs Pulse)
- ANSI/ESDA/JEDEC JS-001
  - ±15-kV Human Body Model (HBM)
- Four Unidirectional Voltage Suppression Diodes for use in ESD Protection
- I/O Breakdown Voltage, V_{BR} = 6.1 V (Minimum)
- I/O Capacitance 11 pF (Typical)
- Low Leakage Current < 100 nA
- Very Small Printed-Circuit Board (PCB) Area < 2.6 mm^2
- High Integration
- Suitable for High-Density Boards

2 Applications

- Computers
- Printers
- Communication Systems and Cellular Phones
- Video Equipment

3 Description

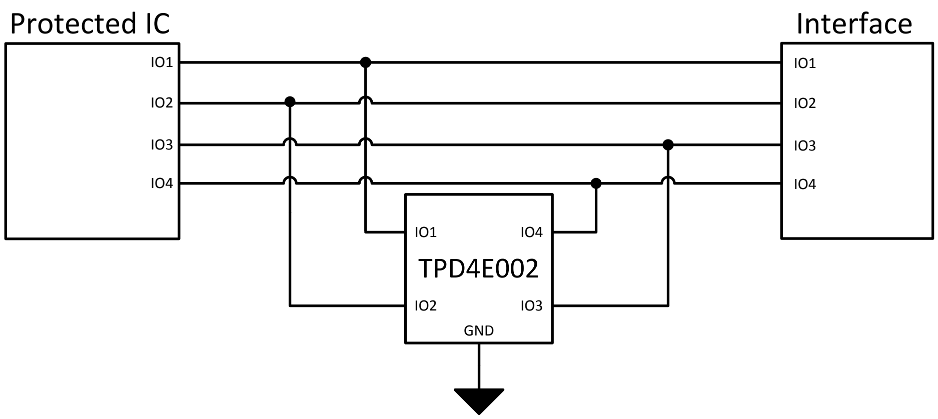
The TPD4E002 device is a transient voltage suppressor (TVS) designed to protect up to four lines against electrostatic discharge (ESD) transients. The monolithic circuit design allows superior capacitance matching between the channels and reduced crosstalk. This device is ideal for applications where both reduced line capacitance and board space-saving are required.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4E002	SOT (5)	1.60 mm × 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (February 2016) to Revision F — **Page**

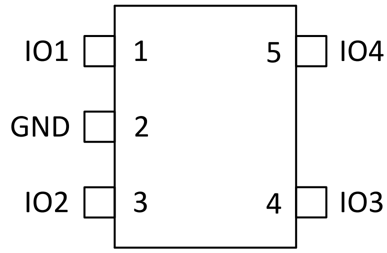
- Updated the *Pin Functions* table ... 3

Changes from Revision D (July 2010) to Revision E — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted Ordering Information table. See POA at the end of the document ... 1

5 Pin Configuration and Functions

DRL Package
5-Pin SOT
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	I/O1	I/O	ESD protection channel
2	GND	—	Ground
3	I/O2	I/O	ESD protection channel
4	I/O3	I/O	ESD protection channel
5	I/O4	I/O	ESD protection channel

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
T_J	Junction temperature		125	°C
T_{op}	Operating temperature	–40	125	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±15000	V
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]		
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]		

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
I_{pp}	Peak pulse current	IEC 61000-4-5 (tp = 8/20 µs)	2.5	A
P_{pp}	Peak pulse power	IEC 61000-4-5 (tp = 8/20 µs)	25	W

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Operating voltage	0	5	V
	Operating temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC[(1)]		TPD4E002 DRL (SOT) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

T_{amb} = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BR}	I/O breakdown voltage	I_R = 1 mA	6.1		7.2	V
I_{RM}	I/O leakage current	V_{RM} = 3 V			0.1	μA
αT	Voltage temperature coefficient			4.5		mV/°C
C	I/O capacitance per line			11		pF
R_d	Dynamic resistance (1)			2		Ω

(1) R_d is measured under reverse breakdown condition with inrush current in the range of 1 A using pulse techniques.

6.7 Typical Characteristics

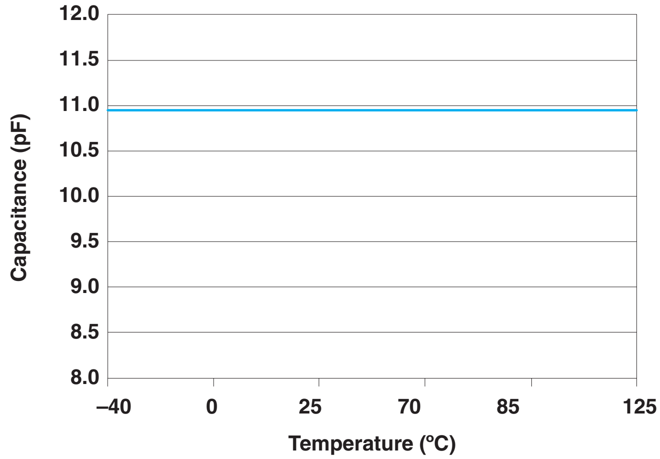


Figure 1. I/O Capacitance vs Temperature

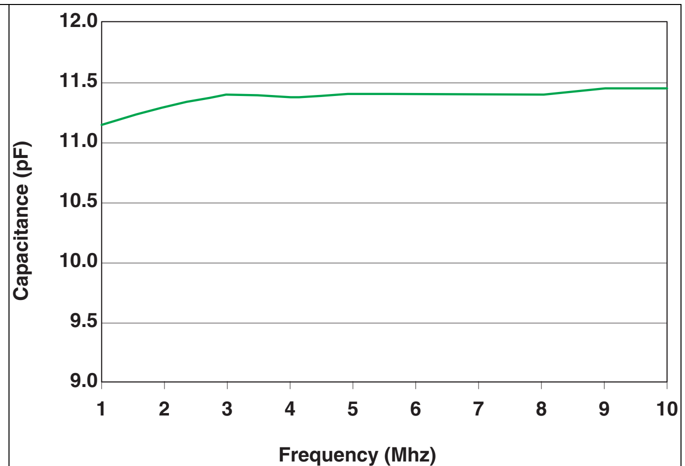


Figure 2. I/O Capacitance vs Frequency (Typical Values)

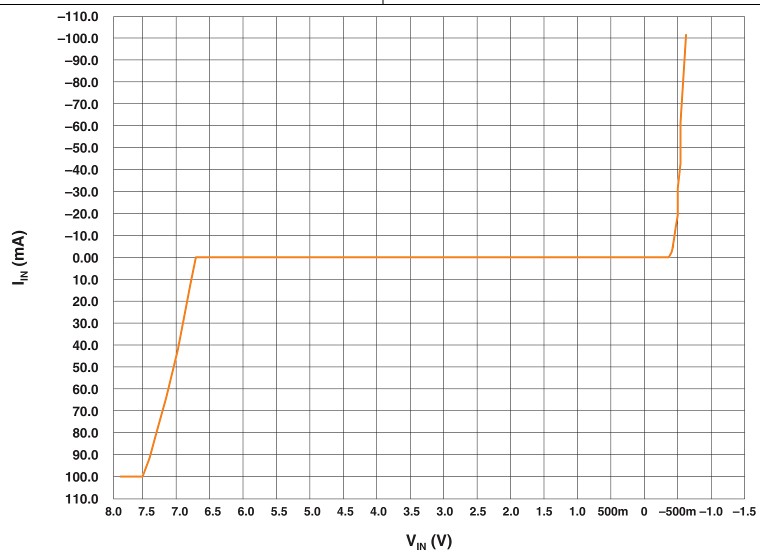


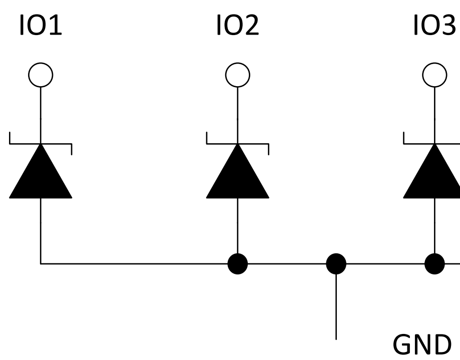
Figure 3. Diode Current Across I/O Voltage (Typical Values)

7 Detailed Description

7.1 Overview

The TPD4E002 is a four-channel TVS protection diode array. The TPD4E002 is rated to dissipate contact ESD strikes of ±15 kV, beyond Level 4 as specified in the IEC 61000-4-2 international standard. This device has an 11-pF I/O capacitance per channel, making it ideal for use in data I/O interfaces of up to 100 MHz.

7.2 Functional Block Diagram



7.3 Feature Description

The TPD4E002 is a TVS that provides ESD protection for up to four channels, withstanding up to ±15-kV contact ESD per IEC 61000-4-2 and 2.5-A peak pulse current per IEC 61000-4-5. The monolithic technology yields exceptionally small variations in capacitance between any I/O pin of the TPD4E002. The small footprint is ideal for applications where space-saving designs are important.

7.4 Device Functional Modes

The TPD4E002 device is a passive integrated circuit that triggers when voltages are above V_{BR} or below the diodes V_F of approximately –0.5 V. During ESD events, voltages as high as ±15-kV contact ESD can be directed to ground through the internal diodes. Once the voltages on the protected line fall below the trigger levels of TPD4E002 (usually within tens of nano seconds) the device reverts to its high-impedance state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4E002 device is a TVS diode array typically used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected integrated circuit (IC). The triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

In a typical design example, one TPD4E002 device is being used to protect an IC against potential ESD from a four-channel human interface port, as shown in Figure 4.

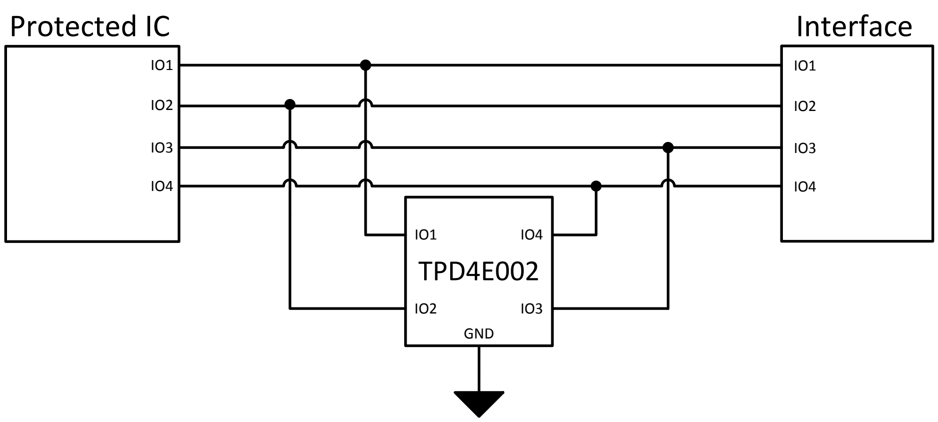


Figure 4. Typical Application for TPD4E002

8.2.1 Design Requirements

Table 1 lists the parameters for this typical application.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal's voltage range on I/O1, I/O2, I/O3, and I/O4	0 V to 5 V
Operating frequency	< 100 MHz

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer must know the following:

- Voltage range of the signal on all protected lines
- Operating frequency on all protected lines

8.2.2.1 Signal Range on I/O1 Through I/O2

The TPD4E002 device has 4 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the four I/O channels will protect which signal lines. Any I/O supports a signal range of 0 V to 5 V and up to 100 MHz.

8.2.3 Application Curves

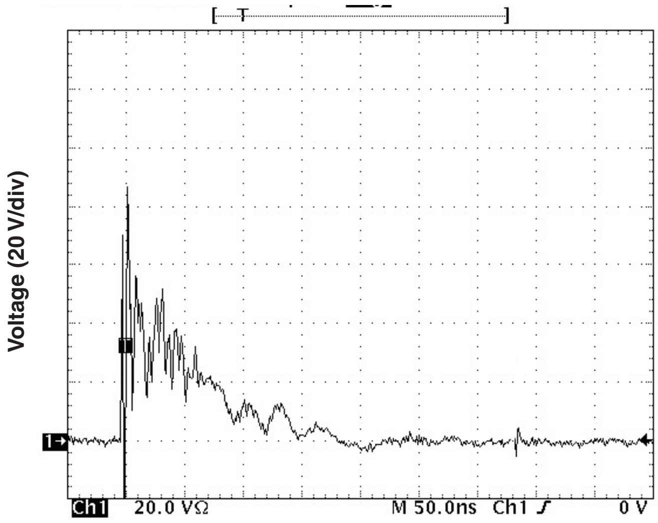


Figure 5. ESD Clamp Voltage at I/O Pins: IEC6100-4-2 15-kV Contact Discharge

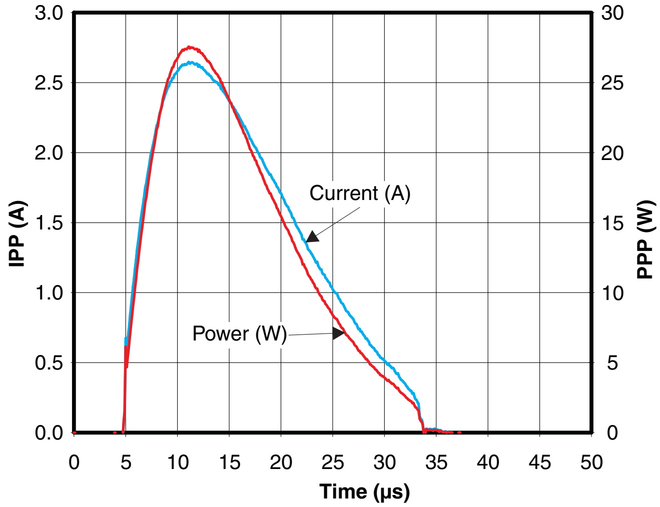


Figure 6. Pulse Waveform (8/20-µs Pulse)

9 Power Supply Recommendations

The TPD4E002 is a passive ESD protection device and there is no need to power it. Do not violate the maximum voltage specifications for each pin.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces, which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

Use external and internal ground planes and stitch them together with VIAs as close to the GND pin of TPD4E002 as possible. This allows for a low impedance path to ground so that the device can properly dissipate an ESD event.

10.2 Layout Example

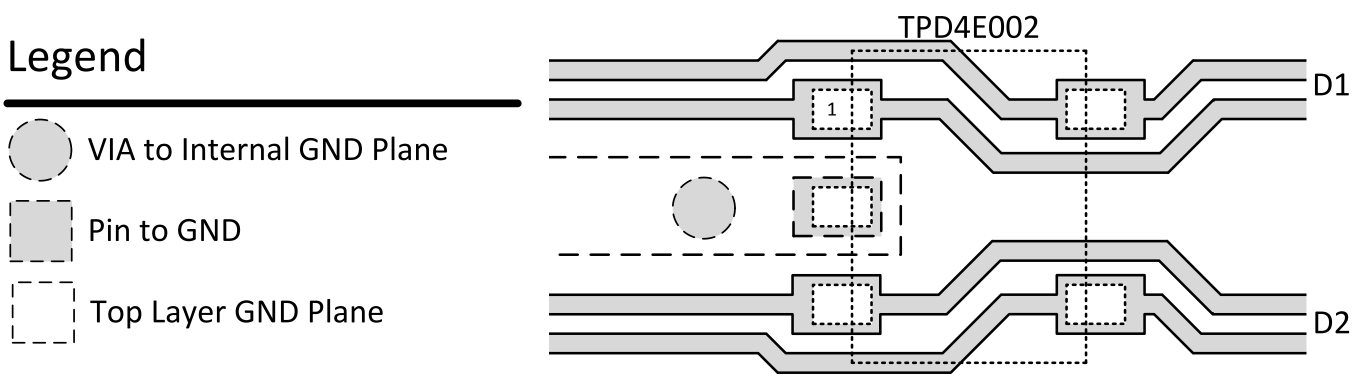


Figure 7. TPD4E002 Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Reading and Understanding an ESD Protection Datasheet*
- *ESD Layout Guide*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4E002DRL2	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	28S
TPD4E002DRL2.A	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	28S
TPD4E002DRL2.B	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	28S
TPD4E002DRLR	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	28S
TPD4E002DRLR.A	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	28S
TPD4E002DRLR.B	Active	Production	SOT-5X3 (DRL) | 5	4000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	28S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

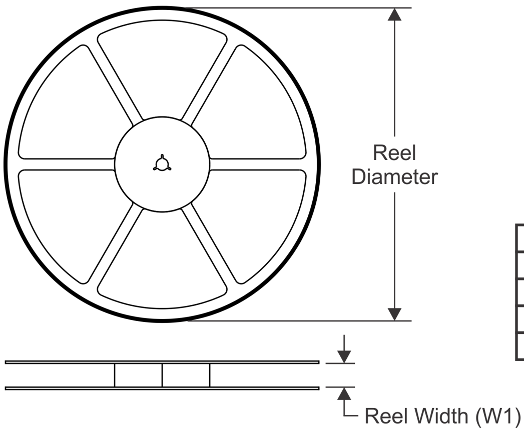
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

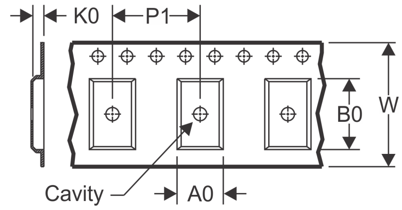
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

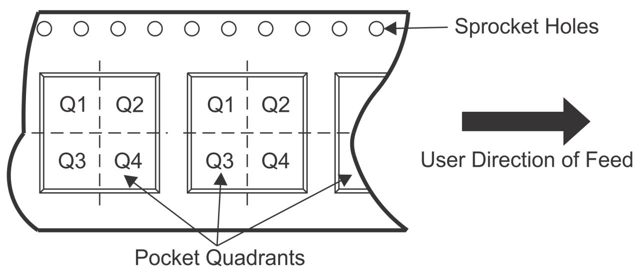


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

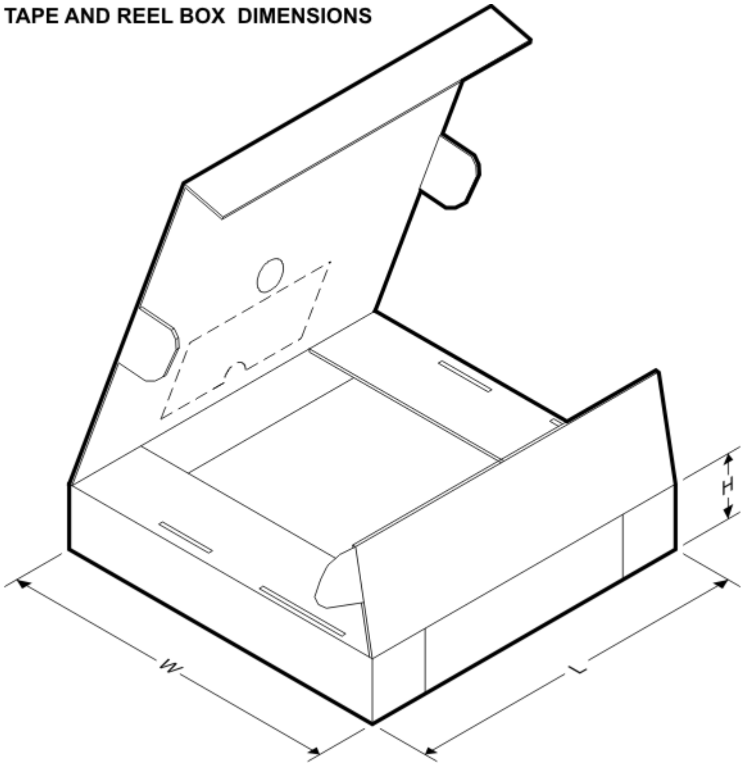
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

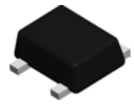
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E002DRL2	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q2
TPD4E002DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

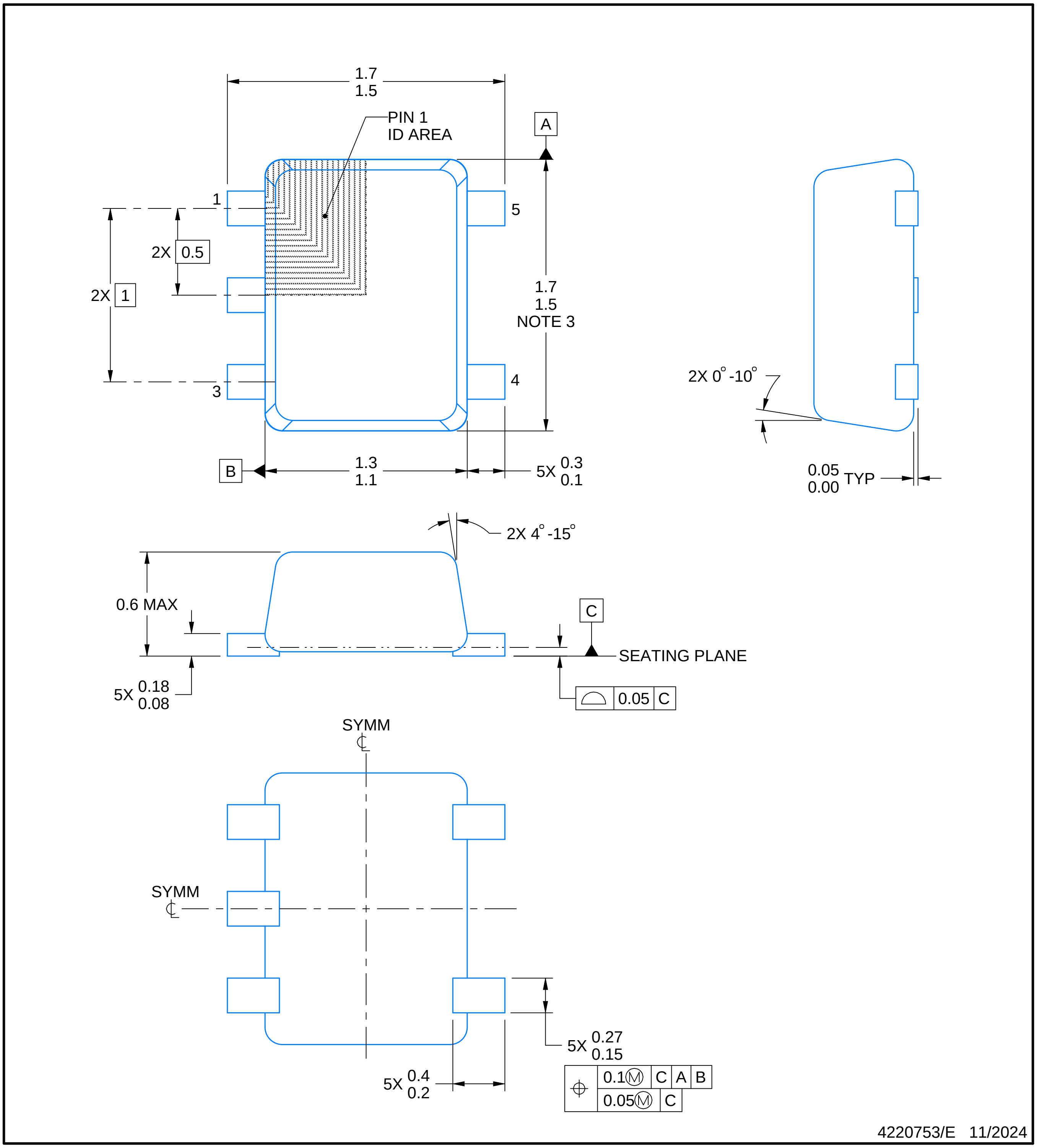
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E002DRL2	SOT-5X3	DRL	5	4000	183.0	183.0	20.0
TPD4E002DRLR	SOT-5X3	DRL	5	4000	183.0	183.0	20.0



DRL0005A

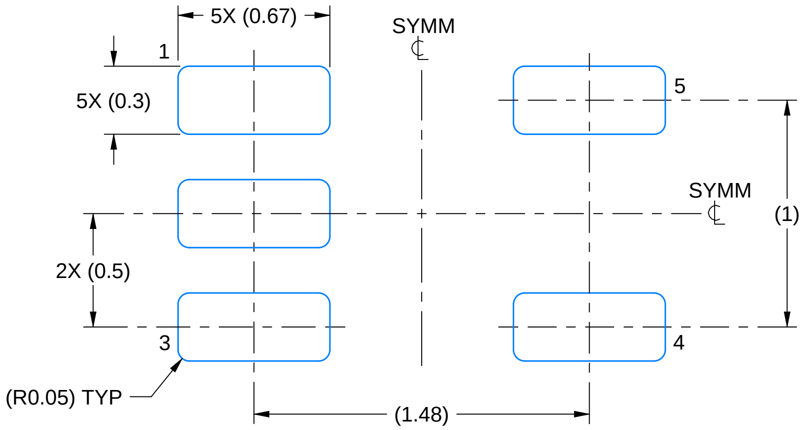
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

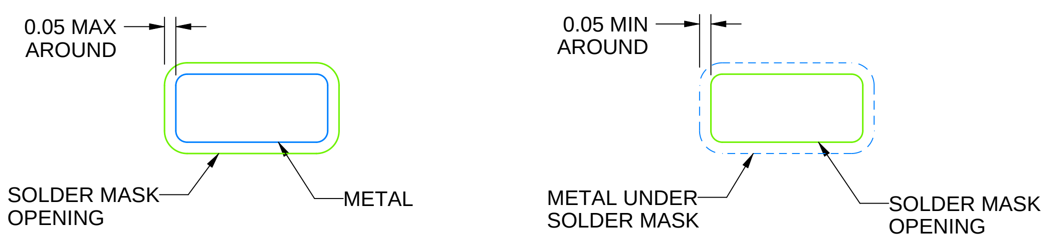


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1



LAND PATTERN EXAMPLE
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDERMASK DETAILS

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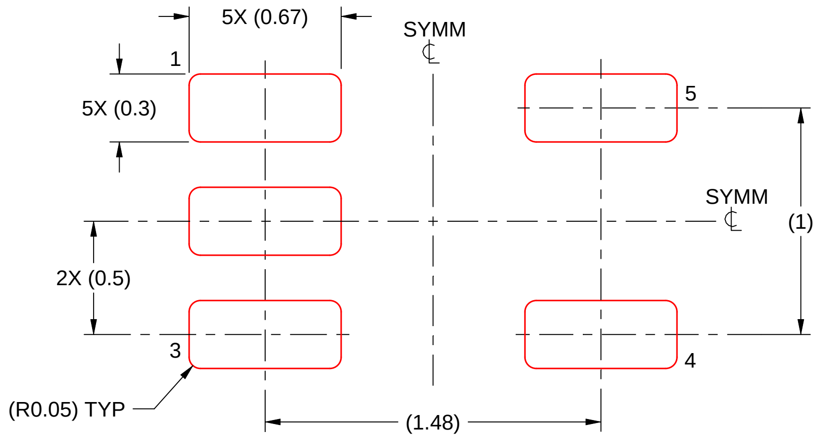
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.