SyncE and Telecom Rate Clock Translator

Short Form Data Sheet

March 2011

Features

- Synchronizes to any Telecom (N * 8 kHz) or any Synchronized Ethernet (SyncE) frequency.
- Generates any Telecom or SyncE frequency independent of the input frequency rate
- Uses proprietary DPLL technology to guarantee a stable synchronization path over any combination of input and output ratios and frequencies
- Provides input reference jitter filtering with programmable loop bandwidth in the range of 14 Hz to 896 Hz
- Supports two input references, each configurable as single ended LVCMOS (up to 177.5 MHz) or differential LVPECL (up to 720 MHz)
- Automatic hitless reference switching and stand-by mode on reference fail
- Digital PLL (DPLL) and high speed clock synthesis engine for generating high speed PHY clocks
- Provides four high performance differential LVPECL outputs with maximum speed up to 720 MHz with jitter below 0.7 psec RMS
- Provides 2 high performance single ended LVCMOS outputs with maximum speed of 177.5 MHz with jitter below 1.3 psec RMS

Ordering Information

ZL30158GGG	64 Pin CABGA	Trays
ZL30158GGG2	64 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Operates from a single crystal resonator or crystal oscillator
- Configurable using a simple SPI/I^{2}C interface

Applications

- Clock Generation for Physical Line Interface:
  - Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
  - SONET/SDH, OC-192/OC-48
  - 100 BaseX, GE, Fibre channel
- Clock Generation and Distribution for back plane Interface:
  - TDM, Telecom Bus, Utopia, SBI
  - XAUI

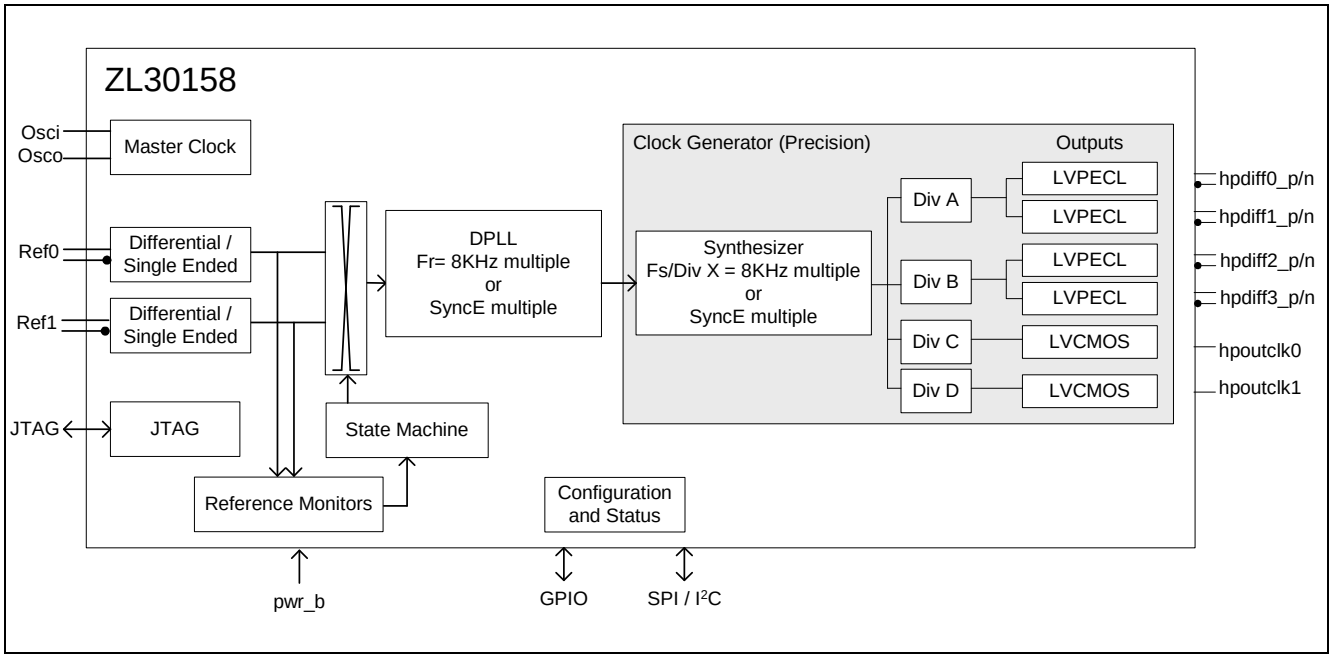


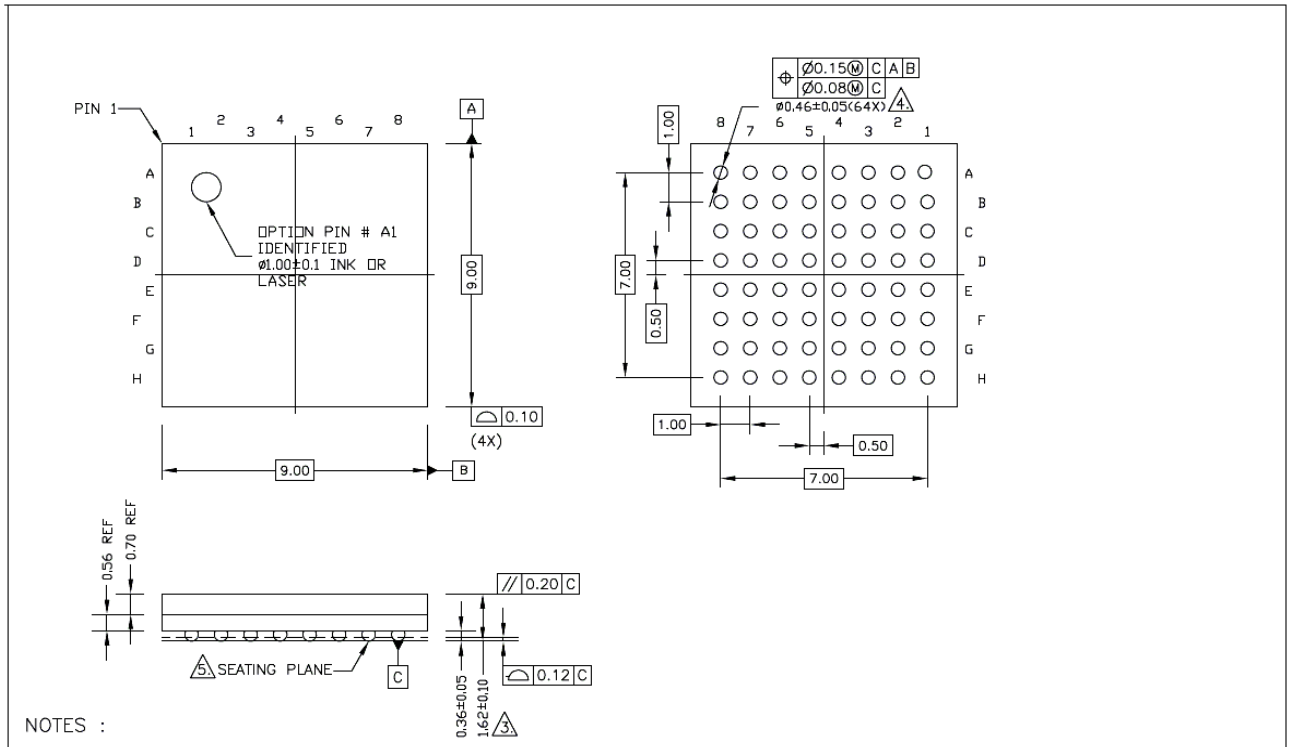
Figure 1 - Functional Block Diagram

Description

The ZL30158 Synchronous Ethernet Clock Translator, part of Zarlink's ClockCenter platform of Synchronous Clock devices, delivers industry leading synchronization performance for high-speed complex applications. The highly integrated and programmable solution synchronizes to any Telecom or any synchronized Ethernet (SyncE) frequency.

The ZL30158 accepts 2 single ended or differential input references and generates 6 high performance programmable clock outputs. The highly integrated solution allows designers to replace multiple components with a single chip, simplifying design and reducing component count and power.

1.0 Mechanical Drawing



NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. SOLDER BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
3. THIS DIMENSION INCLUDES STAND–OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

ZARLINK SEMICONDUCTOR	DWG. NO.	REV.
TITLE: 64L LBGA PACKAGE OUTLINE BODY SIZE :9 X 9 X1.62MM MAX PITCH 1.0MM	CDCA# 22–0006 84–06–128–305	2
	SHEET: 1 OF 1	SIZE: A4

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