

SANYO Semiconductors DATA SHEET

An ON Semiconductor Company

Bi-CMOS IC

LV58063MX — Step-down Switching Regulator

Overview

LV58063MX is a 1ch step-down switching regulator. 0.13Ω FET is incorporated on the upper side to achieve high-efficiency operation for large output current. Low-heat resistance and compact-package MFP8 (200mil) employed. Current mode control type, with superior load current response and easy phase compensation ON/OFF pin, allowing the standby mode with the current drain of 100µA Pulse-by-pulse over-current protection and overheat protection available for protection of load devices Soft start pin to be provided with a capacitance for soft start.

Functions

- 3A 1ch step-down switching regulator
- Wide input dynamic range (to 28V)
- High efficiency (90% $I_{OUT} = 1A$, $V_{IN} = 12V$, $V_O = 5V$)
- Standby mode
- Over-current protection
- Overshoot control function

- Thermal shutdown
- Reference voltage: 0.8V
- Fixed frequency: 370kHz
- Soft start
- Compact package: MFP8 (200mil) with Exposed Pad

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum input V _{IN} voltage	V _{IN} max		32	V
BOOT pin maximum voltage	V _{BT} max		37	V
SW pin maximum voltage	V _{SW} max		V _{IN} max	V
BOOT pin-SW pin maximum voltage	V _{BS-SW} max		7	V
FB, EN, COMP, SS pin maximum	Vfs max		7	V
Allowable power dissipation	Pd max	Mount on a specified board *	2.05	W
Junction temperature	Tj max		150	°C
Operating temperature	Topr		-20 to 80	°C
Storage temperature	Tstg		-40 to 150	°C

^{*} Specified board: 46.4mm × 31.8mm ×1.7mm, glass epoxy.

Note: Plan the maximum voltage while including coil and surge voltages, so that the maximum voltage is not exceeded even for an instant.

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V _{IN} pin voltage	V _{IN}		8 to 28	V
BOOT pin voltage	V _{BT}		-0.3 to 34	V
SW pin voltage	V _{SW}		-0.4 to V _{IN}	V
BOOT pin-SW pin maximum voltage	V _{BS-SW}		6.5	V
FB, EN, COMP, SS pin voltage	V _{FSO}		6	V

Electrical Characteristics at Ta = 25 °C, $V_{\mbox{IN}} = 12 \mbox{V}$, unless otherwise specified.

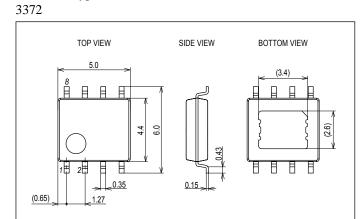
Parameter	Symbol	Conditions	Ratings			11.2
		Conditions	min	typ	max	Unit
IC current drain at standby	I _{CC} 1	EN=0V		70		μΑ
IC current drain in operation	I _{CC} 2	EN=OPEN, FB=1V		5		mA
Efficiency	Effcy	V _{IN} =12V, I _{OUT} =1A, Vo=5V, Design target *1		90		%
Reference voltage	Vref	V _{IN} =8V to 28V (±2%)	- 2%	0.8	+ 2%	V
FB pin bias current	Iref	FB=0.8V application		10	100	nA
High-side ON resistance	RonH	BOOT=5V		0.13		Ω
Low-side ON resistance	RonL			7		Ω
Oscillation frequency	fosc		296	370	444	kHz
Oscillation frequency during short-circuit protection	foscs		30	38	46	kHz
EN high-threshold voltage	Venh				1.9	V
EN low-threshold voltage	VenI		0.8			V
EN pull-up corrent	I _{EN}	EN = 0V		16		μΑ
Maximum ON DUTY	D max			80		%
Current limit peak value	Icl1	V _{IN} =12V, V _{OUT} =5V, L=10μH	3.8			Α
Thermal shutdown temperature	Ttsd	*Design guarantee *2		160		°C
Thermal shutdown temperature hysteresis	Dtsd	*Design guarantee *2		40		°C
Soft start current	I _{SS}	SS=0V	6	10	14	μΑ

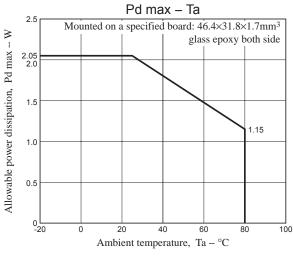
^{*1:} Reference value (not tested before shipment)

^{*2:} Design guarantee (value guaranteed by design and not tested before shipment)

Package Dimensions

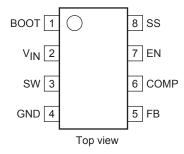
unit: mm (typ)





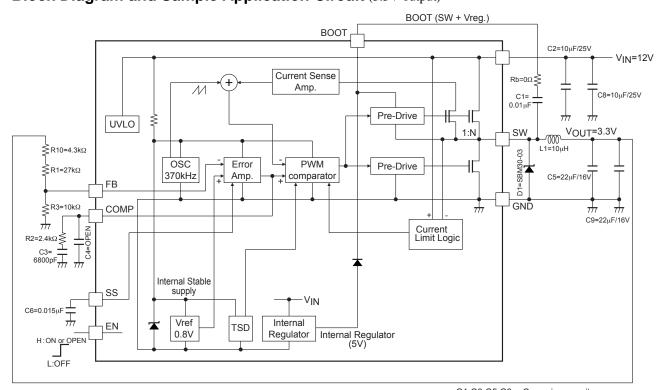
Pin Assignment

SIDE VIEW



SANYO: MFP8(200mil)

Block Diagram and Sample Application Circuit (3.3V output)



•C1,C8,C5,C9 = Ceramic capacitor •L1 = CDRH105RNP-100NC (sumida)

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Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	ВООТ	Upper MOS transistor boot strap capacitance connection pin. Connect the boot capacitance of about $0.01\mu F$ between SW pins. To protect the SW pin's absolute maximum rating, to ensure stable operation, and to eliminate noise, the boot capacitance serial resistance (about 100Ω) Rb proves effective.	VIN CBOOT
2	V _{IN}	Input voltage pin. Connect substantially large (20µF or more) capacitance between this pin and GND.	Hi side MOS
3	SW	Power switch pin. Connect the output LC filter. Connect the above capacitance between this pin and BOOT pin.	Low side MOS
4	GND	Ground pin.	
5	FB	Feedback pin. Sets the output voltage by means of split resistor in the section of the output voltage V_{OUT} - FB - GND. V_{OUT} setting is made as calculated below: $V_{OUT} = Vref \times \{1 + \frac{(R1 + R10)}{R3}\}$ $Vref = 0.8V$ Example: 3.3V output voltage (See Block Diagram and Sample Application Circuit) $V_{OUT} = 0.8 \times \{1 + \frac{(27k + 4.3k)}{10k}\}$	VIN Internal regulation line
8	SS	=3.304V Soft start pin. Sets the soft start time by means of the built-in $10\mu\text{A}$ source voltage and external soft start capacity. The soft start capacity C6 can be set as follows: $C6 = 10\mu\text{A} \times \frac{Tss}{Vref}$ Where, Tss is the soft start time and Vref is the reference voltage. Example: 1.2ms soft start time achieved $C6 = 10\mu\text{A} \times \frac{1.2ms}{0.8 \text{ V}} = 0.015\mu\text{F}$	SS W FB
6	COMP	Phase compensation pin. Connects with the phase compensation external capacitance and resistance of DC/DC converter close loop.	Internal regulation line COMP Clump circuit
7	EN	Enable pin. Converter enabled when set to the HIGH voltage and disabled when LOW voltage or OPEN state.	VIN 5μΑ EN 1kΩ 274.5kΩ Q117 2pF 93kΩ

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Considerations for the design

Insertion of serial beads in the Schottky diode for removal of noise may cause generation of the negative voltage deviating from the absolute maximum rating at the SW pin, resulting in failure of normal operation. In such an event, do not insert beads as above described and, instead, remove noise by means of the BOOT resistance Rb.

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