

## Automotive fully integrated H-bridge motor driver

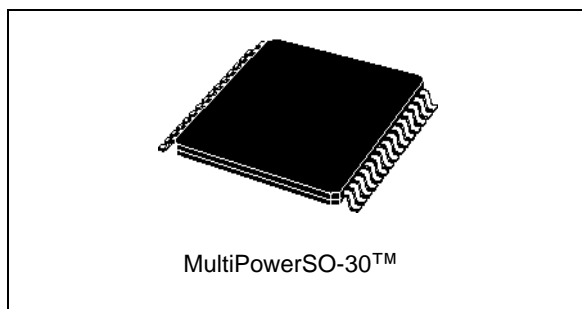
### Features

Type	$R_{DS(on)}$	$I_{out}$	$V_{CCmax}$
VNH3ASP30-E	42mΩ max (per leg)	30A	41V

- 5V logic level compatible inputs
- Undervoltage and overvoltage shutdown
- Overvoltage clamp
- Thermal shut down
- Cross-conduction protection
- Linear current limiter
- Very low standby power consumption
- PWM operation up to 20 kHz
- Protection against loss of ground and loss of  $V_{CC}$
- Current-sense output proportional to motor current
- Package: ECOPACK®

### Description

The VNH3ASP30-E is a full-bridge motor driver intended for a wide range of automotive applications. The device incorporates a dual monolithic high-side driver (HSD) and two low-side switches. The HSD switch is designed using STMicroelectronics proprietary VIPower™ M0 technology that efficiently integrates a true Power MOSFET with an intelligent signal/protection circuit on the same die.



The low-side switches are vertical MOSFETs manufactured using STMicroelectronics proprietary EHD ("STripFET™") process. The three circuits are assembled in a MultiPowerSO-30 package on electrically isolated lead frames. This package, specifically designed for the harsh automotive environment, offers improved thermal performance thanks to exposed die pads. Moreover, its fully symmetrical mechanical design provides superior manufacturability at board level. The input signals  $IN_A$  and  $IN_B$  can directly interface with the microcontroller to select the motor direction and the brake condition. Pins  $DIAG_A/EN_A$  or  $DIAG_B/EN_B$ , when connected to an external pull-up resistor, enable one leg of the bridge. They also provide a feedback digital diagnostic signal. The normal condition operation is explained in [Table 12: Truth table in normal operating conditions on page 14](#). The CS pin monitors the motor current by delivering a current proportional to its value. The speed of the motor can be controlled in all possible conditions by the PWM up to 20 kHz. In all cases, a low level state on the PWM pin will turn off both the  $LS_A$  and  $LS_B$  switches. When PWM rises to a high level,  $LS_A$  or  $LS_B$  turn on again depending on the input pin state.

**Table 1. Device summary**

Package	Order codes	
	Tube	Tape & reel
MultiPowerSO-30	VNH3ASP30-E	VNH3ASP30TR-E

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# 1 Block diagram and pin description

Figure 1. Block diagram

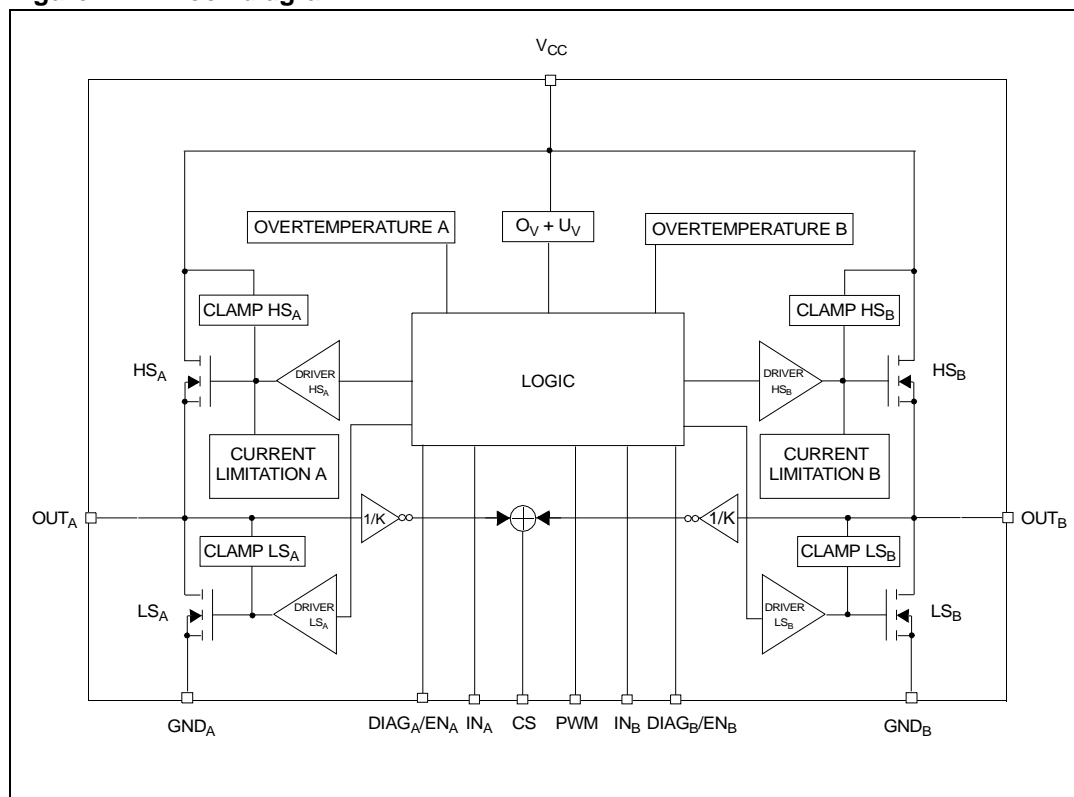
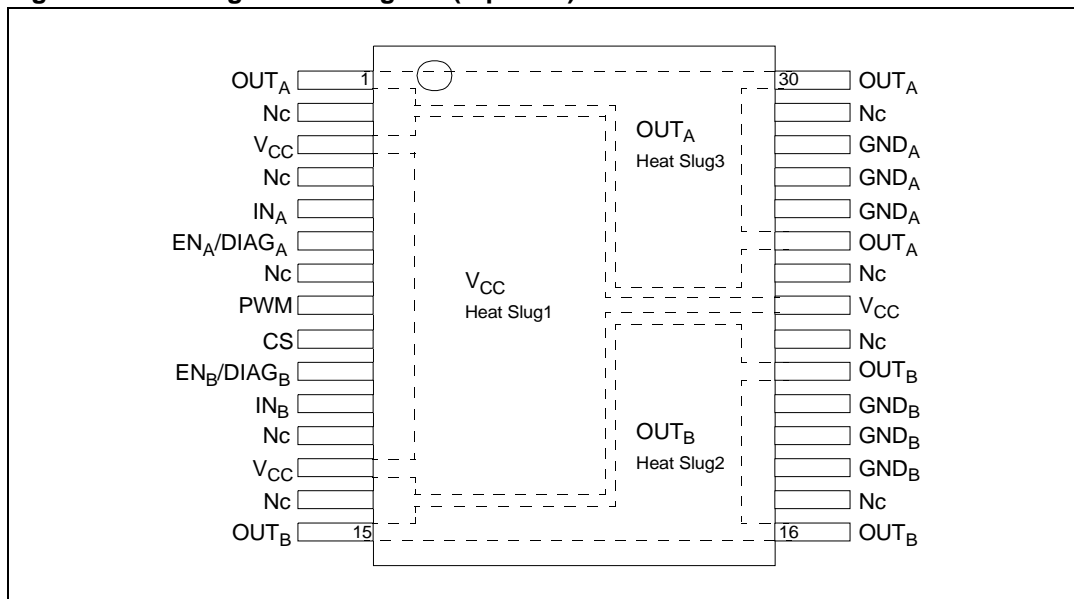


Table 2. Block description

Name	Description
Logic control	Allows the turn-on and the turn-off of the high-side and the low-side switches according to the truth table
Overvoltage + undervoltage	Shuts down the device outside the range [5.5V..16V] for the battery voltage
High-side and low-side clamp voltage	Protect the high-side and the low-side switches from the high voltage on the battery line in all configurations for the motor
High-side and low-side driver	Drives the gate of the concerned switch to allow a good $R_{DS(on)}$ for the leg of the bridge
Linear current limiter	Limits the motor current by reducing the high-side switch gate source voltage when short-circuit to ground occurs
Overtemperature protection	In case of short-circuit with the increase of the junction's temperature, shuts down the concerned high side to prevent its degradation and to protect the die
Fault detection	Signals an abnormal behavior of the switches in the half-bridge A or B by pulling low the concerned $EN_x/DIAG_x$ pin

**Figure 2. Configuration diagram (top view)****Table 3. Pin definitions and functions**

Pin No.	Symbol	Function
1, 25, 30	OUT <sub>A</sub> , Heat Slug3	Source of high-side switch A / Drain of low-side switch A
2, 4, 7, 12, 14, 17, 22, 24, 29	NC	Not connected
3, 13, 23	V <sub>CC</sub> , Heat Slug1	Drain of high-side switches and power supply voltage
5	IN <sub>A</sub>	Clockwise input
6	EN <sub>A</sub> /DIAG <sub>A</sub>	Status of high-side and low-side switches A; open drain output
8	PWM	PWM input
9	CS	Output of current sense
10	EN <sub>B</sub> /DIAG <sub>B</sub>	Status of high-side and low-side switches B; open drain output
11	IN <sub>B</sub>	Counter clockwise input
15, 16, 21	OUT <sub>B</sub> , Heat Slug2	Source of high-side switch B / Drain of low-side switch B
26, 27, 28	GND <sub>A</sub>	Source of low-side switch A <sup>(1)</sup>
18, 19, 20	GND <sub>B</sub>	Source of low-side switch B <sup>(1)</sup>

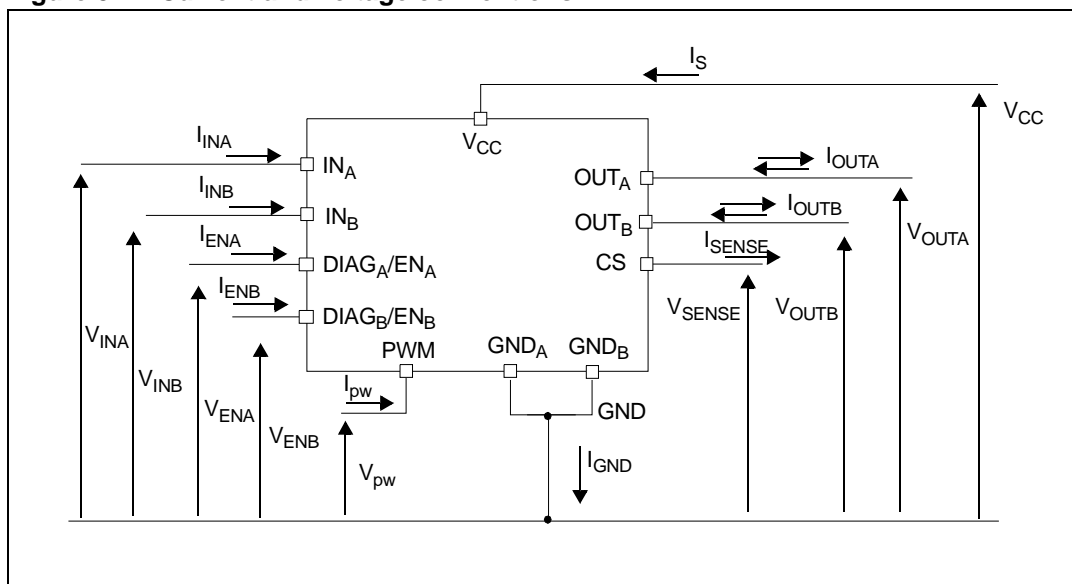
1. GND<sub>A</sub> and GND<sub>B</sub> must be externally connected together.

**Table 4. Pin functions description**

Name	Description
V <sub>CC</sub>	Battery connection
GND <sub>A</sub> , GND <sub>B</sub>	Power grounds; must always be externally connected together
OUT <sub>A</sub> , OUT <sub>B</sub>	Power connections to the motor
IN <sub>A</sub> , IN <sub>B</sub>	Voltage controlled input pins with hysteresis, CMOS compatible: These two pins control the state of the bridge in normal operation according to the truth table (brake to V <sub>CC</sub> , brake to GND, clockwise and counterclockwise).
PWM	Voltage controlled input pin with hysteresis, CMOS compatible: Gates of low-side FETs are modulated by the PWM signal during their ON phase allowing speed control of the motor.
EN <sub>A</sub> /DIAG <sub>A</sub> , EN <sub>B</sub> /DIAG <sub>B</sub>	Open drain bidirectional logic pins. These pins must be connected to an external pull up resistor. When externally pulled low, they disable half-bridge A or B. In case of fault detection (thermal shutdown of a high-side FET or excessive ON state voltage drop across a low-side FET), these pins are pulled low by the device (see truth table in fault condition).
CS	Analog current-sense output. This output sources a current proportional to the motor current. The information can be read back as an analog voltage across an external resistor.

## 2 Electrical specifications

Figure 3. Current and voltage conventions



### 2.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage	+41	V
$I_{max}$	Maximum output current (continuous)	30	A
$I_R$	Reverse output current (continuous)	-30	
$I_{IN}$	Input current ( $IN_A$ and $IN_B$ pins)	$\pm 10$	mA
$I_{EN}$	Enable input current ( $DIAG_A/EN_A$ and $DIAG_B/EN_B$ pins)	$\pm 10$	
$I_{PW}$	PWM input current	$\pm 10$	
$V_{CS}$	Current-sense maximum voltage	-3/+15	V
$V_{ESD}$	Electrostatic discharge ( $R = 1.5k\Omega$ , $C = 100pF$ )		
	– CS pin	2	kV
	– logic pins	4	kV
	– output pins: $OUT_A$ , $OUT_B$ , $V_{CC}$	5	kV
$T_J$	Junction operating temperature	Internally limited	$^{\circ}C$
$T_C$	Case operating temperature	-40 to 150	
$T_{stg}$	Storage temperature	-55 to 150	



## 2.2 Electrical characteristics

$V_{CC} = 9V$  up to  $16V$ ;  $-40^{\circ}C < T_J < 150^{\circ}C$ , unless otherwise specified.

**Table 6. Power section**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{CC}$	Operating supply voltage		5.5		16	V
$I_S$	Supply current	Off state: $IN_A = IN_B = PWM = 0$ ; $T_J = 25^{\circ}C$ ; $V_{CC} = 13V$ $IN_A = IN_B = PWM = 0$ ;		12	30 60	$\mu A$ $\mu A$
		On state: $IN_A$ or $IN_B = 5V$ , no PWM			10	mA
$R_{ONHS}$	Static high-side resistance	$I_{OUT} = 12A$ ; $T_J = 25^{\circ}C$ $I_{OUT} = 12A$ ; $T_J = -40$ to $150^{\circ}C$			30 60	$m\Omega$
$R_{ONLS}$	Static low-side resistance	$I_{OUT} = 12A$ ; $T_J = 25^{\circ}C$ $I_{OUT} = 12A$ ; $T_J = -40$ to $150^{\circ}C$			12 24	$m\Omega$
$V_f$	High-side freewheeling diode forward voltage	$I_f = 12A$		0.8	1.1	V
$I_{L(off)}$	High-side off-state output current (per channel)	$T_J = 25^{\circ}C$ ; $V_{OUTX} = EN_X = 0V$ ; $V_{CC} = 13V$			3	$\mu A$
		$T_J = 125^{\circ}C$ ; $V_{OUTX} = EN_X = 0V$ ; $V_{CC} = 13V$			5	
$I_{RM}$	Dynamic cross-conduction current	$I_{OUT} = 12A$ (see <a href="#">Figure 7</a> )		1.7		A

**Table 7. Logic inputs ( $IN_A$ ,  $IN_B$ ,  $EN_A$ ,  $EN_B$ )**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{IL}$	Input low-level voltage	Normal operation ( $DIAG_X/EN_X$ pin acts as an input pin)			1.25	V
$V_{IH}$	Input high-level voltage		3.25			
$V_{Ihys}$	Input hysteresis voltage		0.5			
$V_{ICL}$	Input clamp voltage	$I_{IN} = 1mA$	5.5	6.3	7.5	
		$I_{IN} = -1mA$	-1.0	-0.7	-0.3	
$I_{INL}$	Input low current	$V_{IN} = 1.25V$	1			$\mu A$
$I_{INH}$	Input high current	$V_{IN} = 3.25V$			10	
$V_{DIAG}$	Enable output low-level voltage	Fault operation ( $DIAG_X/EN_X$ pin acts as an output pin); $I_{EN} = 1mA$			0.4	V

**Table 8. PWM**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>PWL</sub>	PWM low-level voltage				1.25	V
I <sub>PWL</sub>	PWM low-level pin current	V <sub>pw</sub> = 1.25 V	1			μA
V <sub>PWH</sub>	PWM high-level voltage		3.25			V
I <sub>PWH</sub>	PWM high-level pin current	V <sub>pw</sub> = 3.25V			10	μA
V <sub>PWhys</sub>	PWM hysteresis voltage		0.5			V
V <sub>PWCL</sub>	PWM clamp voltage	I <sub>pw</sub> = 1mA	V <sub>CC</sub> + 0.3	V <sub>CC</sub> + 0.7	V <sub>CC</sub> + 1.0	
		I <sub>pw</sub> = -1mA	-6.0	-4.5	-3.0	
C <sub>INPW</sub>	PWM pin input capacitance	V <sub>IN</sub> = 2.5V			25	pF

**Table 9. Switching (V<sub>CC</sub> = 13V, R<sub>LOAD</sub> = 1 Ω )**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
f <sub>PW</sub>	PWM frequency		0		20	kHz
t <sub>d(on)</sub>	Turn-on delay time	Input rise time < 1μs (see <a href="#">Figure 6</a> )			250	μs
t <sub>d(off)</sub>	Turn-off delay time	Input rise time < 1μs (see <a href="#">Figure 6</a> )			250	
t <sub>r</sub>	Rise time	(see <a href="#">Figure 5</a> )		1	1.6	
t <sub>f</sub>	Fall time	(see <a href="#">Figure 5</a> )		1	2.4	
t <sub>DEL</sub>	Delay time during change of operating mode	(see <a href="#">Figure 4</a> )	300	600	1800	
t <sub>rr</sub>	High-side freewheeling diode reverse recovery time	(see <a href="#">Figure 7</a> )		110		ns

**Table 10. Protection and diagnostic**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
V <sub>UV(sd)</sub>	Undervoltage shutdown				5.5	V
V <sub>UV(reset)</sub>	Undervoltage reset			4.7		
V <sub>OV(sd)</sub>	Overvoltage shutdown		16	19	22	
I <sub>LIM</sub>	High-side current limitation		30	50	70	A
V <sub>CLP</sub>	Total clamp voltage (V <sub>CC</sub> to GND)	I <sub>OUT</sub> = 12A	43	48	54	V
T <sub>th(sd)</sub>	Thermal shutdown temperature	V <sub>IN</sub> = 3.25V	150	175	200	°C
T <sub>h(reset)</sub>	Thermal reset temperature		135			
T <sub>th(hys)</sub>	Thermal hysteresis		7	15		

**Table 11. Current sense ( $9V < V_{CC} < 16V$ )**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$K_1$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 30A$ ; $R_{SENSE} = 700\Omega$ ; $T_J = -40$ to $150^\circ C$	4000	4700	5400	
$K_2$	$I_{OUT}/I_{SENSE}$	$I_{OUT} = 8A$ ; $R_{SENSE} = 700\Omega$ ; $T_J = -40$ to $150^\circ C$	3750	4700	5650	
$dK_1/K_1^{(1)}$	Analog sense current drift	$I_{OUT} = 30A$ ; $R_{SENSE} = 700\Omega$ ; $T_J = -40$ to $150^\circ C$	-8		+8	%
$dK_2/K_2^{(1)}$	Analog sense current drift	$I_{OUT} = 8A$ ; $R_{SENSE} = 700\Omega$ ; $T_J = -40$ to $150^\circ C$	-10		+10	
$I_{SENSEO}$	Analog sense leakage current	$I_{OUT} = 0A$ ; $V_{SENSE} = 0V$ ; $T_J = -40$ to $150^\circ C$	0		70	$\mu A$

1. Analog sense current drift is deviation of factor K for a given device over ( $-40^\circ C$  to  $150^\circ C$  and  $9V < V_{CC} < 16V$ ) with respect to its value measured at  $T_J = 25^\circ C$ ,  $V_{CC} = 13V$

Figure 4. Definition of the delay times measurement

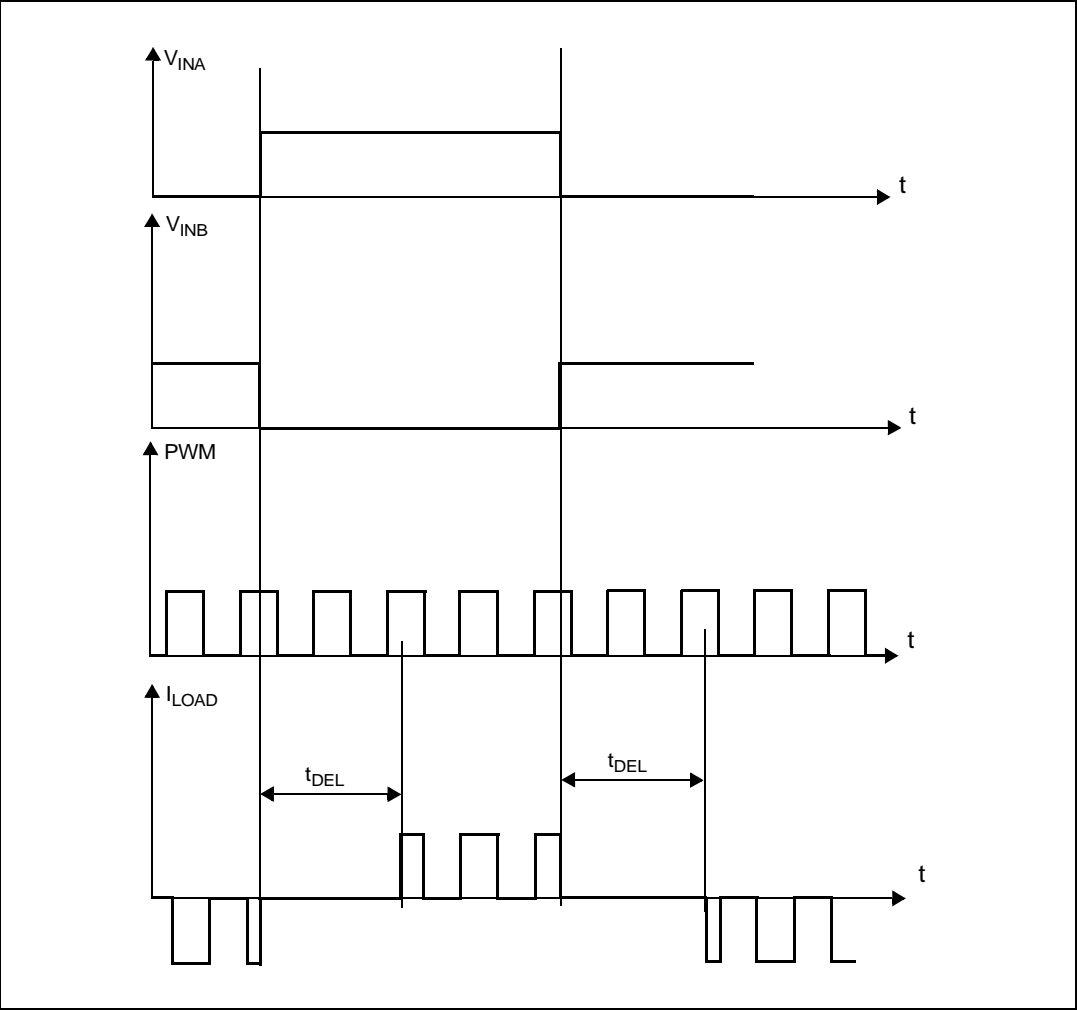
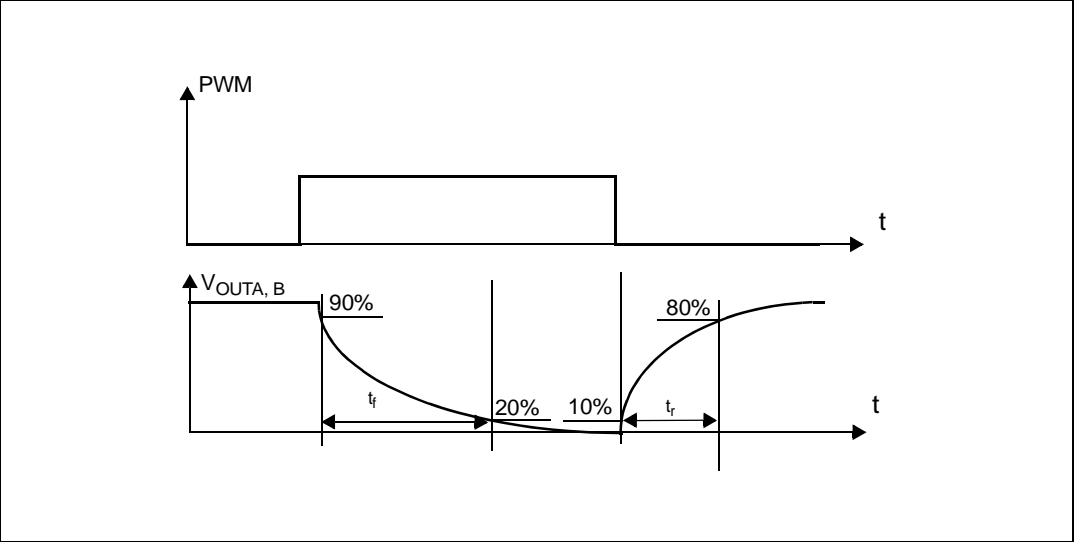
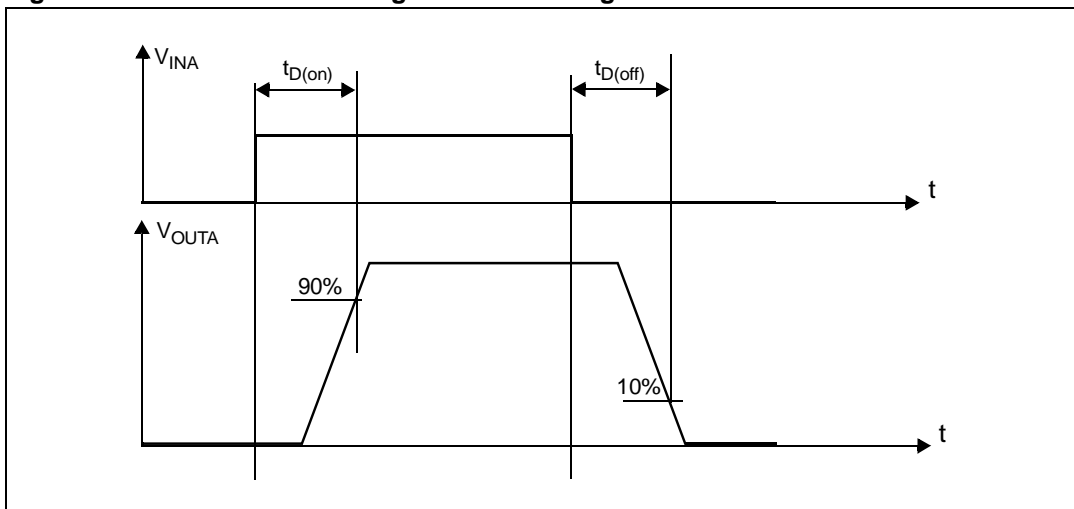
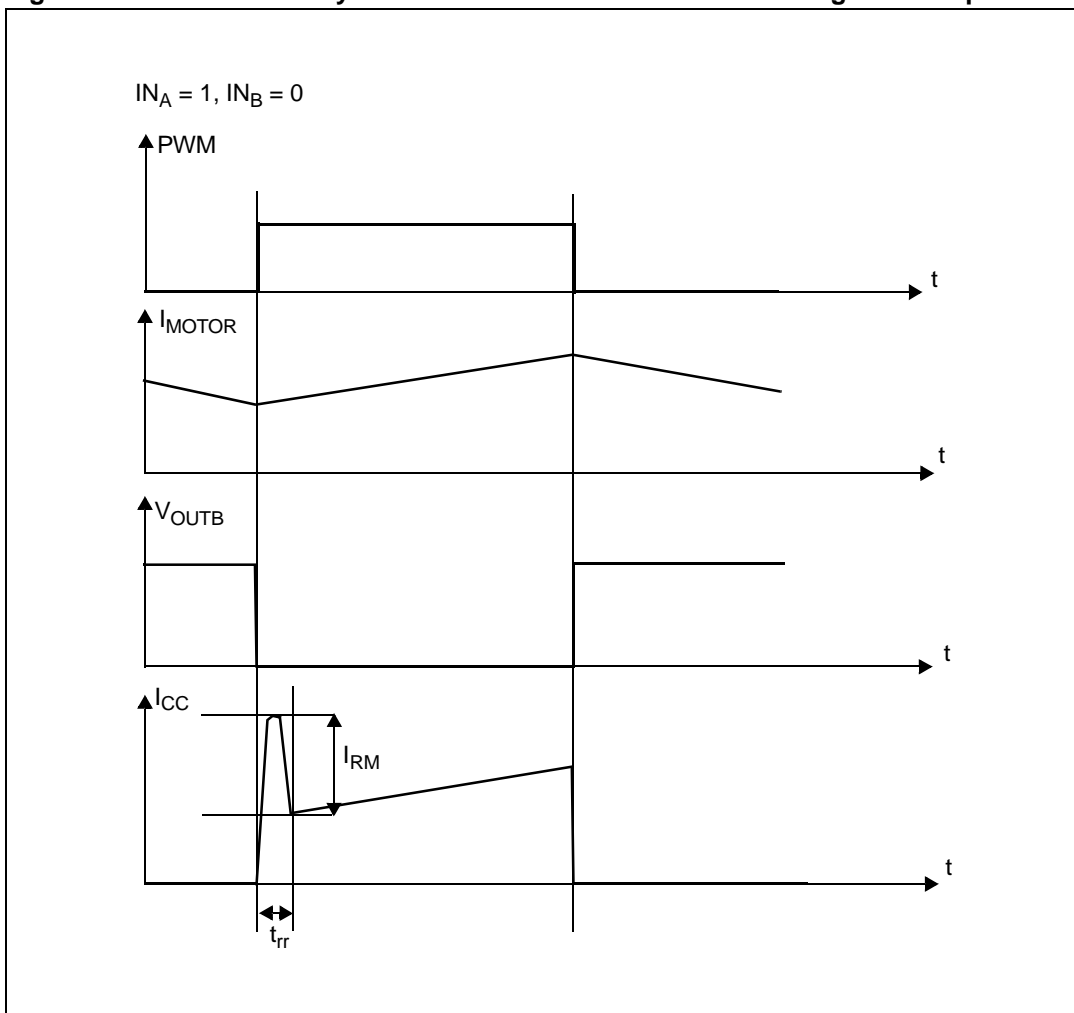


Figure 5. Definition of the low-side switching times

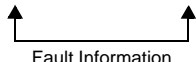
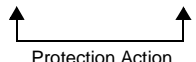


**Figure 6. Definition of the high-side switching times**

**Figure 7. Definition of dynamic cross conduction current during a PWM operation**


**Table 12. Truth table in normal operating conditions**

IN <sub>A</sub>	IN <sub>B</sub>	DIAG <sub>A</sub> /EN <sub>A</sub>	DIAG <sub>B</sub> /EN <sub>B</sub>	OUT <sub>A</sub>	OUT <sub>B</sub>	CS	Operating mode
1	1	1	1	H	H	High Imp.	Brake to V <sub>CC</sub>
	0				L	$I_{SENSE} = I_{OUT}/K$	Clockwise (CW)
0	1			L	H		Counterclockwise (CCW)
	0				L	High Imp.	Brake to GND

**Table 13. Truth table in fault conditions (detected on OUT<sub>A</sub>)**

IN <sub>A</sub>	IN <sub>B</sub>	DIAG <sub>A</sub> /EN <sub>A</sub>	DIAG <sub>B</sub> /EN <sub>B</sub>	OUT <sub>A</sub>	OUT <sub>B</sub>	CS	
1	1	0	1	OPEN	H	High Imp.	
	0				L		
0	1				H	I <sub>OUTB</sub> /K	
	0				L	High Imp.	
X	X		0		OPEN		
	1		1		H	I <sub>OUTB</sub> /K	
	0				L	High Imp.	
<div><div><p>Fault Information</p></div><div><p>Protection Action</p></div></div>							

**Note:**

Notice that saturation detection on the low side power MOSFET is possible only if the impedance of the short-circuit from the output to the battery is less than 100mΩ when the device is supplied with a battery voltage of 13.5V.

Table 14. Electrical transient requirements

ISO T/R - 7637/1 Test Pulse	Test Level I	Test Level II	Test Level III	Test Level IV	Test Levels Delays and Impedance
1	-25V	-50V	-75V	-100V	2ms, 10Ω
2	+25V	+50V	+75V	+100V	0.2ms, 10Ω
3a	-25V	-50V	-100V	-150V	0.1μs, 50Ω
3b	+25V	+50V	+75V	+100V	
4	-4V	-5V	-6V	-7V	100ms, 0.01Ω
5	+26.5V	+46.5V	+66.5V	+86.5V	400ms, 2Ω

ISO T/R - 7637/1 Test Pulse	Test Levels Result I	Test Levels Result II	Test Levels Result III	Test Levels Result IV
1	C	C	C	C
2				
3a				
3b				
4				
5 <sup>(1)</sup>		E	E	E

1. For load dump exceeding the above value a centralized suppressor must be adopted.

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.3 Electrical characteristics curves

Figure 8. On state supply current

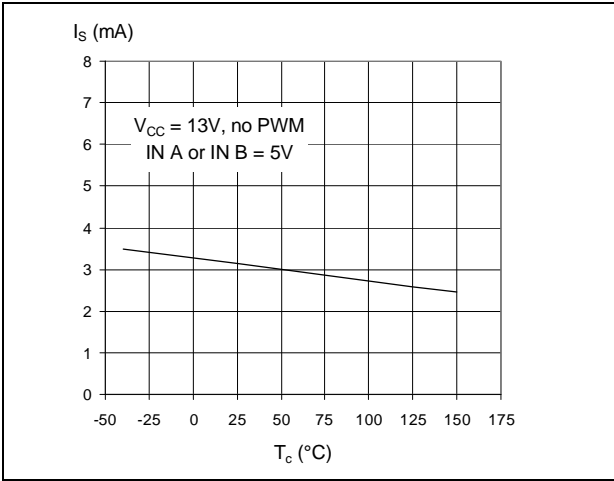


Figure 9. Off state supply current

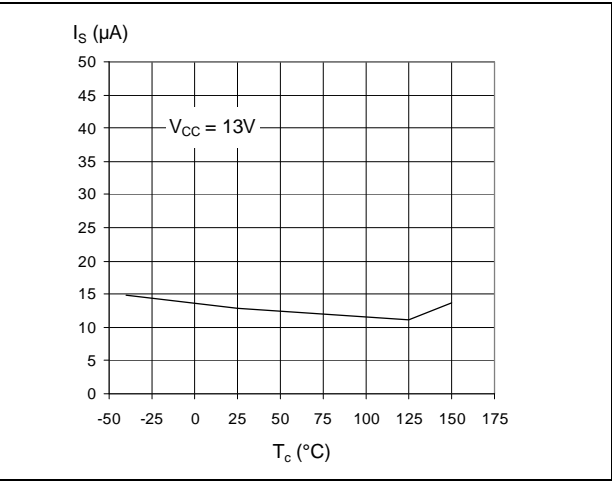


Figure 10. High-level input current

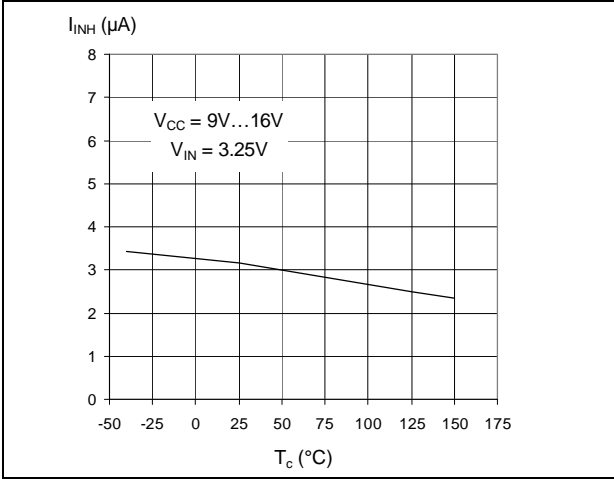


Figure 11. Input clamp voltage

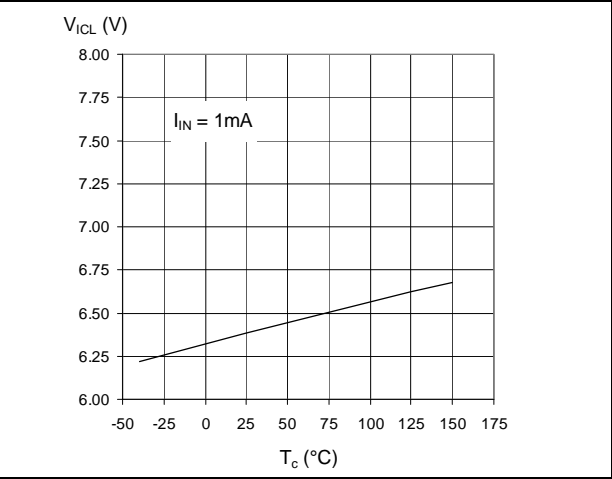


Figure 12. Input high-level voltage

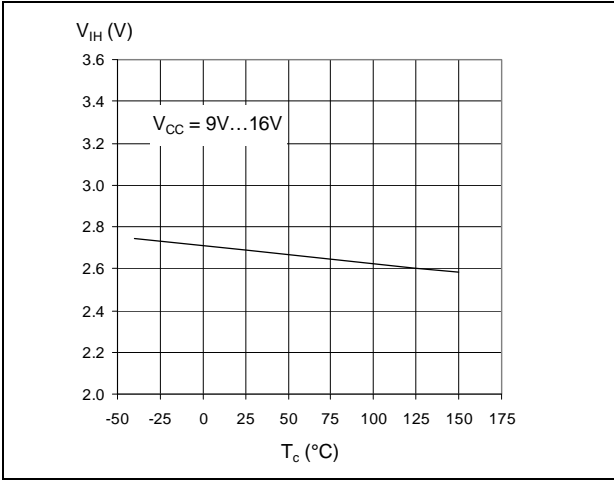


Figure 13. Input low-level voltage

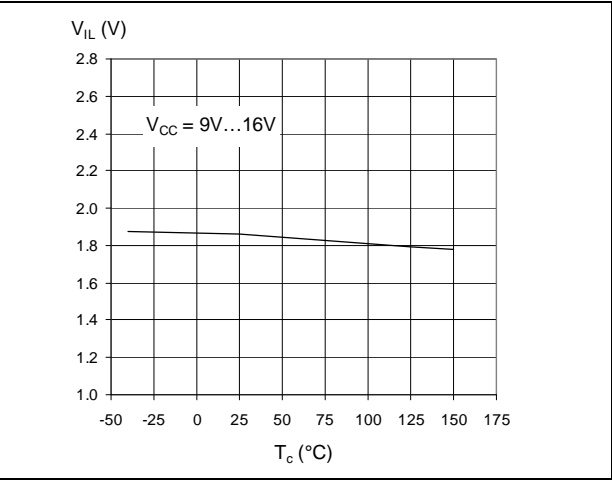




Figure 14. Input hysteresis voltage

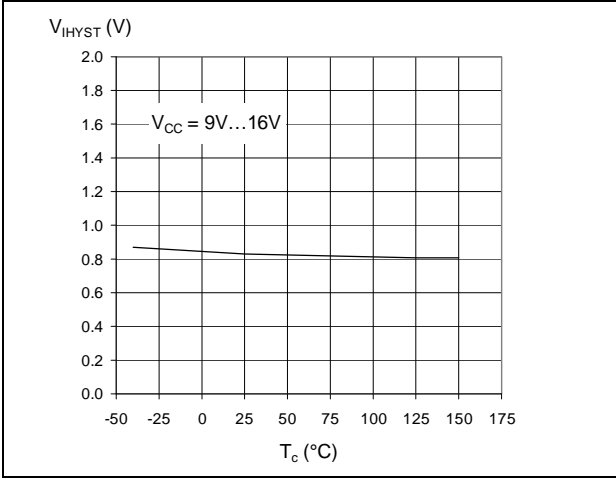


Figure 15. High-level enable pin current

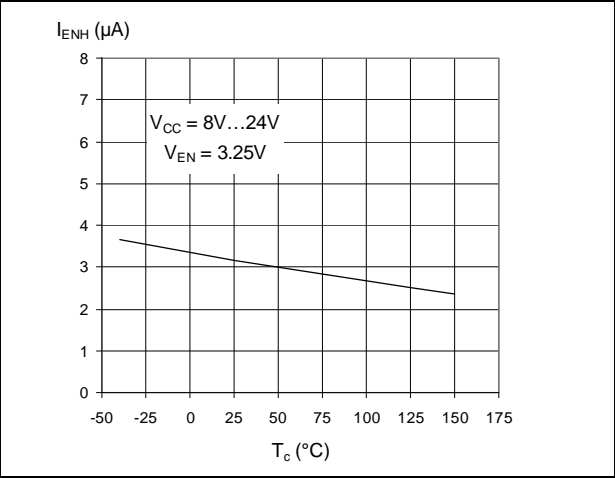


Figure 16. Delay time during change of operation mode

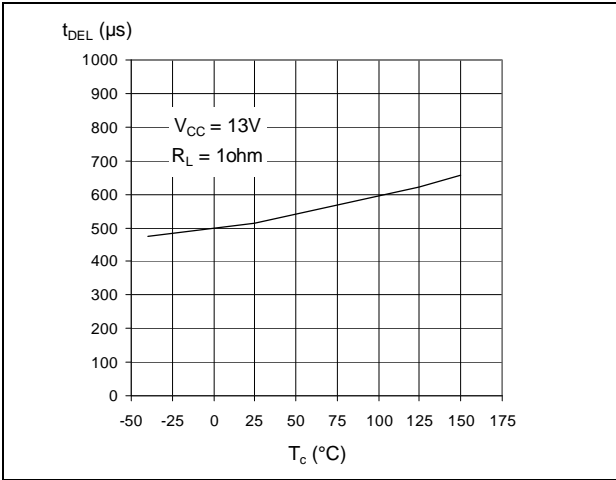


Figure 17. Enable clamp voltage

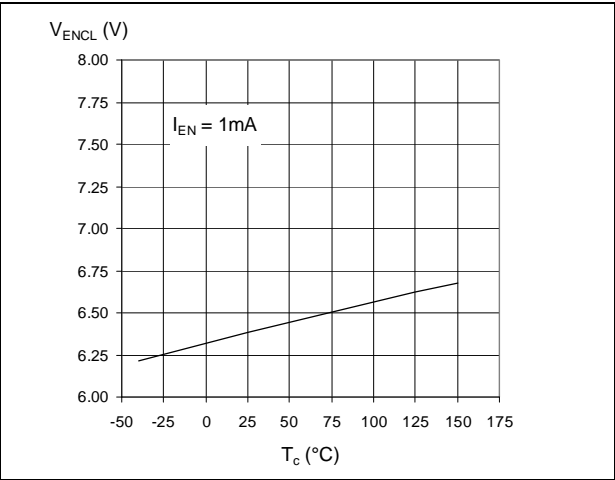


Figure 18. High-level enable voltage

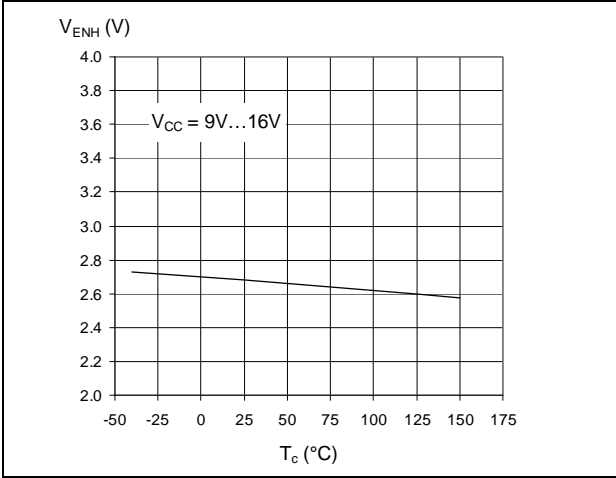


Figure 19. Low-level enable voltage

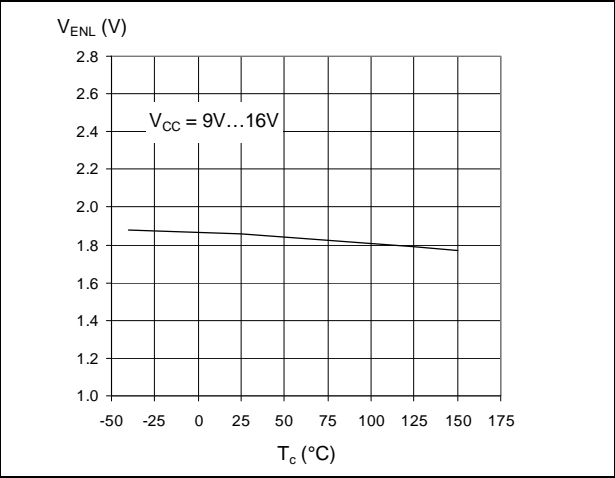


Figure 20. PWM high-level voltage

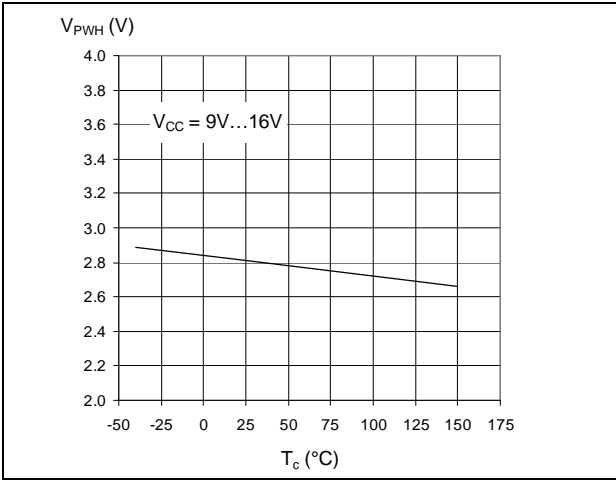


Figure 21. PWM low-level voltage

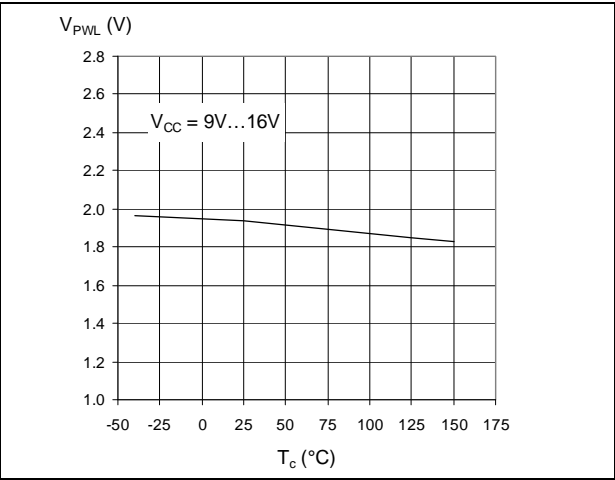


Figure 22. PWM high-level current

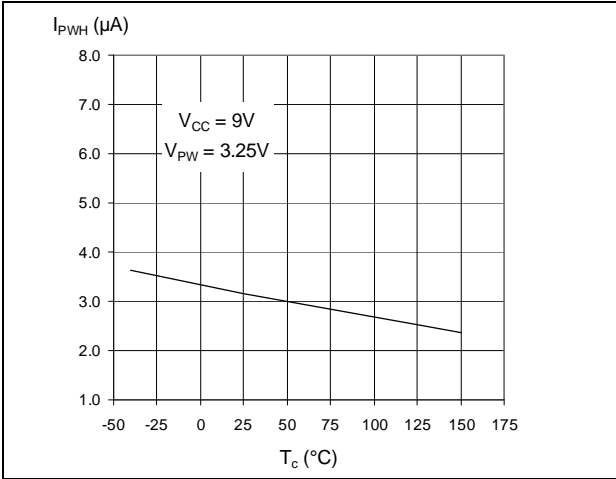


Figure 23. Overvoltage shutdown

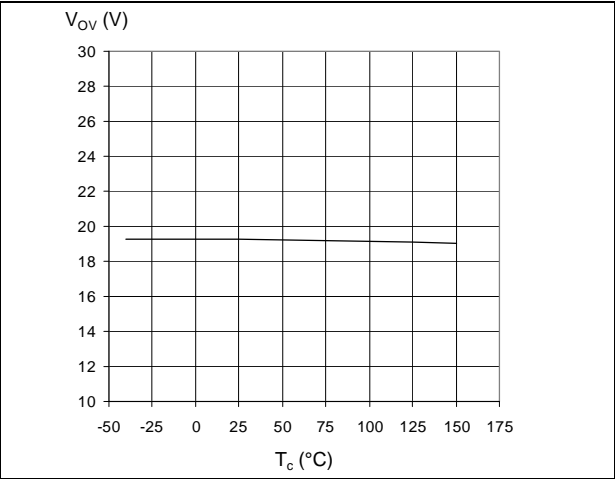


Figure 24. Undervoltage shutdown

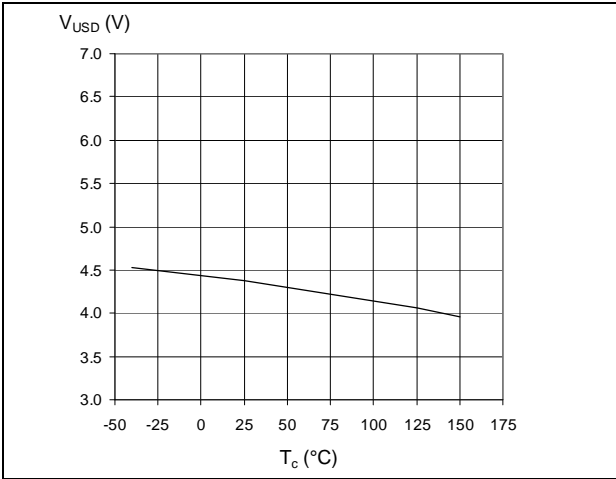


Figure 25. Current limitation

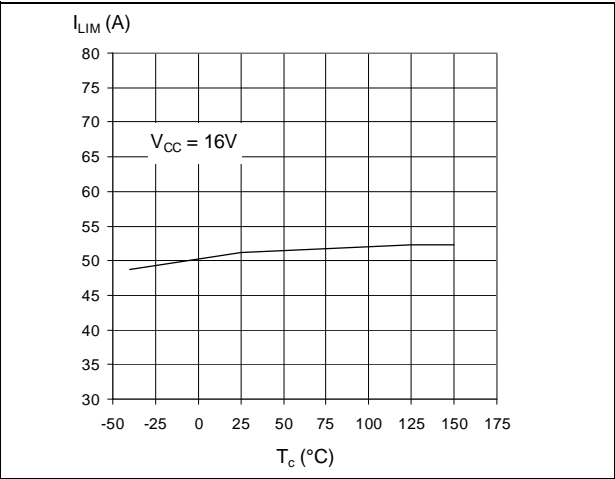


Figure 26. On state high-side resistance vs  $T_{case}$

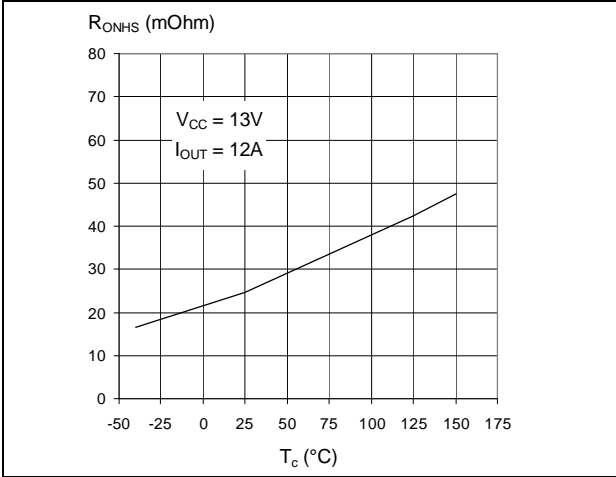


Figure 27. On state low-side resistance vs  $T_{case}$

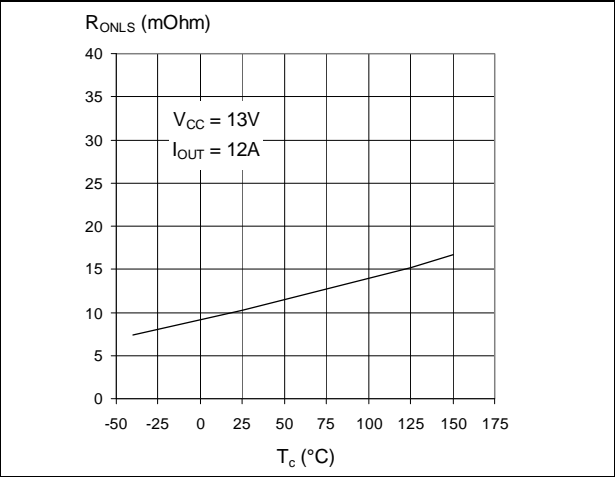


Figure 28. On state high-side resistance vs  $V_{CC}$

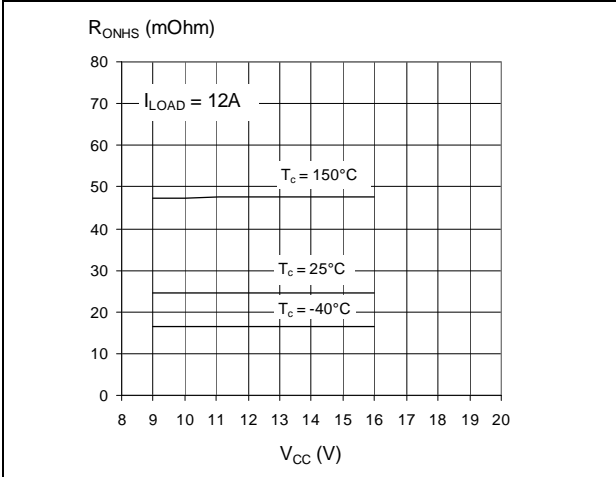


Figure 29. On state low-side resistance vs  $V_{CC}$

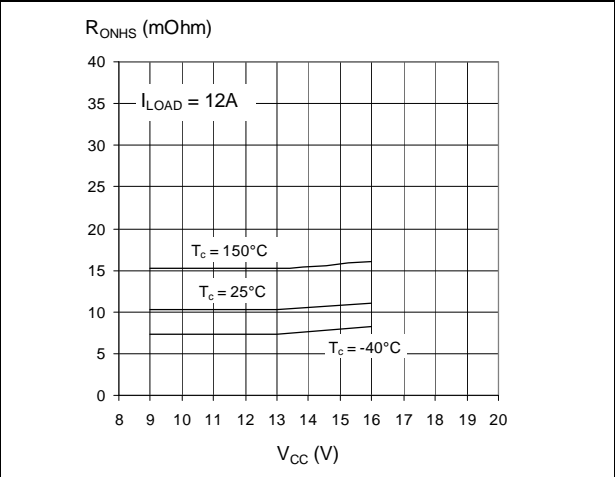


Figure 30. Output voltage rise time

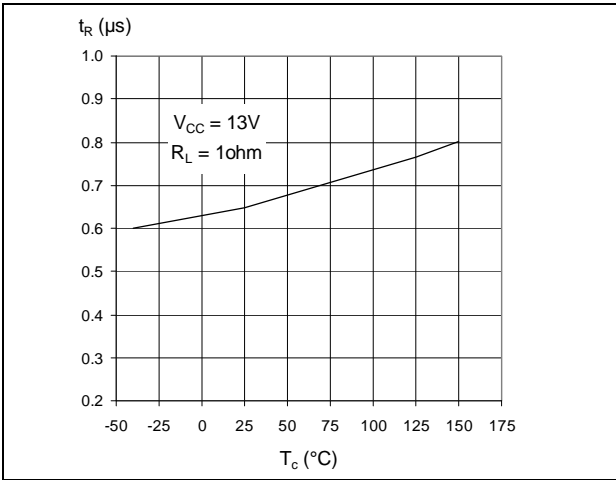
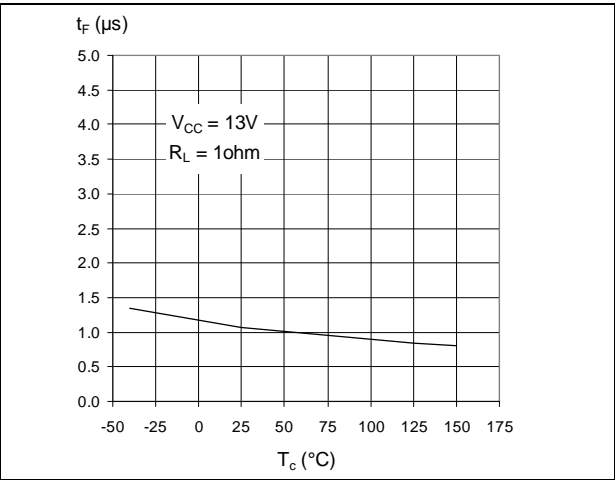


Figure 31. Output voltage fall time





When a fault condition is detected, the user can know which power element is in fault by monitoring the  $IN_A$ ,  $IN_B$ ,  $DIAG_A/EN_A$  and  $DIAG_B/EN_B$  pins.

In any case, when a fault is detected, the faulty leg of the bridge is latched off. To turn on the respective output ( $OUT_X$ ) again, the input signal must rise from low to high level.

### 3.1 Reverse battery protection

Three possible solutions can be considered:

a Schottky diode D connected to  $V_{CC}$  pin

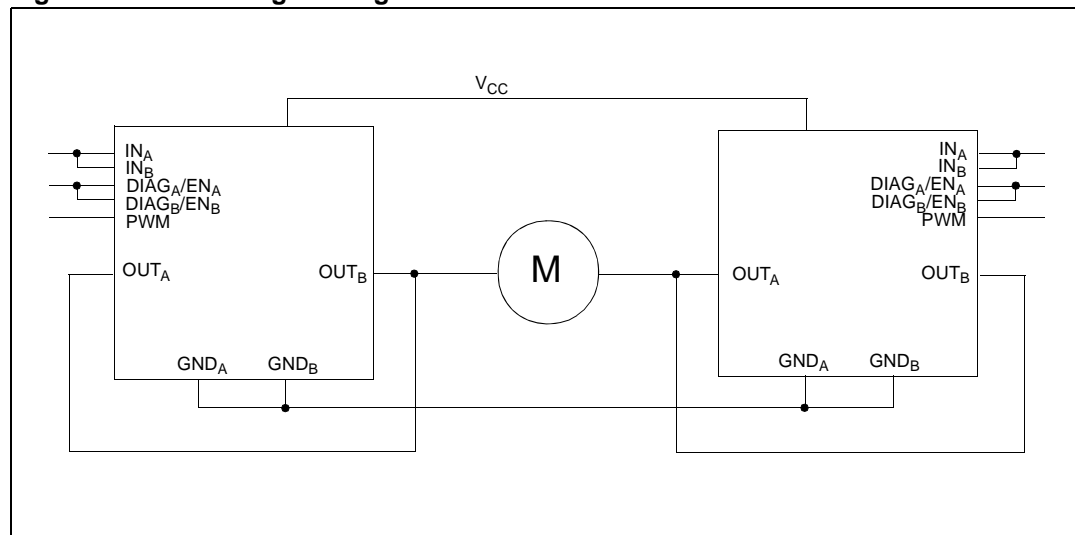
an N-channel MOSFET connected to the GND pin (see [Figure 32: Typical application circuit for DC to 20 kHz PWM operation short circuit protection on page 20](#))

a P-channel MOSFET connected to the  $V_{CC}$  pin

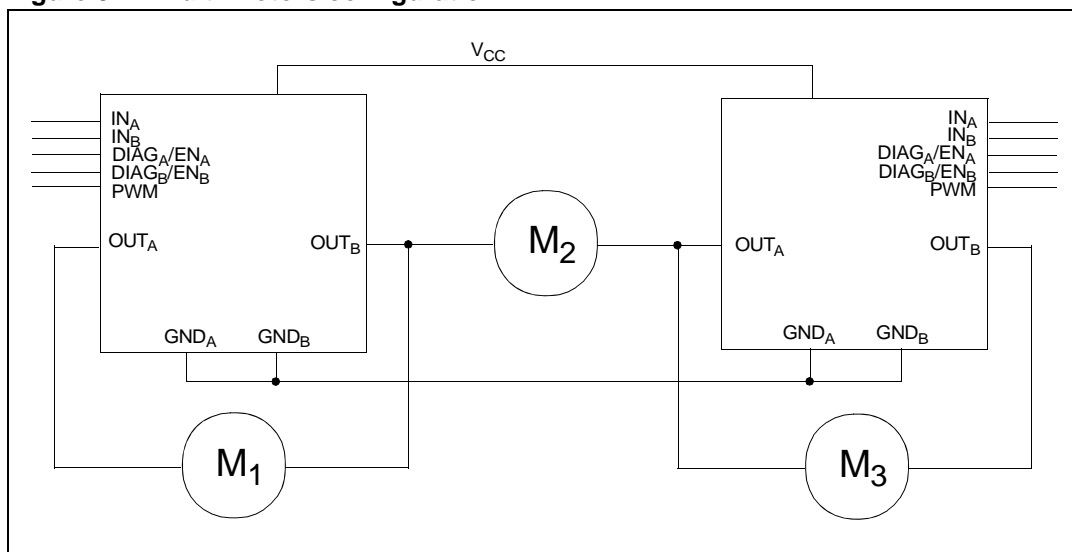
The device sustains no more than -30A in reverse battery conditions because of the two body diodes of the power MOSFETs. Additionally, in reverse battery condition the I/Os of are pulled down to the  $V_{CC}$  line (approximately -1.5V). A series resistor must be inserted to limit the current sunk from the microcontroller I/Os. If  $I_{Rmax}$  is the maximum target reverse current through  $\mu C$  I/Os, the series resistor is:

$$R = \frac{V_{IOs} - V_{CC}}{I_{Rmax}}$$

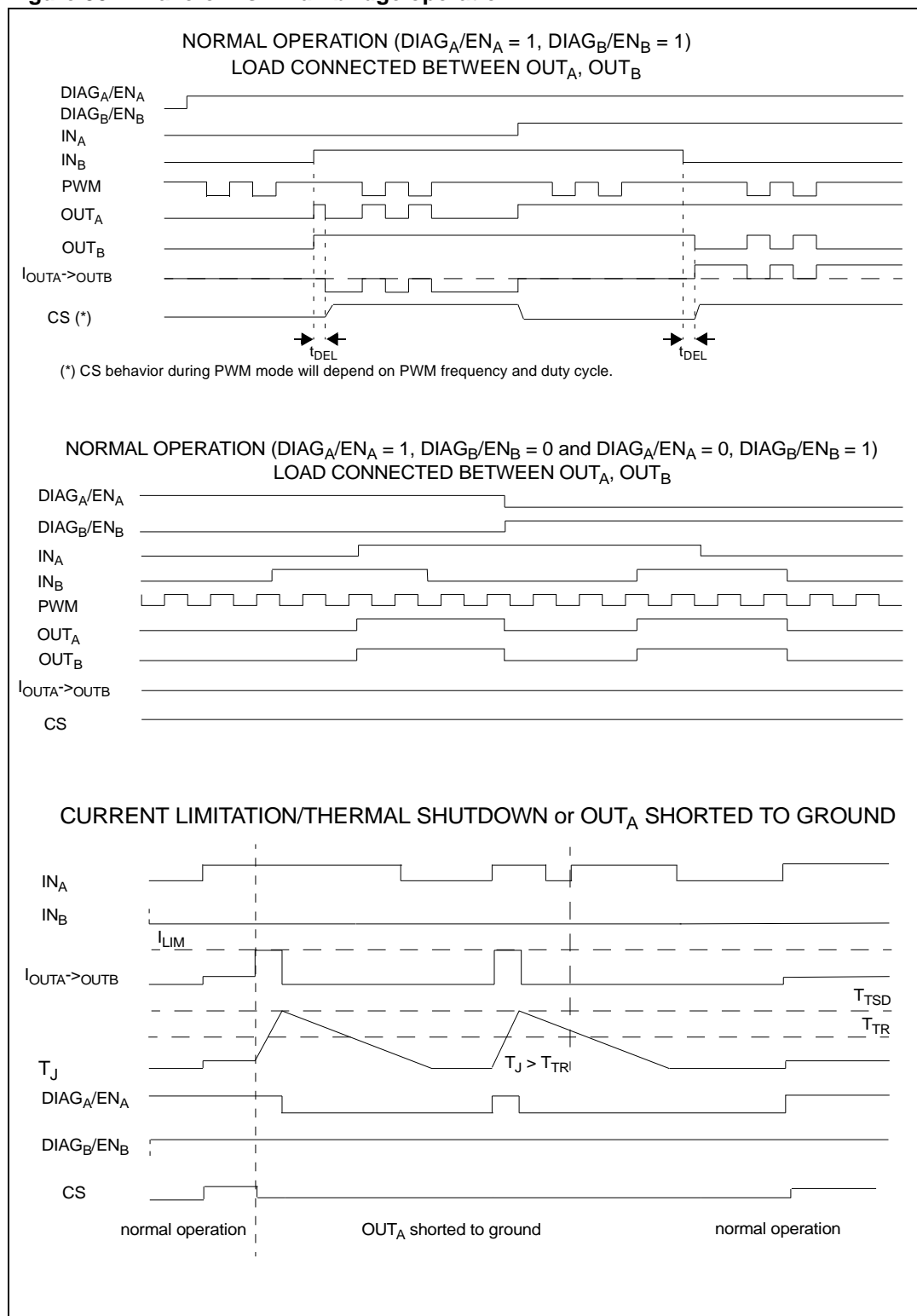
**Figure 33. Half-bridge configuration**

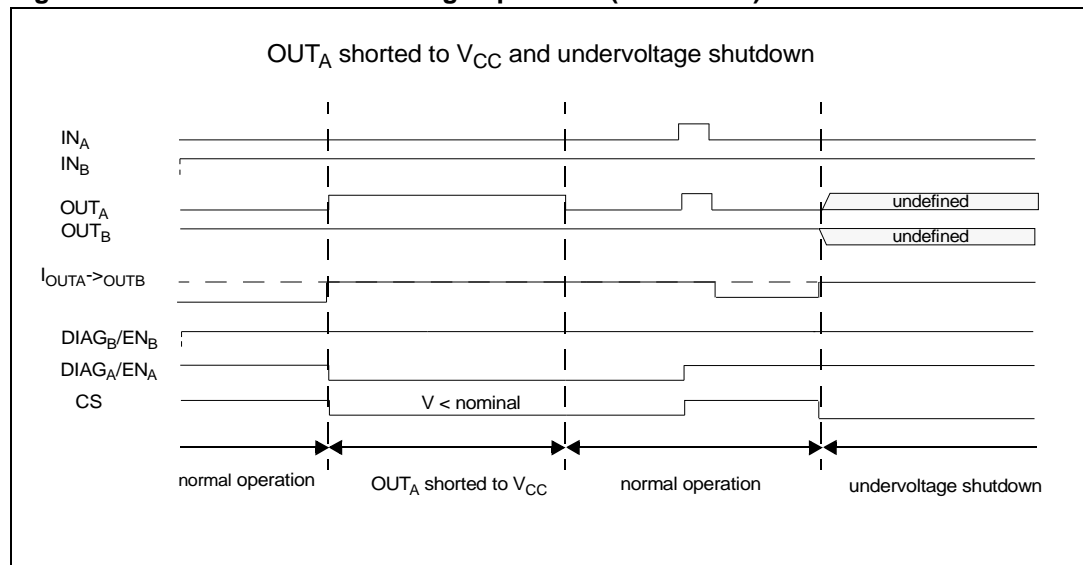


**Note:** The VN3ASP30-E can be used as a high power half-bridge driver achieving an On resistance per leg of 21 mΩ.

**Figure 34. Multi-motors configuration**

**Note:** The VN3ASP30-E can easily be designed in multi-motors driving applications such as seat positioning systems where only one motor must be driven at a time. DIAG<sub>X</sub>/EN<sub>X</sub> pins allow to put unused half-bridges in high impedance.

**Figure 35. Waveforms in full-bridge operation**

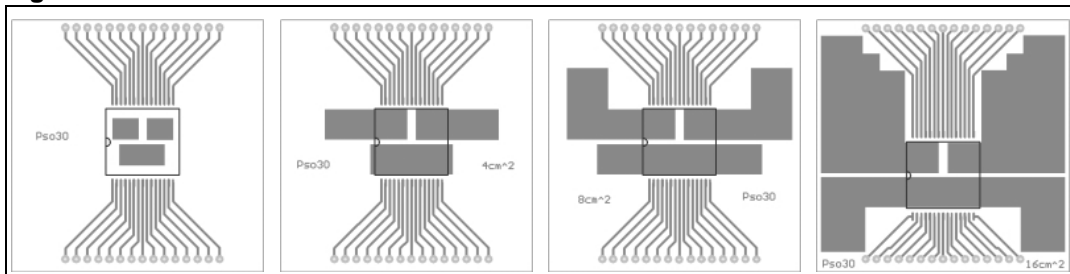
**Figure 36. Waveforms in full-bridge operation (continued )**



## 4 Package and PCB thermal data

### 4.1 MultiPowerSO-30 thermal data

Figure 37. MultiPowerSO-30™ PC board



Note: Layout condition of  $R_{th}$  and  $Z_{th}$  measurements (PCB FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35 $\mu$ m, Copper areas: from minimum pad lay-out to 16cm<sup>2</sup>).

Figure 38. Chipset configuration

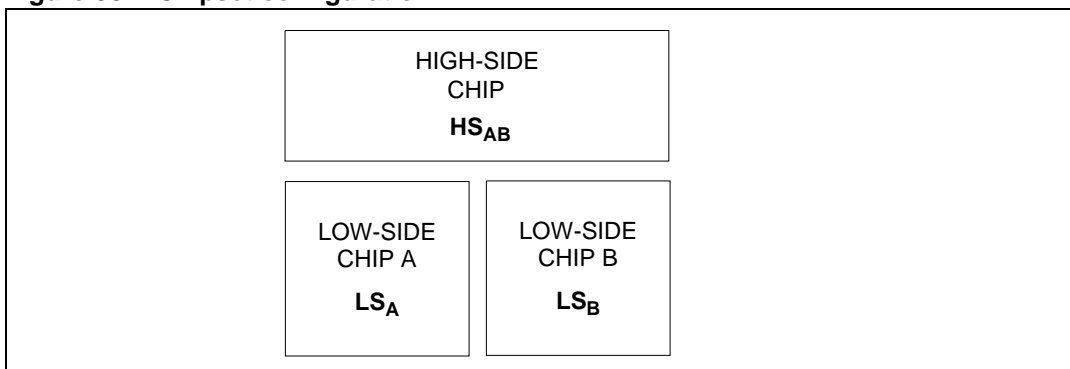
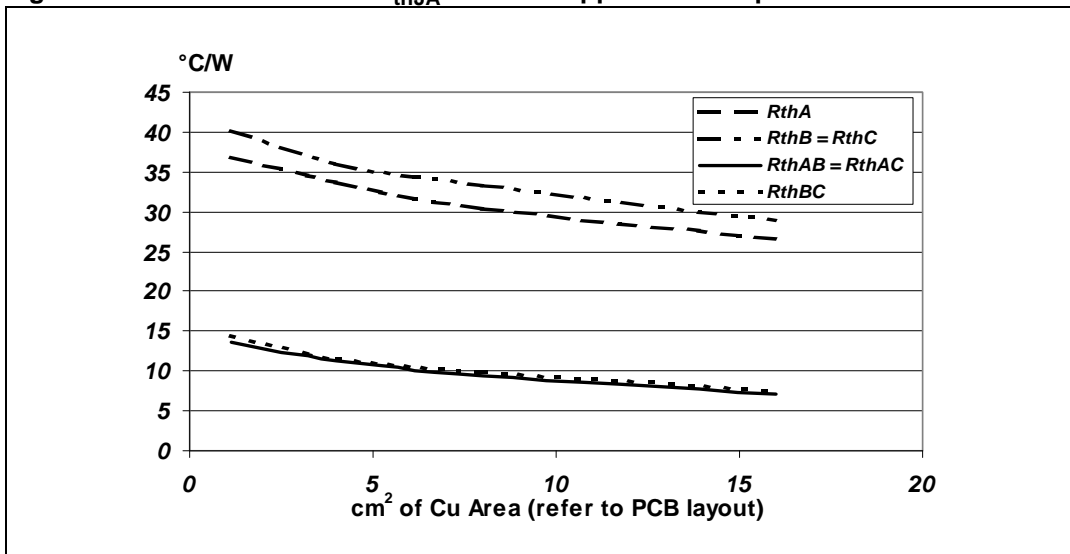


Figure 39. Auto and mutual  $R_{thJA}$  vs PCB copper area in open box free air condition



#### 4.1.1 Thermal calculation in clockwise and anti-clockwise operation in Steady-state mode

Table 15. Thermal calculation in clockwise and anti-clockwise operation in Steady-state mode

HS <sub>A</sub>	HS <sub>B</sub>	LS <sub>A</sub>	LS <sub>B</sub>	T <sub>JHSAB</sub>	T <sub>JLSA</sub>	T <sub>JLSB</sub>
ON	OFF	ON		$P_{dHSA} \times R_{thHS} + P_{dLSB} \times R_{thHSLs} + T_A$	$P_{dHSA} \times R_{thHSLs} + P_{dLSB} \times R_{thLSLS} + T_A$	$P_{dHSA} \times R_{thHSLs} + P_{dLSB} \times R_{thLS} + T_A$
OFF	ON	OFF		$P_{dHSB} \times R_{thHS} + P_{dLSA} \times R_{thHSLs} + T_A$	$P_{dHSB} \times R_{thHSLs} + P_{dLSA} \times R_{thLS} + T_A$	$P_{dHSB} \times R_{thHSLs} + P_{dLSA} \times R_{thLSLS} + T_A$

#### 4.1.2 Thermal resistances definition (values according to the PCB heatsink area)

$R_{thHS} = R_{thHSA} = R_{thHSB}$  = High-Side Chip Thermal Resistance Junction to Ambient (HS<sub>A</sub> or HS<sub>B</sub> in ON state)

$R_{thLS} = R_{thLSA} = R_{thLSB}$  = Low-Side Chip Thermal Resistance Junction to Ambient

$R_{thHSLs} = R_{thHSALSB} = R_{thHSBLSA}$  = Mutual Thermal Resistance Junction to Ambient between High-Side and Low-Side Chips

$R_{thLSLS} = R_{thLSALSB}$  = Mutual Thermal Resistance Junction to Ambient between Low-Side Chips

#### 4.1.3 Thermal calculation in Transient mode<sup>(a)</sup>

$$T_{JHSAB} = Z_{thHS} \times P_{dHSAB} + Z_{thHSLs} \times (P_{dLSA} + P_{dLSB}) + T_A$$

$$T_{JLSA} = Z_{thHSLs} \times P_{dHSAB} + Z_{thLS} \times P_{dLSA} + Z_{thLSLS} \times P_{dLSB} + T_A$$

$$T_{JLSB} = Z_{thHSLs} \times P_{dHSAB} + Z_{thLSLS} \times P_{dLSA} + Z_{thLS} \times P_{dLSB} + T_A$$

#### 4.1.4 Single pulse thermal impedance definition (values according to the PCB heatsink area)

$Z_{thHS}$  = High-Side Chip Thermal Impedance Junction to Ambient

$Z_{thLS} = Z_{thLSA} = Z_{thLSB}$  = Low-Side Chip Thermal Impedance Junction to Ambient

$Z_{thHSLs} = Z_{thHSABLSA} = Z_{thHSABLSB}$  = Mutual Thermal Impedance Junction to Ambient between High-Side and Low-Side Chips

$Z_{thLSLS} = Z_{thLSALSB}$  = Mutual Thermal Impedance Junction to Ambient between Low-Side Chips

a. Calculation is valid in any dynamic operating condition. P<sub>d</sub> values set by user.

## Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where  $\delta = t_p / T$

Figure 40. MultiPowerSO-30 HSD thermal impedance junction ambient single pulse

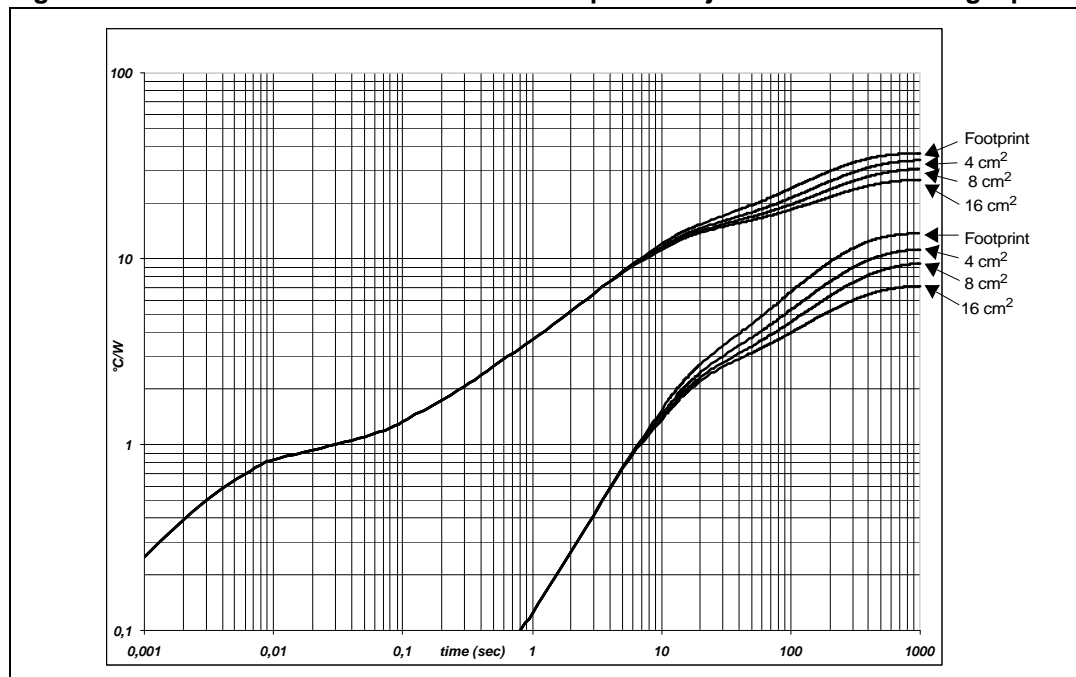
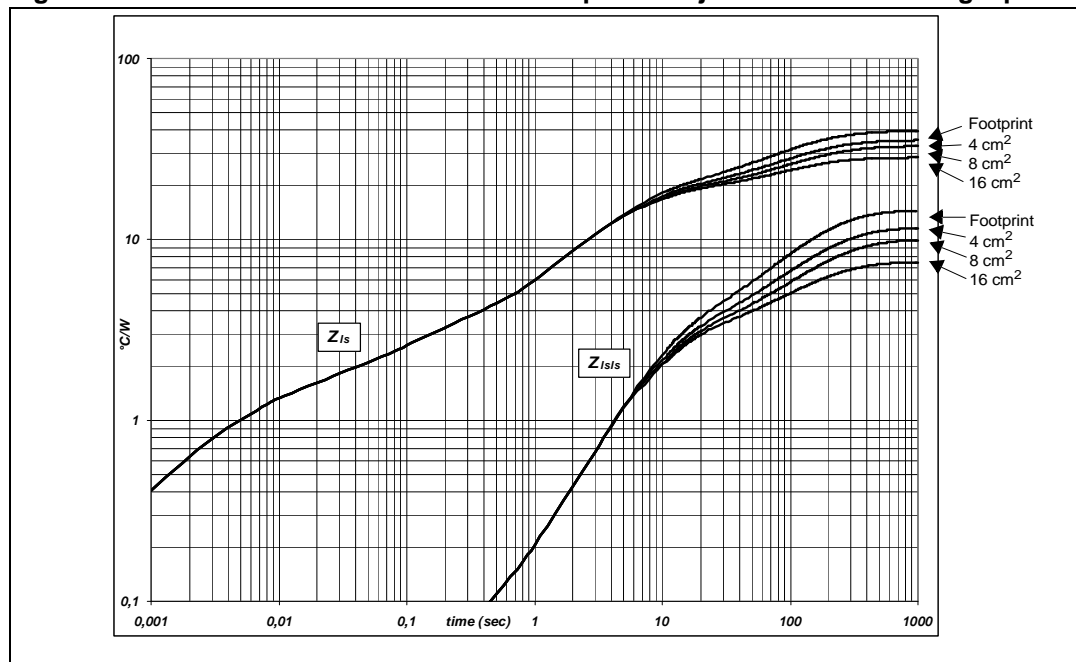
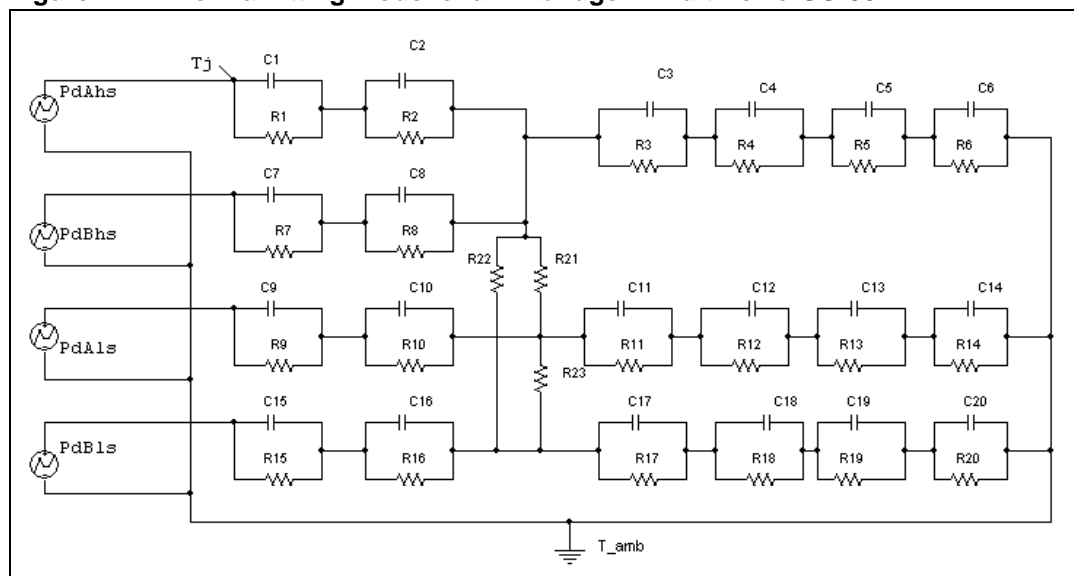


Figure 41. MultiPowerSO-30 LSD thermal impedance junction ambient single pulse



**Figure 42. Thermal fitting model of an H-bridge in MultiPowerSO-30****Table 16. Thermal parameters<sup>(1)</sup>**

Area/island (cm <sup>2</sup> )	Footprint	4	8	16
R1 = R7 (°C/W)	0.05			
R2 = R8 (°C/W)	0.3			
R3 (°C/W)	0.5			
R4 (°C/W)	1.3			
R5 (°C/W)	14			
R6 (°C/W)	44.7	39.1	31.6	23.7
R9 = R15 (°C/W)	0.11			
R10 = R16 (°C/W)	0.21			
R11 = R17 (°C/W)	0.42			
R12 = R18 (°C/W)	1.5			
R13 = R19 (°C/W)	20			
R14 = R20 (°C/W)	46.9	36.1	30.4	20.8
R21 = R22 = R23 (°C/W)	115			
C1 = C7 (W.s/°C)	0.005			
C2 = C8 (W.s/°C)	0.008			
C3	0.01			
C4 = C13 = C19 (W.s/°C)	0.3			
C5 (W.s/°C)	0.6			
C6 (W.s/°C)	5	7	9	11
C9 = C15 (W.s/°C)	0.0016			
C10 = C16 (W.s/°C)	0.0032			
C11 = C17 (W.s/°C)	0.0053			
C12 = C18 (W.s/°C)	0.075			
C14 = C20 (W.s/°C)	2.5	3.5	4.5	5.5

1. The blank space means that the value is the same as the previous one.

## 5 Package and packing information

### 5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

### 5.2 MultiPowerSO-30 package mechanical data

Figure 43. MultiPowerSO-30 package outline

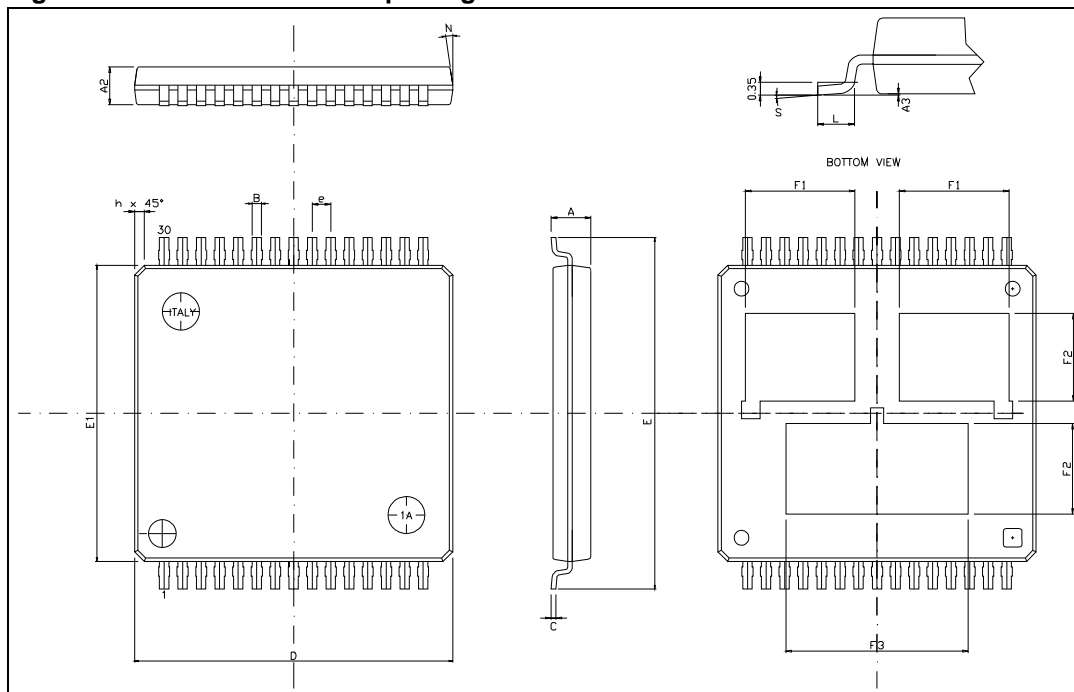


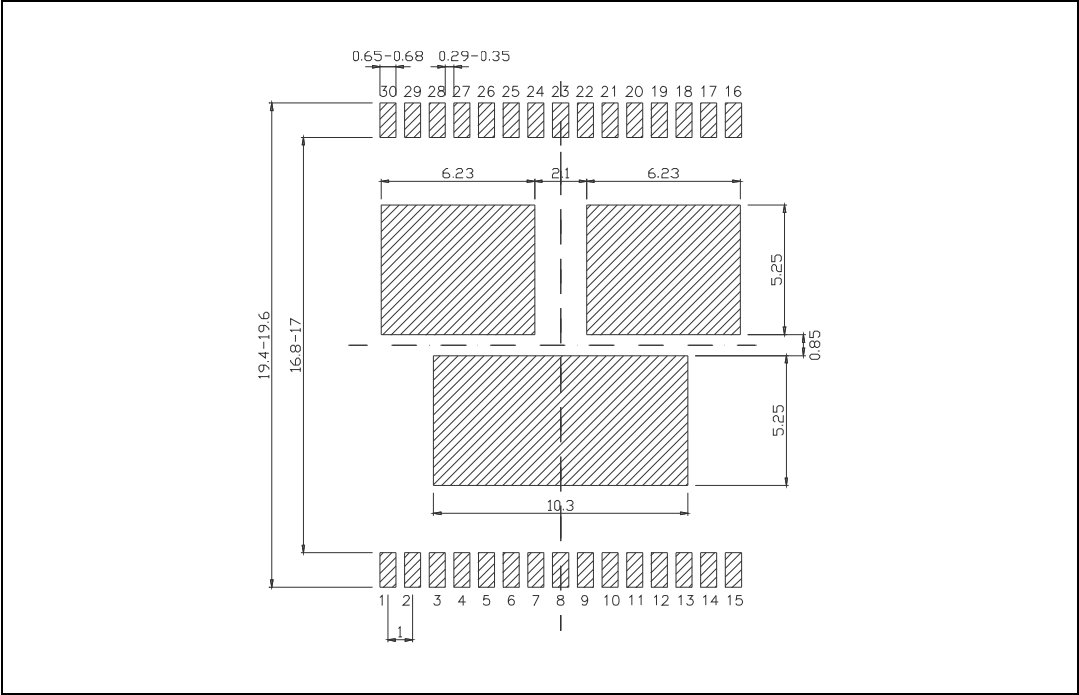
Table 17. MultiPowerSO-30 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			2.35
A2	1.85		2.25
A3	0		0.1
B	0.42		0.58
C	0.23		0.32
D	17.1	17.2	17.3
E	18.85		19.15

Table 17. MultiPowerSO-30 mechanical data (continued)

Symbol	Millimeters		
	Min	Typ	Max
E1	15.9	16	16.1
e		1	
F1	5.55		6.05
F2	4.6		5.1
F3	9.6		10.1
L	0.8		1.15
N			10 deg
S	0 deg		7 deg

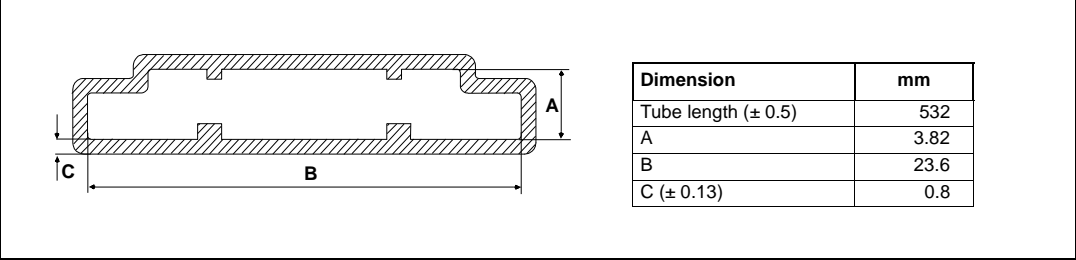
Figure 44. MultiPowerSO-30 suggested pad layout



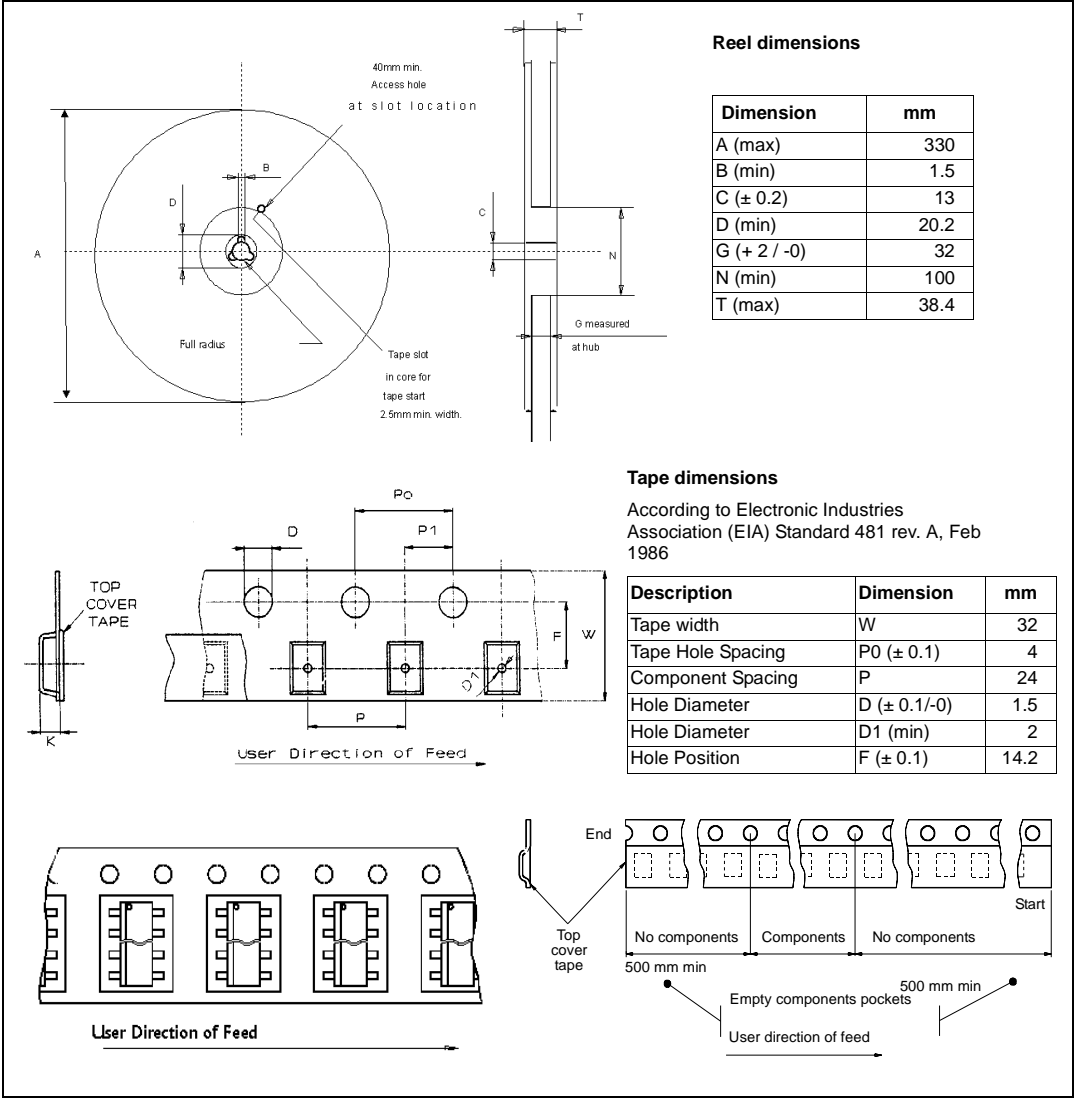
### 5.3 Packing information

*Note:* The devices can be packed in tube or tape and reel shipments (see the [Device summary on page 1](#) for packaging quantities).

**Figure 45. MultiPowerSO-30 tube shipment (no suffix)**



**Figure 46. MultiPowerSO-30 tape and reel shipment (suffix “TR”)**



## 6 Revision history

**Table 18. Document revision history**

Date	Revision	Description of changes
Sep-2004	1	First issue
Dec-2005	2	Resistance per leg modification <a href="#">Figure 33: Half-bridge configuration on page 21</a>
23-Feb-2007	3	<p>Document converted into new ST template.</p> <p>Changed <a href="#">Features on page 1</a> to add ECOPACK<sup>®</sup> package</p> <p>Removed Table 7. Thermal Data from page 4</p> <p><a href="#">Table 6: Power section on page 9</a>: Changed test conditions and max values for supply current in Off state and On state</p> <p><a href="#">Table 7: Logic inputs (INA, INB, ENA, ENB) on page 9</a>: Modified parameter descriptions for <math>I_{INL}</math> and <math>I_{INH}</math></p> <p><a href="#">Table 8: PWM on page 10</a>: Modified parameter descriptions for <math>I_{PWL}</math> and <math>I_{PWH}</math></p> <p><a href="#">Table 10: Protection and diagnostic on page 10</a>: Modified all symbols except <math>I_{LIM}</math> and <math>V_{CLP}</math></p> <p><a href="#">Table 11 on page 11</a>: Changed test conditions for <math>K_2</math> analog sense current drift</p> <p><a href="#">Section Table 13.: Truth table in fault conditions (detected on OUTA) on page 14</a>: Changed first of two fault conditions</p> <p><a href="#">Figure 6: Definition of the high-side switching times on page 13</a>: Added vertical limitation line to left side of <math>t_{D(off)}</math> arrow</p> <p><a href="#">Figure 36: Waveforms in full-bridge operation (continued) on page 24</a>: Added dotted vertical limitation lines</p> <p>Added <a href="#">Section 2.3: Electrical characteristics curves on page 16</a></p> <p>Added <a href="#">Section 4: Package and PCB thermal data on page 25</a></p> <p>Added <a href="#">Section 5: Package and packing information on page 29</a></p> <p>Updated disclaimer on last page</p>
01-Jun-2007	4	<p>Document reformatted.</p> <p><a href="#">Table 6: Power section on page 9</a>: changed test conditions and max values for supply current in Off state</p>
06-Feb-2008	5	Corrected Heat Slug numbers in <a href="#">Table 3: Pin definitions and functions</a> .
23-Sep-2013	6	Updated Disclaimer.



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