

# AS5270

## High-Resolution On-Axis Magnetic Angular Position Sensor

### General Description

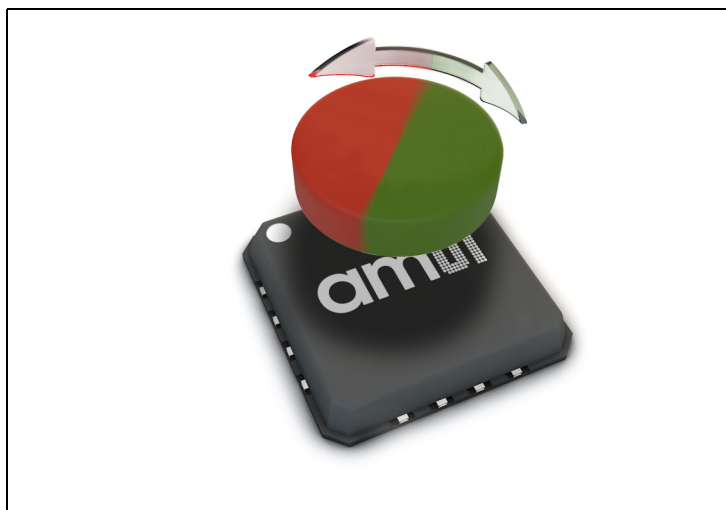
The AS5270 is a dual-die, high-resolution angular position sensor for precise absolute angle measurement. The AS5270 is available with an analog output interface (AS5270A) or a digital output interface (AS5270B). The latter can be programmed as a PWM or a SENT-compliant output interface.

Based on a Hall sensor technology, this device measures the orthogonal component of the flux density ( $B_z$ ) over a full-turn rotation and compensates for external stray magnetic fields with a robust architecture based on a 14-bit sensor array and analog front-end (AFE). A sub-range can be programmed to achieve the best resolution for the application. To measure the angle, only a simple two-pole magnet rotating over the center of the package is required. The magnet may be placed above or below the device. The absolute angle measurement provides an instant indication of the magnet's angular position. The AS5270 operates at a supply voltage of 5V, and the supply and output pins are protected against overvoltage up to +20V. In addition the supply pins are protected against reverse polarity up to -20V.

The AS5270A is a stacked dual-chip for high-reliability redundant operation. In this device, two chips are aligned and encapsulated in the same package. Separate pins are provided for each chip, so no electrical fault in the device can affect both chips.

*Ordering Information and Content Guide appear at end of datasheet.*

**Figure 1:**  
**Typical Arrangement of AS5270 and a Magnet**



## Key Benefits and Features

The benefits and features of this device are listed below:

**Figure 2:**  
**Added Value of Using AS5270**

| Benefits  | Features  |
|---|---|
| <ul style="list-style-type: none"> <li>Resolve small angular excursion with high accuracy</li> </ul>          | <ul style="list-style-type: none"> <li>12-bit resolution @90° minimum arc</li> </ul>                  |
| <ul style="list-style-type: none"> <li>Accurate angle measurement</li> </ul>                                  | <ul style="list-style-type: none"> <li>Low output noise, low inherent INL</li> </ul>                  |
| <ul style="list-style-type: none"> <li>Higher durability and lower system costs (no shield needed)</li> </ul> | <ul style="list-style-type: none"> <li>Magnetic stray field immunity</li> </ul>                       |
| <ul style="list-style-type: none"> <li>Enabler for safety critical applications</li> </ul>                    | <ul style="list-style-type: none"> <li>Functional safety, diagnostics, dual redundant chip</li> </ul> |
| <ul style="list-style-type: none"> <li>Suitable for automotive applications</li> </ul>                        | <ul style="list-style-type: none"> <li>AEC-Q100 Grade 0 qualified</li> </ul>                          |

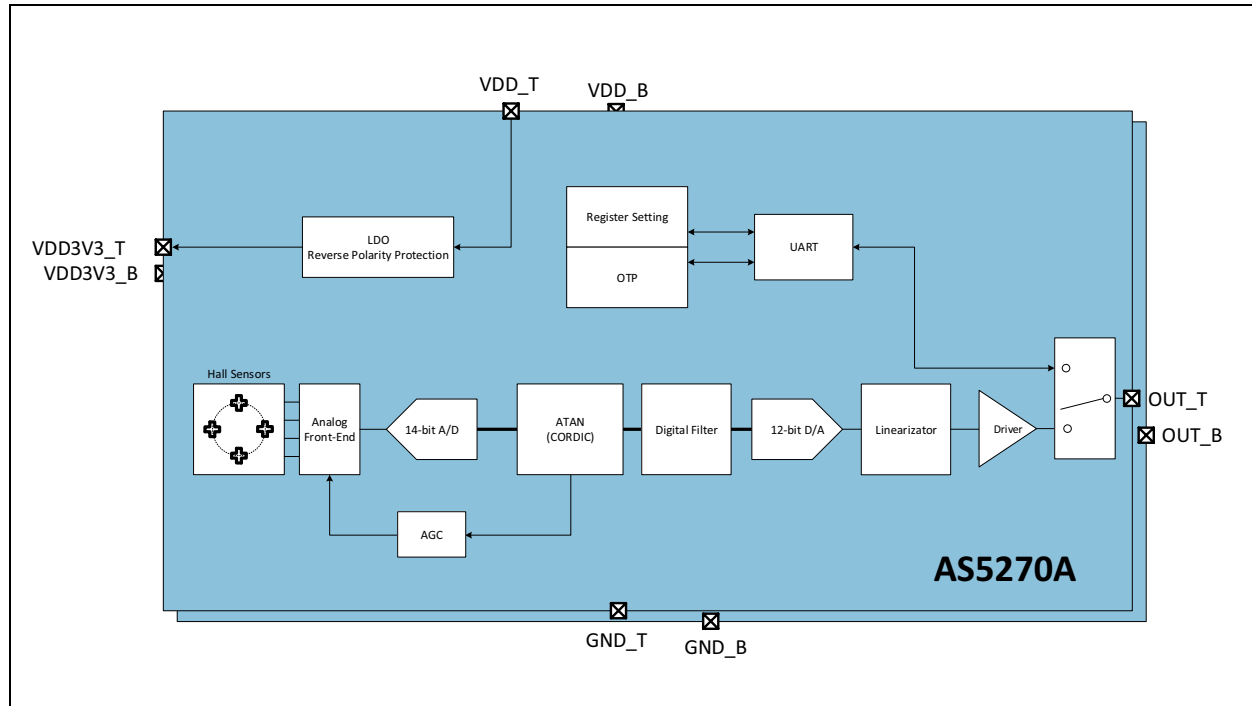
## Applications

The AS5270 is ideal for automotive applications like brake and gas pedals, throttle valve and tumble flaps, steering angle sensors, chassis ride, EGR, fuel-level measurement systems, 2/4WD switch, and contactless potentiometers.

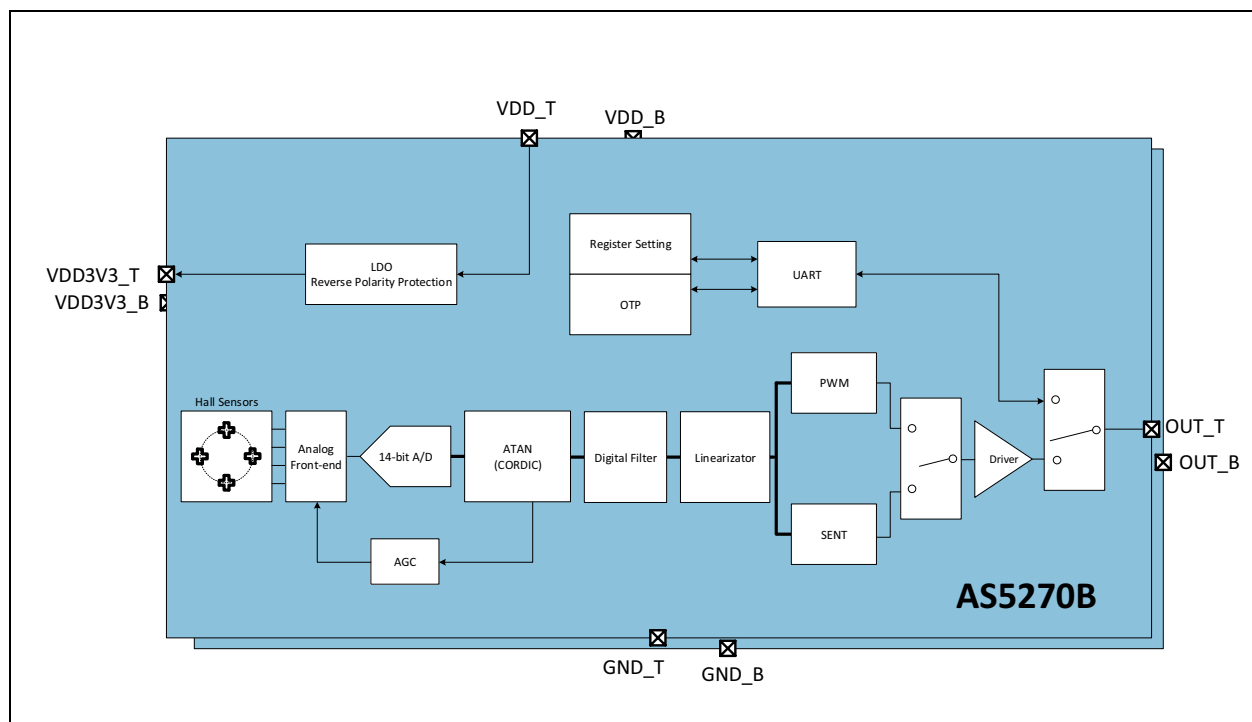
## Block Diagram

The functional blocks of the AS5270A and AS5270B are shown below:

**Figure 3:**  
**Functional Blocks of the AS5270A**



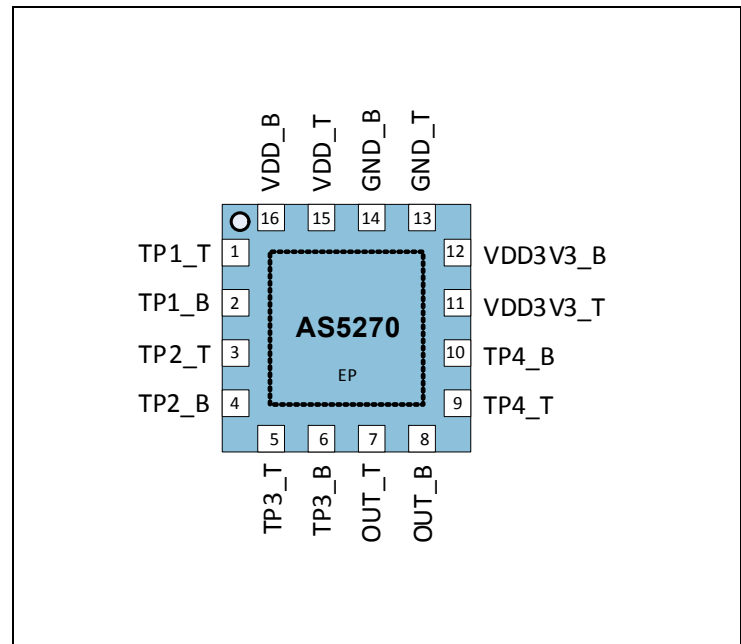
**Figure 4:**  
**Functional Blocks of the AS5270B**



## Pin Assignments

**Figure 5:**  
AS5270A/B Pin Assignment (Top View, MLF-16)

The suffix on the signal name indicates which of the two internal chips is connected to the pin (T = top die, B = bottom die). The package contains two identical chips, and no pins are shared by both chips.



**Figure 6:**  
AS5270A/B Pin Description (MLF-16)

| Pin Number | Pin Name | Pin Type  | Description            | Comments  |
|------------|----------|---|------------------------|---|
| MLF-16     |          |   |                        |   |
| 1          | TP1_T    | n.a.  | Test pin               | Connected to ground                                   |
| 2          | TP1_B    | n.a.  | Test pin               | Connected to ground                                   |
| 3          | TP2_T    | n.a.  | Test pin               | Leave open  |
| 4          | TP2_B    | n.a.  | Test pin               | Leave open  |
| 5          | TP3_T    | n.a.  | Test pin               | Connected to ground                                   |
| 6          | TP3_B    | n.a.  | Test pin               | Connected to ground                                   |
| 7          | OUT_T    | Analog output (AS5270A)<br>Digital output (AS5270B) | Output interface die 1 | AS5270A: Analog output<br>AS5270B: PWM or SENT output |
| 8          | OUT_B    | Analog output (AS5270A)<br>Digital output (AS5270B) | Output interface die 2 | AS5270A: Analog output<br>AS5270B: PWM or SENT output |

| Pin Number | Pin Name | Pin Type | Description           | Comments  |
|------------|----------|----------|-----------------------|---|
| MLF-16     |          |          |                       |   |
| 9          | TP4_T    | n.a.     | Test pin              | To be connected to OUT_T if both OUT_T and OUT_B are connected to a pull-down or pull-up resistor. To be connected to the output pin (OUT_T or OUT_B, respectively) which is connected to the pull-down resistor in case OUT_T and OUT_B are connected one to a pull-down resistor and the other to a pull-up resistor. |
| 10         | TP4_B    | n.a.     | Test pin              | To be connected to OUT_B if both OUT_T and OUT_B are connected to a pull-down or pull-up resistor. To be connected to the output pin (OUT_T or OUT_B, respectively) which is connected to the pull-down resistor in case OUT_T and OUT_B are connected one to a pull-down resistor and the other to a pull-up resistor. |
| 11         | VDD3V3_T | Supply   | Positive supply die 1 |   |
| 12         | VDD3V3_B | Supply   | Positive supply die 2 |   |
| 13         | GND_T    | Supply   | Ground die 1          |   |
| 14         | GND_B    | Supply   | Ground die 2          |   |
| 15         | VDD_T    | Supply   | Positive supply die 1 |   |
| 16         | VDD_B    | Supply   | Positive supply die 2 |   |
| EP         |          |          | Exposed pad           | Must be connected to ground   |

## Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 7:**  
**Absolute Maximum Ratings**

| Symbol  | Parameter                                 | Min     | Max | Units | Comments        |
|---|---|---------|-----|-------|-----------------|
| <b>Electrical Parameters</b>  |   |         |     |       |                 |
| VDD   | DC Supply Voltage at VDD pin              | -20     | 20  | V     | Not operational |
| VOUT  | External DC voltage at OUT pin            | -0.3    | 20  | V     | Permanent       |
| VDIFF   | DC voltage difference between VDD and OUT | -20     | 20  |       |                 |
| VREGOUT   | DC voltage at the VDD3V3 pin              | -0.3    | 5.0 | V     |                 |
| ISCR  | Input Current (latch-up immunity)         | -100    | 100 | mA    | AEC-Q100-004    |
| <b>Continuous Power Dissipation (<math>T_{AMB} = 70^{\circ}\text{C}</math>)</b> |   |         |     |       |                 |
| $P_T$   | Continuous Power Dissipation              |         | 300 | mW    |                 |
| <b>Electrostatic Discharge</b>  |   |         |     |       |                 |
| ESD <sub>HBM</sub>  | Electrostatic Discharge HBM               | $\pm 2$ |     | kV    | AEC-Q100-002    |

| Symbol   | Parameter                          | Min | Max | Units | Comments   |
|--|------------------------------------|-----|-----|-------|--|
| <b>Temperature Ranges and Storage Conditions</b> |                                    |     |     |       |  |
| $T_{AMB}$  | Operating Temperature Range        | -40 | 150 | °C    | Ambient temperature  |
| $T_{STRG}$                                       | Storage Temperature Range          | -55 | 125 | °C    | 150°C for 1000h  |
| $T_{BODY}$                                       | Package Body Temperature           |     | 260 | °C    | The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn) |
| $RH_{NC}$  | Relative Humidity (non-condensing) | 5   | 85  | %     |  |
| MSL  | Moisture Sensitivity Level         | 3   |     |       | Represents a maximum floor life time of 168 hours  |

## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 8:**  
Operating Conditions

| Symbol | Parameter                  | Conditions   | Min | Typ  | Max | Unit |
|--------|----------------------------|--|-----|------|-----|------|
| VDD    | Positive supply voltage    |  | 4.5 | 5.0  | 5.5 | V    |
| VREG   | Regulated Voltage          | VDD3V3 should not be loaded by any external DC current | 3.3 | 3.45 | 3.6 | V    |
| IDD_A  | Supply current AS5270A     | AGC=255 (no magnet placed); 2 times for AS5270A        | 4   |      | 12  | mA   |
| IDD_B  | Supply current AS5270B     | AGC=255 (no magnet placed); 2 times for AS5270B        | 4   |      | 10  | mA   |
| ISTART | Supply current at start-up | VREG = 2.25V   | 2.5 | 5    | 10  | mA   |
| TSUP   | Start-up time              | Functional mode  |     |      | 10  | ms   |

**Note(s):**

- The given tolerances for external components need to be assured over the whole operation conditions range and also over lifetime. Overall condition:  $T_{AMB} = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , VDD=4.5V to 5.5V; Components spec; unless otherwise noted.

**Figure 9:**  
Electrical System Characteristics

| Symbol  | Parameter                        | Conditions  | Min  | Typ | Max | Unit |
|---------|----------------------------------|---|------|-----|-----|------|
| CRES    | Core resolution                  |   |      |     | 14  | bit  |
| ARES    | Analog resolution (AS5270A)      | Range > 90°   |      |     | 12  | bit  |
| DRES    | Digital resolution (AS5270B)     |   |      |     | 12  | bit  |
| INLopt  | Integral non-linearity (optimum) | Best aligned reference magnet <sup>(2)</sup> at 25°C over full turn 360°                            | -0.5 |     | 0.5 | deg  |
| INLtemp | Integral non-linearity (optimum) | Best aligned reference magnet <sup>(2)</sup> over temperature -40°C to 150°C over full turn 360°    | -0.9 |     | 0.9 | deg  |
| INL     | Integral non-linearity           | Best aligned reference magnet* over temperature -40°C to 150°C over full turn 360° and displacement | -1.4 |     | 1.4 | deg  |
| ON      | Output noise peak to peak        | Static conditions - filter on   |      |     | 1   | LSB  |
| ST      | Sampling time                    |   |      | 125 |     | μs   |

**Note(s):**

- $T_{AMB} = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$ , VDD = 4.5V to 5.5V (5Voperation), Magnetic Characterization; unless otherwise noted.
- Reference magnet: NdFeB, 8 mm diameter, 2.5 mm thickness



**Figure 10:**  
**Power Management - Supply Monitor - Timing**

| Symbol  | Parameter                        | Conditions  | Min | Typ  | Max  | Unit |
|---------|----------------------------------|---|-----|------|------|------|
| VDDUVTH | VDD undervoltage upper threshold |   | 3.5 | 4.0  | 4.5  | V    |
| VDDUVTL | VDD undervoltage lower threshold |   | 3.0 | 3.5  | 4.0  | V    |
| VDDUV   | VDD undervoltage hysteresis      |   | 300 | 500  | 900  | mV   |
| UVDT    | VDD undervoltage detection time  |   | 10  | 50   | 250  | μs   |
| UVRT    | Undervoltage recovery time       |   | 10  | 50   | 250  | μs   |
| VDDOVTH | VDD overvoltage upper threshold  |   | 6.0 | 6.5  | 7.0  | V    |
| VDDOVL  | VDD overvoltage lower threshold  |   | 5.5 | 6.0  | 6.5  | V    |
| VDDOH   | VDD overvoltage hysteresis       |   | 300 | 500  | 900  | V    |
| OVDT    | VDD overvoltage detection time   | From the time VDD exceeding 5.5V  | 500 | 1000 | 2000 | μs   |
| OVRT    | VDD overvoltage recovery time    | From the time VDD returning from VDD > 5.5V to normal operating voltage (4.5V < VDD < 5.5V) | 500 | 1000 | 2000 | μs   |
| TDETWD  | WatchDog error detection time    |   |     |      | 12   | ms   |

**Figure 11:**  
**Magnetic Characteristics**

| Symbol              | Parameter   | Conditions  | Min | Typ | Max | Unit |
|---------------------|---|---|-----|-----|-----|------|
| Bz                  | Orthogonal magnetic field strength                | Required orthogonal component of the magnetic field strength measured at the package surface along a circle of 1.25 mm<br>$M_{FER} = 0$ | 30  |     | 70  | mT   |
| BzE                 | Orthogonal magnetic field strength –Extended mode | Required orthogonal component of the magnetic field strength measured at the package surface along a circle of 1.25mm<br>$M_{FER} = 1$  | 10  |     | 90  | mT   |
| Disp <sup>(2)</sup> | Displacement radius                               | Offset between defined device center and magnet axis. Dependent on the selected magnet.   |     | 0.5 |     | mm   |

**Note(s):**

1.  $T_{AMB} = -40^{\circ}$  to  $150^{\circ}\text{C}$ ,  $V_{DD} = 4.5\text{V}$  to  $5.5\text{V}$ , unless otherwise noted.
2. Reference magnet: NdFeB, 6 mm diameter, 2.5 mm thickness

**Figure 12:**  
**Electrical and Timing Characteristics Analog Output (AS5270A)**

| Symbol | Parameter  | Conditions   | Min   | Typ | Max  | Unit          |
|--------|--|--|-------|-----|------|---------------|
| INLOS  | INL output stage                                     |  | -6    |     | +6   | LSB           |
| DNLOS  | DNL output stage                                     |  | -5    |     | +5   | LSB           |
| RERR   | Ratiometricity error                                 |  | -0.5% |     | 0.5% | VDD           |
| BVPU   | Output voltage broken VDD with pull-up resistor      | Pull-up resistor must be in the specified range (see <a href="#">Figure 31</a> )   | 96    |     | 100  | %VDD          |
| BGPD   | Output voltage broken ground with pull-down resistor | Pull-down resistor must be in the specified range (see <a href="#">Figure 31</a> ) | 0     |     | 4    | %VDD          |
| OSSCG  | Output short-circuit current GND                     | OUT = GND  | 5     | 10  | 20   | mA            |
| OSSCV  | Output short-circuit current VDD                     | OUT = VDD  | -20   | -10 | -5   | mA            |
| OSSDT  | Output short-circuit detection time                  | OUT = GND or OUT = VDD   | 20    | 200 | 600  | $\mu\text{s}$ |
| OSSRT  | Output short-circuit recovery time                   |  | 2     | 5   | 20   | ms            |

| Symbol | Parameter   | Conditions  | Min  | Typ | Max | Unit |
|--------|---|---|------|-----|-----|------|
| OLCH   | Output level clamping high                        | Output current at OUT pin -3 mA   | 96   |     |     | %VDD |
| OLCL   | Output level clamping low                         | Output current at OUT pin 3 mA  |      |     | 4   | %VDD |
| OSPSR  | Output stage positive step response (driver only) | From 0 to 90%VDD, measured at OUT pin, with RPUOUT = 4.7kΩ, CLOAD = 1nF, VDD = 5V   |      |     | 250 | μs   |
| OSNSR  | Output stage negative step response (driver only) | From VDD to 10%VDD, measured at OUT pin, with RPUOUT = 4.7kΩ, CLOAD = 1nF, VDD = 5V |      |     | 250 | μs   |
| OSTD   | Output stage temperature drift                    | Of value at mid code, info parameter not tested in production                       | -0.2 |     | 0.2 | %    |

**Note(s):**

1. For each code the ratiometricity error is defined as follows:

$$VOUTRATE = ((VOUTact - (VOUTtyp * (VDDact / VDDtyp))) / VDDtyp) * 100$$

Where

- VOUTact is the actual output voltage
- VOUTtyp is the typical output voltage
- VDDact is the actual supply voltage
- VDDtyp is the typical supply voltage

**Figure 13:**  
**Electrical and Timing Characteristics PWM Output (AS5270B)**

| Symbol   | Parameter                                   | Conditions  | Min   | Typ | Max   | Unit             |
|----------|---|---|-------|-----|-------|------------------|
| PWMSSOCG | Short-circuit output current                | OUT = GND   | 5     | 10  | 20    | mA               |
| PWMSSOCV | Short-circuit output current                | OUT = VDD   | -20   | -10 | -5    | mA               |
| PWMSSDT  | PWM short-circuit detection time            | OUT = GND or OUT = VDD  |       |     | 5     | PWM clock cycles |
| PWMSSRT  | PWM short circuit recovery time             |   |       | 6   |       | PWM clock cycles |
| BKPWMVOH | PWM output voltage high in broken condition | Broken VDD or broken GND, OUT = high, RPU = 10kΩ, PWMVOH = VDD - VOUT | 0     |     | 0.4   | V                |
| BKPWMVOL | PWM output voltage low in broken condition  | Broken VDD or broken GND, OUT = low, RPD = 10kΩ                       | 0     |     | 0.4   | V                |
| PWMF7    | PWM frequency                               | PWMFR = 111   | 112.5 | 125 | 137.5 | Hz               |
| PWMF6    | PWM frequency                               | PWMFR = 110   | 180   | 200 | 220   | Hz               |
| PWMF5    | PWM frequency                               | PWMFR = 101   | 225   | 250 | 275   | Hz               |

| Symbol | Parameter                     | Conditions  | Min  | Typ  | Max  | Unit             |
|--------|-------------------------------|---|------|------|------|------------------|
| PWMF4  | PWM frequency                 | $PWMFR = 100$   | 360  | 400  | 440  | Hz               |
| PWMF3  | PWM frequency                 | $PWMFR = 011$   | 450  | 500  | 550  | Hz               |
| PWMF2  | PWM frequency                 | $PWMFR = 010$   | 720  | 800  | 880  | Hz               |
| PWMF1  | PWM frequency                 | $PWMFR = 001$   | 900  | 100  | 1100 | Hz               |
| PWMF0  | PWM frequency                 | $PWMFR = 000$   | 1800 | 2000 | 2200 | Hz               |
| PWMVOH | PWM output voltage level high | $I_{OUT} = 5\text{ mA}$ ,<br>$PWMVOH = VDD - V_{OUT}$   | 0    |      | 0.4  | V                |
| PWMVOL | PWM output voltage level low  | $I_{OUT} = 5\text{ mA}$   | 0    |      | 0.4  | V                |
| PWMSRF | PWM slew rate fast            | Between 25% and 75% of VDD, $R_{PUOUT} = 4.7\text{ k}\Omega$ ,<br>$C_{LOUT1} = 1\text{ nF}$ , $PWMSR = 0$ | 1    | 2    | 4    | V/ $\mu\text{s}$ |
| PWMSRS | PWM slew rate slow            | Between 25% and 75% of VDD, $R_{PUOUT} = 4.7\text{ k}\Omega$ ,<br>$C_{LOUT1} = 1\text{ nF}$ , $PWMSR = 1$ | 0.5  | 1    | 2    | V/ $\mu\text{s}$ |

## Timing Characteristics

**Figure 14:**  
Electrical and Timing Characteristics SENT Output (AS5270B)

| Symbol    | Parameter                               | Conditions   | Min | Typ | Max | Unit |
|-----------|---|--|-----|-----|-----|------|
| SENTSSOC  | SENT short-circuit output current       | OUT = 20V  | 10  | 20  | 40  | mA   |
| SENTSSOC  | SENT short-circuit output current       | OUT = 0V   | -40 | -20 | -10 | mA   |
| BKSENTVOH | SENT output voltage in broken condition | Broken VDD or broken GND, RPU = 50kΩ, SENT constantly high | 0   |     | 1.2 | V    |
| SENTVOH   | SENT output voltage high                |  | 4.1 |     |     |      |
| SENTVOL   | SENT output voltage low                 |  |     |     | 0.5 | V    |
| SENTFT    | SENT fall time                          |  |     |     | 6.5 | μs   |
| SENTRT    | SENT rise time                          |  |     |     | 18  | μs   |

**Figure 15:**  
Electrical and Timing Characteristics UART Interface

| Symbol    | Parameter                      | Conditions | Min        | Typ | Max  | Unit |
|-----------|--------------------------------|------------|------------|-----|------|------|
| UARTVIH   | UART high level input voltage  |            | 70         |     |      | %VDD |
| UARTVIL   | UART low level input voltage   |            |            |     | 30   | %VDD |
| UARTVOH   | UART high level output voltage |            | VDD - 0.5V |     |      | V    |
| UARTVOL   | UART low level output voltage  |            |            |     | 0.5  | V    |
| UARTBRLIM | UART Baud rate                 |            | 2400       |     | 9600 | Baud |

## Detailed Description

The AS5270 is a Hall-based rotary magnetic position sensor using a CMOS technology. The lateral Hall sensor array converts the magnetic field component perpendicular to the surface of the chip into a voltage.

The signals coming from the Hall sensors are first amplified and filtered before being converted by the analog-to-digital converter (ADC). The output of the ADC is processed by the CORDIC block (Coordinate-Rotation Digital Computer) to compute the angle and magnitude of the magnetic field vector. The sensor and analog front-end (AFE) section works in a closed loop alongside an AGC to compensate for temperature and magnetic field variations. The calculated magnetic field strength (**MAG**), the automatic gain control (**AGC**) and the angle can be read through the output pin (OUT) in **UART** mode.

The magnetic field coordinates provided by the CORDIC block are fed to a digital filter which reduces noise. A linearization block generates the transfer function, including linearization. The AS5270 is available with three different output interfaces: analog ratiometric (AS5270A), digital PWM or SENT (AS5270B).

The output of the AS5270 can be programmed to define a starting position (zero angle) and a stop position (maximum angle). An embedded linearization algorithm allows reducing the system INL error due, for example, to mechanical misalignment, magnet imperfections, etc.

The AS5270 can be programmed through the OUT pin with a UART interface which allows writing an on-chip non-volatile memory (OTP) where the specific settings are stored. The AS5270 can be programmed by the **ams** programming tool, both at the component and board level.

## Register Description

**Figure 16:**  
Non-Volatile Memory Register Description

| Address | Bit Position | Field   | Description   |
|---------|--------------|---------|---|
| 0x0A    | 7:0          | CUSTID0 | Customer ID byte 0  |
| 0x0B    | 7:0          | CUSTID1 | Customer ID byte 1  |
| 0x0C    | 7:0          | CUSTID2 | Customer ID byte 2  |
| 0x0D    | 7:0          | CUSTID3 | Customer ID byte 3  |
| 0x0E    | 0            | PWMINV  | PWM inverted  |
|         | 1            | PWMSR   | PWM slew rate<br>(0 = PWM slew rate fast <a href="#">PWMSRF</a> ,<br>1 = PWM slew rate slow <a href="#">PWMSRS</a> )                  |
|         | 3:2          | DIGOS   | Digital output stage<br>(00 = PWM push-pull<br>01 = PWM pull-down<br>10 = PWM pull-up<br>11 = SENT)<br>It applies to the AS5710B only |
|         | 6:4          | RBKDEB  | Read-back debouncing  |
|         | 7            | n.a     | No use  |
| 0x0F    | 0            | FBS     | Failure band selection (0 = lower failure band, 1 = upper failure band)   |
|         | 2:1          | HYST    | Hysteresis across the brake point   |
|         | 4:3          | QUAD    | Quadrant selection  |
|         | 7:5          | PWMFR   | <a href="#">PWM frequency selection</a>   |
| 0x10    | 1:0          | PWMRTH  | PWM rising threshold tbd  |
|         | 3:2          | PWMFTH  | PWM falling threshold tbd   |
|         | 7:4          | SENTMID | SENT Message ID   |
| 0x11    | 4:0          | SENTTK  | SENT tick   |
|         | 5            | SENTESM | Enable SENT serial message  |
|         | 6            | SENTPP  | SENT pause pulse enable (0 = disable, 1 = enable)   |
|         | 7            | SENTRC  | SENT rolling counter enable (0 = disable, 1 = enable)   |
| 0x12    | 3:0          | n.a     | No use. Default 0   |
|         | 7:4          | n.a     | No use. Default 0   |

| Address | Bit Position | Field    | Description  |
|---------|--------------|----------|--|
| 0x13    | 3:0          | n.a      | No use. Default 0  |
|         | 7:4          | n.a      | No use. Default 0  |
| 0x14    | 7:0          | CLMPH    | Clamping level high<br>Reg 0x14[0] =LSB<br>Reg 0x15[3]=MSN                               |
| 0x15    | 3:0          |          |  |
| 0x15    | 7:4          | CLMPL    | Clamping level low<br>Reg 0x15[4] =LSB<br>Reg 0x16[7]=MSN                                |
|         | 7:0          |          |  |
| 0x16    | 7:0          |          |  |
| 0x17    | 7:0          | PPOFFSET | Post processing offset<br>Reg 0x17[0] =LSB<br>Reg 0x19[3]=MSB                            |
| 0x18    | 7:0          |          |  |
| 0x19    | 3:0          | PPGAIN   | Post processing gain<br>Reg 0x19[4] =LSB<br>Reg 0x1B[3]=MSB                              |
|         | 7:4          |          |  |
| 0x1A    | 7:0          |          |  |
| 0x1B    | 4:0          |          |  |
|         | 7:5          | BP       | Break point<br>Reg 0x1B[5] =LSB<br>Reg 0x1D[2]=MSB                                       |
| 0x1C    | 7:0          |          |  |
| 0x1D    | 2:0          |          |  |
|         | 3            | MFER     | Magnetic field extended range (1 = Bz, 0= BzE)   |
|         | 4            | AER      | Angle extended range (set to 1 if the maximum angle excursion is smaller than 22 degree) |
|         | 6:5          | FILTER   | Post processing filter   |
|         | 7            | CUSLOCK  | Customer settings lock   |
| 0x1E    | 7:0          | SIGN     | Signature for error correction code  |



**Figure 17:**  
**Volatile Memory Register Description**

| Address | Bit Position | Field       | R/W | Description  |
|---------|--------------|-------------|-----|--|
| 0x22    | 7:0          | DAC12IN     | R/W | Input word of the 12-bit output DAC<br>(Reg0x23[3] = MSB, Reg0x22[0] = LSB)      |
| 0x23    | 3:0          |             | R/W |  |
|         | 4            | DAC12INSEL  | R/W | DAC 12 input buffer selection  |
|         | 5            | DSPRN       | R/W | Digital signal processing reset  |
|         | 6            | GLOAD       | R/W | Enable of gload  |
|         | 7            | -           | -   | Not used   |
| 0x32    | 7:0          | ANGLECORDIC | R   | Angle of the CORDIC output block.<br>(Reg0x33[5] = MSB, Reg0x32[0] = LSB)        |
| 0x33    | 5:0          |             |     |  |
|         | 7:6          | -           | -   | Not used   |
| 0x34    | 7:0          | MAG         | R   | CORDIC magnitude   |
| 0x35    | 7:0          | AGC         | R   | AGC value  |
| 0x36    | 7:0          | ANGLEFILTER | R   | Angle of the digital filter output block<br>(Reg0x37[3] = MSB, Reg0x36[0] = LSB) |
| 0x37    | 3:0          |             |     |  |
| 0x37    | 7:4          | -           | -   | Not used   |

**Figure 18:**  
**Special Functions**

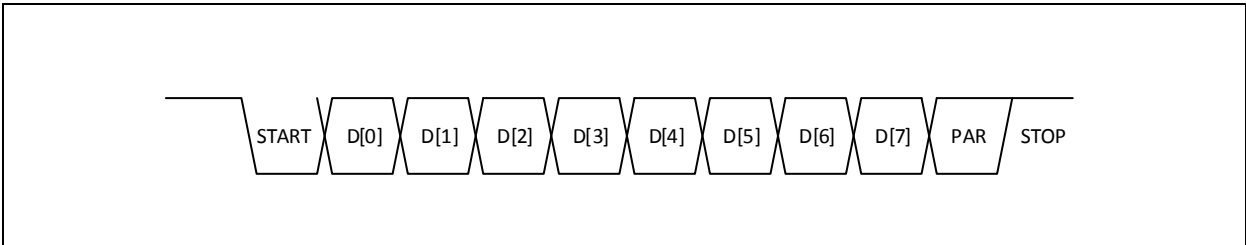
| Address | Bit Position | Field   | Description                                    |
|---------|--------------|---------|--|
| 0x60    | 7:0          | P2F     | Pass-to-functions, see <a href="#">UART</a>    |
| 0x61    | 7:0          |         |  |
| 0x62    | 7:0          | BURNOTP | Permanently burn OTP, see <a href="#">UART</a> |
| 0x63    | 7:0          |         |  |

UART Interface

The AS5270 is equipped with a UART interface, which allows reading and writing the registers as well as permanently programming the non-volatile memory (OTP). By default (factory setting) the AS5270 is in the so-called *Communication Mode* and the UART is connected at the output pin (OUT). In this mode, it is possible to configure the register settings. In this mode, the device is in open-drain mode and therefore a pull-up resistor has to be connected on the output.

The UART interface allows reading and writing two consecutive addresses. The standard UART sequence consists of four frames. Each frame begins with a start bit (START), which is followed by 8 data bits (D[0:7]), one parity bit (PAR), and a stop bit (STOP), as shown in [Figure 19](#).

Figure 19:  
UART Frame



The PAR bit is even parity calculated over the data bits (D[0:7]). Each frame is transferred from LSB to MSB.

The four frames are shown in [Figure 20](#).

Figure 20:  
UART Frame Sequence

| Frame Number | D[7]  | D[6]    | D[5] | D[4] | D[3] | D[2] | D[1] | D[0] |
|--------------|-------|---------|------|------|------|------|------|------|
| 1            | 0x55  |         |      |      |      |      |      |      |
| 2            | R/W   | ADDRESS |      |      |      |      |      |      |
| 3            | DATA1 |         |      |      |      |      |      |      |
| 4            | DATA2 |         |      |      |      |      |      |      |

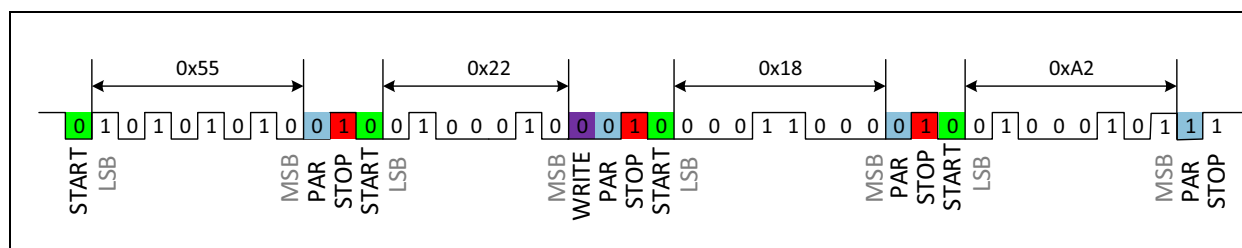
The first frame is the synchronization frame and consists of D[0:7] = 0xAA followed by the parity bit (PAR=0) and the stop bit. This frame synchronizes the baud rate between the AS5270 and the host microcontroller.

The second frame contains the read/write command (D[7] = 0 Write, D[7] = 1 Read) and the address of the register (D[6:0] = ADDRESS).

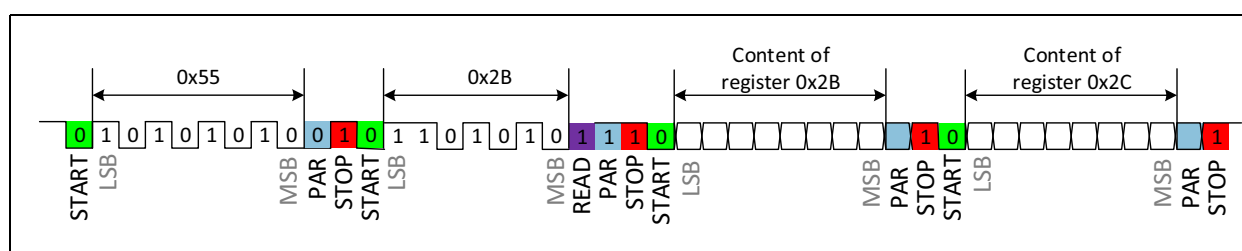
The content of the third and fourth frames (DATA1 and DATA2) will be written to or read from the location specified by ADDRESS and ADDRESS+1, respectively.

Figure 21 and Figure 22 show examples of read and write.

**Figure 21:**  
Example of Write (Reg[0x22] = 0x18, Reg[0x23] = 0xA2)



**Figure 22:**  
Example of Read (Reg[0x2B], Reg[0x2C])



## Exiting Communication Mode

Communication mode is exited and operational mode is entered with a Pass-to-function (P2F) command, by writing to the virtual registers 0x60 and 0x61:

**P2F:** write(0x60) = 0x70, write(0x61) = 0x51

No more commands can be sent after sending this command, because the device is permanently placed in operational mode.

## Burning the OTP Registers

The BURNOTP command writes the OTP registers with their programmed values. The command is issued by writing to virtual registers 0x62 and 0x63:

**BURNOTP:** write(0x62) = 0x70, write(0x63) = 0x51

## Customer ID

A specific identifier chosen by the user can be stored in the non-volatile memory. This identifier consists of 4 bytes and can be stored in the locations [CUSTID0](#), [CUSTID1](#), [CUSTID2](#), and [CUSTID3](#).

## Output Linear Transfer Function

A linear transfer function controls the state of the output in response to the absolute orientation of the external magnet. The parameters which control this function are shown in [Figure 24](#).

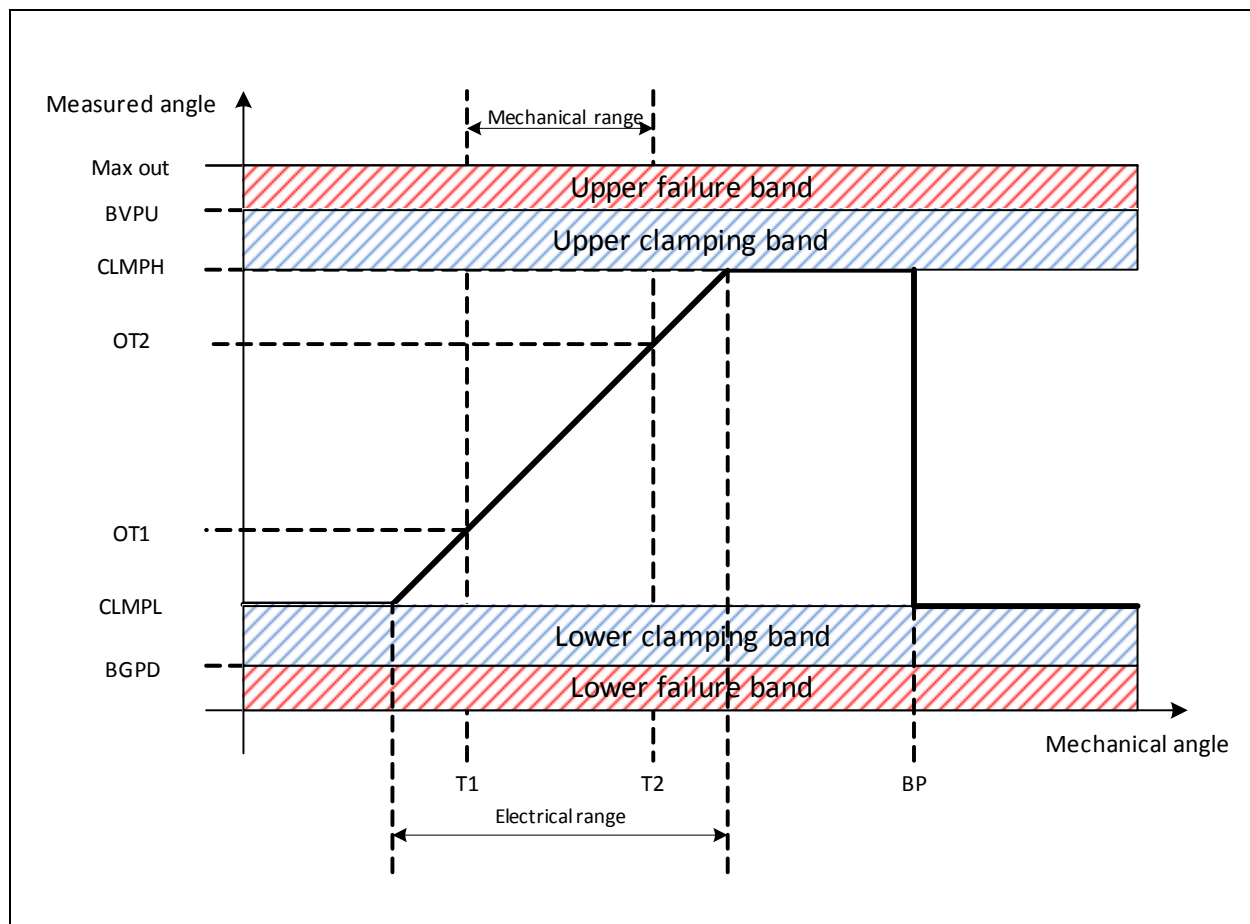
**Figure 23:**  
Transfer Function Control Parameters

| Symbol | Parameter                         | Resolution [bit] |
|--------|-----------------------------------|------------------|
| T1     | Mechanical angle starting point   | 14               |
| T2     | Mechanical angle stop point       | 14               |
| OT1    | Output at the starting point (T1) | 12               |
| OT2    | Output at the stop point (T2)     | 12               |
| CLMPL  | Clamping level low                | 12               |
| CLMPH  | Clamping level high               | 12               |
| BP     | Breakpoint                        | 14               |

As shown in the [Figure 24](#), the parameters T1, T2, OT1, and OT2 define the input-to-output linear transfer function. The dedicated programmer for the AS5270 uses the parameters from [Figure 23](#) to generate the corresponding settings [CLMPL](#), [CLMPHH](#), [PPOFFSET](#), [PPGAIN](#) and [BP](#) (see [Figure 24](#)).

The clamping level parameters [CLMPL](#) and [CLMPH](#) define the absolute minimum and maximum level of the output. Both clamping levels can be set with the 9 LSBs out of the 12-bit output resolution. This means that the maximum value for [CLMPL](#) is one eighth, while [CLMPH](#) minimum value is seven-eighths of the output diagnostic. [CLMPL](#) and [CLMPH](#) must always be set outside of the lower and upper diagnostic failure band defined by the output broken wire voltage (see [Figure 24: BGPD](#) and [BVPU](#)).

**Figure 24:**  
**Output Transfer Function**



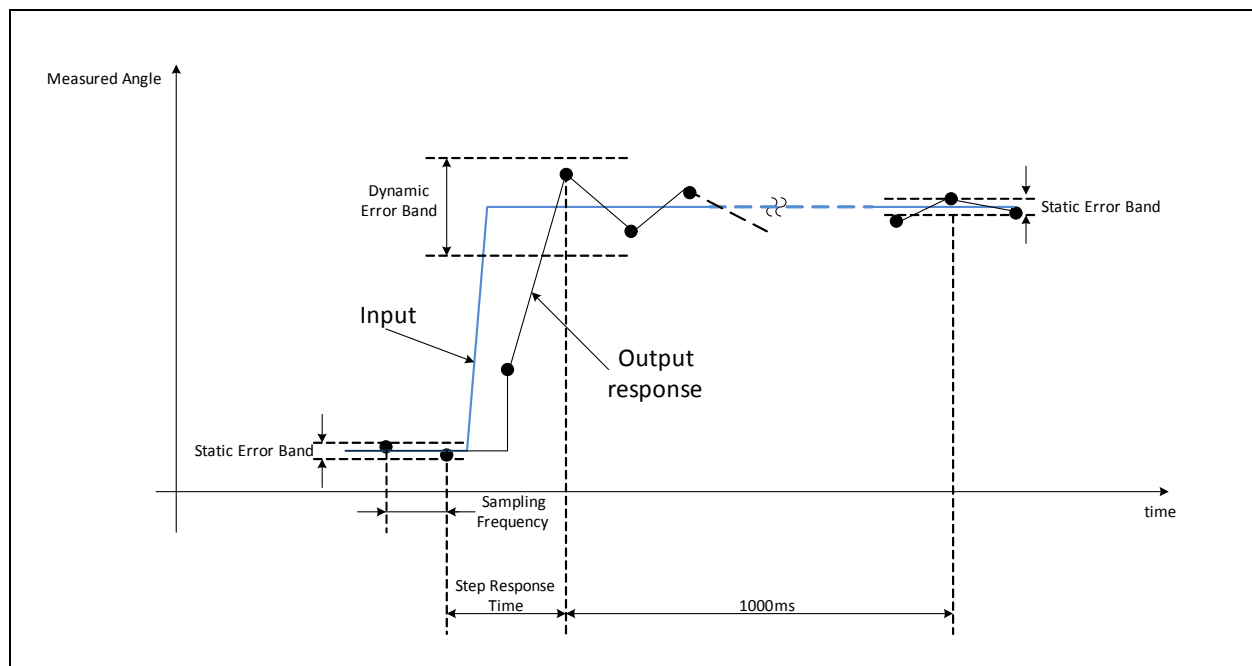
The breakpoint **BP** sets the discontinuity point where the output jumps from one clamping level to the other. It is strongly recommended to set the breakpoint at the maximum distance from the start and stop position (T1 and T2). To handle the case of a full turn, a hysteresis function across the breakpoint can be used to avoid sudden jumps between the lower and upper clamping level.

**Figure 25:**  
**Hysteresis Setting**

| HYST | Hysteresis LSBs |
|------|-----------------|
| 00   | 0               |
| 01   | 56              |
| 10   | 91              |
| 11   | 137             |

The hysteresis LSB is based on the core resolution (14-bit). The AS5270 features a programmable digital filter. As shown in Figure 25 in a static condition (no change of the input), the static error band is  $\pm 0.5$  LSB (at 12-bit resolution). Whenever an input step occurs, the output (measured angle) follows the input (mechanical angle) entering a certain error band within the step response time. From the time when the output is within the static error band the output takes 1000 ms to settle to the static error band achieving again  $\pm 0.5$  LSB output noise. The filter is not usable in  $360^\circ$  range, if the Hysteresis setting is on.

**Figure 26:**  
**Step Response**



**Figure 27:**  
**FILTER Setting**

| <b>FILTER</b> | <b>Dynamic Error Band [LSB]</b> | <b>Step Response Time [<math>\mu</math>s]</b> |
|---------------|---------------------------------|---|
| 00            | Filter off                      | Not applicable                                |
| 01            | 23                              | 5 CORDIC cycles                               |

The **FBS** setting allows selecting the failure band (lower or upper) when the output goes into diagnostic mode.

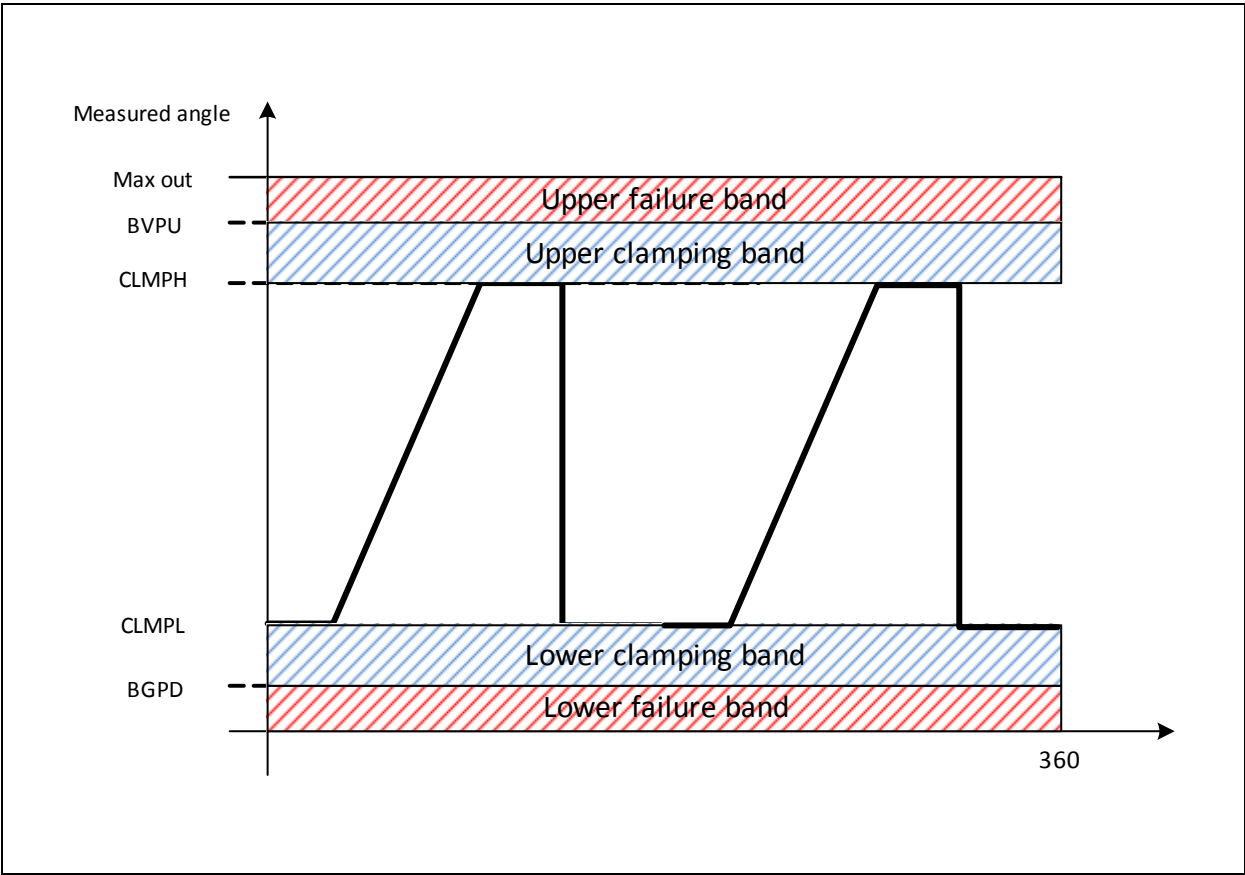
### Multiple Quadrants

The multiple quadrants option allows repeating the same output control parameters up to 4 times over the full turn rotation as shown in the Figure 29, Figure 30, and Figure 31. The **QUAD** parameter sets the number of quadrants, as shown in the Figure 28.

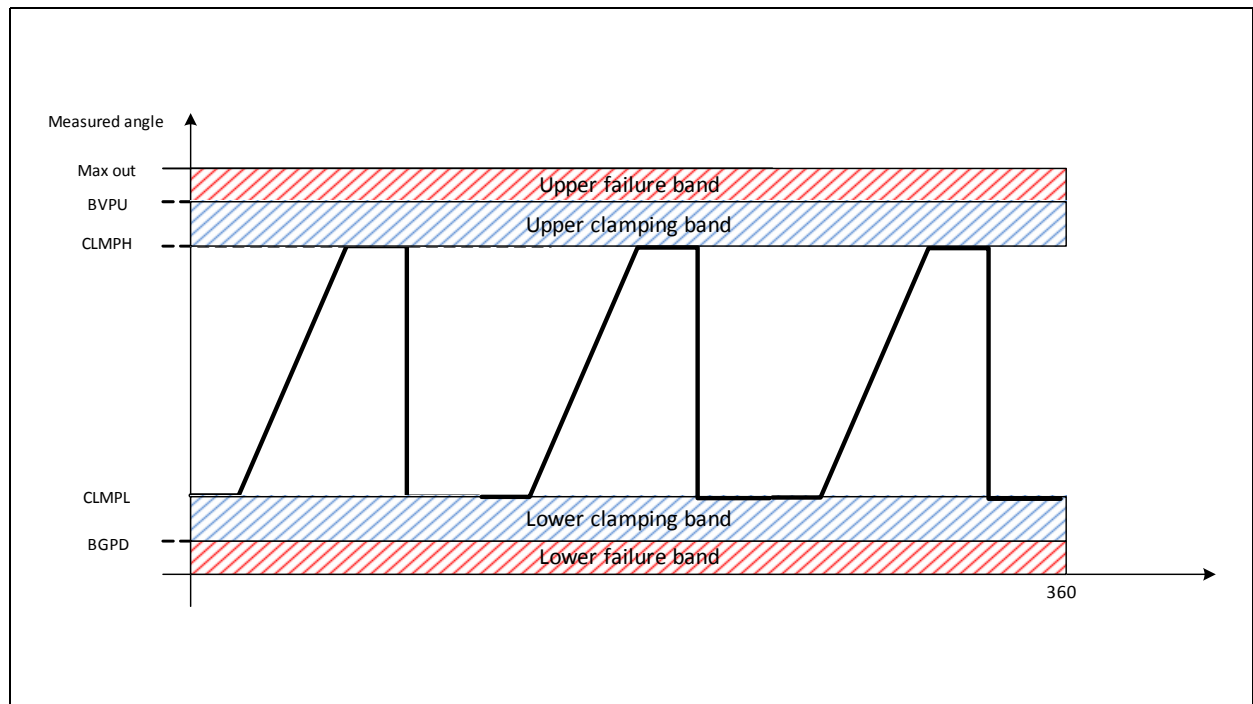
Figure 28:  
Number of Quadrants

| QUADEN | Number of Quadrants |
|--------|---------------------|
| 00     | Single              |
| 01     | Double              |
| 10     | Triple              |
| 11     | Quadruple           |

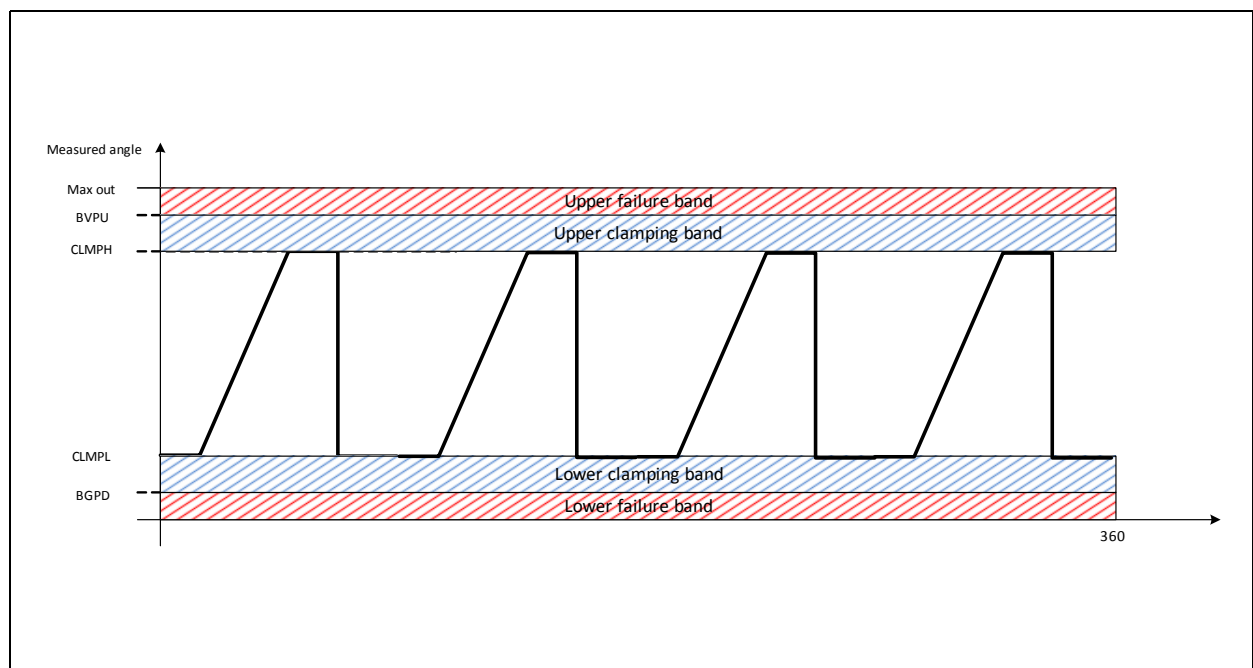
Figure 29:  
Dual Quadrant Mode



**Figure 30:**  
**Triple Quadrant Mode**



**Figure 31:**  
**Quadruple Quadrant Mode**





## Extended Magnetic Input Range

The magnetic input field range can be boosted with the [MFER](#) bit. The extended magnetic field allows increasing the maximum air gap between the AS5270 and the magnet.

More information can be found in the Application Note.

## Analog Output (AS5270A)

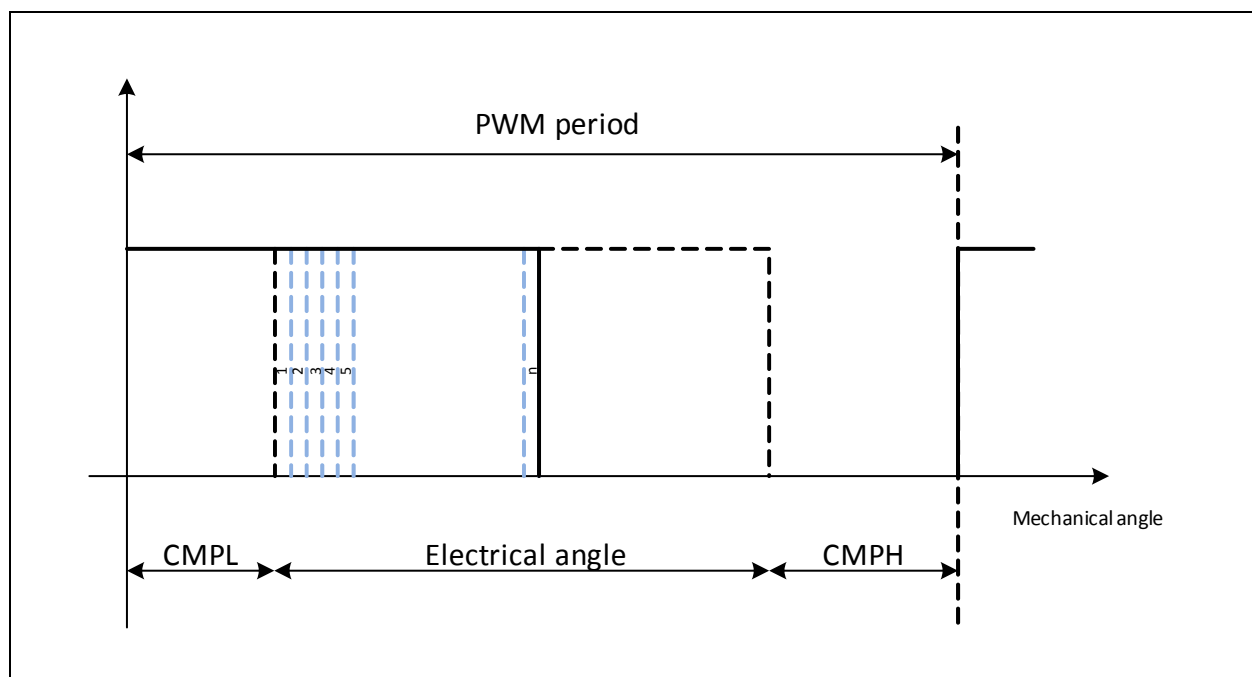
The AS5270A provides a linear analog ratiometric output signal. The output buffer features a push-pull analog output stage which can be loaded with a pull-down or a pull-up resistor. The output voltage represents the angular orientation of the magnet above the AS5270A on a linear absolute scale and is ratiometric to VDD.

## PWM Output (AS5270B)

The AS5270B has a PWM output. With the [DIGOS](#) setting, the PWM output stage can be programmed as a push-pull, pull-down, or pull-up driver. The duty-cycle of each pulse is proportional to the absolute angular position of the external magnet.

The PWM signal consists of a frame of 4096 clock periods as shown in [Figure 32](#). The PWM frame begins with a certain number of clocks high, defined by the [CLMPL](#), which is followed by the electrical angle information. The frame ends with a certain number of clock pulses low, as defined by the [CLMPH](#). It is possible to invert the frame using the [PWMINV](#) setting.

**Figure 32:**  
Pulse Width Modulation Frame



The [PWMFR](#) setting sets the duration of the PWM frequency.

The [PWMSR](#) setting chooses between fast and slow steps.

### SENT Output (AS5270B)

The AS5270B provides a SENT-compatible output (Single Edge Nibble Transmission) interface which is compliant with the SAE-J2716 standard (Jan-2010) and features the Single Secure Sensor and the Single Sensor protocol (refer to SENT\_J2716\_Standard - Appendix A.3 and A.4). SENT is a single-wire interface based on a unidirectional communication scheme from the sensor (transmitter) to the engine control unit (receiver). The sensor constantly transmits data to the receiver.

The SENT interface can be enabled on the AS5270B with the [DIGOS](#) setting.

The SENT frame consists of 8 nibbles in which each nibble is made up by 4 bits. The duration of the nibbles is variable and depends on its content and tick frequency. With the AS5270B, the tick frequency is selected by the [SENTTK](#) setting, as shown in [Figure 33](#).

**Figure 33:**  
**SENT Tick Period**

| <a href="#">SENTTK</a> | SENT Tick Period (μs) |
|------------------------|-----------------------|
| 00000                  | 3                     |
| 00001                  | 4                     |
| 00010                  | 4.5                   |
| 00011                  | 5                     |
| 00100                  | 5.5                   |
| 00101                  | 5.75                  |
| 00110                  | 6.5                   |
| 00111                  | 6.75                  |
| 01000                  | 7.5                   |
| 01001                  | 8                     |
| 01010                  | 8.5                   |
| 01011                  | 9                     |
| 01100                  | 9.5                   |
| 01101                  | 10                    |
| 01110                  | 10.25                 |
| 01111                  | 10.5                  |
| 10000                  | 10.75                 |
| 10001                  | 11                    |

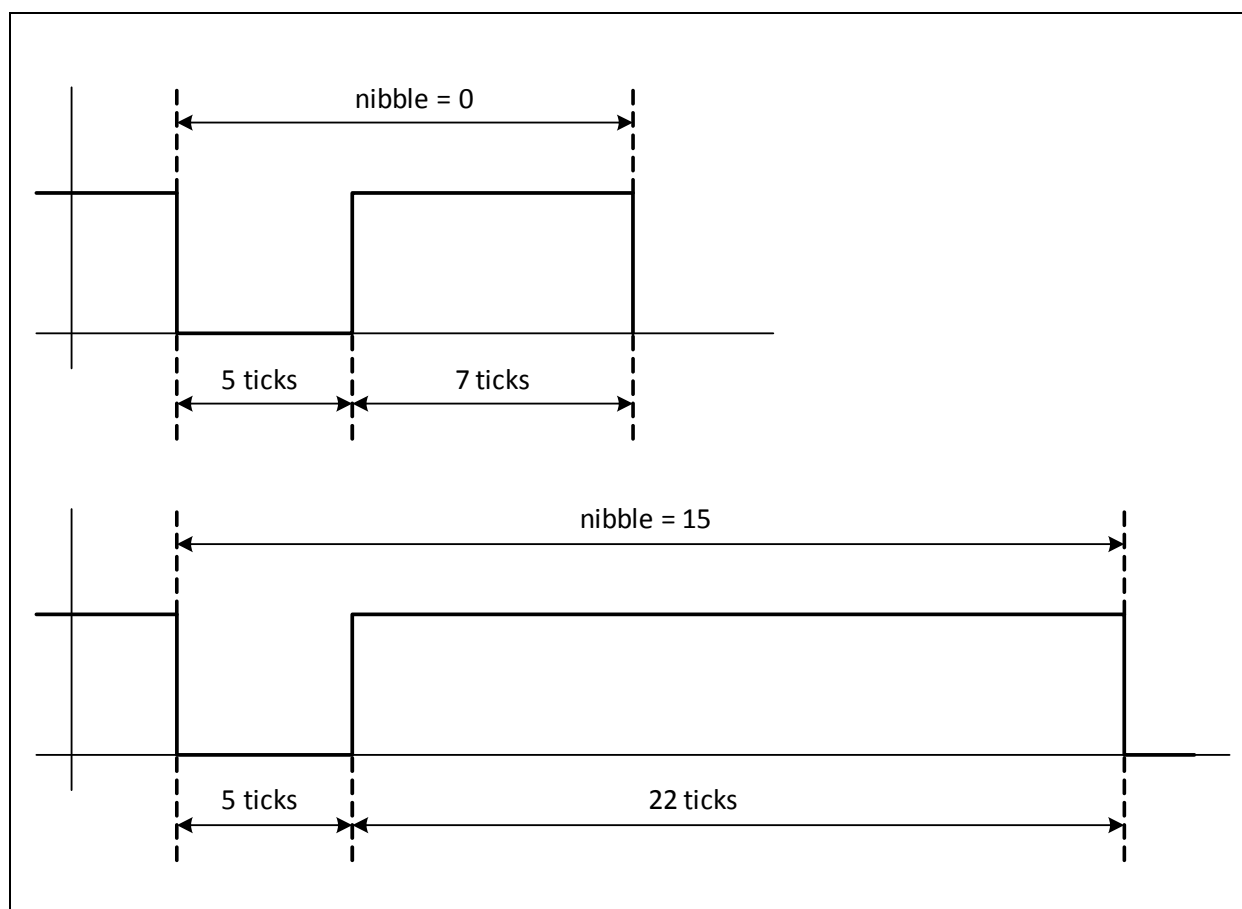
| SENTTK | SENT Tick Period ( $\mu$ s) |
|--------|-----------------------------|
| 10010  | 11.25                       |
| 10011  | 11.5                        |
| 10100  | 11.75                       |
| 10101  | 12                          |
| 10110  | 12.25                       |
| 10111  | 12.5                        |
| 11000  | 2.25                        |
| 11001  | 2.5                         |
| 11010  | 2.75                        |
| 11011  | 3                           |
| 11100  | 3.25                        |
| 11101  | 3.5                         |
| 11110  | 3.5                         |
| 11111  | 3.5                         |

The nibble protocol consists of:

- 5 clock ticks low
- 7 clock ticks + n clock ticks high

Where n is the decimal representation of the 4 bit data. If the nibble data is zero (data = 0x00, n = 0) the nibble duration is 12 ticks, while if the nibble data is 15 (data = 0xFF, n = 15) its duration is 27 ticks.

**Figure 34:**  
PWM Clock Period and Frequency



The SENT protocol consists of a 56-tick synchronization pulse followed by 8 nibbles. Each nibble is described in [Figure 35](#).

**Figure 35:**  
Nibble Description

| Nibble | Description                              |
|--------|--|
| 1      | Status and communication                 |
| 2      | Angle data most significant nibble       |
| 3      | Angle data middle significant nibble     |
| 4      | Angle data least significant nibble      |
| 5      | Rolling counter most significant nibble  |
| 6      | Rolling counter least significant nibble |
| 7      | Inverted nibble #2                       |
| 8      | CRC checksum                             |

The Status and Communication nibble includes diagnostic status and the Short Serial Message Format, as defined in the SAE J2716 protocol.

**Figure 36:**  
**Status and Communication Nibble**

| Bit | Description                                      |
|-----|--|
| 0   | Error bit: 0 = no sensor error, 1 = sensor error |
| 1   | 0 (always)                                       |
| 2   | Short Serial Message                             |
| 3   | Message Start                                    |

The Short Serial Message is transmitted one bit per SENT frame in bit 2 of consecutive frames and consists of 16 bits. The starting bit of a Short Serial Message is indicated by a 1 in bit 3 (Message Start) of the Status and Communication Nibble.

**Figure 37:**  
**Serial Message**

|                         |         |   |   |   |     |   |   |   |   |    |    |    |     |    |    |    |
|-------------------------|---------|---|---|---|-----|---|---|---|---|----|----|----|-----|----|----|----|
| SENT Message Number     | 1       | 2 | 3 | 4 | 5   | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13  | 14 | 15 | 16 |
| Message Start           | 1       | 0 | 0 | 0 | 0   | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0   | 0  | 0  | 0  |
| Short Serial Message[2] | SENTMID |   |   |   | MAG |   |   |   |   |    |    |    | CRC |    |    |    |

The Short Serial Message consists of a message ID ([SENTMID](#)) and the magnitude of the magnetic field ([MAG](#)). The Short Serial Message is protected by a 4-bit CRC.

The [SENTESM](#) bit enables the Short Serial Message, which is otherwise by default disabled.

The angular information is contained in nibbles 2, 3 and 4.

Nibbles 5 and 6 contain a rolling counter which counts the number of sent telegrams and rolls over to 0 after reaching the maximum value of 255. The rolling counter can be disabled, which is not needed in the Single Sensor mode, with the [SENTRC](#) bit.

Because the tick clock period is 3  $\mu$ s, the minimum duration of a SENT telegram is 456  $\mu$ s, while the maximum duration is 816  $\mu$ s. the [SENTPP](#) bit enables the Pause Pulse, which creates a SENT transmission with a constant duration of 272 ticks.

## Diagnostic

The AS5270 allows a high ASIL level through a robust embedded self-diagnostic.

**Figure 38:**  
**Diagnostic Table**

| SM   | Safety Mechanism                      | Recoverable   | Safe State   |
|------|---------------------------------------|---|--|
| SM1  | Watchdog failure                      | No, if a watchdog error is detected, the sensor provides the error information till a sensor reset happens    | Output is going into HIZ --> failure band (depending on output resistor)   |
| SM2  | Offset compensation not complete      | Yes, if the offset is below the specified threshold, sensor recovers the output                               | Output is forced in failure band. Depending on <a href="#">FBS</a> setting |
| SM3  | CORDIC overflow                       | Yes, if the magnetic input field is below the specified threshold, sensor recovers the output                 | Output is forced in failure band. Depending on <a href="#">FBS</a> setting |
| SM4  | Magnetic input field too high/too low | Yes, if the magnetic field is inside the specific range, after the recovery time the sensor leave the failure | Output is forced in failure band. Depending on <a href="#">FBS</a> setting |
| SM5  | Vreg undervoltage                     | Yes   | Hi-z: Failure band related to the out load                                 |
| SM6  | Reverse polarity                      | Yes, if reverse polarity issue is solved. No direct safety mechanism, it's a protection!                      | Hi-z: Failure band related to the out load                                 |
| SM7  | VDD overvoltage                       | Yes, if the VDD is below the specified threshold.   | Hi-z: Failure band related to the out load                                 |
| SM8  | VDD undervoltage                      | Yes, if the VDD is above the specified threshold  | Hi-z: Failure band related to the out load                                 |
| SM9  | Broken VDD                            | Yes   | Hi-z: Failure band related to the out load                                 |
| SM10 | ADC check                             | No, sensor stays in failure band till the Sensor is resetting.  | Hi-z: Failure band related to the out load                                 |
| SM11 | Analog read fail                      | Yes   | Hi-z: Failure band related to the out load                                 |
| SM12 | Short circuit                         | Yes   | Hi-z: Failure band related to the out load                                 |
| SM13 | Signature                             | No, sensor stays in failure band till the sensor is resetting   | Hi-z: Failure band related to the out load                                 |
| SM14 | Broken GND                            | Yes   | Hi-z: Failure band related to the out load                                 |

The [FBS](#) setting allows selecting the failure band (lower or upper) when the output goes into diagnostic mode.

**Diagnostic Explanations**

For a detailed explanation of the diagnostic and the SPFM please contact the **ams** application team for magnetic position sensor.

**Analog Read Fail (SM11)**

This safety mechanism operates differently for AS5270A (analog) and AS5270B (digital):

- For AS5270B readout failure: After a falling edge there must be a rising edge after a defined time.  
In case this is not respected output driver is kept in high impedance. After a certain time this condition is checked again.

The readout mechanism for AS5270B is defined by [PWMRTH](#) and [PWMFTH](#), which set the maximum timeout period to wait for a falling/rising before triggering an error condition, according to the figures below.

**Figure 39:**  
**PWMRTH Conditions**

| PWMRTH |   | Delay (μs)                  |
|--------|---|-----------------------------|
| 0      | 0 | PWM Read Back rise disabled |
| 0      | 1 | 24-28                       |
| 1      | 0 | 56-60                       |
| 1      | 1 | 112-120                     |

**Figure 40:**  
**PWMFTH Conditions**

| PWMFTH |   | Delay (μs)                  |
|--------|---|-----------------------------|
| 0      | 0 | PWM Read Back fall disabled |
| 0      | 1 | 24-28                       |
| 1      | 0 | 56-60                       |
| 1      | 1 | 112-120                     |

- For AS5270A readout failure: Comparison of the analog output information versus the digital information of the sensor. If the difference is too high output driver is kept in high impedance. After a certain time this condition is checked again.

The readout mechanism for AS5270A is defined by [RDBCKDEB](#), which set the maximum timeout period to wait before triggering an error condition, according to the tables below.

**Figure 41:**  
**AS5270A Readout Mechanisms**

| RDBCKDEB02 | RDBCKDEB01 | RDBCKDEB00 | CORDIC Cycles <sup>(1)</sup> | Note                      |
|------------|------------|------------|------------------------------|---------------------------|
| 0          | 0          | 0          | 0                            | Analog Read Back disabled |
| 0          | 0          | 1          | 1                            |                           |
| 0          | 1          | 0          | 2                            |                           |
| 0          | 1          | 1          | 4                            |                           |
| 1          | 0          | 0          | 8                            |                           |
| 1          | 0          | 1          | 16                           |                           |
| 1          | 1          | 0          | 32                           |                           |
| 1          | 1          | 1          | 64                           |                           |

**Note(s):**

1. 1 CORDIC cycle typ.:111µs



## Application Information

### Signature Calculation

The OTP of AS5270A and AS5270B uses a BIST technique with Multiple Input Signature Register circuits.

To activate this BIST a calculation of the Signature Byte is necessary and has to store into the OTP during the programming sequence.

For calculating the signature byte the content of the whole memory (0x02 to 0x1D) has to be read.

Out of this information the following calculation has to be done.

Byte: 0x02 = data2

....

Byte: 0x1D = data29

```
Unsigned int signature (unsigned int * content)
{
```

```
    unsigned int misr,misr_shift,misr_xor,misr_msb;
```

```
    misr = 0;
    for (int i=0; i<28; i++) {
        misr_shift = (misr<<1);
        misr_xor = (misr_shift ^ content[i])%256;
        misr_msb = misr/(128);
        if (misr_msb == 0)
            misr = misr_xor;
        else
            misr = (misr_xor ^ 29)%256;
    }
    return misr;
}
```

```
content= {,data2,data3,data4,data5,data6,
          data7,data8,data9,data10,data11,
          data12,data13,data14,data15,data16,
          data17,data18,data19,data20,data21,data22,
          data23,data24,data25,data26,data27,data28,data29};
```

## Programming Parameter

The programming has to be performed in communication mode. If the `cust_lock=0`, the sensor starts in communication mode.

The following procedure and the block diagram are showing the common 2 point calibration. For special calibration procedure:

AS5270A: Analog output driver calibration

AS5270A/AS5270B: Linearization.

Please go in contact with the **ams** application team.

## Burn and Verification of the OTP Memory

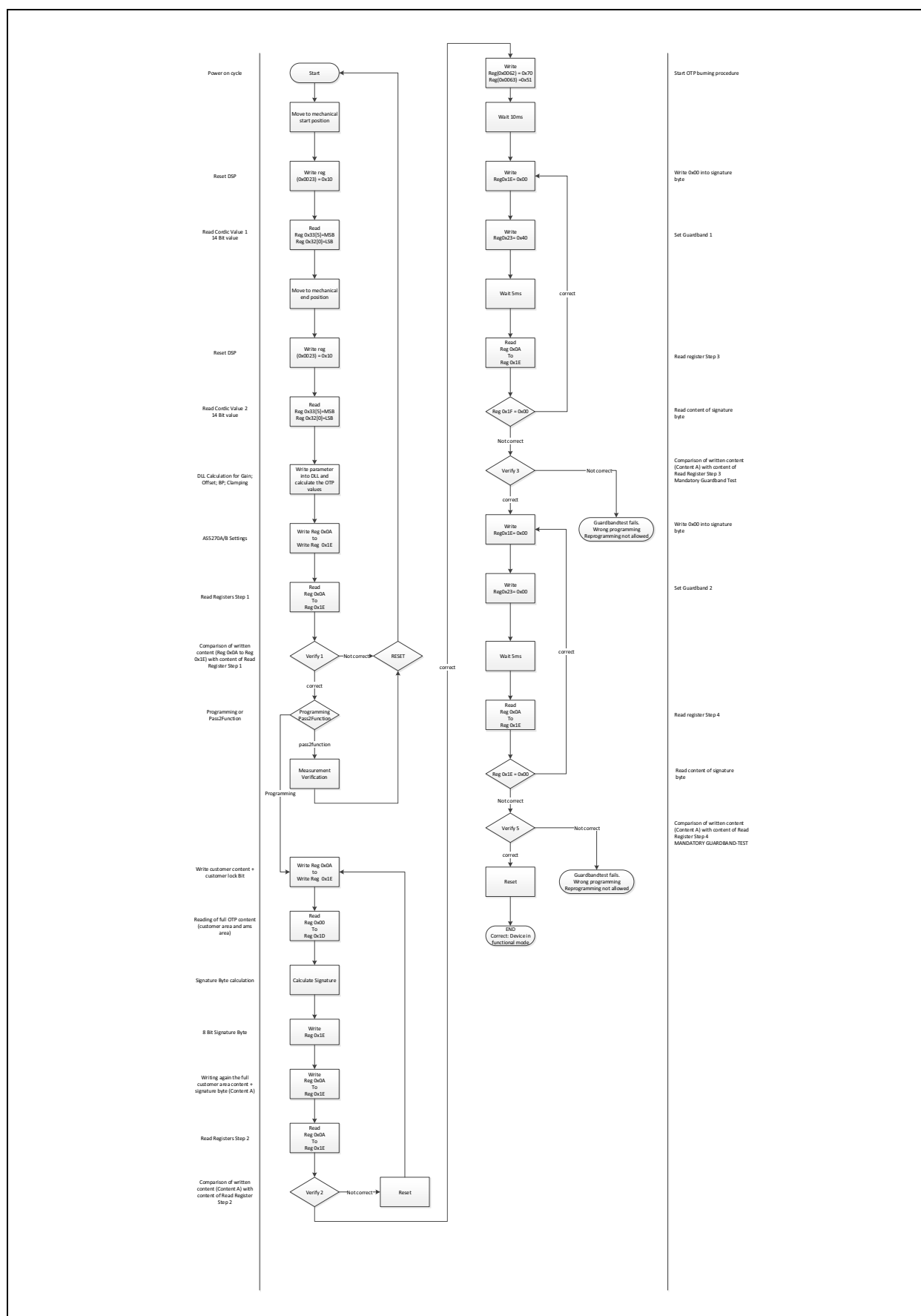
1. Power on cycle
2. Move magnet to the first mechanical start position
3. Reset the DSP. Writing 0x20 into Reg(0x0023)
4. Read out the measured angle from ANGLECORDIC register: T1 Value
5. Moving of magnet to the second mechanical position (stop position)
6. Read out the measured angle from ANGLECORDIC register: T2 Value
7. Write T1,T2 and all other transfer parameter into the DLL: Calculation of GAIN, Offset, BP, Clamping
8. Write reg(0x000A) to reg (0x001E) with the custom settings and the calculated values from point 7. --> AS5270 Settings
9. Read reg(0x000A) to reg (0x001E) ---> Read register step 1
10. Comparison of AS5270 settings with content of read register step 1
11. If point 10 is correct: Decision: pass 2 function (measurement verification) or programming. Programming sequence starts with point 12.
12. Write reg(0x000A) to reg (0x001E) with the custom settings and the calculated values from point 7 + customer lock Bit. --> AS5270 Settings\_Prog
13. Read reg(0x0000) to reg (0x001D) ---> Read register step 2
14. Calculation of Signature Byte out of Read register step 2 content: Signature Byte
15. Write 8Bit Signature to reg(0x001E)
16. Write reg(0x000A) to reg (0x001E) with the custom settings and the calculated values from point 7 + customer lock Bit + Signature byte. --> AS5270 Settings\_Prog\_final

17. Read reg(0x000A) to reg (0x001E) ---> Read register step 3
18. Comparison of AS5270 Settings\_Prog\_final with content of read register step 3
19. If point 18 is correct, start the OTP burn procedure by writing: Reg(0x0062)=0x70 and Reg(0x0063)=0x51
20. Programming procedure is complete after 10ms
21. Clear the memory content writing 0x00 into reg (0x001E)
22. Write Reg0x23=0x40 to set the threshold for the guard band test (1)
23. 5ms wait time to refresh the non-volatile memory content with the OTP content
24. Read reg(0x000A) to reg (0x001E) ---> Read register step 4
25. If content from reg (0x001E) compares with content from "Signature Byte" refresh was successful
26. Comparison of AS5270 Settings\_Prog\_final with content of read register step 4. Mandatory: guard band test (1).
27. If point 26 fails, the test with the guard band (1) was not successful and the device is incorrectly programmed. A reprogramming is not allowed.
28. Clear the memory content writing 0x00 into reg (0x001E)
29. Write Reg0x23=0x00 to set the threshold for the guard band test (1)
30. 5ms wait time to refresh the non-volatile memory content with the OTP content
31. Read reg(0x000A) to reg (0x001E) ---> Read register step 5
32. If content from reg (0x001E) compares with content from "Signature Byte" refresh was successful
33. Comparison of AS5270 Settings\_Prog\_final with content of read register step 5. Mandatory: guard band test (1)
34. If point 33 fails, the test with the guard band (1) was not successful and the device is incorrectly programmed. A reprogramming is not allowed.
35. Reset of the device. After power on the Sensor starts in functional mode

**Note(s):**

1. Guard band test:  
 Restricted to temperature range: 25 °C ± 20 °C  
 Right after the programming procedure (max. 1 hour with same Conditions 25°C ± 20 °C)  
 Same VDD voltage  
 The guard band test is only for the verification of the burned OTP fuses during the programming sequence.  
 A use of the guard band in other cases is not allowed.

**Figure 42:**  
**OTP Memory Burn and Verification Flowchart**



MLF

Figure 43:  
Application with Pull-Down Load Resistor on Both Outputs (MLF-16)

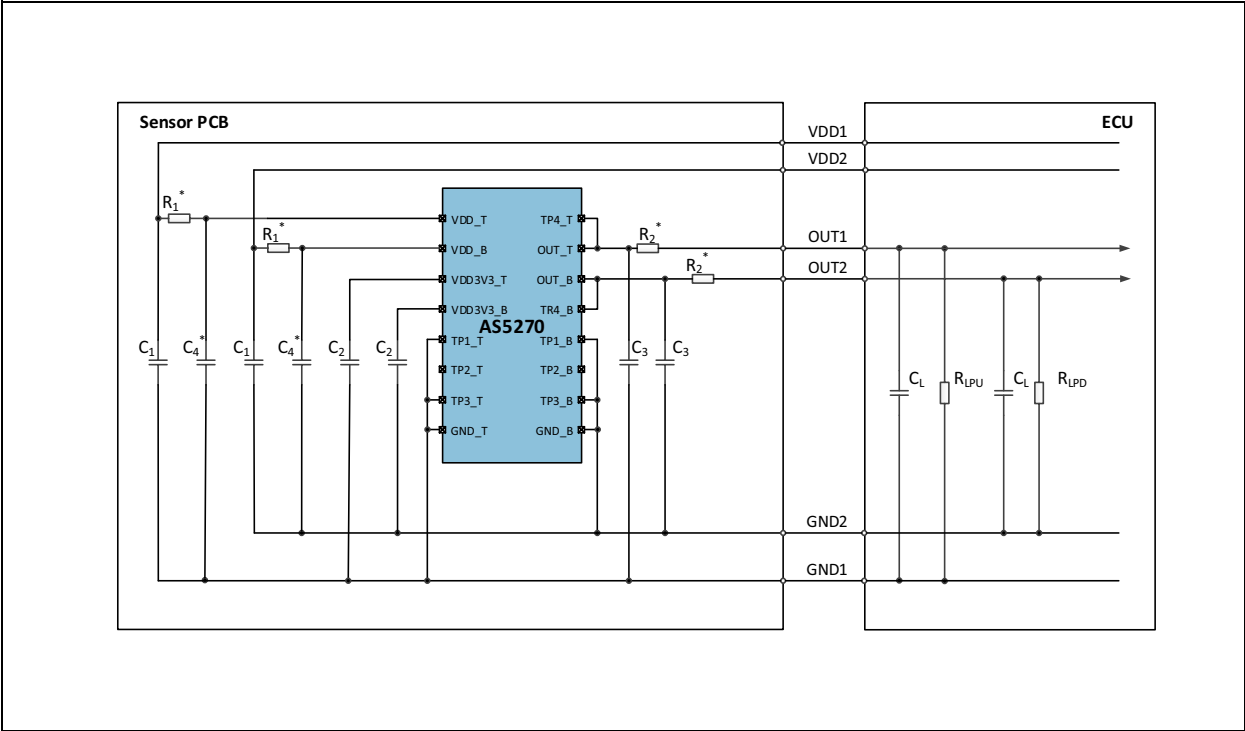
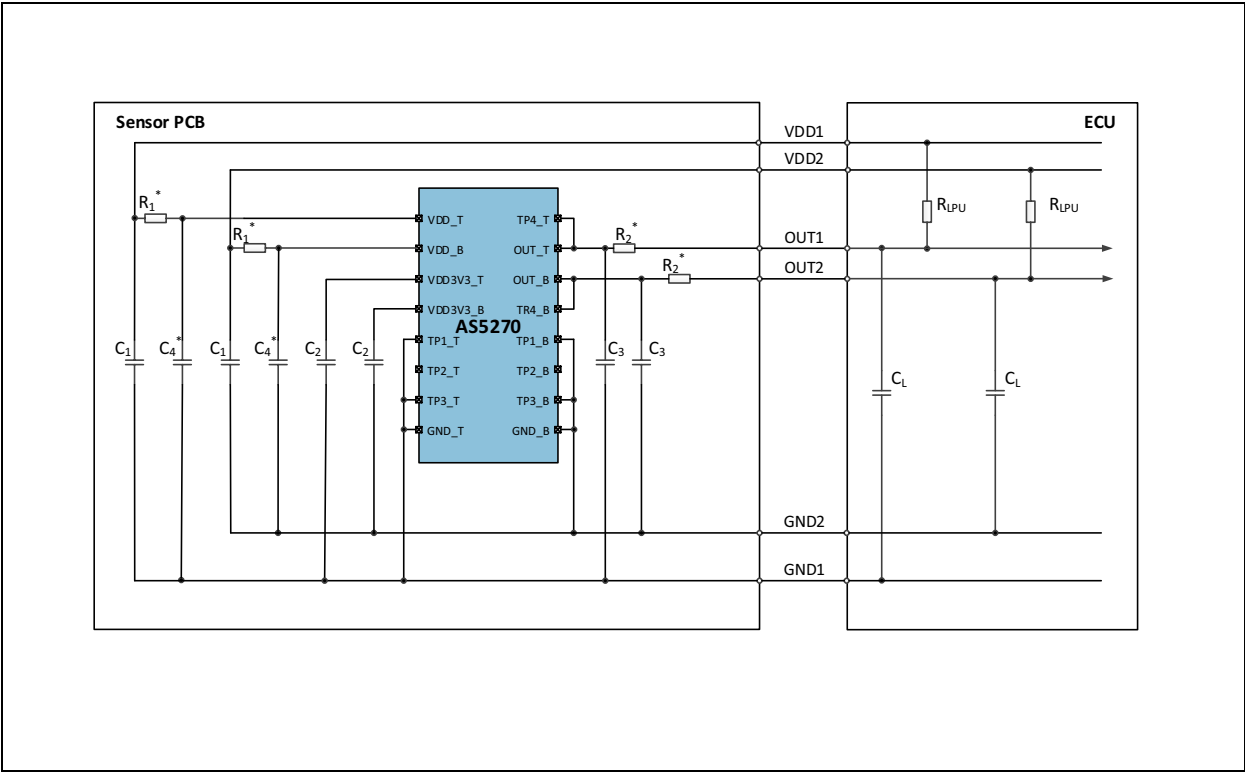
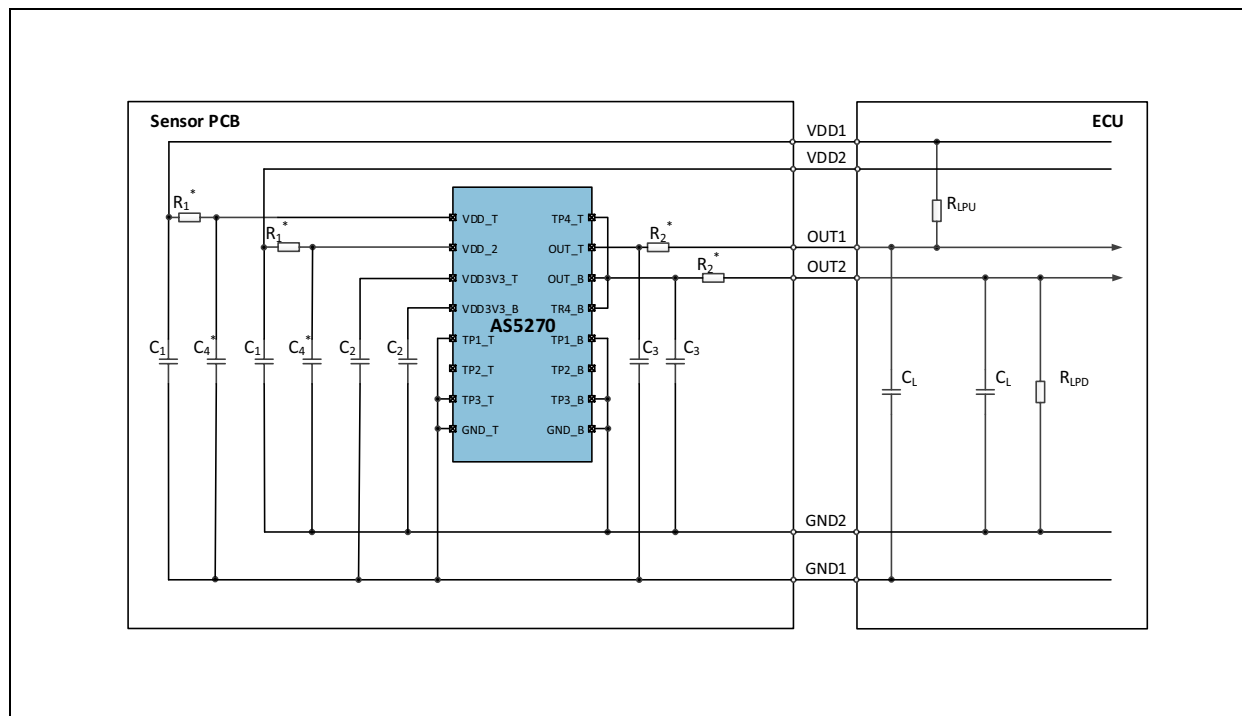


Figure 44:  
Application with Pull-Up Load Resistor on Both Outputs (MLF-16)



**Figure 45:**  
Application with Pull-Up Load Resistor on One Output and Pull-Down Resistor on the Other One (MLF-16)



## External Components

**Figure 46:**  
Recommended External Components for AS5270A

| Component                       | Symbol    | Min | Typ | Max | Unit       | Notes   |
|---------------------------------|-----------|-----|-----|-----|------------|---|
| VDD buffer capacitor            | $C_1$     | 80  | 100 | 120 | nF         |   |
| VDD3V3 regulator capacitor      | $C_2$     | 80  | 100 | 120 | nF         |   |
| OUT load capacitor (sensor PCB) | $C_3$     | 0   |     | 4.7 | nF         | Do not increase due to programming over output. |
| VDD capacitor (optional)        | $C_4^*$   |     | 4.7 |     | nF         |   |
| VDD serial resistor (optional)  | $R_1^*$   |     | 10  |     | k $\Omega$ |   |
| OUT load capacitor (ECU)        | $C_L$     | 0   |     | 20  | nF         |   |
| OUT serial resistor (optional)  | $R_2^*$   |     | 50  |     | k $\Omega$ |   |
| OUT pull-up resistance          | $R_{LPU}$ | 4   |     | 10  | k $\Omega$ |   |
| OUT pull-down resistance        | $R_{LPD}$ | 4   |     | 10  | k $\Omega$ |   |

**Figure 47:**  
**Recommended External Components for AS5270B with PWM Output**

| Component                       | Symbol    | Min | Typ | Max | Unit       | Notes   |
|---------------------------------|-----------|-----|-----|-----|------------|---|
| VDD buffer capacitor            | $C_1$     | 80  | 100 | 120 | nF         |   |
| VDD3V3 regulator capacitor      | $C_2$     | 80  | 100 | 120 | nF         |   |
| OUT load capacitor (sensor PCB) | $C_3$     | 0   |     | 4.7 | nF         | Do not increase due to programming over output. |
| VDD capacitor (optional)        | $C_4^*$   |     | 4.7 |     | nF         |   |
| VDD serial resistor (optional)  | $R_1^*$   |     | 10  |     | k $\Omega$ |   |
| OUT load capacitor (ECU)        | $C_L$     | 0   |     | 20  | nF         |   |
| OUT serial resistor (optional)  | $R_2^*$   |     | 50  |     | k $\Omega$ |   |
| OUT pull-up resistance          | $R_{LPU}$ | 1   |     | 10  | k $\Omega$ |   |
| OUT pull-down resistance        | $R_{LPD}$ | 1   |     | 10  | k $\Omega$ |   |

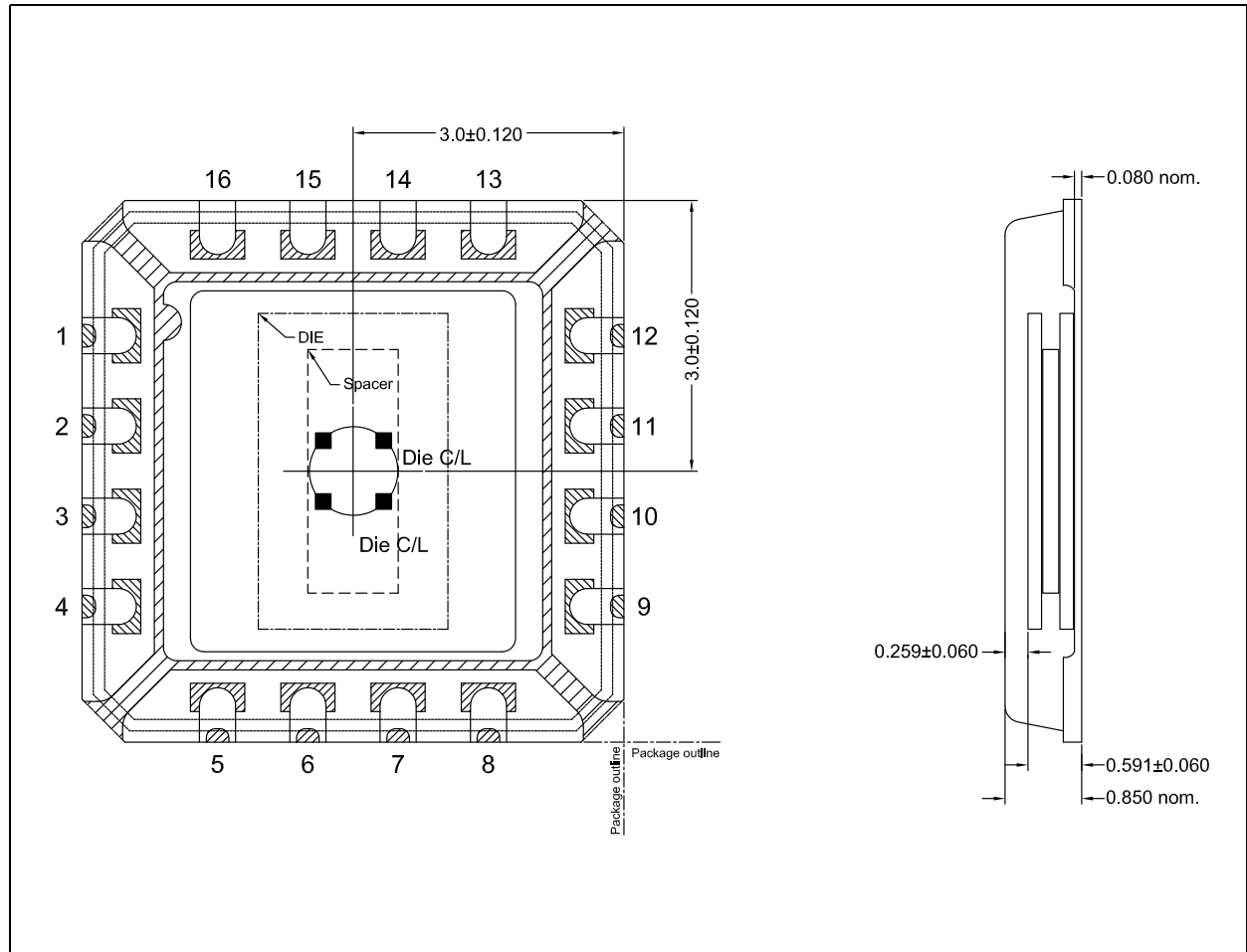
**Figure 48:**  
**Recommended External Components for the AS5270B with SENT Output**

| Component                       | Symbol    | Min | Typ | Max | Unit       | Notes   |
|---------------------------------|-----------|-----|-----|-----|------------|---|
| VDD buffer capacitor            | $C_1$     | 0.8 | 1   | 1.2 | $\mu$ F    |   |
| VDD3V3 regulator capacitor      | $C_2$     | 80  | 100 | 120 | nF         |   |
| OUT load capacitor (sensor PCB) | $C_3$     | 0   |     | 4.7 | nF         | Do not increase due to programming over output. |
| VDD capacitor (optional)        | $C_4^*$   |     | 4.7 |     | nF         |   |
| VDD serial resistor (optional)  | $R_1^*$   |     | 10  |     | k $\Omega$ |   |
| OUT load capacitor (ECU)        | $C_L$     | 0   |     | 20  | nF         |   |
| OUT serial resistor (optional)  | $R_2^*$   |     | 50  |     | k $\Omega$ |   |
| OUT pull-up resistance          | $R_{LPU}$ | 10  |     | 50  | k $\Omega$ |   |
| OUT pull-down resistance        | $R_{LPD}$ | 10  |     | 50  | k $\Omega$ |   |

## Mechanical Data

The internal Hall elements are placed in the center of the package on a circle with a radius of 1.25mm.

**Figure 49:**  
**Hall Element Position**



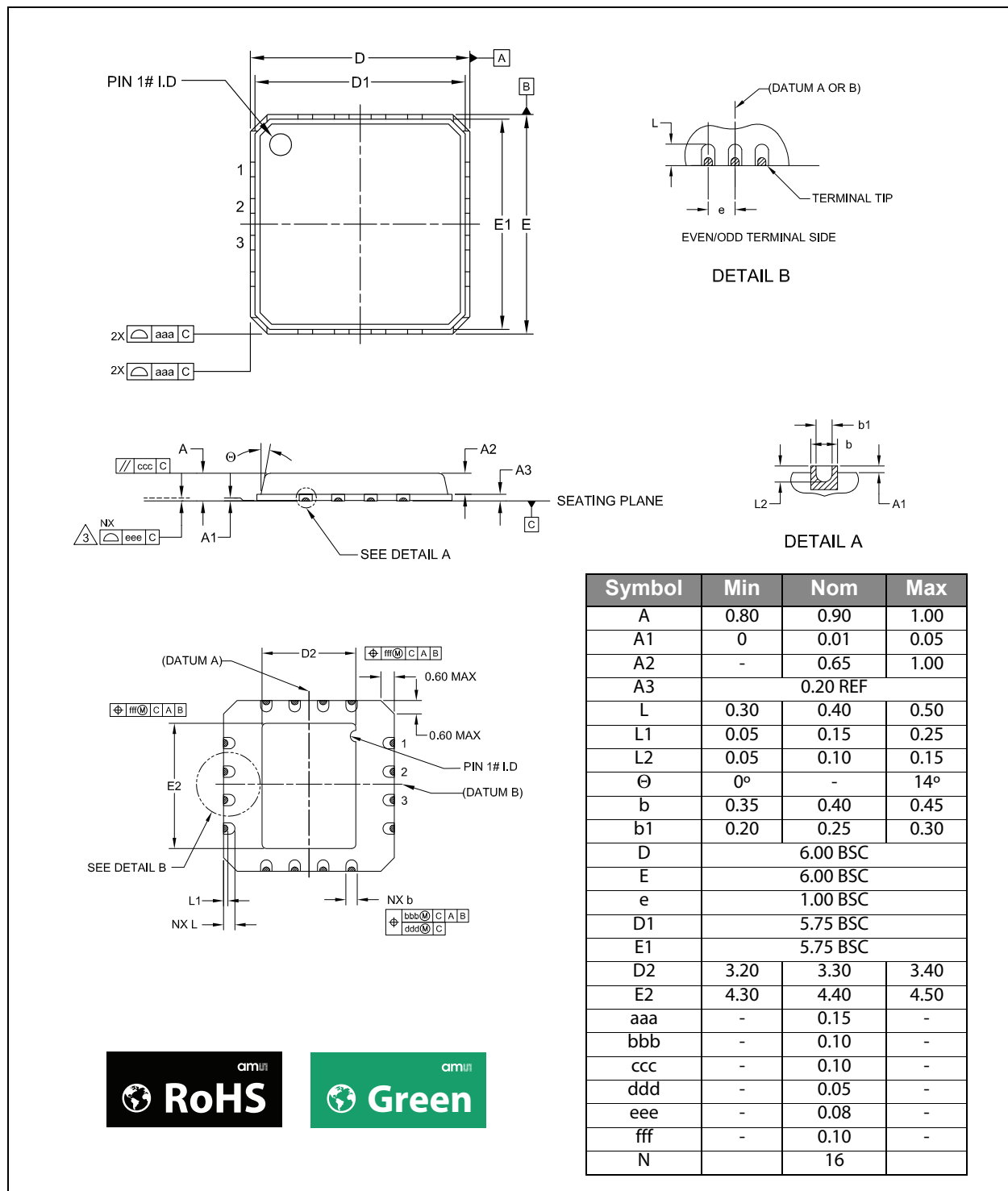
**Note(s) and/or Footnote(s):**

1. All dimensions in mm.
2. Die thickness 0.150mm nom.
3. Adhesive thickness 0.011mm nom.
4. Spacer thickness 0.178mm typ.



## Package Drawings & Markings

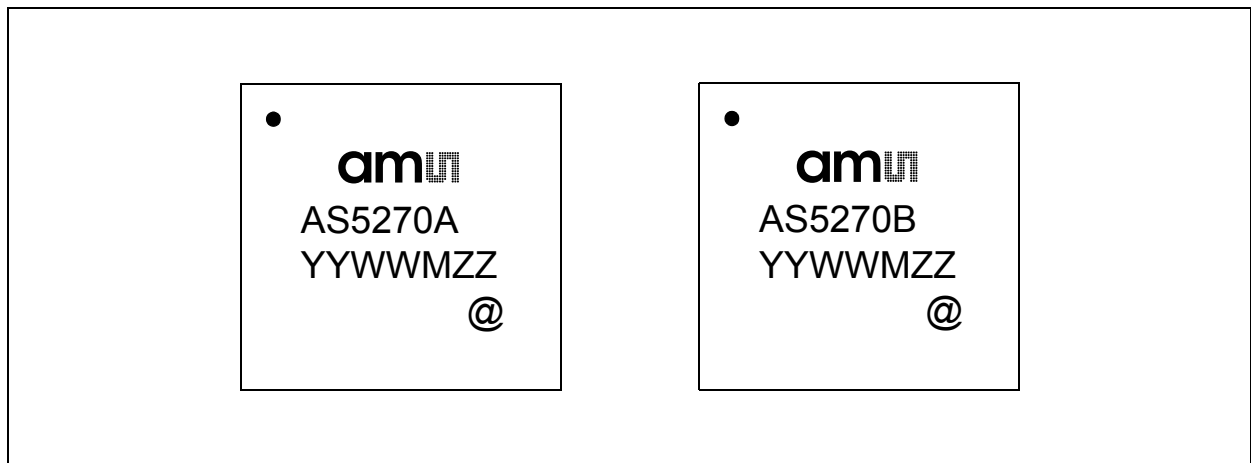
**Figure 50:**  
**Packaging Outline Drawing (MLF-16)**



**Note(s):**

1. Dimensions and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles in degrees.
3. Bilateral coplanarity zone applies to the exposed pad as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

**Figure 51:**  
Package Marking AS5270 - MLF16



**Figure 52:**  
Packaging Code YYWWMZZ@

| YY  | WW                 | M                | ZZ                                | @                 |
|---|--------------------|------------------|-----------------------------------|-------------------|
| Last two digits of the manufacturing year | Manufacturing week | Plant identifier | Free choice/<br>traceability code | Sublot identifier |

## Ordering & Contact Information

**Figure 53:**  
**Ordering Information**

| Ordering Code | Package | Marking | Delivery Form               | Delivery Quantity |
|---------------|---------|---------|-----------------------------|-------------------|
| AS5270A-HMFT  | MLF-16  | AS5270A | 13" Tape & Reel in dry pack | 4000 pcs/reel     |
| AS5270A-HMFM  | MLF-16  | AS5270A | 7" Tape & Reel in dry pack  | 1000 pcs/reel     |
| AS5270B-HMFT  | MLF-16  | AS5270B | 13" Tape & Reel in dry pack | 4000 pcs/reel     |
| AS5270B-HMFM  | MLF-16  | AS5270B | 7" Tape & Reel in dry pack  | 1000 pcs/reel     |

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## Revision Information

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| <b>1-02 (2016-Oct-01) to 1-03 (2017-Nov-17)</b>                        |      |
| Updated Figure 10  | 9    |
| Updated Figure 15  | 13   |
| Updated Figures 21 and 22  | 19   |
| Updated Figure 50  | 41   |
| <b>1-03 (2017-Nov-17) to 1-04 (2017-Dec-06)</b>                        |      |
| Updated Figure 15  | 13   |

**Note(s):**

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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