ATBTLC1000XR/ZR

Ultra Low Power BLE 4.1 ATBTLC1000-XR1100A SiP/ ATBTLC1000-ZR110CA Module Datasheet

Description

The Microchip ATBTLC1000-XR1100A is an ultra-low power Bluetooth® low energy 4.1 System in a Package (SiP) with Integrated MCU, Transceiver, Modem, MAC, PA, Transmit/Receive (T/R) Switch, and Power Management Unit (PMU). It can be used as a Bluetooth Low Energy link controller or data pump with external host MCU. The host interface between MCU and ATBTLC1000-XR1100A is a UART with hardware flow control.

The Bluetooth® SIG qualified protocol stack is stored in a dedicated ROM. The firmware includes L2CAP service layer protocols, Security Manager, Attribute protocol (ATT), Generic Attribute Profile (GATT), and the Generic Access Profile (GAP). Additionally, example applications are available for application profiles such as Proximity, Thermometer, Heart Rate, Blood Pressure and many others SIG defined profiles.

The ATBTLC1000-XR1100A provides a compact footprint and various embedded features such as a 26MHz crystal oscillator. It provides the right solution for the customer, whose BLE design requires full features, using low power consumption and minimal PCB space.

The ATBTLC1000-ZR110CA is a fully certified module that contains the ATBTLC1000-XR1100A and all external circuitry required including a ceramic high gain antenna. The customer simply needs to place the module into their PCB design, provide power, a 32.768kHz Real Time Clock or crystal, and an I/O path for interfacing with the host MCU.

Microchip BluSDK offers a comprehensive set of tools - including reference applications for several Bluetooth SIG defined profiles and a custom profile. The BluSDK will help the user to quickly evaluate, design and develop BLE products with the ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA.

Features

- 2.4GHz Transceiver and Modem:
  - -91.5dBm receiver sensitivity
  - -20dBm to +4dBm programmable TX output power
  - Integrated T/R switch
  - Single wire antenna connection (ATBTLC1000-XR1100A)
  - Incorporated chip antenna (ATBTLC1000-ZR110CA)
- Processor Features:
  - ARM® Cortex®-M0 32-bit processor
  - Serial Wire Debug (SWD) interface
  - Four-channel Direct Memory Access(DMA) controller
  - Brown-out detector and Power-on Reset
  - Watchdog timer

- Memory:
  - 128KB embedded Random Access Memory(RAM) - 96KB available for application
  - 128KB embedded ROM
- Hardware Security Accelerators:
  - Advanced Encryption Standard (AES)-128
  - Secure Hash Algorithm (SHA)-256
- Peripherals:
  - 22 digital and 4 mixed-signal General Purpose Input Outputs (GPIOs) with 96kΩ internal programmable pull-up or down resistors and retention capability, and one wakeup GPIO with 96kΩ internal pull-up resistor(1)
  - Two Serial Peripheral Interface(SPI) Master/Slave(1)
  - Two Inter-Integrated Circuit (I2C) Master/Slave and one I2C Slave interface(1)
  - Two UART(1)
  - Three-axis quadrature decoder(1)
  - Four Pulse Width Modulation (PWM) channels(1)
  - Three General Purpose Timers and one Wakeup Timer(1)
  - 2-channel 11-bit Analog-to-Digital Converter(ADC)(1)
- Host Interface:
  - Host MCU can control through UART with hardware flow control
  - Only two microcontroller GPIO lines necessary
  - One interrupt pin from ATBTLC1000 which can be used for host wakeup
- Clock:
  - Integrated 26MHz RC oscillator
  - Integrated 2MHz sleep RC oscillator
  - 26MHz crystal oscillator(XO)
  - 32.768kHz Real Time Clock crystal oscillator(RTC XO)
- Ultra-Low Power:
  - 1.88 µA sleep current (8KB RAM retention and RTC running)
  - 4.78 mA peak TX current (2)
  - 5.66 mA peak RX current
  - 15.8 µA average advertisement current(3)
- Integrated Power Management:
  - 1.8V to 4.3V battery voltage range
  - Fully integrated Buck DC/DC converter
- Temperature Range:
  - -40°C to 85°C
- Package:
  - 40-pin IC package 5.5mm x4.5mm
  - 34-pin module package 10.541mm x7.503mm

Note:

1. Usage of this feature is not supported by the BluSDK. The datasheet will be updated once support for this feature is added in BluSDK.

2. TX output power - 0 dBm
3. Advertisement channels - 3 ; Advertising interval - 1 second ; Advertising event type - Connectable undirected; Advertisement data payload size - 31 octets

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1. Ordering Information

Table 1-1. Ordering Details

Ordering Code	Package	Description
ATBTLC1000-XR1100A	5.5mm x 4.5mm	ATBTLC1000 SiP tray
ATBTLC1000-ZR110CA	7.5mm X 10.5mm	ATBTLC1000 chip antenna module

2. Package Information

Table 2-1. ATBTLC1000-XR1100A SiP 40 Package Information [1]

Parameter	Value	Units	Tolerance
Package size	5.5 x 4.5	mm	±0.05 mm
Pad count	40		
Total thickness	1.36	mm	±0.05 mm
Pad pitch	0.4		
Pad width	0.21		
Exposed pad size	0.5 x 0.5		

Note:

1. For drawing details, see ATBTLC1000-XR1100A Package Outline Drawing.

Table 2-2. ATBTLC1000-ZR110CA Module Information [1]

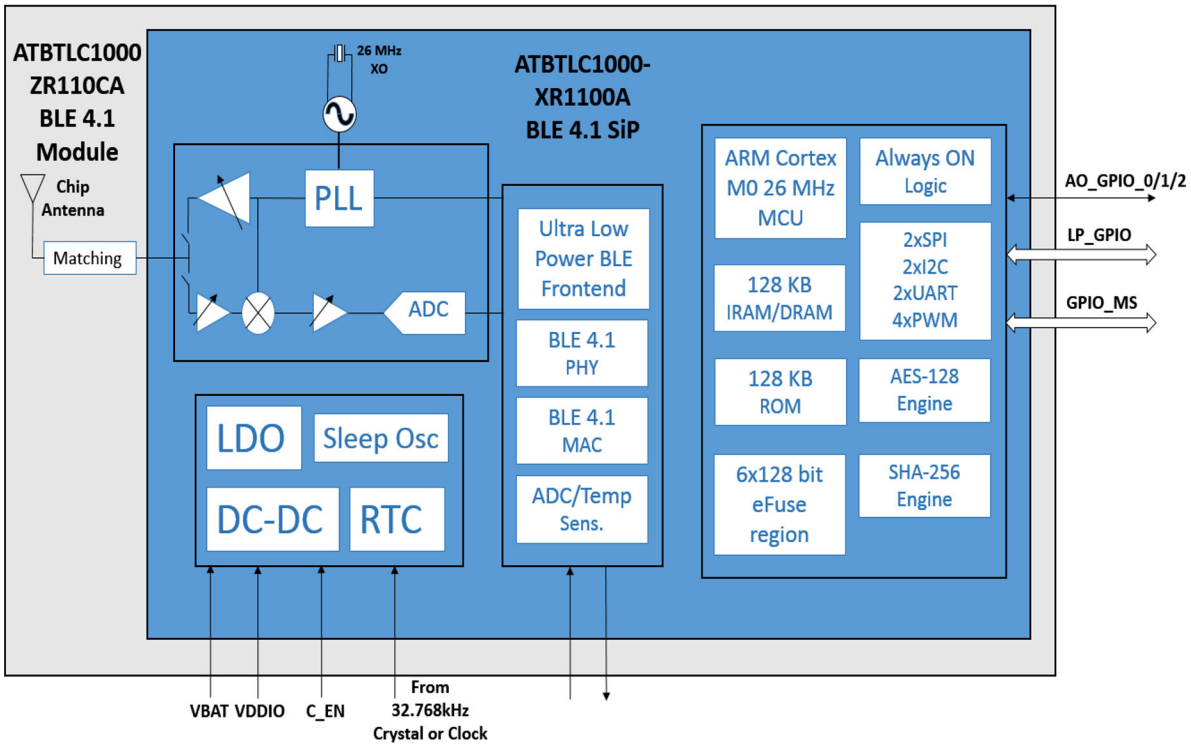
Parameter	Value	Units	Tolerance
Package size	7.503 x 10.541	mm	Untoleranced dimension
Pad count	34		
Total thickness	1.868	mm	Untoleranced dimensions
Pad pitch	0.61		
Pad width	0.406		
Exposed pad size	2.705 x 2.705		

Note:

1. For drawing details, see ATBTLC1000-ZR110CA Module Package Outline Drawing.

3. Block Diagram

Figure 3-1. Block Diagram



4. Pinout Information

The ATBTLC1000-XR1100A is offered in an exposed pad 40-pin SiP package. This package has an exposed paddle that must be connected to the system board ground. In ATBTLC1000-XR1100A Pin Assignment, the SiP package pin assignment is shown. The color shading is used to indicate the pin type as follows:

- Red – analog
- Green – digital I/O (switchable power domain)
- Blue – digital I/O (always-on power domain)
- Yellow – power
- Purple – PMU
- Shaded green/red – configurable mixed-signal GPIO (digital/analog)

The ATBTLC1000-ZR110CA module is a castellated PCB with the ATBTLC1000-XR1100A integrated with a matched chip antenna. The pins are identified in the pinout table and the module has a paddle pad on the bottom of the PCBA that must be soldered to the system ground.

Figure 4-1. ATBTLC1000-XR1100A Pin Assignment

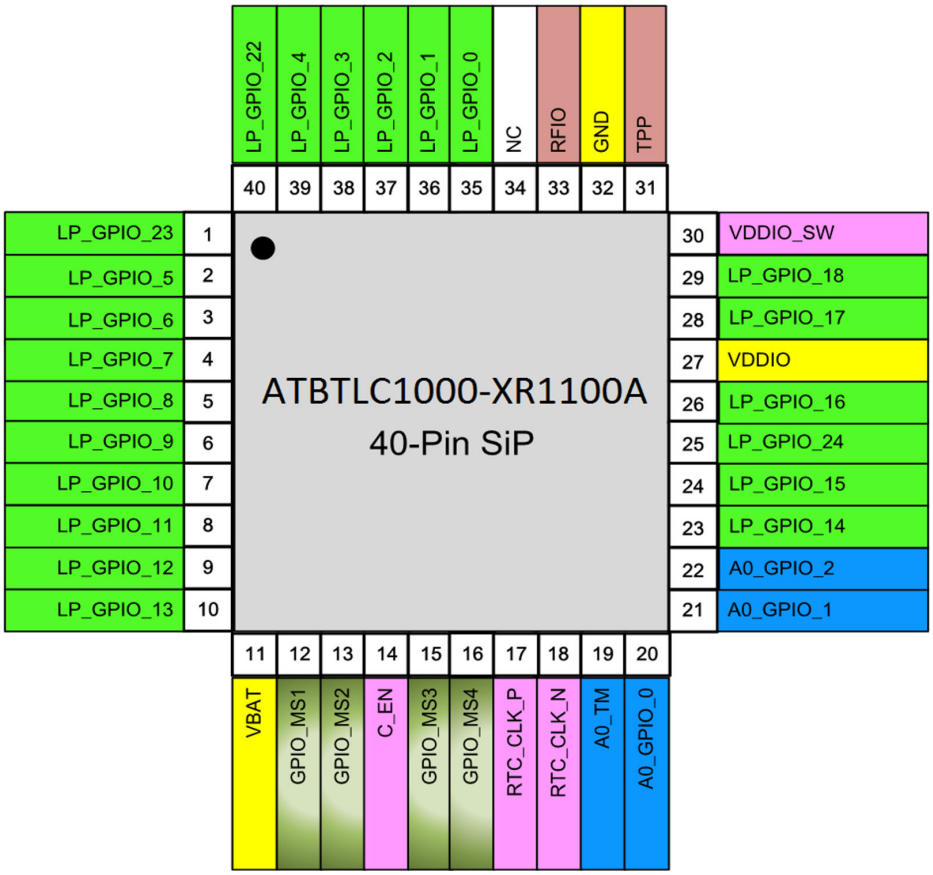
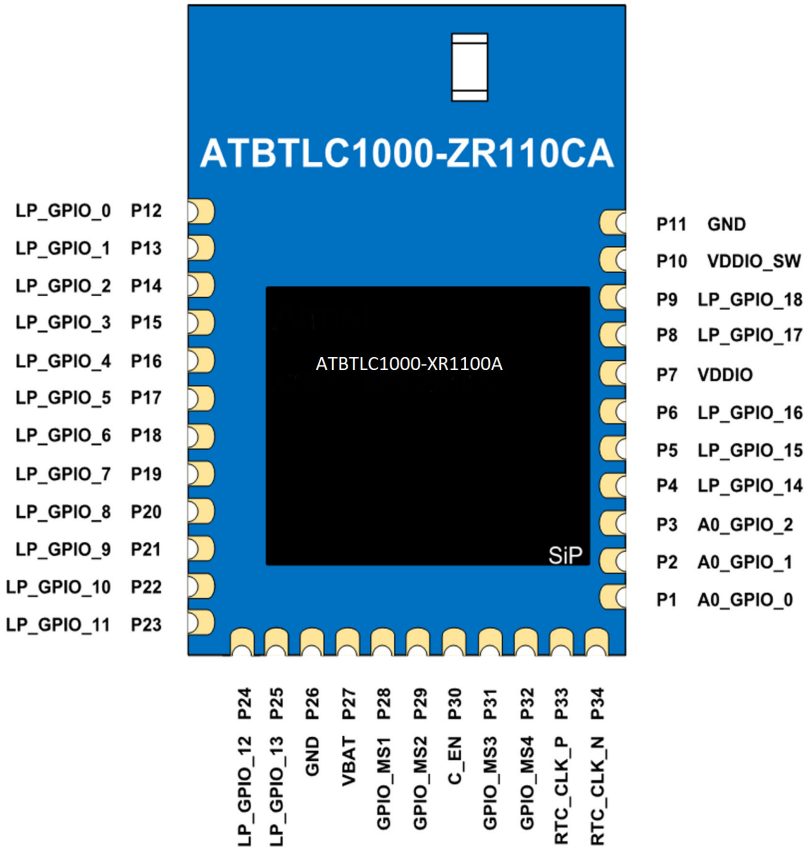


Figure 4-2. ATBTLC1000-ZR110CA Pin Descriptions



The pin description for ATBTLC1000-XR1100A SiP and ATBTLC1000-ZR110CA module is detailed in the following table.

Table 4-1. ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA Pin Description

XR1100A Pin #	ZR110CA Pin #	Pin Name	Pin Type	Description / Default Function
1	-	LP_GPIO_23	Digital I/O	GPIO with Programmable Pull-Up/Down
2	17	LP_GPIO_5	Digital I/O	GPIO with Programmable Pull-Up/Down
3	18	LP_GPIO_6	Digital I/O	GPIO with Programmable Pull-Up/Down
4	19	LP_GPIO_7	Digital I/O	GPIO with Programmable Pull-Up/Down
5	20	LP_GPIO_8(1)	Digital I/O	Default function: UART_CTS. To be connected with UART_RTS of host MCU
6	21	LP_GPIO_9(1)	Digital I/O	Default function: UART_RTS. To be connected with UART_CTS of host MCU
7	22	LP_GPIO_10	Digital I/O	GPIO with Programmable Pull-Up/Down
8	23	LP_GPIO_11	Digital I/O	GPIO with Programmable Pull-Up/Down

XR1100A Pin #	ZR110CA Pin #	Pin Name	Pin Type	Description / Default Function
9	24	LP_GPIO_12	Digital I/O	GPIO with Programmable Pull-Up/Down
10	25	LP_GPIO_13	Digital I/O	GPIO with Programmable Pull-Up/Down
11	27	VBAT	Power supply	Power supply pin for the DC/DC convertor
12	28	GPIO_MS1	Mixed Signal I/O	GPIO with Programmable Pull-Up/ Down. Default function in BluSDK: Host wakeup (2)
13	29	GPIO_MS2	Mixed Signal I/O	GPIO with Programmable Pull-Up/Down
14	30	C_EN	Digital Input	Can be used to control the state of PMU. High level enables the module; low- level places module in Power Down mode. Connect to a host Output that defaults low at power up. If the host output is tri-stated, add a 1MΩ pull-down resistor to ensure a low level at power up.
15	31	GPIO_MS3	Mixed Signal I/O	GPIO with Programmable Pull-Up/Down
16	32	GPIO_MS4	Mixed Signal I/O	GPIO with Programmable Pull-Up/Down
17	33	RTC_CLK_P	Analog	Crystal pin or external clock supply, see Section 32.768kHz RTC Crystal Oscillator
18	34	RTC_CLK_N	Analog	Crystal pin, see Section 32.768kHz RTC Crystal Oscillator
19	-	A0_TM	Digital Input	Always On Test Mode. Connect to GND
20	1	A0_GPIO_0	Always On Digital I/O, Programmable Pull-Up/ Down	Can be used to Wakeup the device from Ultra_Low_Power mode by the host MCU
21	2	A0_GPIO_1	Always-On Digital I/O	GPIO with Programmable Pull-Up/Down
22	3	A0_GPIO_2	Always-On Digital I/O	GPIO with Programmable Pull-Up/Down
23	4	LP_GPIO_14	Digital I/O	GPIO with Programmable Pull-Up/Down
24	5	LP_GPIO_15	Digital I/O	GPIO with Programmable Pull-Up/Down
25	-	LP_GPIO_24	Digital I/O	GPIO with Programmable Pull-Up/Down
26	6	LP_GPIO_16	Digital I/O	GPIO with Programmable Pull-Up/Down
27	7	VDDIO	Power supply	Power supply pin for the I/O pins. Can be less than or equal to voltage supplied at VBAT

XR1100A Pin #	ZR110CA Pin #	Pin Name	Pin Type	Description / Default Function
28	8	LP_GPIO_17	Digital I/O	GPIO with Programmable Pull-Up/Down
29	9	LP_GPIO_18	Digital I/O	GPIO with Programmable Pull-Up/Down
30	10	VDDIO_SW	DC/DC Power Switch	Do not connect
31	-	TPP		Do not connect
32	11, 26	GND	Ground	
33	-	RFIO	Analog I/O	RX input and TX output. Single-ended RF I/O; To be connected to antenna
34	-	NC		Do not connect
35	12	LP_GPIO_0	Digital I/O	SWD clock
36	13	LP_GPIO_1	Digital I/O	SWD I/O
37	14	LP_GPIO_2	Digital I/O	Default function: UART_RXD. To be connected with UART_TXD of host MCU
38	15	LP_GPIO_3	Digital I/O	Default function: UART_TXD. To be connected with UART_RXD of host MCU
39	16	LP_GPIO_4	Digital I/O	GPIO with Programmable Pull-Up/Down
40	-	LP_GPIO_22	Digital I/O	GPIO with Programmable Pull-Up/Down
41	35	Paddle	Ground	Exposed paddle must be soldered to system ground

Note:

1. These GPIO pads are high-drive pads. Refer Table 11-3
2. Refer section ATBTLC1000-XR/ZR Host Microcontroller Interface

5. Device States

5.1 Description of Device States

The ATBTLC1000-XR1100A and the ATBTLC1000-ZR110CA have multiple device states, depending on the state of the ARM processor and BLE subsystem.

Note: The ARM is required to be powered-on if the BLE subsystem is active.

- BLE_On_Transmit – Device is actively transmitting a BLE signal (Irrespective of whether ARM processor is active or not)
- BLE_On_Receive – Device is actively receiving a BLE signal (Irrespective of whether ARM processor is active or not)
- Ultra_Low_Power – BLE subsystem and ARM processor is powered-down (with or without RAM retention)
- Power_Down – Device core supply off

5.1.1 Controlling the Device States

The following pins are used to switch between the main device states:

- C_EN – used to enable PMU
- VDDIO – I/O supply voltage from an external power supply
- AO_GPIO_0 - can be used to control the device from entering/exiting Ultra_Low_Power mode

To be in the Power_Down state, the VDDIO supply must be turned on and the C_EN must be maintained at logic low (at GND level). To switch between the Power_Down state and the MCU_Only state, C_EN is to be maintained at logic high (VDDIO voltage level). Once the device is in the MCU_Only state, all other state transitions are controlled entirely by software. When VDDIO supply is turned off and C_EN is in logic low, the chip is powered-off with no leakage.

When VDDIO supply is turned off, voltage cannot be applied to the ATBTLC1000-XR1100A pins as each pin contains an ESD diode from the pin to supply. This diode will turn on when a voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the Power_Down state must be used. Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

The AO_GPIO_0 pin can be used to control the device from entering and exiting Ultra_Low_Power mode. When AO_GPIO_0 is maintained in logic high state, the device will not enter Ultra_Low_Power mode. When the AO_GPIO_0 is maintained in logic low, the device will enter Ultra_Low_Power mode provided there are no BLE events to be handled.

5.2 Power Sequences

The power sequences for the ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA are shown in Power-up/Power-down Sequence. The timing parameters are provided in Power-up/Power-down Sequence Timing.

Figure 5-1. Power-up/Power-down Sequence

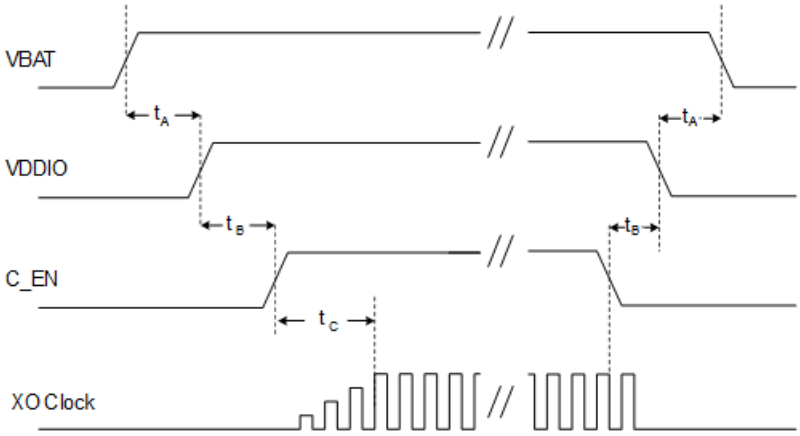


Table 5-1. Power-up/Power-down Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_A	0		ms	VBAT rise to VDDIO rise	VBAT and VDDIO can rise simultaneously or can be tied together
t_B	0			VDDIO rise to C_EN rise	C_EN must not rise before VDDIO. C_EN must be driven high or low, not left floating.
t_C	10		µs	C_EN rise to 31.25kHz (2MHz/64) oscillator stabilizing	
$t_{B'}$	0		ms	C_EN fall to VDDIO fall	C_EN must fall before VDDIO. C_EN must be driven high or low, not left floating.
$t_{A'}$	0			VDDIO fall to VBAT fall	VBAT and VDDIO can fall simultaneously or be tied together

5.3 Digital and Mixed-Signal I/O Pin Behavior during Power-Up Sequences

The following table represents I/O pin states corresponding to device power modes.

Table 5-2. I/O Pin Behavior in the Different Device States (1)

Device State	VDDIO	CHIP_EN	Output Driver	Input Driver	Pull Up/Down Resistor (2)
Power_Down: core supply off	High	Low	Disabled (Hi-Z)	Disabled	Disabled
Power-On Reset: core supply on, POR hard reset pulse on	High	High	Disabled (Hi-Z)	Disabled	Disabled (3)

Device State	VDDIO	CHIP_EN	Output Driver	Input Driver	Pull Up/Down Resistor [2]
Power-On Default: core supply on, device out of reset but not programmed yet	High	High	Disabled (Hi-Z)	Enabled [4]	Enabled Pull-Up [4]
BLE_On: core supply on, device programmed by firmware	High	High	Programmed by firmware for each pin: Enabled or Disabled (Hi-Z) [5] ,when Enabled driving 0 or 1	Opposite of Output Driver state: Disabled or Enabled [5]	Programmed by firmware for each pin: Enabled or Disabled, Pull-Up or Pull- Down [5]
Ultra_Low_Power: core supply on for always-on domain, core supply off for switchable domains	High	High	Retains previous state[6] for each pin: Enabled or Disabled (Hi-Z), when Enabled driving 0 or 1	Opposite of Output Driver state: Disabled or Enabled [5]	Retains previous state [6] for each pin: Enabled or Disabled, Pull-Up or Pull-Down

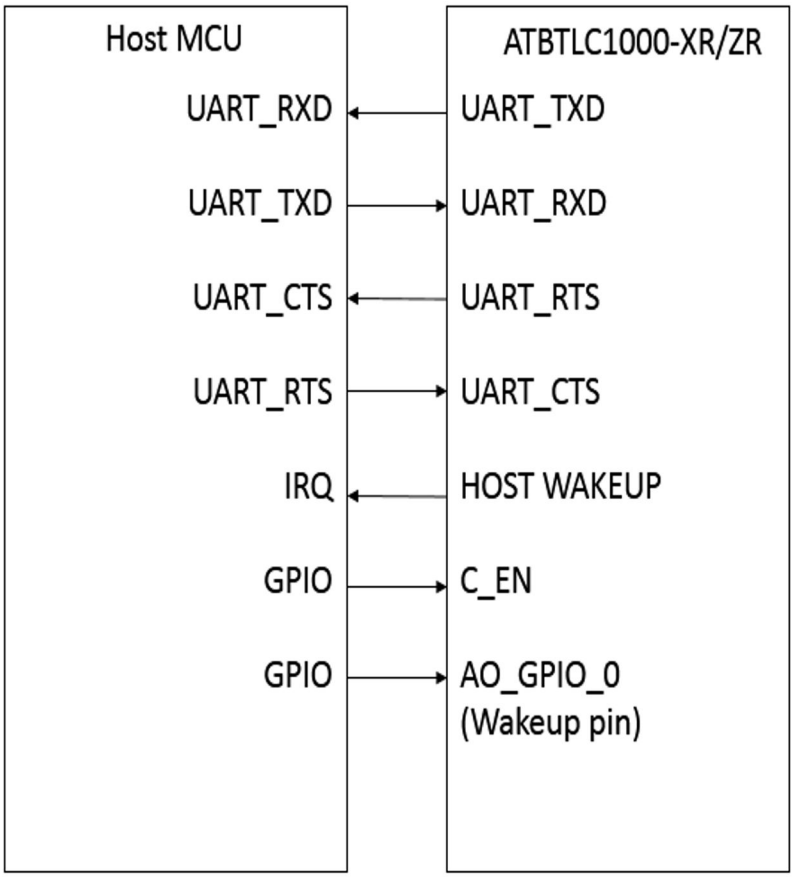
Note:

1. This table applies to all three types of I/O pins (digital switchable domain GPIOs, digital always-on/ wakeup GPIO, and mixed-signal GPIOs) unless otherwise noted
2. Pull-up/down resistor value is 96kΩ ±10%
3. In Power-On Reset state pull-up resistor is enabled in the always-on/wakeup GPIO only
4. In Power-On Default state input drivers and pull-up/down resistors are disabled in the mixed-signal GPIOs only (mixed-signal GPIOs are defaulted to analog mode, see the note below)
5. Mixed-signal GPIOs can be programmed to be in analog or digital mode for each pin: when programmed to analog mode (default), the output driver, input driver, and pull-up/down resistors are all disabled
6. In Ultra_Low_Power state always-on/wakeup GPIO does not have retention capability and behaves same as in MCU_Only or BLE_On states, also for mixed-signal GPIOs programming analog mode overrides retention functionality for each pin

6. ATBTLC1000-XR/ZR Host Microcontroller Interface

This section describes the interface of ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA with the host MCU. The interface to be used is UART with hardware flow control. It requires two additional GPIOs and one interrupt pin from the host MCU. See the below figure:

Figure 6-1. Host Microcontroller to ATBTLC1000-XR/ZR Interface



The host wakeup pin from ATBTLC1000 can be connected to any interrupt pin of the host MCU. The host MCU could monitor this pin level and decide to wakeup based on events from ATBTLC1000.

The host wakeup pin will be held in logic high ('1') by default and at conditions where there is no pending event data in the ATBTLC1000. The host wakeup pin will be held in logic low ('0') when there is event data available from ATBTLC1000 and the pin will be held in this state until all event data is sent out from ATBTLC1000. By default in BluSDK, GPIO_MS1 is used as the host wakeup pin. Refer to release notes and API user manual documents available in the BluSDK release package for more details on available options to re-configure the host wakeup pin from ATBTLC1000.

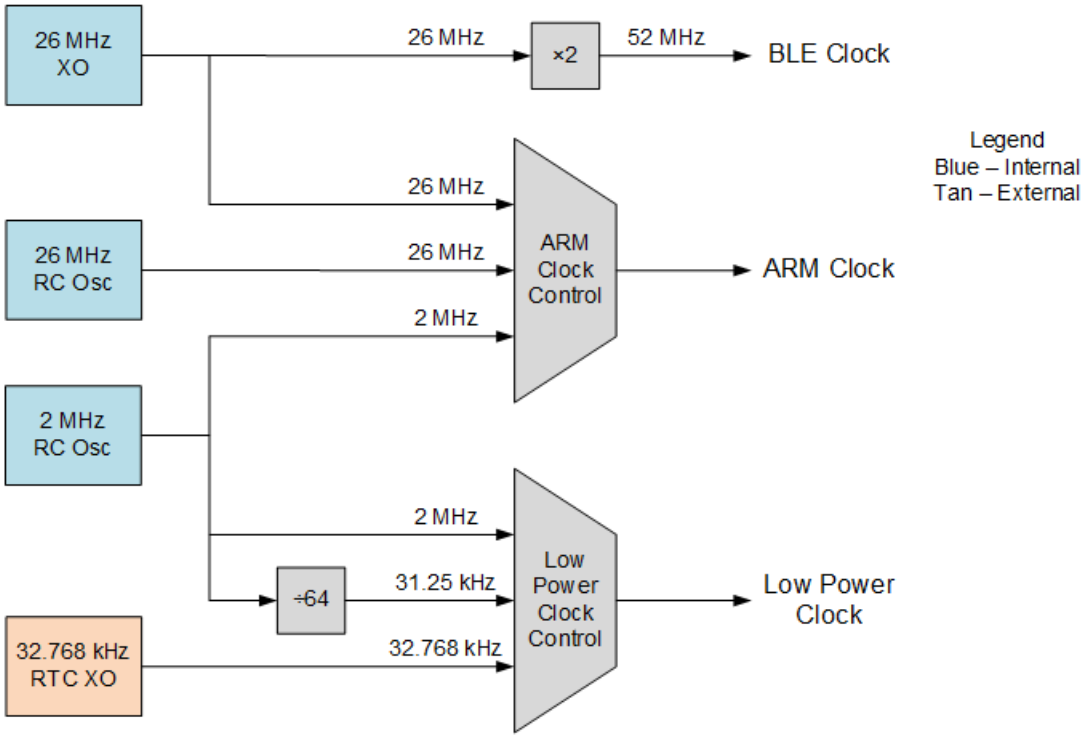
The UART configuration to be used are as below:

- Baud rate: configurable in the BluSDK during initialization. Refer to release notes and API user manual documents available in the BluSDK release package for more details
- Parity: None
- Stop bits: 1
- Data size: 8 bits

7. Clocking

7.1 Overview

Figure 7-1. Clock Architecture



Clock Architecture provides an overview of the clock tree and clock management blocks.

The BLE Clock is used to drive the BLE subsystem. The ARM clock is used to drive the Cortex-M0 MCU and its interfaces (UART, SPI, and I2C); the recommended MCU clock speed is 26MHz. The Low Power Clock is used to drive all the low-power applications like the BLE sleep timer, always-on power sequencer, always-on timer, and others.

The 26MHz integrated RC Oscillator is used for most general purpose operations on the MCU and its peripherals. In cases when the BLE subsystem is not used, the RC oscillator can be used for lower power consumption. The frequency variation of this RC oscillator is up to ±50% over process, voltage, and temperature.

The frequency variation of 2MHz integrated RC Oscillator is up to ±50% over process, voltage, and temperature.

The 32.768kHz RTC Crystal Oscillator (RTC XO) is used for BLE operations as it will reduce power consumption by providing the best timing for wakeup precision, allowing circuits to be in low-power sleep mode for as long as possible until they need to wake up and connect during the BLE connection event.

7.2 26MHz Crystal Oscillator (XO)

A 26MHz crystal oscillator is integrated into the ATBTLC1000-XR1100A and ATBTC1000-ZR110CA to provide the precision clock for the BLE operations.

7.3 32.768kHz RTC Crystal Oscillator (RTC XO)

32.768kHz RTC Crystal Oscillator (RTC XO).

7.3.1 General Information

The ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA have a 32.768kHz RTC oscillator that is preferably used for BLE activities involving connection events. To be compliant with the BLE specifications for connection events, the frequency accuracy of this clock has to be within ±500ppm. Because of the high accuracy of the 32.768kHz crystal oscillator clock, the power consumption can be minimized by leaving radio circuits in low-power sleep mode for as long as possible until they need to wake up for the next connection timed event.

The block diagram in the below Figure(a) shows how the internal low-frequency Crystal Oscillator (XO) is connected to the external crystal.

The RTC XO has a programmable internal capacitance with a maximum of 15pF on each terminal, RTC_CLK_P, and RTC_CLK_N. When bypassing the crystal oscillator with an external signal, one can program down the internal capacitance to its minimum value (~1pF) for easier driving capability. The driving signal can be applied to the RTC_CLK_P terminal as shown in the below Figure (b).

The need for external bypass capacitors depends on the chosen crystal characteristics. Typically, the crystal should be chosen to have a load capacitance of 7pF to minimize the oscillator current. Refer to the datasheet of the preferred crystal and take into account the on-chip capacitance.

Alternatively, if an external 32.768kHz clock is available, it can be used to drive the RTC_CLK_P pin instead of using a crystal. The XO has 6pF internal capacitance on the RTC_CLK_P pin. To bypass the crystal oscillator, an external signal capable of driving 6pF can be applied to the RTC_CLK_P terminal as shown in Figure (b). RTC_CLK_N must be left unconnected when driving an external source into RTC_CLK_P. Refer to the Table 7-1 for the specification of the external clock to be supplied at RTC_CLK_P.

Figure 7-2. Connections to RTC XO

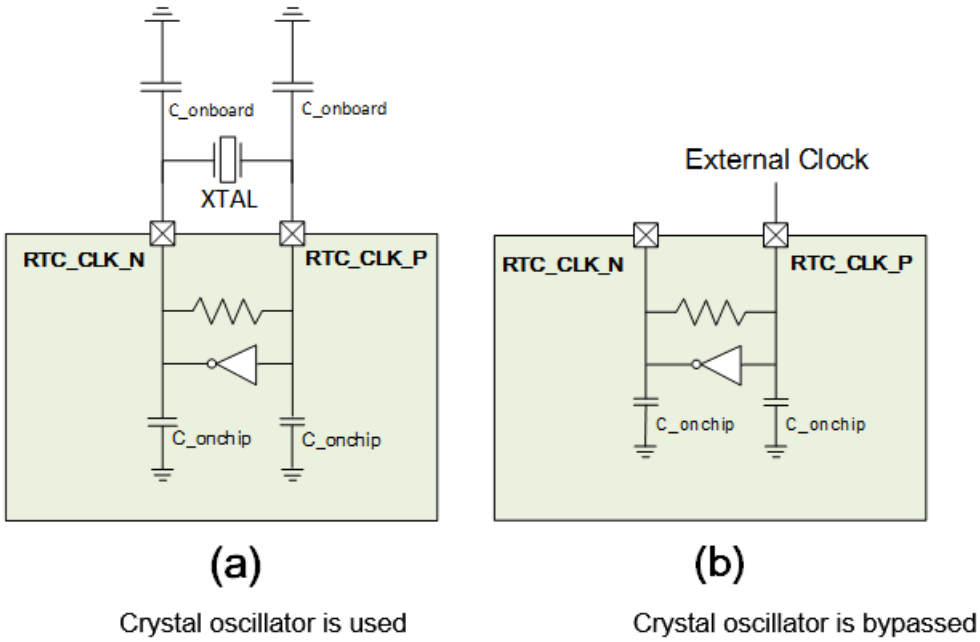


Table 7-1. 32.768kHz External Clock Specification

Parameter	Min.	Typ.	Max	Unit	Comments
Oscillation frequency		32.768		kHz	Must be able to drive 6pF load @ desired frequency
VinH	0.7		1.2	V	High level input voltage
VinL	0		0.2		Low level input voltage
Stability – Temperature	-250		+250	ppm	

Additional internal trimming capacitors (C_onchip) are available. They provide the possibility to tune the frequency output of RTC XO without changing the external load capacitors.

Note:
Refer the BluSDK BLE API Software Development Guide for details on how to enable the 32.768kHz clock output and tune the internal trimming capacitors.

Table 7-2. 32.768kHz XTAL C_onchip Programming

Register: pierce_cap_ctrl[3:0]	C_onchip [pF]
0000	0.0
0001	1.0
0010	2.0
0011	3.0
0100	4.0
0101	5.0
0110	6.0
0111	7.0
1000	8.0
1001	9.0
1010	10.0
1011	11.0
1100	12.0
1101	13.0
1110	14.0
1111	15.0

7.3.2 RTC XO Design and Interface Specification

The RTC consists of two main blocks: The Programmable Gm stage and tuning capacitors. The programmable Gm stage is used to guarantee startup and to sustain oscillation. Tuning capacitors are used to adjust the XO center frequency and control the XO precision for different crystal models. The output of the XO is driven to the digital domain via a digital buffer stage with a supply voltage of 1.2V.

Table 7-3. RTC XO Interface

Pin Name	Function	Register Default
Digital Control Pins		
Pierce_res_ctrl	Control feedback resistance value: 0 = 20MΩ Feedback resistance 1 = 30MΩ Feedback resistance	0X4000F404<15>='1'
Pierce_cap_ctrl<3:0>	Control the internal tuning capacitors with step of 700fF: 0000=700fF 1111=11.2pF Refer to crystal datasheet to check for optimum tuning cap value	0X4000F404<23:20>="1000"
Pierce_gm_ctrl<3:0>	Controls the Gm stage gain for different crystal mode: 0011= for crystal with shunt cap of 1.2pF 1000= for crystal with shunt cap >3pF	0X4000F404<19:16>="1000"
VDD_XO	1.2V	

7.3.3 RTC Characterization with Gm Code Variation at Supply 1.2V and Temp. = 25°C

This section shows the RTC total drawn current and the XO accuracy versus different tuning capacitors and different GM codes, at a supply voltage of 1.2V and temperature = 25°C.

Figure 7-3. RTC Drawn Current vs. Tuning Caps at 25°C

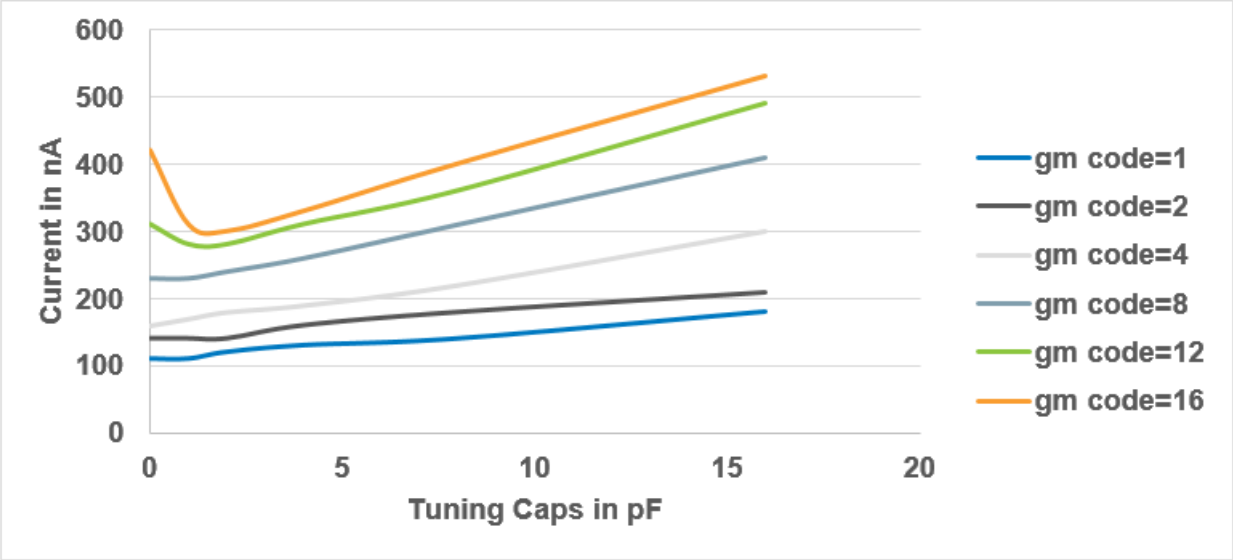
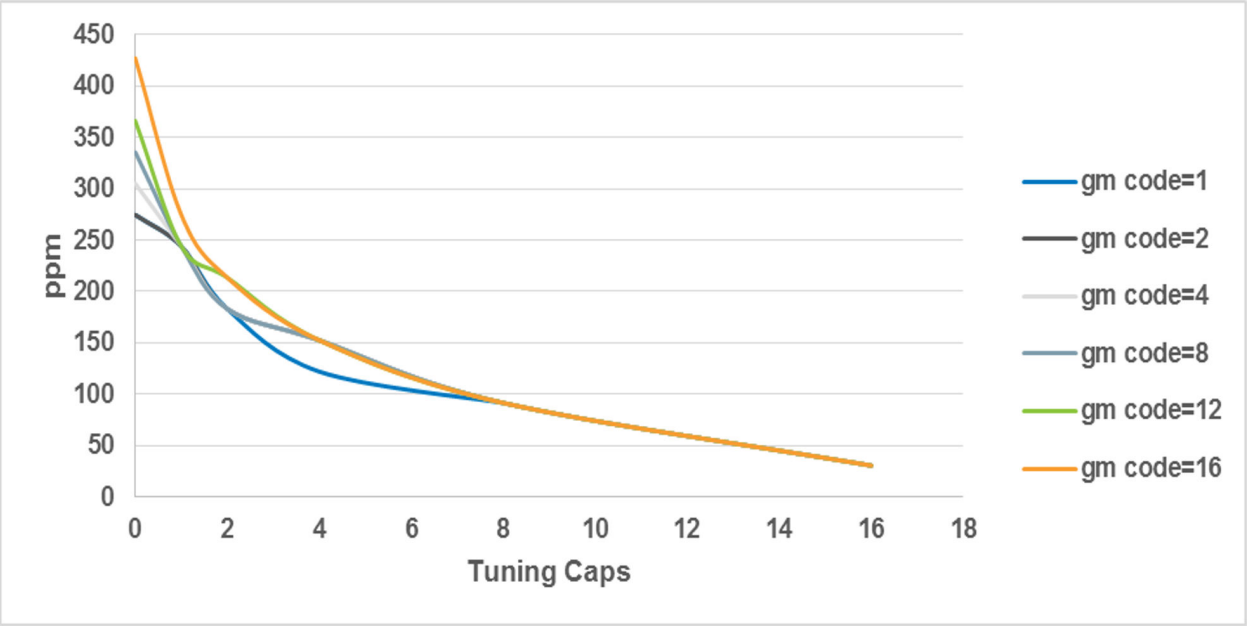


Figure 7-4. RTC Oscillation Frequency Deviation vs. Tuning Caps at 25°C



7.3.4 RTC Characterization with Supply Variation and Temp. = 25°C

Figure 7-5. RTC Drawn Current vs. Supply Variation

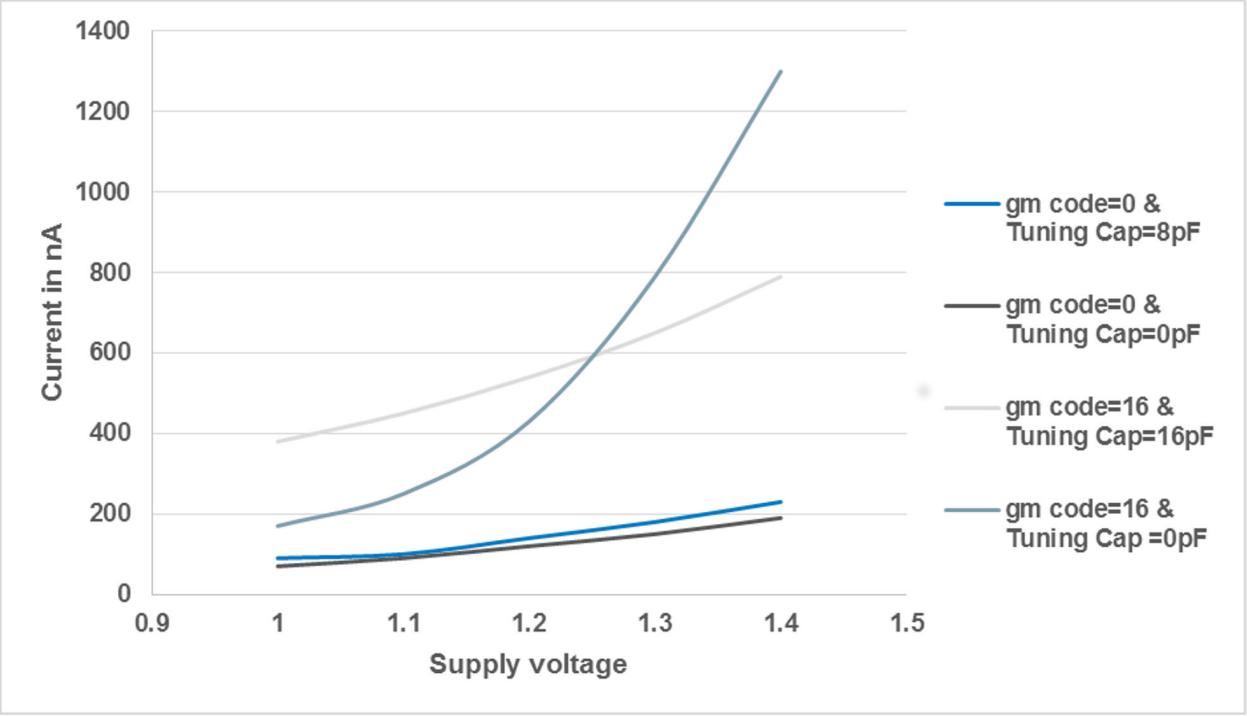
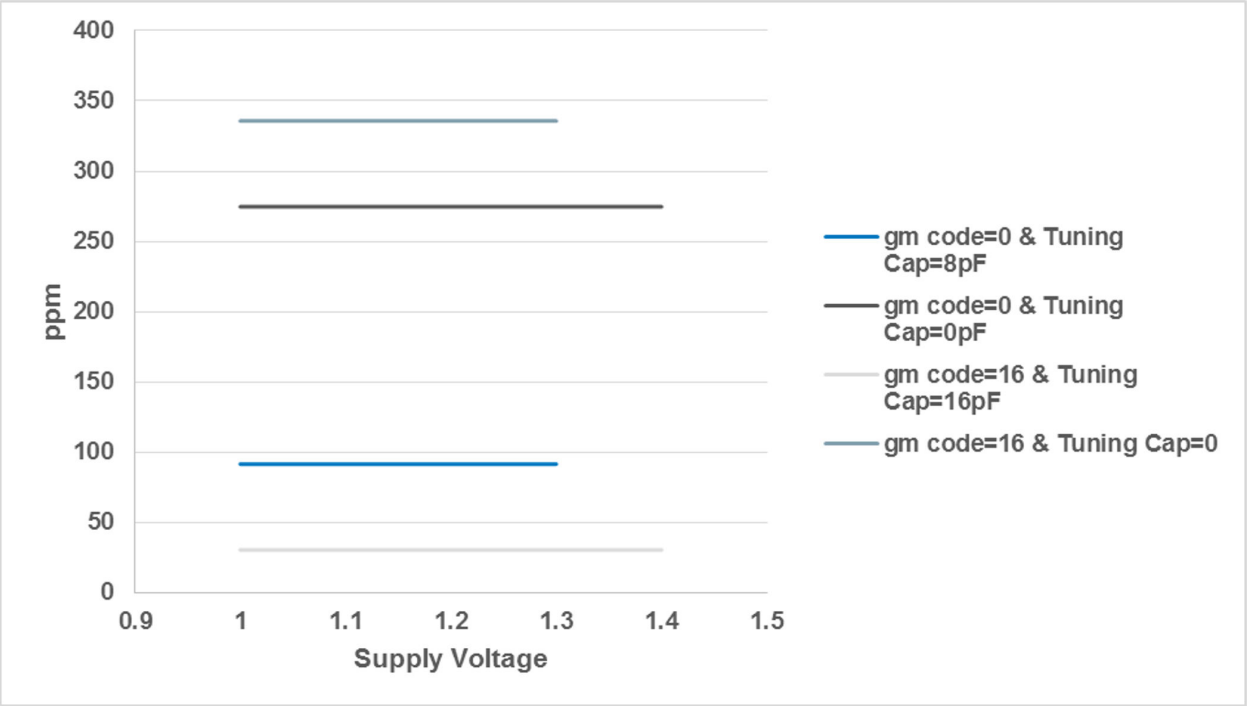


Figure 7-6. RTC Frequency Deviation vs. Supply Voltage



7.4 2MHz Integrated RC Oscillator

The 2MHz integrated RC Oscillator circuit without calibration has a frequency variation of 50% over process, temperature, and voltage variation. As described above, calibration over process, temperature, and voltage is required to maintain the accuracy of this clock.

Figure 7-7. 32kHz RC Oscillator PPM Variation vs. Calibration Time at Room Temperature

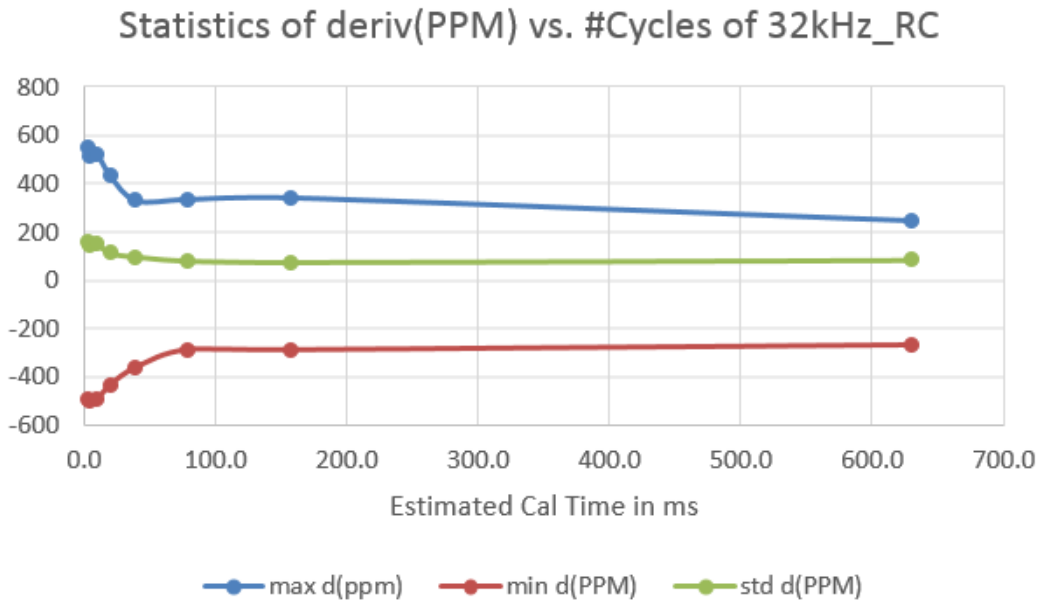
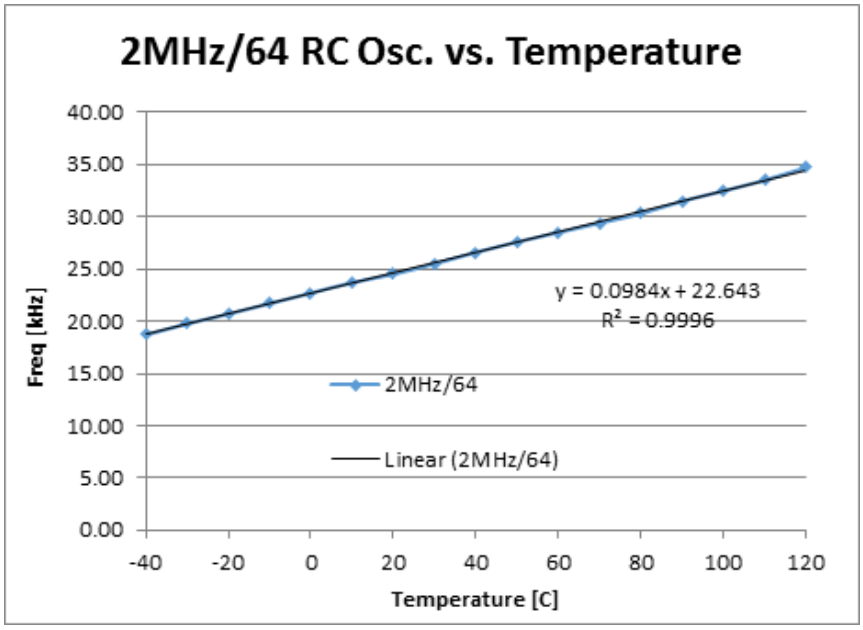


Figure 7-8. 32kHz RC Oscillator Frequency Variation over Temperature



8. CPU and Memory Subsystem

8.1 ARM Subsystem

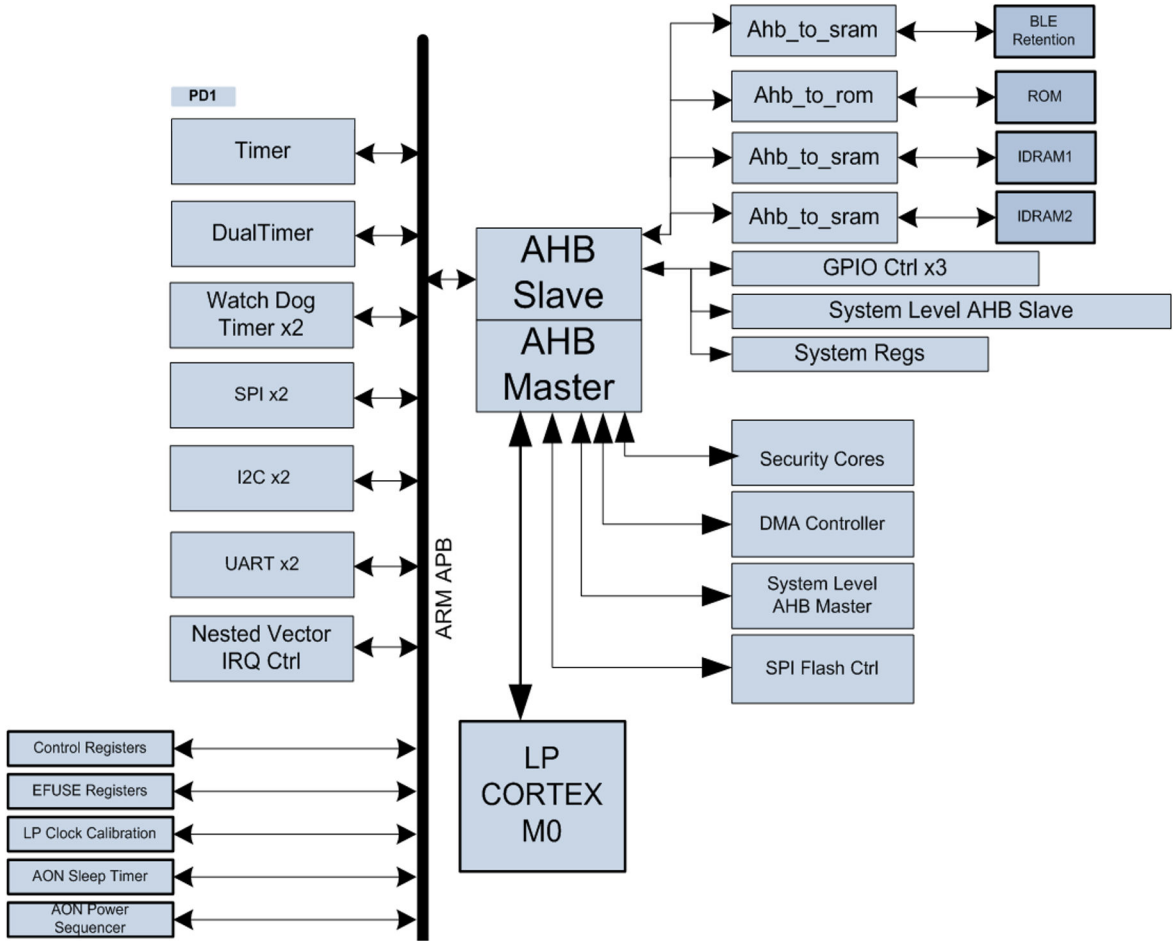
The ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA have an ARM Cortex-M0 32-bit processor. It is responsible for controlling the BLE Subsystem and handling all application features.

The Cortex-M0 Microcontroller consists of a full 32-bit processor capable of addressing 4GB of memory. It has a RISC-like load/store instruction set and internal 3-stage Pipeline Von Neumann architecture.

The Cortex-M0 processor provides a single system-level interface using AMBA technology to provide high speed, low latency memory accesses.

The Cortex-M0 processor implements a complete hardware debug solution, with four hardware breakpoint and two watchpoint options. This provides high system visibility of the processor, memory, and peripherals through a 2-pin Serial Wire Debug (SWD) port that is ideal for microcontrollers and other small package devices.

Figure 8-1. ARM Cortex-M0 Subsystem



8.1.1 Features

The processor features and benefits are:

- Tight integration with the system peripherals to reduce area and development costs

- Thumb instruction set combines high code density with 32-bit performance
- Integrated sleep modes using a Wakeup Interrupt Controller for low power consumption
- Deterministic, high-performance interrupt handling via Nested Vector Interrupt Controller for time-critical applications
- Serial Wire Debug reduces the number of pins required for debugging
- DMA engine for Peripheral-to-Memory, Memory-to-Memory, and Memory-to-Peripheral operation

8.1.2 ARM Module Descriptions

8.1.2.1 Timer

The 32-bit timer block allows the CPU to generate a time tick at a programmed interval. This feature can be used for a wide variety of functions such as counting, interrupt generation, and time tracking.

Note: Usage of this peripheral is not supported by the SDK. Datasheet will be updated once support for this feature is added in SDK.

8.1.2.2 Dual Timer

The APB dual-input timer module is an APB slave module consisting of two programmable 32-bit down-counters that can generate interrupts when they expire. The timer can be used in a Free-running, Periodic, or One-shot mode.

Note: Usage of this peripheral is not supported by the SDK. Datasheet will be updated once support for this feature is added in SDK.

8.1.2.3 Watchdog Timer

The two watchdog blocks allow the CPU to be interrupted if it has not interacted with the watchdog timer before it expires. In addition, this interrupt will be an output of the core so that it can be used to reset the CPU in the event that a direct interrupt to the CPU is not useful. This will allow the CPU to get back to a known state in the event a program is no longer executing as expected. The watchdog module applies a reset to a system in the event of a software failure, providing a way to recover from software crashes.

Watchdog timer is being used by the BLE stack. It cannot be used by user application.

8.1.2.4 Wake up Timer

This timer is a 32-bit countdown timer that operates on the 32kHz sleep clock. It can be used as a general-purpose timer for the ARM or as a wakeup source for the chip. It has the ability to be a one-time programmable timer, as it will generate an interrupt/wakeup on expiration and stop operation. It also has the ability to be programmed in an auto reload fashion where it will generate an interrupt/wakeup and then proceed to start another countdown sequence.

Note: Usage of this peripheral is not supported by the SDK. Datasheet will be updated once support for this feature is added in SDK.

8.1.2.5 SPI Controller

See Section SPI Master/Slave Interface.

Note: Usage of this peripheral is not supported by the SDK. Datasheet will be updated once support for this feature is added in SDK.

8.1.2.6 I2C Controller

See Section I2C Master/Slave Interface.

Note: Usage of this peripheral is not supported by the SDK. Datasheet will be updated once support for this feature is added in SDK.

8.1.2.7 UART

See Section UART Interface.

Note: Accessing and controlling the registers of this peripheral is not supported by the SDK. Datasheet will be updated once support for this feature is added in SDK.

8.1.2.8 DMA Controller

Direct Memory Access (DMA) allows certain hardware subsystems to access main system memory independently of the Cortex-M0 Processor.

The DMA features and benefits are:

- Supports any address alignment
- Supports any buffer size alignment
- Peripheral flow control, including peripheral block transfer
- The following modes are supported:
  - Peripheral to peripheral transfer
  - Memory to memory
  - Memory to peripheral
  - Peripheral to memory
  - Register to memory
- Interrupts for both TX done and RX done in memory and peripheral mode
- Scheduled transfers
- Endianness byte swapping
- Watchdog timer
- 4-channel operation
- 32-bit Data width
- AHB MUX (on read and write buses)
- Command lists support
- Usage of tokens

Note: Usage of this peripheral is not supported by the SDK. Datasheet will be updated once support for this feature is added in SDK.

8.1.2.9 Nested Vector Interrupt Controller

External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0 processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts.

All NVIC registers are accessible via word transfers and are little endian. Any attempt to read or write a half-word or byte individually is unpredictable.

The NVIC allows the CPU to be able to individually enable, disable each interrupt source, and hold each interrupt until it has been serviced and cleared by the CPU.

Table 8-1. NVIC Register Summary

Name	Description
ISER	Interrupt Set-Enable Register
ICER	Interrupt Clear-Enable Register
ISPR	Interrupt Set-Pending Register
ICPR	Interrupt Clear-Pending Register
IPR0-IPR7	Interrupt Priority Registers

For a description of each register, see the Cortex-M0 documentation from ARM.

8.1.2.10 GPIO Controller

The AHB GPIO is a general-purpose I/O interface unit allowing the CPU to independently control all input or output signals on the ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA. These can be used for a wide variety of functions pertaining to the application.

The AHB GPIO provides a 16-bit I/O interface with the following features:

- Programmable interrupt generation capability
- Programmable masking support
- Thread-safe operation by providing separate set and clear addresses for control registers
- Inputs are sampled using a double flip-flop to avoid meta-stability issues

Note: Usage of this peripheral is not supported by the SDK. Datasheet will be updated once support for this feature is added in SDK.

8.2 Memory Subsystem

The Cortex-M0 core uses a 128KB instruction/boot ROM along with a 128KB shared instruction and data RAM.

8.2.1 Shared Instruction and Data Memory

The Instruction and Data Memory (IDRAM1 and IDRAM2) contains instructions and data used by the ARM. The size of IDRAM1 and IDRAM2 is 128KB that can be used for BLE subsystem as well as for the user application. IDRAM1 contains three 32KB and IDRAM2 contains two 16KB memories that are accessible to the ARM and used for instruction/data storage.

8.2.2 ROM

The ROM is used to store the boot code and BLE firmware, stack, and selected user profiles. ROM contains the 128KB memory that is accessible to the ARM.

8.2.3 BLE Retention Memory

The BLE functionality requires 8KB retention memory for retaining state, instruction, and data when the processor either goes into Sleep Mode or Power Off Mode. The RAM is separated into specific power domains to allow tradeoff in power consumption with retention memory size.

8.3 Non-Volatile Memory

The ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA have 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This memory region is one time programmable. It is partitioned into six 128-bit banks. Each bank is divided into 4 blocks with each block containing 32 bits of memory locations. This non-volatile one-time-programmable memory is used to store customer-specific parameters as listed below

- 26 MHz XO Calibration information
- UART hardware flow control pin selection
- BT address

The bit map for the block containing the above parameters are detailed in the following figures.

Figure 8-2. Bank 5 Block 0

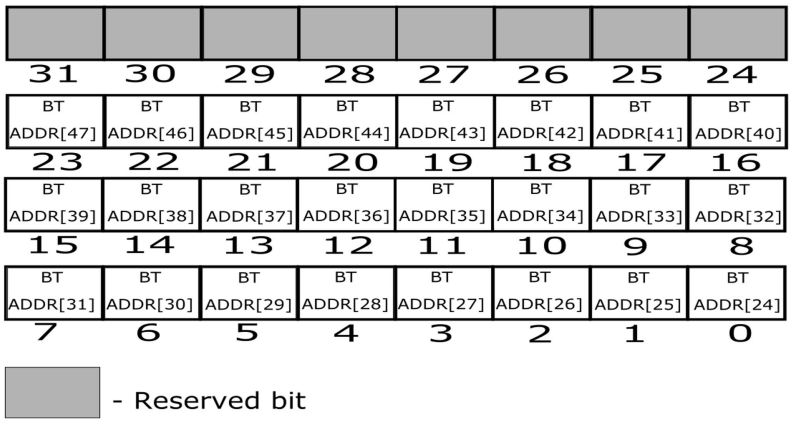


Figure 8-3. Bank 5 Block 1

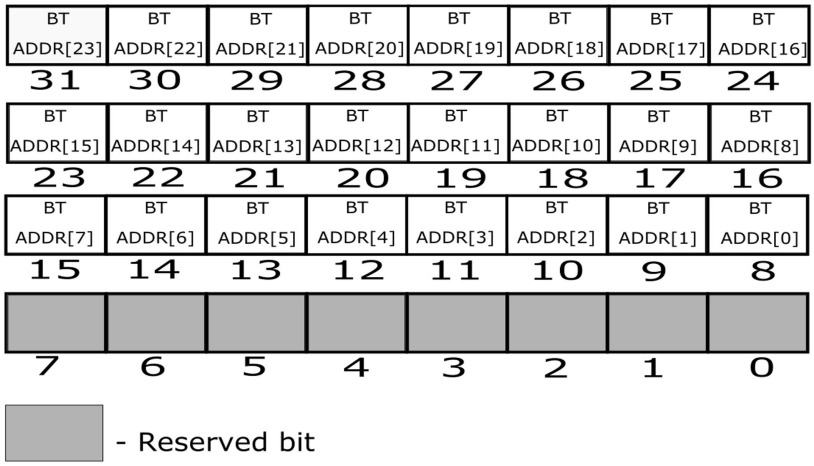
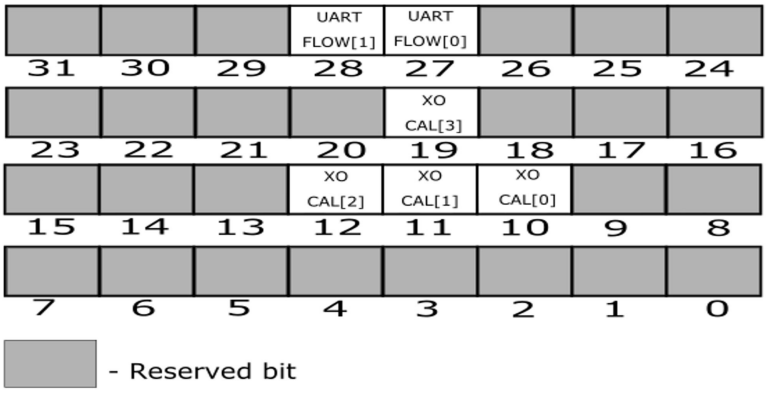


Figure 8-4. Bank 5 Block 3



The bits that are not depicted in the above register description are all reserved for future use.

8.3.1 26 MHz XO Calibration information

For both ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA, this information will be pre-programmed. The user does not need to reconfigure them.

8.3.2 UART hardware flow control pin selection

These bits determine the LP_GPIO pins to be used as the hardware flow control pins(RTS and CTS) of the UART interface with host MCU. For both ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA, these bits will have a default value of 0b10. Find below the possible values for this bits and the corresponding configuration.

Table 8-2. UART Flow control Bank 5 Block 3

UART Flow control Bank 5 Block 3[28:27]	UART RTS	UART CTS
0b10	LP_GPIO_9	LP_GPIO_8
0b11	LP_GPIO_5	LP_GPIO_4

Note: Other values for this bits are reserved

8.3.3 BT Address

These bits contain the BT address which could be used by the user application. For ATBTLC1000-ZR110CA modules, BT address will be pre-programmed. For ATBTLC1000-XR1100A, user must purchase the MAC address from IEEE and store in the non-volatile memory section of the host MCU. During initialization of the ATBTLC1000-XR1100A, the BLE address could be set by the host MCU. Refer to API User manual available in the BluSDK release package for more details on acheiving this.

9. Bluetooth Low Energy (BLE) Subsystem

The BLE subsystem implements all the critical real-time functions required for full compliance with Specification of the Bluetooth System, v4.1, Bluetooth SIG.

It consists of a Bluetooth 4.1 baseband controller (core), radio transceiver and the Microchip Bluetooth Smart Stack, the BLE Software Platform.

9.1 BLE Core

The baseband controller consists of a modem and a Medium Access Controller (MAC) and it constructs baseband data packages, schedules frames, and manages and monitors connection status, slot usage, data flow, routing, segmentation, and buffer control.

The core performs Link Control Layer management supporting the main BLE states, including advertising and connection.

9.1.1 Features

- Broadcaster, Central, Observer, Peripheral
- Simultaneous Master and Slave operation, connect up to eight connections
- Frequency Hopping
- Advertising/Data/Control packet types
- Encryption (AES-128)
- Bitstream processing (CRC, whitening)
- Operating clock 52MHz

9.2 BLE Radio

The radio consists of a fully integrated transceiver, including Low Noise Amplifier, Receive (RX) down converter, and analog baseband processing as well as Phase Locked Loop (PLL), Transmit (TX) Power Amplifier, and Transmit/Receive switch. At the RF front end, no external RF components on the PCB are required other than the antenna and a matching component.

9.3 Microchip BluSDK

BluSDK offers a comprehensive set of tools - including reference applications for several Bluetooth SIG defined profiles and custom profile. This will help the user to quickly evaluate, design and develop BLE products with ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA.

The ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA have a completely integrated Bluetooth Low Energy stack on chip, fully qualified, mature, and Bluetooth V4.1 compliant.

Customer applications interface with the BLE protocol stack through the adaptor library API, which supports direct access to the GAP, SMP, ATT, GATT client / server, and L2CAP service layer protocols in the embedded firmware.

The stack includes numerous BLE profiles for applications like:

- Smart Energy
- Consumer Wellness
- Home Automation

- Security
- Proximity Detection
- Entertainment
- Sports and Fitness
- Key fob

Together with the Atmel Studio Software Development environment, additional customer profiles can be easily developed.

Refer to BluSDK release notes for more details on the supported host MCU architecture and compilers.

9.3.1 Direct Test Mode (DTM) Example Application

One among the reference application offered in BluSDK is DTM example application. Using this application, customer will be able to configure the device in the different test modes as defined in the Bluetooth Low Energy Core 4.1 specification (Vol6,Part F Direct Test Mode). Please refer the example getting started guide available in the BluSDK release package.

10. External Interfaces

10.1 Overview

ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA external interfaces include: 2xSPI Master/Slave (SPI0 and SPI1), 2xI2C Master/Slave (I2C0 and I2C1), 1xI2C Slave-only (I2C2), 2xUART (UART1 and UART2), 1xSPI Flash, 1xSWD, and General Purpose Input/Output (GPIO) pins.

Caution: Usage of the above mentioned peripherals is not supported by the SDK. Datasheet will be updated once support is added in SDK. The host interface is UART with flow control and refer to ATBTLC1000-XR/ZR Host Microcontroller Interface for the configurations.

Table Pin-MUX Matrix of External Interfaces illustrates the different peripheral functions that are software selectable for each pin. This allows for maximum flexibility of mapping desired interfaces on GPIO pins. The MUX1 option allows for any MEGAMUX option from Table Software Selectable MEGAMUX Options to be assigned to a GPIO.

Table 10-1. Pin-MUX Matrix of External Interfaces

Pin Name	XR Pin #	ZR Pin #	Pull	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	MUX7
LP_GPIO_0	35	12	Up/ Down	GPIO 0	MEGAMUX 0	SWD CLK					TEST OUT 0
LP_GPIO_1	36	13	Up/ Down	GPIO 1	MEGAMUX 1	SWD I/O					TEST OUT 1
LP_GPIO_2	37	14	Up/ Down	GPIO 2	MEGAMUX 2	UART1 RXD		SPI1 SCK	SPI0 SCK		TEST OUT 2
LP_GPIO_3	38	15	Up/ Down	GPIO 3	MEGAMUX 3	UART1 TXD		SPI1 MOSI	SPI0 MOSI		TEST OUT 3
LP_GPIO_4	39	16	Up/ Down	GPIO 4	MEGAMUX 4	UART1 CTS		SPI1 SSN	SPI0 SSN		TEST OUT 4
LP_GPIO_5	2	17	Up/ Down	GPIO 5	MEGAMUX 5	UART1 RTS		SPI1 MISO	SPI0 MISO		TEST OUT 5
LP_GPIO_6	3	18	Up/ Down	GPIO 6	MEGAMUX 6	UART2 RXD			SPI0 SCK		TEST OUT 6
LP_GPIO_7	4	19	Up/ Down	GPIO 7	MEGAMUX 7	UART2 TXD			SPI0 MOSI		TEST OUT 7
LP_GPIO_8	5	20	Up/ Down	GPIO 8	MEGAMUX 8	I2C0 SDA	I2C2 SDA		SPI0 SSN		TEST OUT 8
LP_GPIO_9	6	21	Up/ Down	GPIO 9	MEGAMUX 9	I2C0 SCL	I2C2 SCL		SPI0 MISO		TEST OUT 9

Pin Name	XR Pin #	ZR Pin #	Pull	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	MUX7
LP_GPIO_10	7	22	Up/ Down	GPIO 10	MEGAMUX 10	SPI0 SCK					TEST OUT 10
LP_GPIO_11	8	23	Up/ Down	GPIO 11	MEGAMUX 11	SPI0 MOSI					TEST OUT 11
LP_GPIO_12	9	24	Up/ Down	GPIO 12	MEGAMUX 12	SPI0 SSN					TEST OUT 12
LP_GPIO_13	10	25	Up/ Down	GPIO 13	MEGAMUX 13	SPI0 MISO					TEST OUT 13
LP_GPIO_14	23	4	Up/ Down	GPIO 14	MEGAMUX 14	UART2 CTS		I2C1 SDA			TEST OUT 14
LP_GPIO_15	24	5	Up/ Down	GPIO 15	MEGAMUX 15	UART2 RTS		I2C1 SLC			TEST OUT 15
LP_GPIO_16	25	6	Up/ Down	GPIO 16	MEGAMUX 16			SPI1 SSN	SPI0 SCK		TEST OUT 16
LP_GPIO_17	28	8	Up/ Down	GPIO 17	MEGAMUX 17		I2C2 SDA	SPI1 SCK	SPI0 MOSI		TEST OUT 17
LP_GPIO_18	29	9	Up/ Down	GPIO 18	MEGAMUX 18		I2C2 SCL	SPI1 MISO	SPI0 SSN		TEST OUT 18
LP_GPIO_22	40		Up/ Down	GPIO 22	MEGAMUX 22						
LP_GPIO_23	1		Up/ Down	GPIO 23	MEGAMUX 23						
AO_GPIO_0	20	1	Up	GPIO 31	WAKEUP	RTC CLK IN	32kHZ CLK OUT				
AO_GPIO_1	21	2	Up		WAKEUP	RTC CLK IN	32kHZ CLK OUT				

Pin Name	XR Pin #	ZR Pin #	Pull	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	MUX7
AO_GPIO_2	22	3	Up		WAKEUP	RTC CLK IN	32kHZ CLK OUT				
GPIO_MS1	12	17	Up/ Down	GPIO 47							
GPIO_MS2	13	18	Up/ Down	GPIO 46							
GPIO_MS3	15	31	Up/ Down	GPIO 45							
GPIO_MS4	16	32	Up/ Down	GPIO 44							

Table Software Selectable MEGAMUX Options shows the various software selectable MEGAMUX options that correspond to specific peripheral functionality.

Table 10-2. Software Selectable MEGAMUX Options

MUX_Sel	Function	Notes
0	UART1 RXD	
1	UART1 TXD	
2	UART1 CTS	
3	UART1 RTS	
4	UART2 RXD	
5	UART2 TXD	
6	UART2 CTS	
7	UART2 RTS	
8	I2C0 SDA	
9	I2C0 SCL	
10	I2C1 SDA	
11	I2C1 SCL	
12	PWM 1	
13	PWM 2	
14	PWM 3	
15	PWM 4	
16	LP CLOCK OUT	32kHz clock output (RC Osc. or RTC XO)
17	Reserved	

MUX_Sel	Function	Notes
18	Reserved	
19	Reserved	
20	Reserved	
21	Reserved	
22	Reserved	
23	Reserved	
24	Reserved	
25	Reserved	
26	Reserved	
27	Reserved	
28	Reserved	
29	QUAD DEC X IN A	
30	QUAD DEC X IN B	
31	QUAD DEC Y IN A	
32	QUAD DEC Y IN B	
33	QUAD DEC Z IN A	
34	QUAD DEC Z IN B	

An example of peripheral assignment using these MEGAMUX options is as follows:

- I2C0 pin-MUXed on LP_GPIO_8 and LP_GPIO_9 via MUX1 and MEGAMUX=8 and 9 (Table Software Selectable MEGAMUX Options)
- I2C1 pin-MUXed on LP_GPIO_14 and LP_GPIO_15 via MUX1 and MEGAMUX=14 and 15 (Table Software Selectable MEGAMUX Options)
- UART1 pin-MUXed on LP_GPIO_2 and LP_GPIO_3 via MUX1 and MEGAMUX=2 (Table Software Selectable MEGAMUX Options)

Another example is to illustrate the available options for pin LP_GPIO_3, depending on the pin-MUX option selected:

- MUX0: the pin will function as bit 3 of the GPIO bus and is controlled by the GPIO controller in the ARM subsystem
- MUX1: any option from the MEGAMUX table can be selected, for example, it can be a quad_dec, pwm, or any of the other functions listed in the MEGAMUX table
- MUX2: the pin will function as UART1 TXD; this can be also achieved with the MUX1 option via MEGAMUX, but the MUX2 option allows a shortcut for the recommended pinout
- MUX3: this option is not used and thus defaults to the GPIO option (same as MUX0)
- MUX4: the pin will function as SPI1 MOSI (this option is not available through MEGAMUX)
- MUX5: the pin will function as SPI0 MOSI (this option is not available through MEGAMUX)
- MUX7: the pin will function as bit 3 of the test output bus, giving access to various debug signals

10.2 I2C Master/Slave Interface

10.2.1 Description

The ATBTLC1000-XR1100A and ATBTLC1000-110CA provides an I2C Interface that can be configured as Slave or Master. I2C Interface is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). The ATBTLC1000-XR1100A and ATBTLC1000-110CA I2C support I2C bus Version 2.1 - 2000 and can operate in the following speed modes:

- Standard mode (100kb/s)
- Fast mode (400kb/s)
- High-speed mode (3.4Mb/s)

The I2C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I2C -Bus Specification, Ver 2.1”.

10.3 SPI Master/Slave Interface

10.3.1 Description

ATBTLC1000-XR1100A and ATBTLC1000-ZR100CA provides a Serial Peripheral Interface (SPI) that can be configured as Master or Slave. The SPI Interface pins are mapped as shown in Table SPI Interface Pin Mapping. The SPI Interface is a full-duplex slave-synchronous serial interface. When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line. The SPI Slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

Table 10-3. SPI Interface Pin Mapping

Pin Name	SPI Function
SSN	Active Low Slave Select
SCK	Serial Clock
MOSI	Master Out Slave In (Data)
MISO	Master In Slave Out (Data)

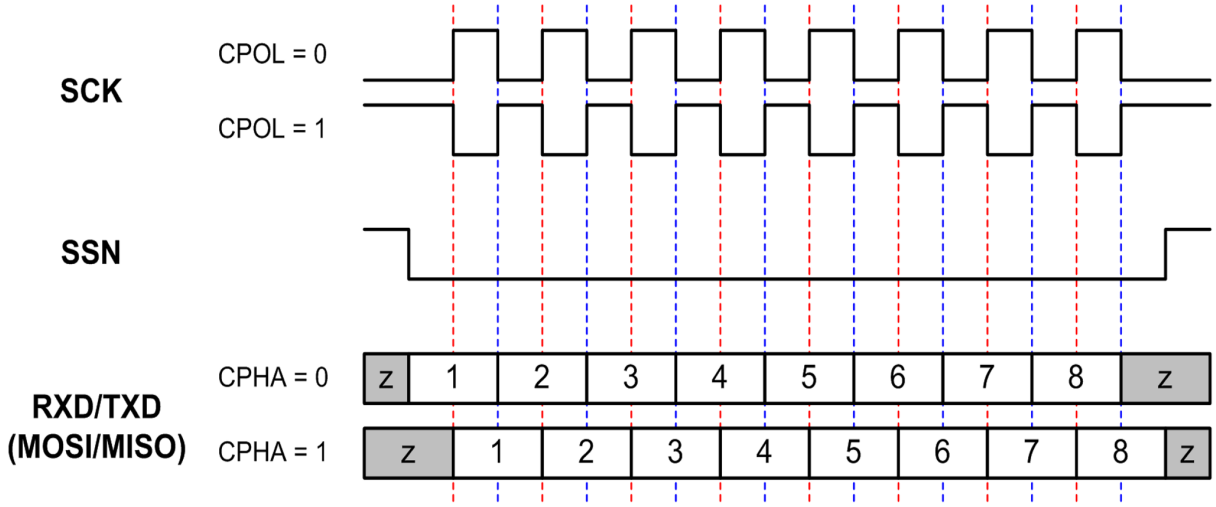
10.3.2 SPI Interface Modes

The SPI Interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in Table SPI Modes and Figure SPI Clock Polarity and Clock Phase Timing. The red lines in Figure SPI Clock Polarity and Clock Phase Timing correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Table 10-4. SPI Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Figure 10-1. SPI Clock Polarity and Clock Phase Timing



10.4 UART Interface

The ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA provide Universal Asynchronous Receiver/Transmitter (UART) interfaces for serial communication. The Bluetooth subsystem has two UART interfaces: a 2-Pin interface with TX and RX, and a 4-pin interface with TX and RX and hardware flow control (RTS and CTS). The UART interfaces are compatible with the RS-232 standard, where the ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA operate as Data Terminal Equipment (DTE).

Caution: The RTS and CTS are used for hardware flow control; they MUST be connected to the host MCU UART and enabled for the UART interface to be functional.

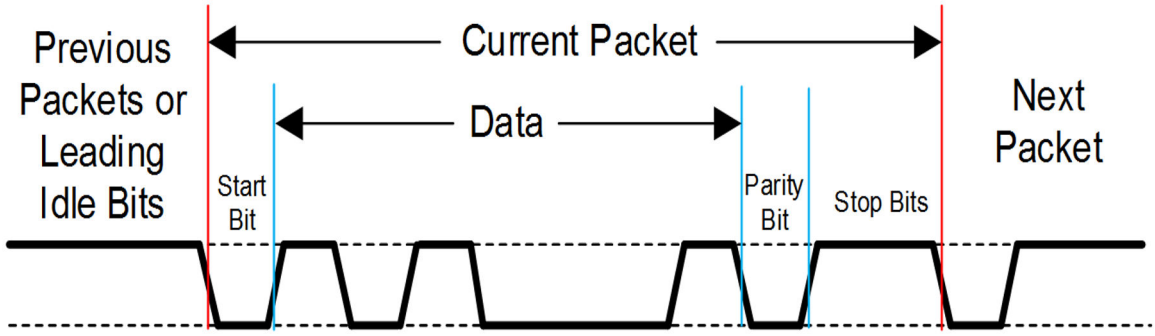
The pins associated with each the UART interfaces can be enabled on several alternative pins by programming their corresponding pin-MUX control registers (see Table Pin-MUX Matrix of External Interfaces and Table Software Selectable MEGAMUX Options for available options).

The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The Bluetooth UART input clock is selectable between 26MHz, 13MHz, 6.5MHz, and 3.25MHz. The clock divider value is programmable as 13 integer bits and three fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 26MHz/8.0 = 3.25MBd.

The UART can be configured for seven or eight-bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has RX and TX FIFOs, which ensure reliable high-speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in Figure Example of UART RX or TX Packet. This example shows 7-bit data (0x45), odd parity, and two stop bits.

Figure 10-2. Example of UART RX or TX Packet



10.5 GPIOs

15 General Purpose Input/Output (GPIO) pins total, labeled LP_GPIO, GPIO_MS, and AO_GPIO, are available to allow for application specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output. The host or internal processor can program the output values.

LP_GPIO are digital interface pins, GPIO_MS are mixed signal/analog interface pins, and AO_GPIO is an always-on digital interface pin that can detect interrupt signals while in deep sleep mode for wake-up purposes.

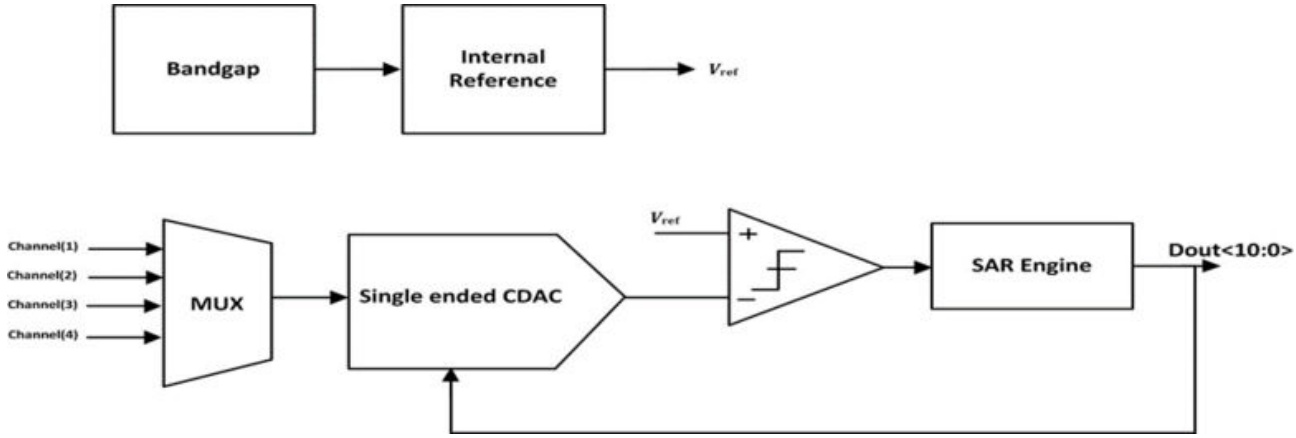
The LP_GPIO have interrupt capability, but only when in active/standby mode. In sleep mode, they are turned off to save power consumption.

10.6 Analog to Digital Converter (ADC)

10.6.1 Overview

The ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA have an integrated Successive Approximation Register (SAR) ADC with 11-bit resolution and variable conversion speed up 1MS/s. The key building blocks are the capacitive DAC, comparator, and synchronous SAR engine as shown in Figure SAR ADC Block Diagram.

Figure 10-3. SAR ADC Block Diagram



The ADC reference voltage can be either generated internally or set externally via one of the four available Mixed Signal GPIO pins on the ATBTLC1000-XR1100A and the ATBTLC1000-ZR110CA.

There are two modes of operation:

High resolution (11-bit): Set the reference voltage to half the supply voltage or below. In this condition the input signal dynamic range is equal to twice the reference voltage (ENOB=10bit).

Medium Resolution (10-bit) : Set the reference voltage to any value below supply voltage (up to supply voltage - 300mV) and in this condition the input dynamic range is from zero to the reference voltage (ENOB = 9bit).

Four input channels are time multiplexed to the input of the SAR ADC. However, on the ATBTLC1000, only four channel inputs are accessible from the outside, through pins 28, 29, 31, and 32 (Mixed Signal GPIO pins).

In power saving mode, the internal reference voltage is completely off and the reference voltage is set externally.

The ADC characteristics are summarized in Table SAR ADC Characteristics.

Table 10-5. SAR ADC Characteristics

Conversion rate	1ks → 1MS
Selectable Resolution	10 → 11bit
Power consumption	13.5µA (at 100KS/s) (1)

Note:

1. With external reference.

10.6.2 Timing

The ADC timing is shown in Figure SAR ADC Timing. The input signal is sampled twice, in the first sampling cycle the input range is defined either to be above reference voltage or below it and in the second sampling instant the ADC start its normal operation.

The ADC takes two sampling instants and N-1 conversion cycle (N=ADC resolution) and one cycle to sample the data out. Therefore, for the 11-bit resolution, it takes 13 clock cycles to do one Sample conversion.

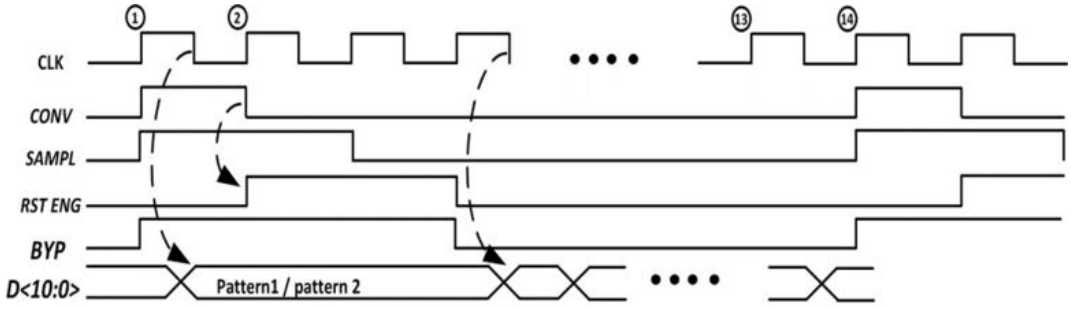
The Input clock equals N+2 the sampling clock frequency (N is the ADC resolution).

CONV signal : Gives indication about end of conversion.

SAMPL : The input signal is sampled when this signal is high.

RST ENG : When High SAR Engine is in reset mode (SAR engine output is set to mid-scale).

Figure 10-4. SAR ADC Timing



10.7 Software Programmable Timer and Pulse Width Modulator

The ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA contain four individually configurable pulse width modulator (PWM) blocks to provide external control voltages. The base frequency of the PWM block (f_{PWM} _base) is derived from the XO clock (26MHz) or the RC oscillator followed by a programmable divider.

The frequency of each PWM pulse (f_{PWM}) is programmable in steps according to the following relationship:

$$f_{PWM} = \frac{f_{PWM\_base}}{64*2^{i}} \qquad i = 0,1,2,\ldots,8$$

The duty cycle of each PWM signal is configurable with 10-bit resolution (minimum duty cycle is 1/1024 and the maximum is 1023/1024).

$f_{PWM\ base}$ can be selected to have different values according to Table f_{PWM} Range for Different f_{PWM} Base Frequencies. Minimum and maximum frequencies supported for each clock selection are listed in the table as well.

Table 10-6. f_{PWM} Range for Different f_{PWM} Base Frequencies

$f_{PWM\ base}$	f_{PWM} max.	f_{PWM} min.
26MHz	406.25kHz	1.586kHz
13MHz	203.125kHz	793.25Hz
6.5MHz	101.562kHz	396.72Hz
3.25MHz	50.781kHz	198.36Hz

10.8 Clock Output

The ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA have an option to output a clock. The clock can be output to any GPIO pin via the test MUX. Note that this feature requires that the ARM and BLE power domains stay on. If BLE is not used, the clocks to the BLE core are gated off, resulting in small leakage. The following two methods can be used to output a clock.

Note:

Refer the BluSDK BLE API Software Development Guide for details on how to enable the 32.768kHz clock output.

10.8.1 Variable Frequency Clock Output Using Fractional Divider

The ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA can output the variable frequency ADC clock using a fractional divider of the 26MHz oscillator. This clock needs to be enabled using bit 10 of the lpmcu_clock_enables_1 register. The clock frequency can be controlled by the divider ratio using the sens_adc_clk_ctrl register (12-bits integer part, 8-bit fractional part).The division ratio can vary from 2 to 4096 delivering output frequency between 6.35kHz to 13MHz. This is a digital divider with pulse swallowing implementation so the clock edges may not be at exact intervals for the fractional ratios. However, it is exact for integer division ratios.

10.8.2 Fixed Frequency Clock Output

The ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA can output the following fixed-frequency clocks:

- 52MHz derived from XO
- 26MHz derived from XO
- 2MHz derived from the 2MHz RC Osc.
- 31.25kHz derived from the 2MHz RC Osc.
- 32.768kHz derived from the RTC XO
- 26MHz derived from 26MHz RC Osc.
- 6.5MHz derived from XO
- 3.25MHz derived from 26MHz RC Osc.

For clocks 26MHz and above, ensure that external pad load on the board is minimized to get a clean waveform.

10.9 Three-axis Quadrature Decoder

The ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA have a three-axis Quadrature decoder (X, Y, and Z) that can determine the direction and speed of movement on three axes, requiring in total six GPIO pins to interface with the sensors. The sensors are expected to provide pulse trains as inputs to the quadrature decoder.

Each axis channel input will have two pulses with ±90 degrees phase shift depending on the direction of movement. The decoder counts the edges of the two waveforms to determine the speed and uses the phase relationship between the two inputs to determine the direction of motion.

The decoder is configured to interrupt ARM based on independent thresholds for each direction. Each quadrature clock counter (X, Y, and Z) is an unsigned 16-bit counter and the system clock uses a programmable sampling clock ranging from 26MHz, 13, 6.5, to 3.25MHz.

If wakeup is desired from threshold detection on an axis input, an always-on GPIO needs to be used (there are three always-on GPIOs on ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA).

11. Electrical Characteristics

There are voltage ranges where different VDDIO levels apply. The reason for this separation is for the IO drivers whose drive strength is directly proportional to the IO supply voltage. In the ATBTLC1000 products, there is a large gap in the IO supply voltage range (1.8 to 4.3v). A guarantee on drive strength across this voltage range would be intolerable to most vendors who only use a subsection of the IO supply range. As such, these voltages are segmented into three manageable sections referenced as VDDIOL, VDDIOM, and VDDIOH in tables listed in this document.

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings

Symbol	Characteristics	Min.	Max.	Unit
VDDIO	I/O Supply Voltage	-0.3	5.0	V
VBAT	Battery Supply Voltage	-0.3	5.0	
V_{IN} (1)	Digital Input Voltage	-0.3	VDDIO	
V_{AIN} (2)	Analog Input Voltage	-0.3	1.5	
V_{ESDHBM} (3)	ESD Human Body Model	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	
T_A	Storage Temperature	-65	150	°C

Note:

1. V_{IN} corresponds to all the digital pins
2. V_{AIN} corresponds to all the analog pins, RFIO, XO_N, XO_P, TPP, RTC_CLK_N, RTC_CLK_P
3. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
   - The Class 1 pins include all the pins (both analog and digital)
   - The Class 2 pins include all digital pins only
   - V_{ESDHBM} is ±1kV for Class1 pins. V_{ESDHBM} is ±2kV for Class2 pins

11.2 Recommended Operating Conditions

Table 11-2. Recommended Operating Conditions

Symbol	Characteristic	Min.	Typ.	Max.	Unit
$VDDIO_L$	I/O Supply Voltage Low Range	1.62	1.80	2.00	V
$VDDIO_M$	I/O Supply Voltage Mid-Range	2.00	2.50	3.00	
$VDDIO_H$	I/O Supply Voltage High Range	3.00	3.30	3.60	
VBAT	Battery Supply Voltage (1)	1.8	3.6	4.3	
	Operating Temperature	-40		85	°C

Note:

1. VBAT must not be less than VDDIO.

2. When powering up the device, VBAT must be greater or equal to 1.9V to ensure BOD does not trigger. BOD threshold is typically 1.8V and the device will be held in reset if VBAT is near this threshold on startup. After startup, BOD can be disabled and the device can operate down to 1.8V.

11.3 DC Characteristics

Table DC Electrical Characteristics provides the DC characteristics for the digital pads.

Table 11-3. DC Electrical Characteristics

VDDIO Condition	Characteristic	Min.	Typ.	Max.	Unit
$VDDIO_L$	Input Low Voltage V_{IL}	-0.30		0.60	V
	Input High Voltage V_{IH}	VDDIO-0.60		VDDIO+0.30	
	Output Low Voltage V_{OL}			0.45	
	Output High Voltage V_{OH}	VDDIO-0.50			
$VDDIO_M$	Input Low Voltage V_{IL}	-0.30		0.63	
	Input High Voltage V_{IH}	VDDIO-0.60		VDDIO+0.30	
	Output Low Voltage V_{OL}			0.45	
	Output High Voltage V_{OH}	VDDIO-0.50			
$VDDIO_H$	Input Low Voltage V_{IL}	-0.30		0.65	
	Input High Voltage V_{IH}	VDDIO-0.60		VDDIO+0.30 (up to 3.60)	
	Output Low Voltage V_{OL}			0.45	
	Output High Voltage V_{OH}	VDDIO-0.50			
All	Output Loading			20	pF
	Digital Input Load			6	
$VDDIO_L$	Pad drive strength (regular pads (1))	1.7	2.5		mA
$VDDIO_M$	Pad drive strength (regular pads (1))	3.4	6.6		
$VDDIO_H$	Pad drive strength (regular pads (1))	10.5	14		
$VDDIO_L$	Pad drive strength (high-drive pads (1))	3.4	5.0		
$VDDIO_M$	Pad drive strength (high-drive pads (1))	6.8	13.2		
$VDDIO_H$	Pad drive strength	21	28		

VDDIO Condition	Characteristic	Min.	Typ.	Max.	Unit
	(high-drive pads [1])				

Note:

1. The following GPIO pads are high-drive pads: GPIO_8, GPIO_9; all other pads are regular pads.

11.4 Current Consumption in Various Device States

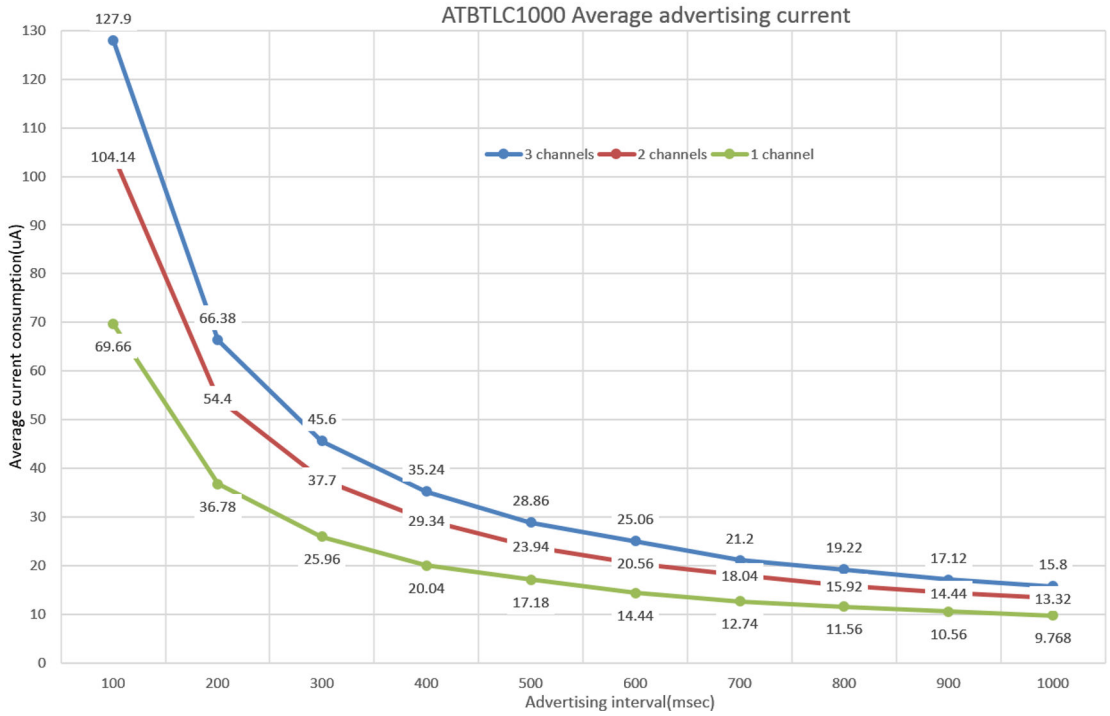
Table 11-4. ATBTLC1000 XR1100A/ATBTLC1000-ZR110CA Device State Current Consumption

Device State	C_EN	VDDIO	$I_{VBAT}+I_{VDDIO}$ (typical) [2]
Power_Down	Off	On	0.04 µA
Ultra_Low_Power with BLE timer, with RTC [1]	On	On	1.88 µA
BLE_On_Receive @channel 37(2402 MHz)	On	On	5.66 mA
BLE_On_Transmit, 0 dBm output power @channel 37(2402 MHz)	On	On	4.78 mA
BLE_On_Transmit, 0 dBm output power @channel 39(2480 MHz)	On	On	4.33 mA
BLE_On_Transmit, 3 dBm output power @Channel 37(2402 MHz)	On	On	6.20 mA
BLE_On_Transmit, 3 dBm output power @Channel 39(2480 MHz)	On	On	5.43 mA

Note:

1. Sleep clock derived from external 32.768 kHz crystal specified for CL=7pF, using the default on-chip capacitance only, without using external capacitance.
2. Measurement conditions
   - 2.1. VBAT=3.3V
   - 2.2. VDDIO=3.3V
   - 2.3. Temperature - 25°C
   - 2.4. These measurements are taken with FW BluSDK V6.1.7072

Figure 11-1. Average Advertising Current



Note:

1. The Average advertising current is measured at VBAT = 3.3 V, VDDIO = 3.3 V, TX output power=0dBm. Temperature - 25°C
2. Advertisement data payload size - 31 octets
3. Advertising event type - Connectable Undirected
4. Advertising channels used in 2 channel : 37 and 38
5. Advertising channels used in 1 channel: 37

11.5 Receiver Performance

Table 11-5. ATBTLC1000 XR1100A – ZR110CA BLE Receiver Performance

Parameter	Minimum	Typical	Maximum	Unit
Frequency	2,402		2,480	MHz
Sensitivity with on-chip DC/DC(1)	-91.5	-90		dBm
Maximum receive signal level		+5		
CCI		12.5		dB
ACI (N±1)		0		
N+2 Blocker (Image)		-20		
N-2 Blocker		-38		
N+3 Blocker (Adj. Image)		-35		
N-3 Blocker		-43		

Parameter	Minimum	Typical	Maximum	Unit
N±4 or greater		-45		dB
Intermod (N+3, N+6)		-32		dBm
OOB (2GHz<f<2.399GHz)	-15			
OOB (f<2GHz or f>2.5GHz)	-10			
RX peak current draw		4.00		mA

All measurements are taken after the RF input matching network. Refer to the reference schematic of ATBTLC1000-XR1100A

All measurements are performed at 3.3V VBAT and 25°C, with tests following the Bluetooth V4.1 standard tests.

Note:

1. Typical receiver sensitivity is average across 40 channels

11.6 Transmitter Performance

The transmitter has fine step power control with Pout variable in <3dB steps below 0dBm and in <0.5dB steps above 0dBm.

Table 11-6. ATBTLC1000 XR1100A – ZR110CA BLE Transmitter Performance

Parameter	Minimum	Typical	Maximum	Unit
Frequency	2,402		2,480	MHz
Output power range	-20	0	5.0	dBm
In-band Spurious (N±2)		-45		
In-band Spurious (N±3)		-50		
2nd harmonic P_{out}	-41			
3rd harmonic P_{out}	-41			
4th harmonic P_{out}	-41			
5th harmonic P_{out}	-41			
Frequency deviation		±250		kHz
TX peak current draw		3.0 (1)		mA

All measurements are taken after the RF input matching network. Refer to the reference schematic of ATBTLC1000-XR1100A

All measurements are performed at 3.3V VBAT and 25°C, with tests following the Bluetooth V4.1 standard tests.

Note:

1. At 0dBm TX output power.

11.7 ADC Characteristics

Table 11-7. Static Performance of SAR ADC

Parameter	Condition	Min.	Typ.	Max.	Unit
Input voltage range		0		VBAT	V
Resolution			11		bits
Sample rate			100	1000	KSPS
Input offset	Internal VREF	-10		+10	mV
Gain error	Internal VREF	-4		+4	%
DNL	100KSPS. Internal VREF=1.6V. Same result for external VREF.	-0.75		+1.75	LSB
INL	100KSPS. Internal VREF=1.6V. Same result for external VREF.	-2		+2.5	LSB
THD	1kHz sine input at 100KSPS		73		dB
SINAD	1kHz sine input at 100KSPS		62.5		dB
SFDR	1kHz sine input at 100KSPS		73.7		dB
Conversion time			13		cycles
Current consumption	Using external VREF, at 100KSPS		13.5		µA
	Using internal VREF, at 100KSPS		25.0		µA
	Using external VREF, at 1MSPS		94		µA
	Using internal VREF, at 1MSPS		150		µA
	Using internal VREF, during VBAT monitoring		100		µA
	Using internal VREF, during temperature monitoring		50		µA
Internal reference voltage	Mean value using VBAT=2.5V		1.026 (1)		V
	Standard deviation across parts		10.5		mV
VBAT Sensor Accuracy	Without calibration	-55		+55	mV
	With offset and gain calibration	-17		+17	mV
Temperature Sensor Accuracy	Without calibration	-9		+9	ºC
	With offset calibration	-4		+4	ºC

Note:

1. Effective VREF is 2xInternal Reference Voltage.

11.8 ADC Typical Characteristics

$T_c = 25^0 C V_{BAT} = 3.0V,$

unless otherwise noted

Figure 11-2. INL of SAR ADC

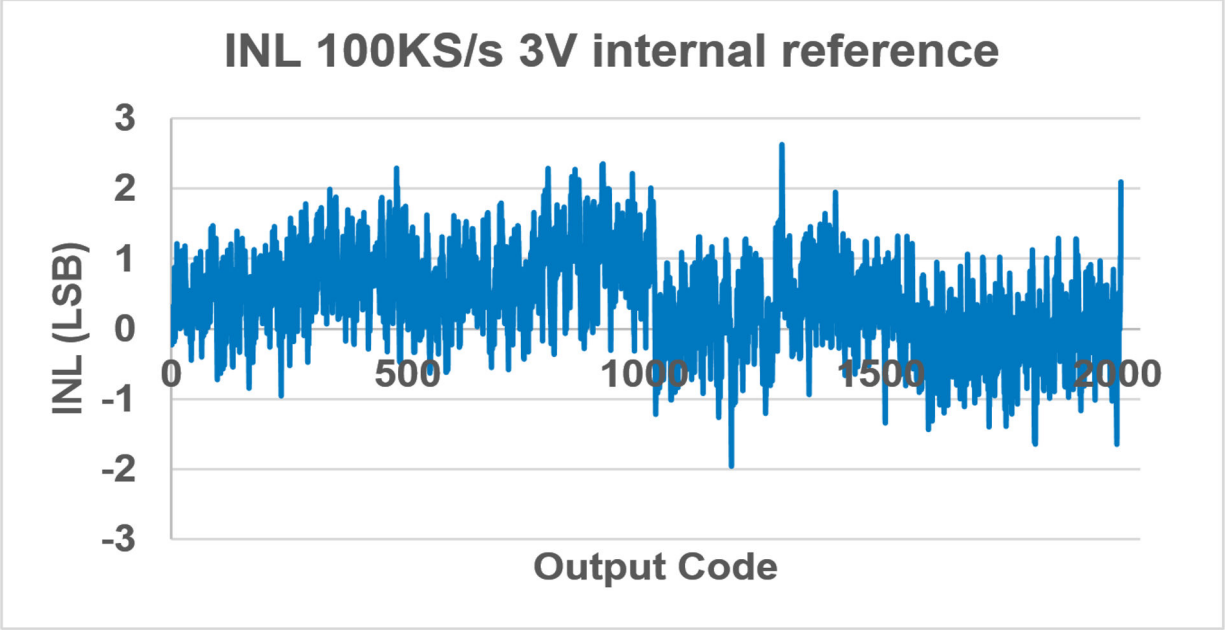


Figure 11-3. DNL of SAR ADC

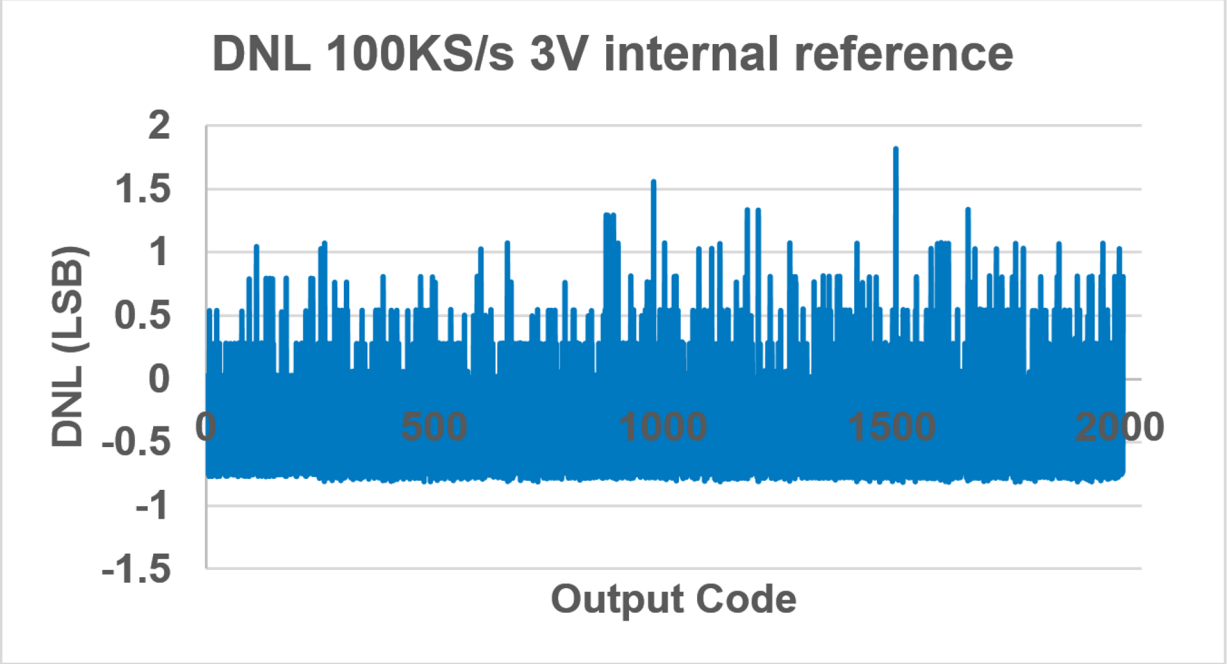
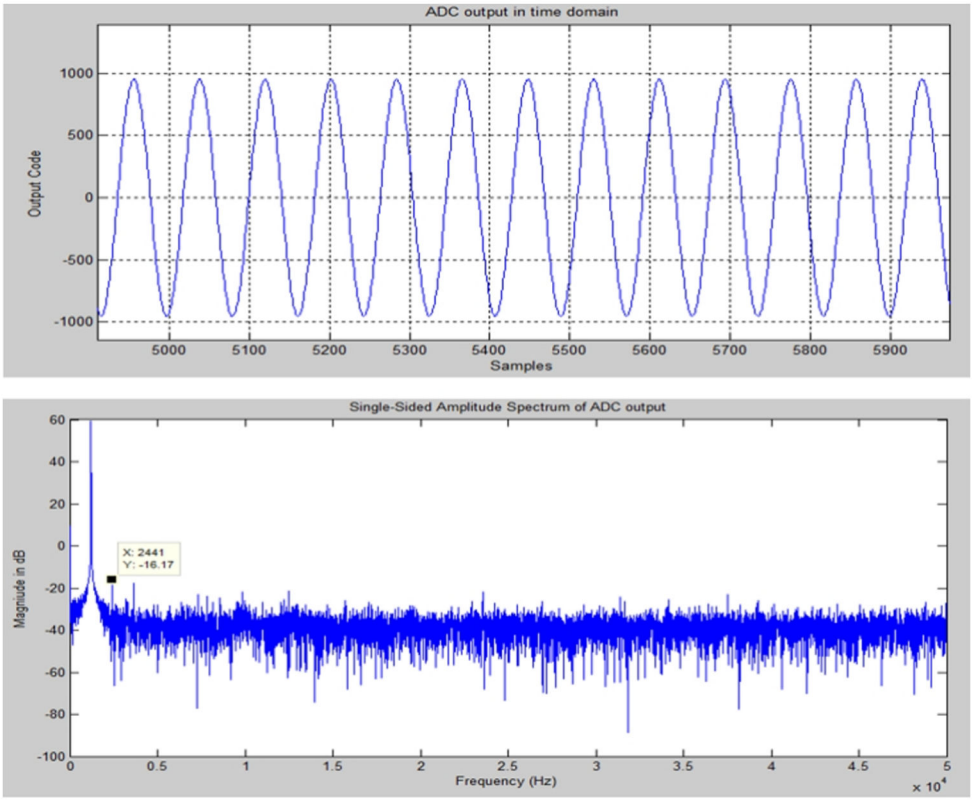


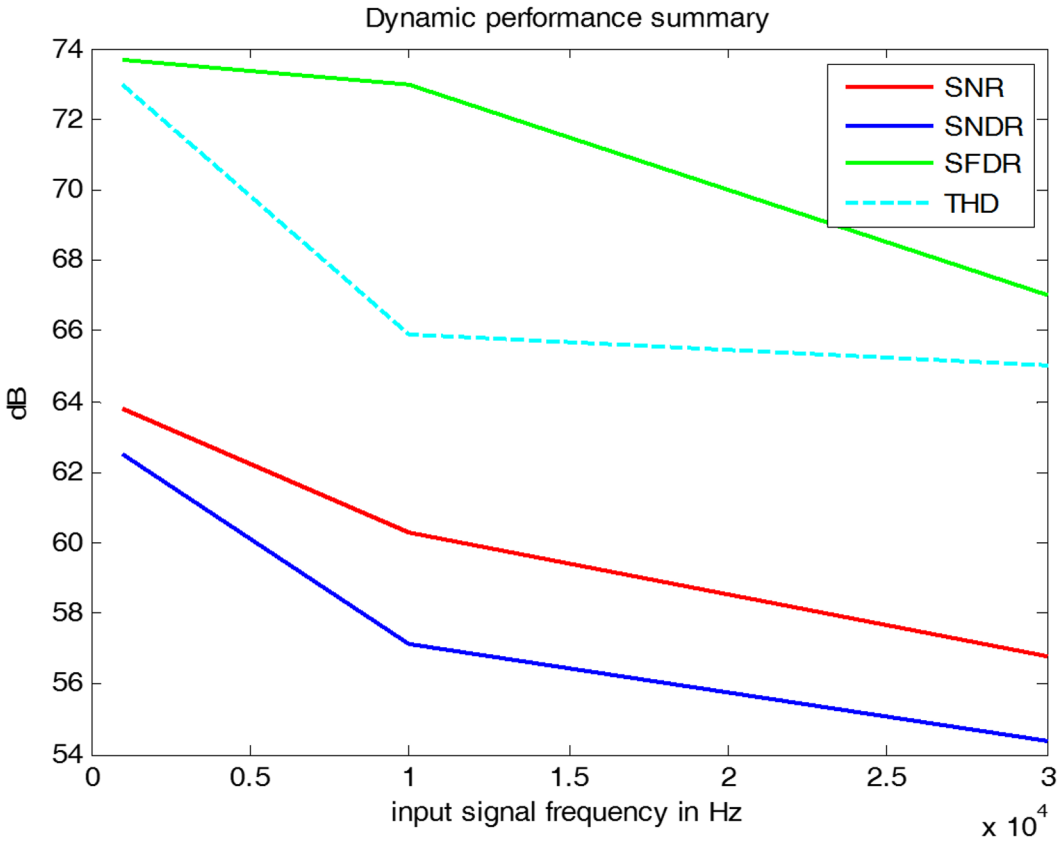
Figure 11-4. Sensor ADC Dynamic Measurement with Sinusoidal Input



Note:

1. 25ºC, 3.6V VBAT, and 100kS/s
   Input signal: 1kHz sine wave, 3Vp-p amplitude
2. SNDR = 62.5dB
   SFDR = 73.7dB
   THD = 73.0dB

Figure 11-5. Sensor ADC Dynamic Performance Summary at 100KSPS



11.9 Timing Characteristics

11.9.1 I2C Interface Timing

The I2C Interface timing (common to both Slave and Master) is provided in I2C Slave Timing Diagram. The timing parameters for Slave and Master modes are specified in tables I2C Slave Timing Parameters and I2C Master Timing Parameters respectively.

Figure 11-6. I2C Slave Timing Diagram

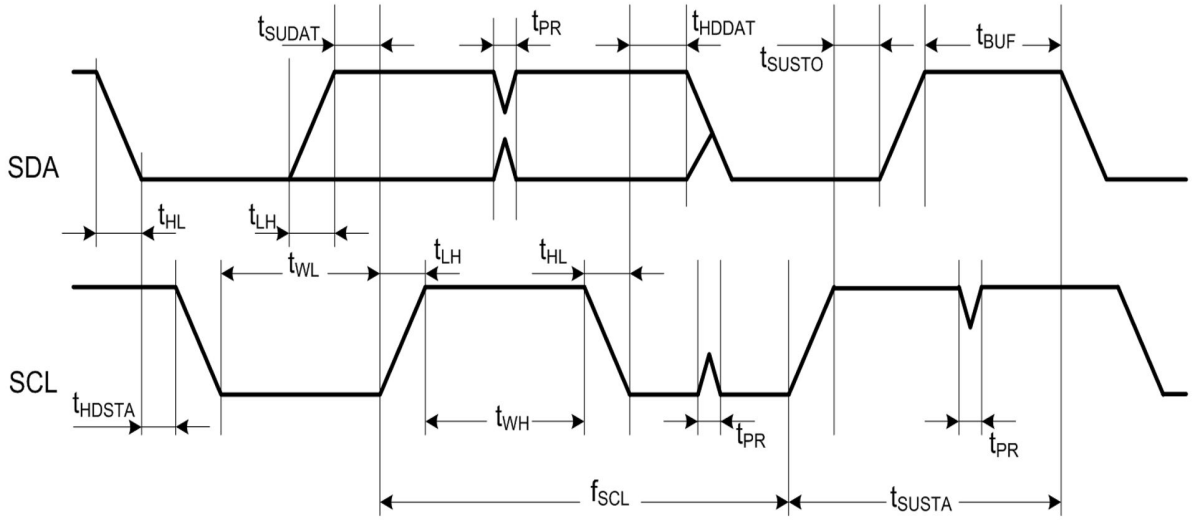


Table 11-8. I2C Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	
SCL Low Pulse Width	t_{WL}	1.3		µs	
SCL High Pulse Width	t_{WH}	0.6			
SCL, SDA Fall Time	t_{HL}		300	ns	
SCL, SDA Rise Time	t_{LH}		300		This is dictated by external components
START Setup Time	t_{SUSTA}	0.6		µs	
START Hold Time	t_{HDSTA}	0.6			
SDA Setup Time	t_{SUDAT}	100		ns	
SDA Hold Time	t_{HDDAT}	0 40			Slave and Master Default Master Programming Option
STOP Setup time	t_{SUSTO}	0.6		µs	
Bus Free Time Between STOP and START	t_{BUF}	1.3			
Glitch Pulse Reject	t_{PR}	0	50	ns	

Table 11-9. I2C Master Timing Parameters

Parameter	Symbol	Standard Mode		Fast Mode		High-speed Mode		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	0	3400	kHz
SCL Low Pulse Width	t_{WL}	4.7		1.3		0.16		µs
SCL High Pulse Width	t_{WH}	4		0.6		0.06		

Parameter	Symbol	Standard Mode		Fast Mode		High-speed Mode		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL Fall Time	t_{HLSCL}		300		300	10	40	ns
SDA Fall Time	t_{HLSDA}		300		300	10	80	
SCL Rise Time	t_{LHSCL}		1000		300	10	40	
SDA Rise Time	t_{LHSDA}		1000		300	10	80	
START Setup Time	t_{SUSTA}	4.7		0.6		0.16		µs
START Hold Time	t_{HDSTA}	4		0.6		0.16		
SDA Setup Time	t_{SUDAT}	250		100		10		ns
SDA Hold Time	t_{HDDAT}	5		40		0	70	
STOP Setup time	t_{SUSTO}	4		0.6		0.16		µs
Bus Free Time Between STOP and START	t_{BUF}	4.7		1.3				
Glitch Pulse Reject	t_{PR}			0	50			ns

11.9.2 SPI Slave Timing

The SPI Slave timing is provided in the figure SPI Slave Timing Diagram and table SPI Slave Timing Parameters.

Figure 11-7. SPI Slave Timing Diagram

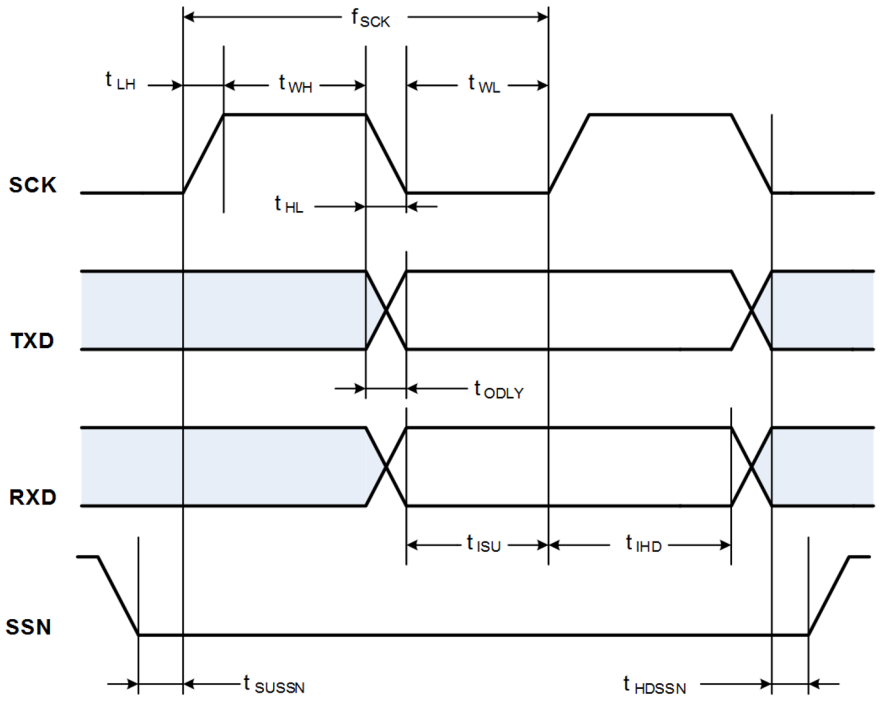


Table 11-10. SPI Slave Timing Parameters (1)

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency (2)	f_{SCK}		2	MHz
Clock Low Pulse Width	t_{WL}	55		ns
Clock High Pulse Width	t_{WH}	55		
Clock Rise Time	t_{LH}	0	7	
Clock Fall Time	t_{HL}	0	7	
TXD Output Delay(3)	t_{ODLY}	7	28	
RXD Input Setup Time	t_{ISU}	5		
RXD Input Hold Time	t_{IHD}	10		
SSN Input Setup Time	t_{SUSSN}	5		
SSN Input Hold Time	t_{HDSSN}	10		

Note:

1. Timing is applicable to all SPI modes
2. Maximum clock frequency specified is limited by the SPI Slave interface internal design, actual maximum clock frequency can be lower and depends on the specific PCB layout
3. Timing based on 15pF output loading

11.9.3 SPI Master Timing

The SPI Master Timing is provided in the figure and table below.

Figure 11-8. SPI Master Timing Diagram

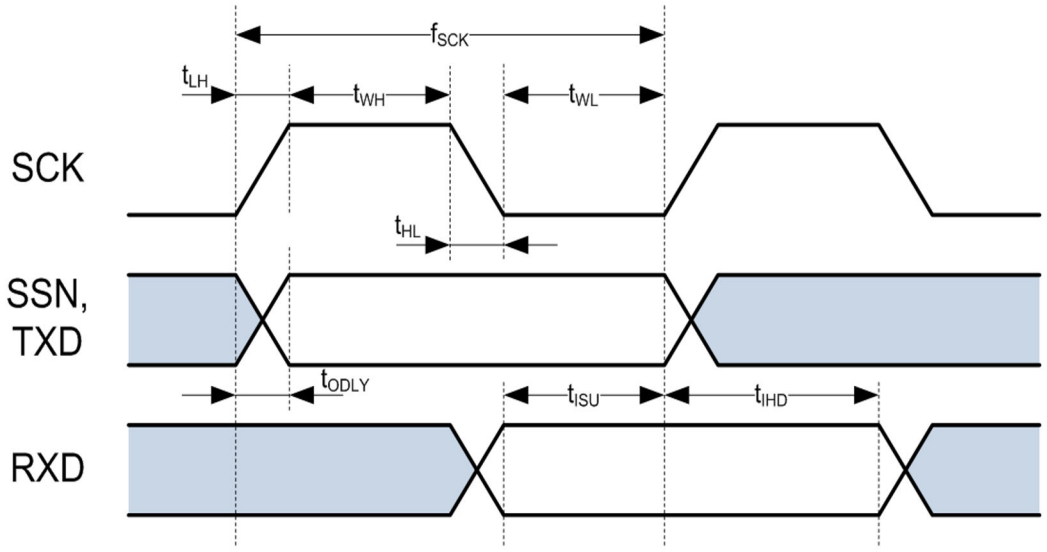


Table 11-11. SPI Master Timing Parameters (1)

Parameter	Symbol	Min.	Max.	Units
Clock Output Frequency (2)	f_{SCK}		4	MHz
Clock Low Pulse Width	t_{WL}	30		ns
Clock High Pulse Width	t_{WH}	32		
Clock Rise Time (3)	t_{LH}		7	
Clock Fall Time (3)	t_{HL}		7	
RXD Input Setup Time	t_{ISU}	23		
RXD Input Hold Time	t_{IHD}	0		
SSN/TXD Output Delay (3)	t_{ODLY}	0	12	

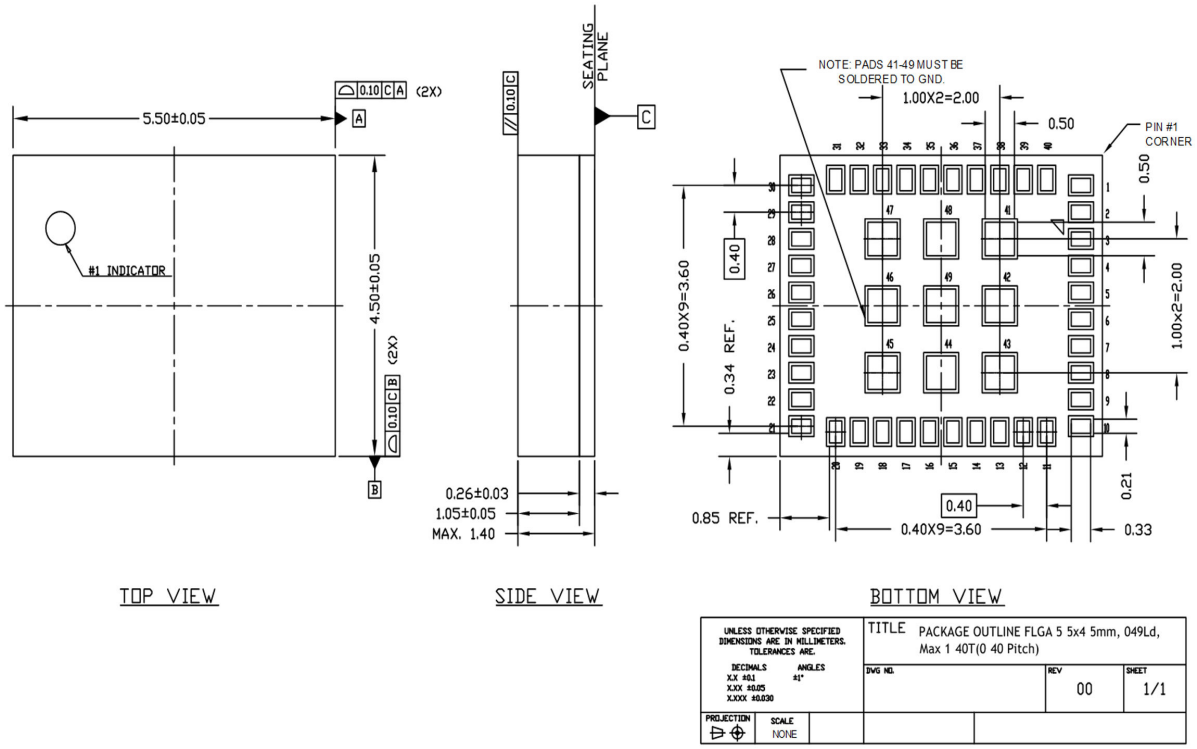
Note:

1. Timing is applicable to all SPI modes.
2. Maximum clock frequency specified is limited by the SPI Master interface internal design. The actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing based on 15pF output loading.

12. Package Outline Drawings

12.1 ATBTLC1000-XR1100A Package Outline Drawing

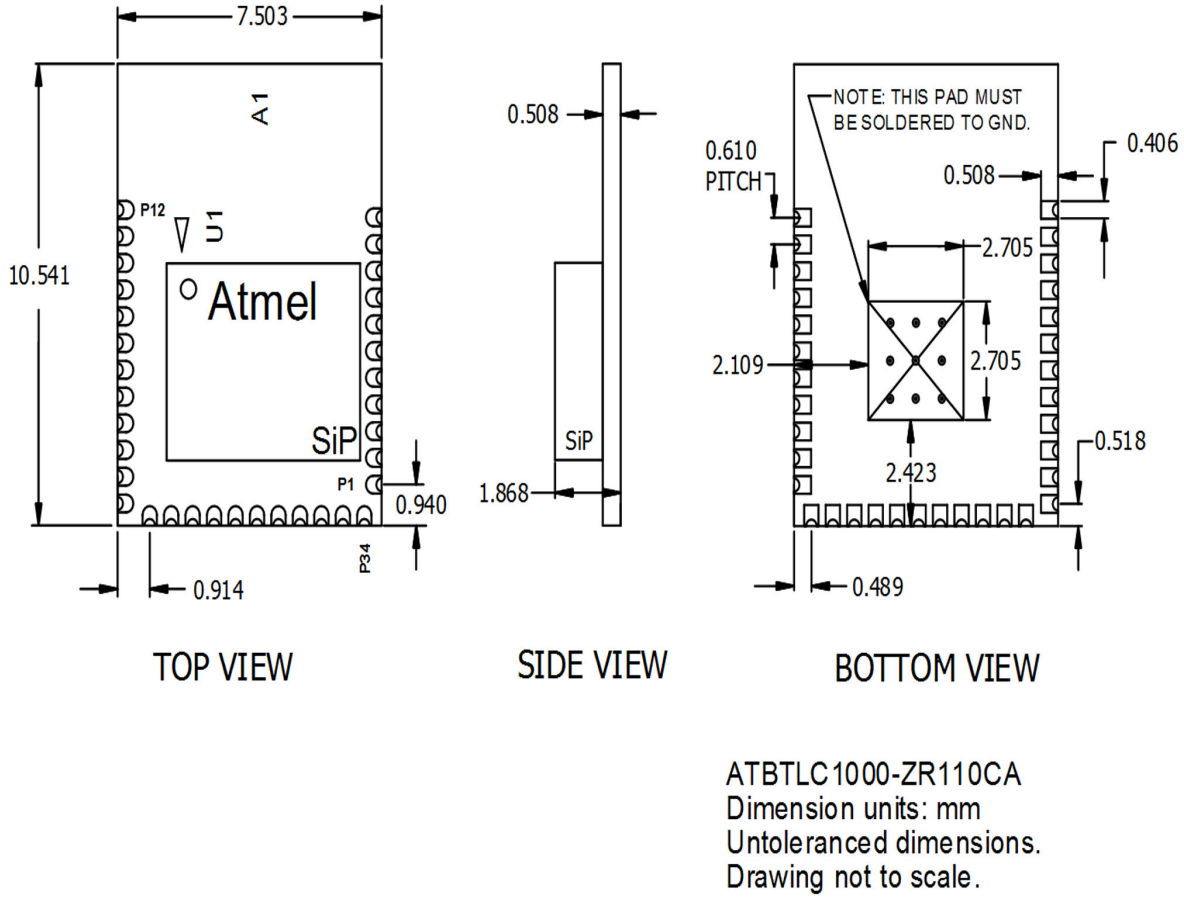
Figure 12-1. ATBTLC1000-XR1100A Package Outline Drawing



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

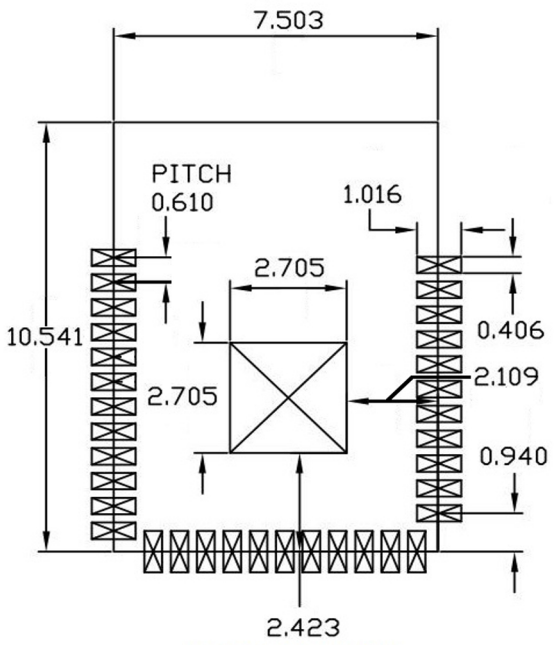
12.2 ATBTLC1000-ZR110CA Module PCB Package Outline Drawing

Figure 12-2. ATBTLC1000-ZR110CA Module Package Outline Drawing



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Figure 12-3. Customer PCB Top View Footprint

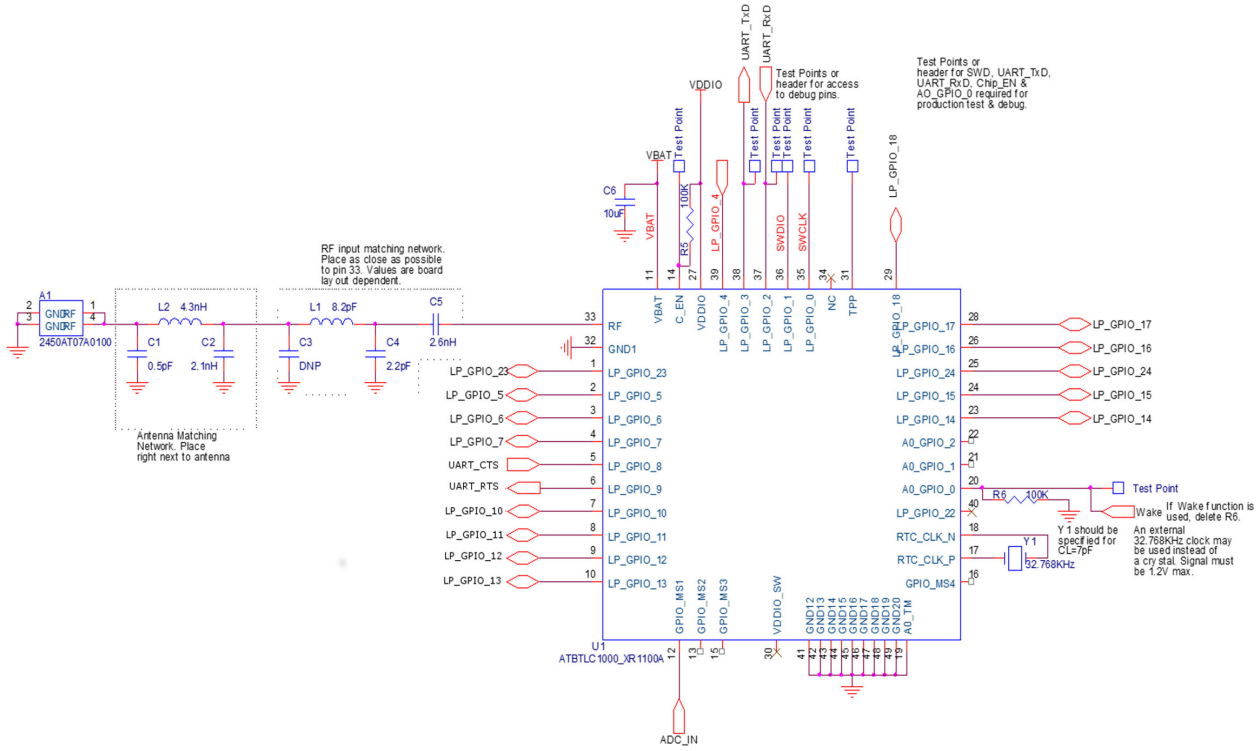


Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

13. ATBTLC1000 Schematics

13.1 ATBTLC1000-XR1100A Reference Schematic

Figure 13-1. ATBTLC1000-XR1100A Reference Schematic



13.2 ATBTLC1000-XR1100A Reference Schematic Bill of Materials (BOM)

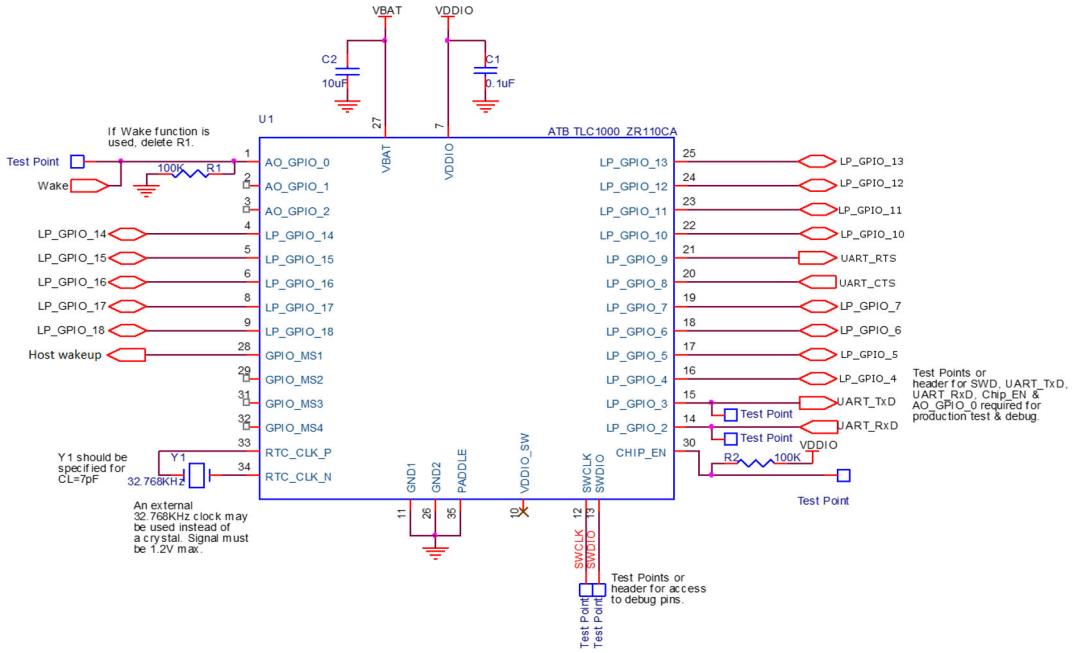
Table 13-1. ATBTLC1000-XR1100A Reference Schematic Bill of Materials (BOM)

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	1	A1	2450AT07A0100	1x0.5mm Ceramic Chip Antenna	Johanson	2450AT07A0100	
2	1	C1	0.5pF	CAP,CER,0.5pF, +/-0.1pF,NPO, 0201,25V,-55-125C	Johanson	250R05L0R5BV4T	0201
3	1	C2	2.1nH	Inductor,2.1nH, +/-0.1nH,Q=14@500MHz,SRF=11GHz,0201,-55-125C	Murata	LQP03TN2N1B02D	0201
4	1	C3	DNP	CAP,CER,2.2pF, +/-0.1pF,NPO,	Johanson	250R05L2R2BV4T	0201

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
				0201,25V,-55-125C			
5	1	C4	2.2pF	CAP,CER,2.2pF, +/-0.1pF,NPO, 0201,25V,-55-125C	Johanson	250R05L2R2BV4T	0201
6	1	C5	2.6nH	Inductor,2.6nH, +/-0.1nH,Q=13@500MHz,SRF=6GHz,0201,-55-125C	Murata	LQP03TG2N6B02D	0201
7	1	C6	10uF	CAP,CER,10uF, 20%,X5R, 0603,6.3V	AVX Corporation	06036D106MAT2A	0603
8	1	L1	8.2pF	CAP,CER,8.2pF, +/-0.1pF,NPO, 0201,25V,-55-125C	Johanson	250R05L8R2BV4T	0201
9	1	L2	4.3nH	Inductor,4.3nH, +/-3%,Q=13@500MHz,SRF=6GHz, 0201,-55-125C	Murata	LQP03TG4N3H02D	0201
10	2	R5,R6	100K	RESISTOR,Thick Film,100k ohm, 0201	Panasonic	ERJ-1GEF1003C	0201
11	7	TP1,TP2,TP4,TP5,TP6, TP7,TP8	Non-Component	Test Point,Surface Mount,0.040"sq w/ 0.25"hole		40X40_SM_TEST_POINT	0.04"SQx 0.025"H
12	1	U1	ATBTLC1000_XR1100A	ATBTLC1000_XR 1100A BLE SIP	Microchip	ATBTLC1000_XR1100A	ATBTLC1000_XR
13	1	Y1	32.768KHz	Crystal, 32.768KHz, +/-20ppm,-40-+85C,CL=7pF, 2 lead, SMD	ECS	ECS-.327-7-34B-TR	

13.3 ATBTLC1000-ZR110CA Reference Schematic

Figure 13-2. ATBTLC1000-ZR110CA Reference Schematic



13.4 ATBTLC1000-ZR110CA Reference Bill of Materials(BOM)

Table 13-2. ATBTLC1000-ZR110CA Reference Schematic Bill of Materials (BOM)

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	1	C1	0.1uF	CAP CER 0.1UF 6.3V +/-10% X5R 0201	AVX Corporation	02016D104KAT2A	0201
7	1	C2	10uF	CAP,CER,10uF, 20%,X5R, 0603,6.3V	AVX Corporation	06036D106MAT2A	0603
10	2	R1,R2	100K	RESISTOR,Thick Film,100k ohm, 0201	Panasonic	ERJ-1GEF1003C	0201
12	1	U1	ATBTLC1000_ZR110CA	ATBTLC1000_ZR110CA BLE Module	Microchip	ATBTLC1000_ZR110CA	ATBTLC1000_ZR
13	1	Y1	32.768KHz	Crystal, 32.768KHz, +/-20ppm,-40-+85C,CL=7pF, 2 lead, SMD	ECS	ECS-.327-7-34B-TR	

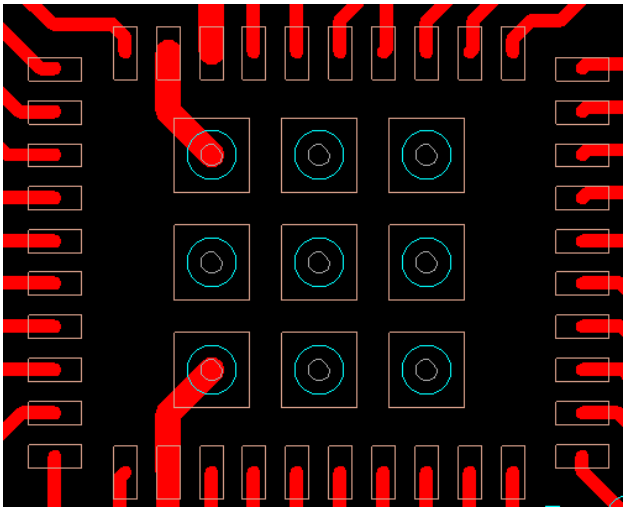
14. ATBTLC1000-XR1100A Design Considerations

The ATBTLC1000-XR1100A is offered in a shielded Land Grid Array (LGA) package with organic laminate substrates. The LGA package makes the second level interconnect (from package to the customer PCB) with an array of solderable surfaces. This may consist of a layout similar to a BGA with no solder spheres. However, it may also have an arbitrary arrangement of solderable surfaces that typically includes large planes for grounding or thermal dissipation, smaller lands for signals or shielding grounds, and in some cases, mechanical reinforcement features for mechanical durability.

14.1 Layout Recommendation

Referring to the SiP footprint dimensions in Figure ATBTLC1000-XR1100A Package Outline Drawing, it is recommended to use solder mask defined with PCB pads 0.22 mm wide that have a 0.4 mm pitch. A Sample PCB pad layout in Figure PCB Footprint For ATBTLC1000-XR1100A shows the required vias for the center ground paddle.

Figure 14-1. PCB Footprint For ATBTLC1000-XR1100A



The land design on the customer PCB should follow the following rules:

1. The solderable area on the customer PCB should match the nominal solderable area on the LGA package 1:1.
2. The solderable area should be finished with organic surface protectant (OSP), NiAu, or a solder cladding.
3. The decision on whether to have a solder mask defined (SMD) land or a non-solder mask defined (NSMD) land depends on the application space.
   - 3.1. SMD: If field reliability is at risk due to impact failures such as dropping a hand-held portable application, then the SMD land is recommended to optimize mechanical durability.
   - 3.2. NSMD: If field reliability is at risk due to a solder fatigue failure (temperature cycle related open circuits), then the NSMD land is recommended to maximize solder joint life.

14.1.1 Power and Ground

Proper grounding is essential for correct operation of the SiP and peak performance. Figure ATBTLC1000-XR1100A Package Outline Drawing shows the bottom view of the ATBTLC1000-XR1100A SiP with exposed ground pads. The SiP exposed ground pads must be soldered to customer PCB ground plane. A solid inner layer ground plane should be provided. The center ground paddle of the SiP must

have a grid of ground vias solidly connecting the pad to the inner layer ground plane (one via per exposed center ground pads J41~J49).

Dedicate one layer as a ground plane, preferably the second layer from the top. Make sure that this ground plane does not get broken up by routes. Power can route on all layers except the ground layer. Power supply routes should be heavy copper fill planes to ensure the lowest possible inductance. The power pins of the ATBTLC1000-XR1100A should have a via directly to the power plane as close to the pin as possible. Decoupling capacitors should have a via right next to the capacitor pin and this via should go directly down to the power plane – that is to say, the capacitor should not route to the power plane through a long trace. The ground side of the decoupling capacitor should have a via right next to the pad which goes directly down to the ground plane. Each decoupling capacitor should have its own via directly to the ground plane and directly to the power plane right next to the pad. The decoupling capacitors should be placed as close to the pin that it is filtering as possible.

14.1.2 Antenna

When designing in the ATBTLC1000-XR1100A, it is important to pay attention to the following recommendations for antenna placement:

1. Make sure to choose an antenna that covers the proper frequency band; 2.400GHz to 2.500GHz.
2. Assure that the antenna is designed matched to 50Ω input impedance.
3. Talk to the antenna vendor and make sure it is understood that the full frequency range must be covered by the antenna.
4. Be sure to follow the antenna vendors best practice layout recommendations when placing the antenna in the customer PCB design.
5. The customer PCB pad that the antenna is connected to must be properly designed for 50Ω impedance.
6. Make sure that the trace from the RF pin on the ATBTLC1000-XR1100A to the antenna matching circuitry has a 50Ω impedance.
7. Do not enclose the antenna within a metal shield.
8. Keep any components that may radiate noise or signals within the 2.4GHz – 2.5GHz frequency band far away from the antenna and RF traces or better yet, shield the noisy components. Any noise radiated from the customer PCB in this frequency band will degrade the sensitivity of the ATBTLC1000-XR1100A device.

15. ATBTLC1000-ZR110CA Design Considerations

15.1 Placement and Routing Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance ATBTLC1000-ZR110CA module:

1. The customer PCB design should have a solid ground plane. The center ground Paddle of the module must be soldered to the ground plane with an array of vias as shown in Figure Customer PCB Top View Footprint. The module ground pins should have ground vias either on or right next to the customer PCB pad.
2. When the ATBTLC1000-ZR110CA is placed on the customer PCB, a provision for the antenna must be made. See the references in Figure ATBTLC1000-ZR110CA Placement Examples. The antenna should not be placed directly on top of the customer PCB design as seen in Figure ATBTLC1000-ZR110CA Placement Examples (a). The best placement, for example, is placing the module at the edge of the board such that the module edge with the antenna extends beyond the main board edge by 3mm as shown in the Figure ATBTLC1000-ZR110CA Placement Examples (b). Alternatively, an acceptable case could be to provide a cutout in the customer PCB as shown in Figure ATBTLC1000-ZR110CA Placement Examples (c). The cutout should be 7.5mm (minimum) x 3mm as shown in the Figure PCB Keep Out Area
3. Keep large metal objects as far away as possible from the antenna, to avoid electromagnetic field blocking
4. Do not enclose the antenna within a metal shield
5. Keep any components that may radiate noise or signals within the 2.4GHz – 2.5GHz frequency band far away from the antenna or better yet, shield those components. Any noise radiated from the customer PCB in this frequency band will degrade the sensitivity of the ATBTLC1000-ZR110CA.

Figure 15-1. ATBTLC1000-ZR110CA Placement Examples

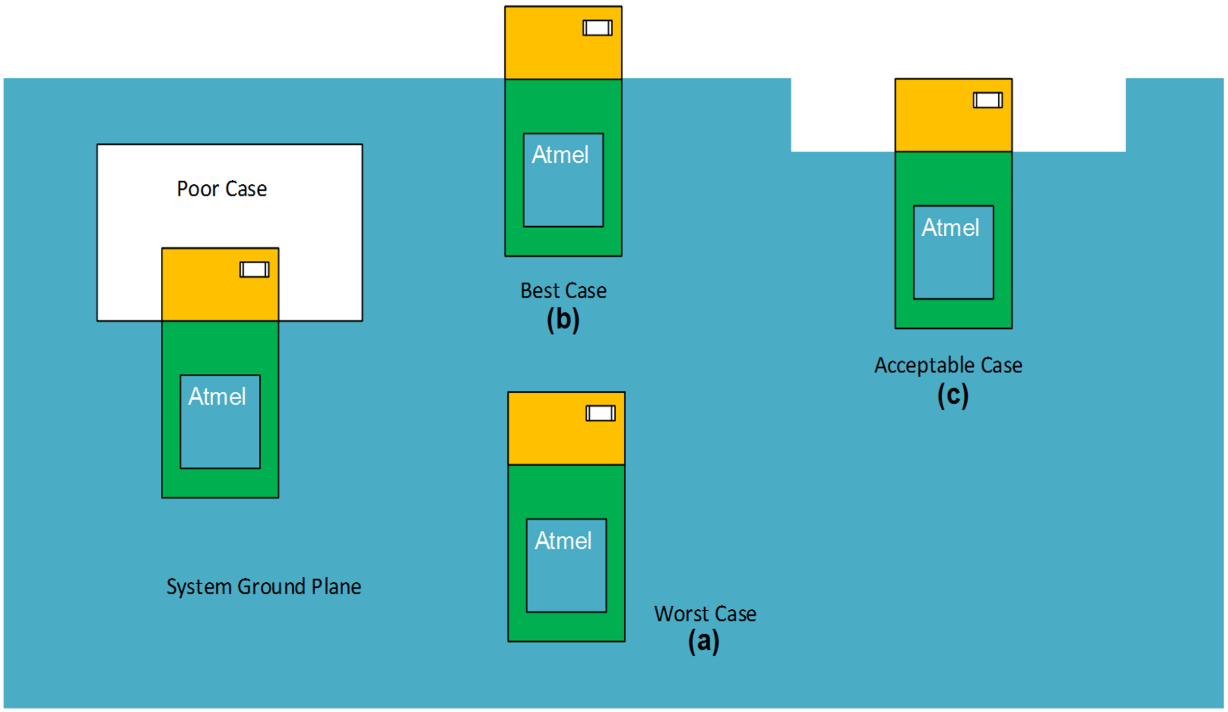
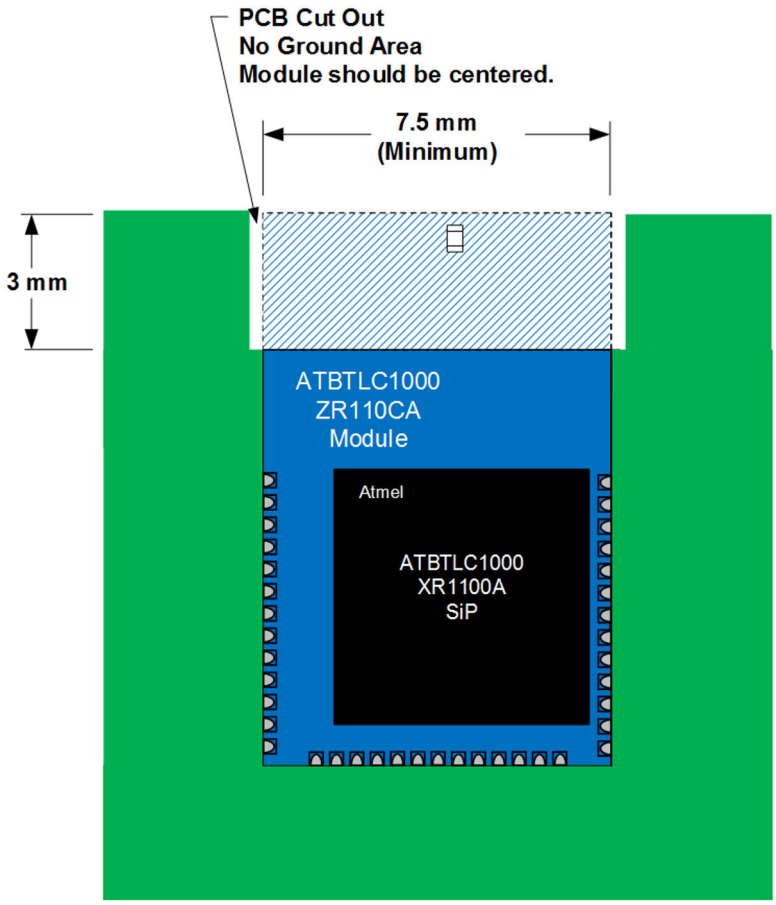


Figure 15-2. PCB Keep Out Area



15.2 Interferers

One of the biggest problems with RF devices is poor performance due to interferers on the board radiating noise into the antenna or coupling into the RF traces going to input LNA. Care must be taken to make sure that there is no noisy circuitry placed anywhere near the antenna or the RF traces. All noise generating circuits should also be shielded so they do not radiate noise that is picked up by the antenna. This applies to all layers. Even if there is a ground plane on a layer between the RF route and another signal, the ground return current will flow on the ground plane and couple into the RF traces.

16. Reflow Profile Information

This section provides guidelines for the reflow process in soldering the ATBTLC1000-XR1100A or the ATBTLC1000-ZR110CA to the customer's design.

16.1 Storage Condition

16.1.1 Moisture Barrier Bag Before Opened

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH.

The calculated shelf life for the dry-packed product shall be 12 months from the date the bag is sealed.

16.1.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, < 30%.

16.2 Stencil Design

The recommended stencil is laser-cut, stainless-steel type with a thickness of 75µm to 100µm and approximately a 1:1 ratio of stencil opening to pad dimension. To improve paste release, a positive taper with bottom opening 25µm larger than the top can be utilized. Local manufacturing experience may find other combinations of stencil thickness and aperture size to get good results.

16.3 Soldering and Reflow Conditions

16.3.1 Reflow Oven

It is strongly recommended that a reflow oven equipped with more heating zones and Nitrogen atmosphere be used for lead-free assembly. Nitrogen atmosphere has shown to improve the wet-ability and reduce temperature gradient across the board. It can also enhance the appearance of the solder joints by reducing the effects of oxidation.

The following items should also be observed in the reflow process:

Some recommended pastes include

- NC-SMQ® 230 flux and Indalloy® 241 solder paste made up of 95.5 Sn/3.8 Ag/0.7 Cu
- SENJU N705-GRN3360-K2-V Type 3, no clean paste.

Allowable reflow soldering iterations:

- Three times based on the following reflow soldering profile (see Figure Solder Reflow Profile).

Temperature profile:

- Reflow soldering shall be done according to the following temperature profile (see Figure Solder Reflow Profile).
- Peak temperature: 250°C.

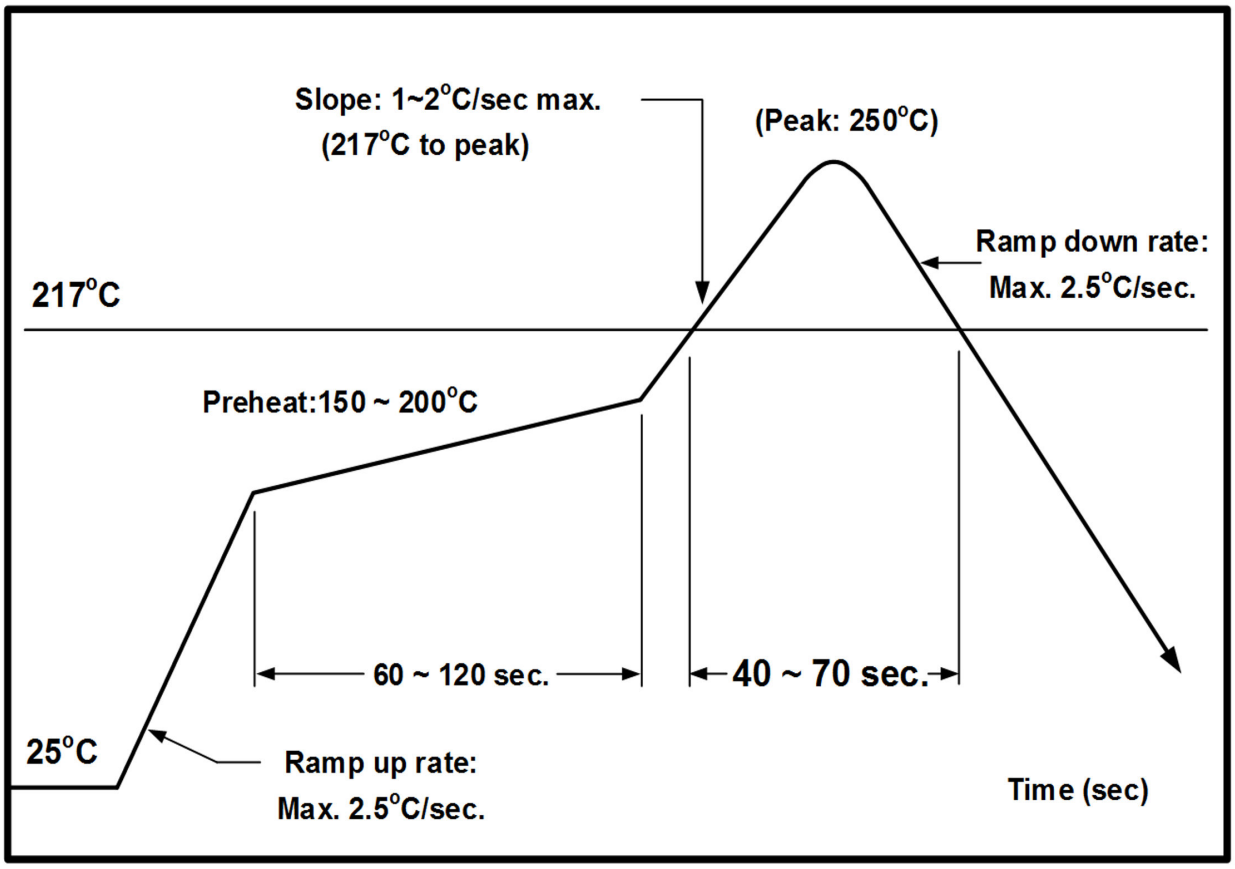
16.4 Baking Conditions

This module is rated at MSL level 3. After sealed bag is opened, no baking is required within 168 hours so long as the devices are held at <= 30 oC/60% RH or stored at <10% RH.

The module will require baking before mounting if:

- The sealed bag has been open for > 168 hours.
- Humidity Indicator Card reads >10%.
- SiP's need to be baked for 8 hours at 125 oC.

Figure 16-1. Solder Reflow Profile



16.5 Module Assembly Considerations

The Microchip ATBTLC1000-ZR110CA module is manufactured without any conformal coating applied. It is the customer's responsibility if a conformal coating is specified and or applied to the ATBTLC1000-ZR110CA module.

Solutions like IPA and similar solvents can be used to clean the ATBTLC1000-ZR110CA module. However, cleaning solutions, which contain acid, should never be used on the module.

17. ATBTLC1000-ZR110CA Module Regulatory Approval

17.1 United States

The ATBTLC1000-ZR110CA module have received Federal Communications Commission (FCC) CFR47 Telecommunications, Part 15 Subpart C “Intentional Radiators” modular approval in accordance with Part 15.212 Modular Transmitter approval. Modular approval allows the end user to integrate the ATBTLC1000-ZR110CA module into a finished product without obtaining subsequent and separate FCC approvals for intentional radiation, provided no changes or modifications are made to the module circuitry. Changes or modifications could void the user’s authority to operate the equipment.

The user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

The finished product is required to comply with all applicable FCC equipment authorizations regulations, requirements and equipment functions not associated with the transmitter module portion. For example, compliance must be demonstrated to regulations for other transmitter components within the host product; to requirements for unintentional radiators (Part 15 Subpart B “Unintentional Radiators”), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non-transmitter functions on the transmitter module (i.e., Verification, or Declaration of Conformity) (e.g., transmitter modules may also contain digital logic functions) as appropriate.

17.1.1 Labeling And User Information Requirements

Due to the limited module size of ATBTLC1000-ZR110CA(7.503 mm x10.541 mm), FCC identifier is displayed only in the datasheet and it cannot be displayed on the module label. When the module is installed inside another device, then the outside of the finished product into which the module is installed must display a label referring to the enclosed module. This exterior label can use wording as follows:

ATBTLC1000-ZR110CA:

Contains Transmitter Module FCC ID: 2ADHKBTZ **or**

Contains FCC ID: 2ADHKBTZ

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation

A user’s manual for the product should include the following statement:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Additional information on labeling and user information requirements for Part 15 devices can be found in KDB Publication 784748 available at the FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) https://apps.fcc.gov/oetcf/kdb/index.cfm

17.1.2 RF Exposure

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

From the FCC Grant: Output power listed is conducted. This grant is valid only when the module is sold to OEM integrators and must be installed by the OEM or OEM integrators.

Module approved for use in mixed mobile-device and portable-device exposure host platforms. The antenna(s) used with this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

17.1.3 Helpful Websites

Federal Communications Commission (FCC): https://www.fcc.gov/

FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB): https://apps.fcc.gov/oetcf/kdb/index.cfm

17.2 Canada

The ATBTLC1000-ZR110CA module has been certified for use in Canada under Innovation, Science, and Economic Development (ISED, formerly Industry Canada) Radio Standards Procedure (RSP) RSP-100, Radio Standards Specification (RSS) RSS-Gen and RSS-247. Modular approval permits the installation of a module in a host device without the need to recertify the device.

17.2.1 Labeling and User Information Requirements

Labeling Requirements (from RSP-100 - Issue 10, Section 3): The host device shall be properly labeled to identify the module within the host device.

Due to the limited module size of ATBTLC1000-ZR110CA (7.503 mm x10.541 mm), IC identifier is displayed only in the datasheet and it cannot be displayed on the module label.

The host device must be labeled to display the Industry Canada certification number of the module, preceded by the words “Contains transmitter module”, or the word “Contains”, or similar wording expressing the same meaning, as follows:

ATBTLC1000-ZR110CA:

Contains Transmitter Module

IC: 20266-BTLC1000ZR

User Manual Notice for License-Exempt Radio Apparatus (from Section 8.4 RSS-Gen, Issue 4, November 2014): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:

This device complies with Industry Canada license exempt RSS standard(s). Operation is subject to the following two conditions:

1. This device may not cause interference, and
2. This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. l'appareil ne doit pas produire de brouillage, et
2. l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Transmitter Antenna (From Section 8.3 RSS-GEN, Issue 4, November 2014): User manuals, for transmitters shall display the following notice in a conspicuous location:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établisse-ment d'une communication satisfaisante.

The above notice may be affixed to the device instead of displayed in the user manual.

17.2.2 RF Exposure

All transmitters regulated by IC must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radio communication Apparatus (All Frequency Bands).

This transmitter is restricted for use with a specific antenna tested in this application for certification, and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with Canada multi-transmitter product procedures.

17.2.3 Helpful Websites

Industry Canada: http://www.ic.gc.ca/

17.3 Europe

The ATBTLC1000-ZR110CA module is in progress to be an Radio Equipment Directive (RED) assessed radio module that is CE marked and has been manufactured and tested with the intention of being integrated into a final product.

The ATBTLC1000-ZR110CA module has been tested to RED 2014/53/EU Essential Requirements for Health and Safety (Article (3.1(a)), Electromagnetic Compatibility (EMC) (Article 3.1(b)), and Radio (Article 3.2) and are summarized in Table Table 17-1. A Notified Body Type Examination Certificate is pending.

The ETSI provides guidance on modular devices in “Guide to the application of harmonised standards covering articles 3.1b and 3.2 of the Directive 2014/53/EU (RED) to multi-radio and combined radio and non-radio equipment” document available for download from the following location: http://www.etsi.org/deliver/etsi_eg/203300_203399/203367/01.01.01_60/eg_203367v010101p.pdf

Note:
To maintain conformance to the testing listed in Table Table 17-1 , the module shall be installed in accordance withe installation instructions in this data sheet and shall not be modified

When integrating a radio module into a completed product the integrator becomes the manufacturer of the final product and is therefore responsible for demonstrating compliance of the final product with the essential requirements against the RED

17.3.1 Labeling and User Information Requirements

The label on the final product which contains the ATBTLC1000-ZR110CA module must follow CE marking requirements.

17.3.2 Conformity Assessment

From ETSI Guidance Note EG 203367, section 6.1 Non-radio products are combined with a radio product:

If the manufacturer of the combined equipment installs the radio product in a host non-radio product in equivalent assessment conditions (i.e. host equivalent to the one used for the assessment of the radio product) and according to the installation instructions for the radio product, then no additional assessment of the combined equipment against article 3.2 of the RED is required.

The European Compliance Testing listed in Table Table 17-1 was performed using the integral ceramic chip antenna.

Table 17-1. European Compliance Testing

Certification	Standards	Article	Laboratory	ReportNumber
Safety	EN60950-1:2006/A11:2010/A1:2010/ A12:2011/A2:2013	3(1)(a)	TBD	TBD
Health	EN62479:2010 or EN 62311:2008			TBD
EMC	EN301489-1 V2.2.0	3(1)(b)		TBD
	EN301489-17 V3.2.0			
Radio	EN300328 V2.1.1	3(2)		TBD
Notified Body (TEC)	TBD			

17.3.3 Agency Europe Helpful Websites

A document that can be used as a starting point in understanding the use of Short Range Devices (SRD) in Europe is the European Radio Communications Committee (ERC) Recommendation 70-03 E, which can be downloaded from the European Communications Committee (ECC) at: http://www.ecodocdb.dk/

Additional helpful web sites are:

- Radio Equipment Directive (2014/53/EU): https://ec.europa.eu/growth/single-market/european-standards/harmonised-standards/rtte_de

- European Conference of Postal and Telecommunications Administrations (CEPT): http://www.cept.org
- European Telecommunications Standards Institute(ETSI): http://www.etsi.org
- European Communications Committee (ECC): http://www.ecodocdb.dk
- The Radio Equipment Directive Compliance Association (REDCA): http://www.redca.eu/

18. Reference Documents and Support

18.1 Reference Documents

Microchip offers a set of collateral documentation to ease integration and device ramp. The following table list documents available on Microchip website or integrated into development tools.

Table 18-1. Reference Documents

Title	Content
Datasheet	This document
ATBTLC1000 BluSDK Release Package	This package contains the software development kit and all the necessary documentation including getting started guides for interacting with different hardware devices, device drivers and API call references.
ATBTLC1000 BluSDK BLE API SW Development Guide	This user guide details the functional description of Bluetooth Low Energy (BLE) Application Peripheral Interface (API) programming model. This also provides the example code to configure an API for Generic Access Profile (GAP), Generic Attribute (GATT) Profile, and other services using the ATBTLC1000.
ATBTLC1000 Platform Porting Guide	This document guides the user to port the Application Peripheral Interface (API) into a new platform

For a complete listing of development support tools and documentation, visit http://www.microchip.com/, or contact the nearest Microchip field representative.

19. Document Revision History

Doc Rev.	Date	Comments
DS60001505A	7/20/17	1. Updated figure Customer PCB Top View Footprint 2. Updated table ATBTLC1000-XR1100A SiP 40 Package Information with tolerance information and dimensions 3. Updated pin description for VBAT, RFIO, AO_TM and TPP in Table ATBTLC1000-XR1100A and ATBTLC1000-ZR110CA Pin Description 4. Modified block diagram to include representation of GPIO_MS pins 5. Added information related to host wakeup pin in sections Pinout Information, ATBTLC1000-XR/ZR Host Microcontroller Interface and ATBTLC1000 Schematics 6. Added note to contact technical support for using clock output and RTC XO on chip trimming capacitor configuration 7. Added regulatory notice for Canada with TBD IC ID 8. Updated reference schematics to remove the reference to using AO_GPIO_1 and AO_GPIO_2 as wakeup sources as this is not supported 9. Updated FCCID for the module 10. Removed references to MCU_Only state as this is not applicable for BTLC1000 11. Removed reference to using 2MHz RC Oscillator as Low power clock for applications as this is not supported 12. Updated the features list for BLE core. SHA-256 has been removed as feature as SHA-256 is not used in BLE security 13. Added BoM for reference schematic of ATBTLC1000-ZR110CA 14. Updated power consumption numbers measured based on BluSDK V6.1 15. Updated the IC certification details 16. Migrated to Microchip format. Replaces former Atmel literature number 42749.
42749B	2/2017	Updated tables ATBTLC1000 XR1100A – ZR110CA BLE Receiver Performance and ATBTLC1000 XR1100A – ZR110CA BLE Transmitter Performance
42749A	1/2017	Initial document release

The Microchip Web Site

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- Field Application Engineer (FAE)
- Technical Support

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Microchip Devices Code Protection Feature

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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ISO/TS 16949

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