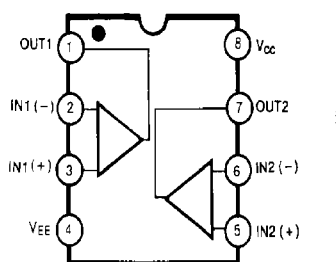


DUAL OPERATIONAL AMPLIFIER

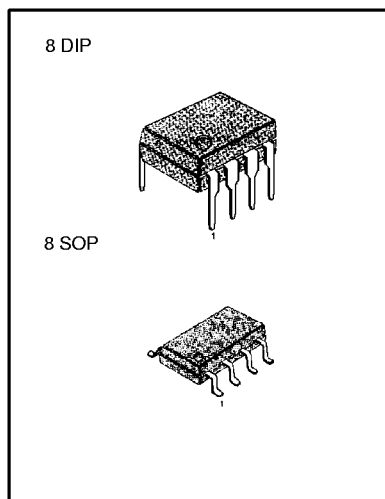
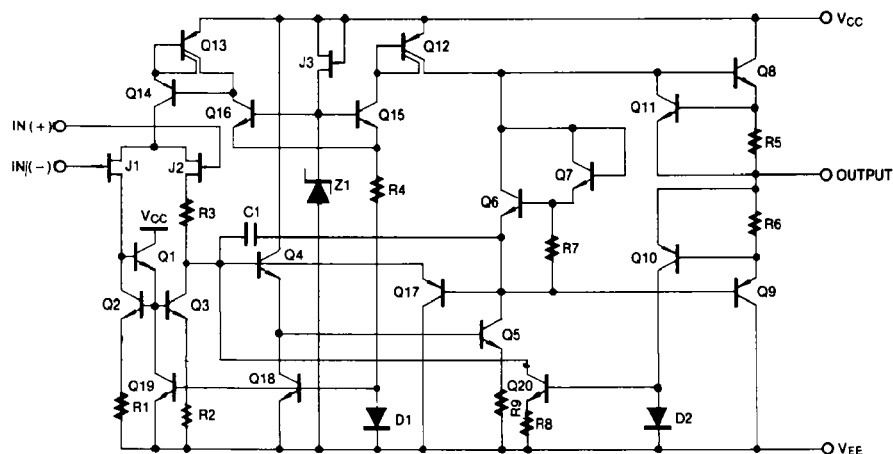
The LF353 is a JFET input operational amplifier with an internally compensated input offset voltage. The JFET input device provides with bandwidth, low input bias currents and offset currents.

FEATURES

- Internally trimmed offset voltage: 10mV
- Low input bias current: 50pA
- Wide gain bandwidth: 4MHz
- High slew rate: 13V/ μ s
- High Input impedance: $10^{12}\Omega$

BLOCK DIAGRAM

ORDERING INFORMATION

Device	Package	Operating Temperature
LF353N	8 DIP	0 ~ + 70°C
LF353M	8 SOP	
LF353S	9 SIP	


SCHEMATIC DIAGRAM (One Section Only)


ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	± 18	V
Differential Input Voltage	$V_{I(DIFF)}$	30	V
Input Voltage Range	V_I	± 15	V
Output Short Circuit Duration		Continuous	
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{OPR}	$0 \sim +70$	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	$-65 \sim +150$	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS

($V_{CC} = +15\text{V}$, $V_{EE} = -15\text{V}$, $T_A = 25^{\circ}\text{C}$, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	$R_S = 10\text{K}\Omega$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$		5.0	10	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	$R_S = 10\text{K}\Omega$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$		10		$\mu\text{V}/^{\circ}\text{C}$
Input Offset Current	I_{IO}	$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$		25	100	pA
Input Bias Current	I_{BIAS}	$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$		50	200	pA
Input Resistance	R_I			10^{12}		Ω
Large Signal Voltage Gain	G_V	$V_{O(P,P)} = \pm 0\text{V}$ $R_L = 2\text{K}\Omega$ $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$	25	100		V/mV
Output Voltage Swing	$V_{O(P,P)}$	$R_L = 10\text{K}\Omega$	± 12	± 13.5		V
Input Voltage Range	$V_{I(R)}$		± 11	$\pm 15/-12$		V
Common Mode Rejection Ratio	CMRR	$R_S \geq 10\text{K}\Omega$	70	100		dB
Power Supply Rejection Ratio	PSRR	$R_S \geq 10\text{K}\Omega$	70	100		dB
Power Supply Current	I_{CC}			3.6	6.5	mA
Slew Rate	SR	$G_V = 1$		13		V/ μs
Gain-Bandwidth Product	GBM			4		MHz
Channel Separation	CS	$f = 1\text{Hz} \sim 20\text{KHz}$ (Input referenced)	120	120		dB
Equivalent Input Noise Voltage	V_{NI}	$R_S = 100\Omega$ $f = 1\text{KHz}$	16	16		$\text{nV}/\sqrt{\text{Hz}}$
Equivalent Input Noise Current	I_{NI}	$f = 1\text{KHz}$	0.01	0.01		$\text{pA}/\sqrt{\text{Hz}}$

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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