CMOS 4-BIT MICROCONTROLLER

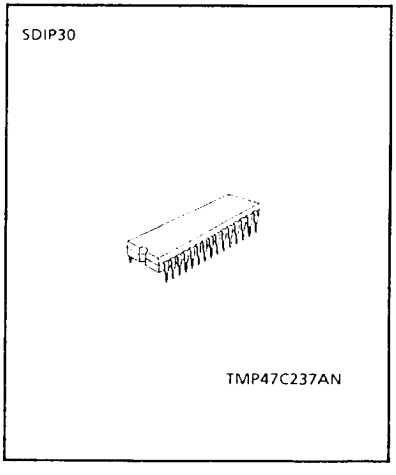
TMP47C237AN

The 47C237A is based on the TLCS-47 CMOS series. The 47C237A has display on-screen circuit (OSD) to display bar which indicate channel or volume on TV screen, A/D converter input, D/A converter output which is suitable for application to the digital tuning system such as TV.

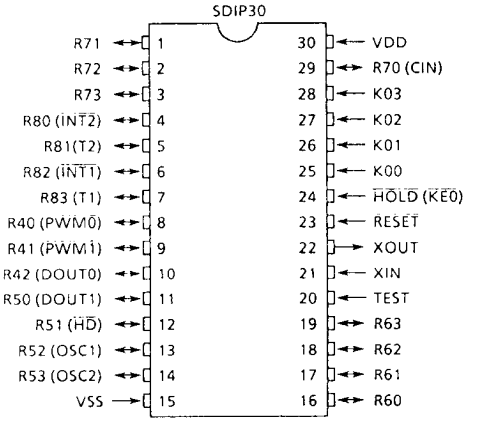
PART No.	ROM	RAM	PACKAGE
TMP47C237AN	2048 x 8-bit	128 x 4-bit	SDIP30

FEATURES

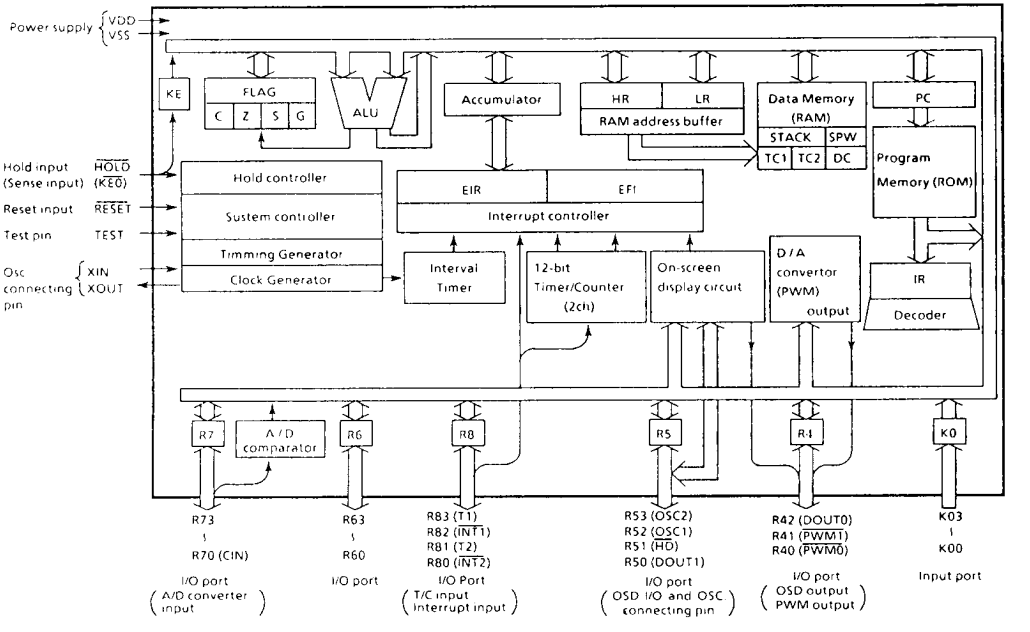
- ◆4-bit single chip microcomputer
- ◆Instruction execution time : 1.9μs (at 4.2MHz)
- ◆89 basic instructions.
- ◆Table look-up instructions
- ◆Subroutine nesting : 15 levels max.
- ◆6 interrupt sources (External : 2, Internal : 4)
  All sources have independent latches, and multiple interrupt control is available.
- ◆I/O port
  - Input 2 ports 5 pins
  - I/O 5 ports 19 pins
- ◆Interval Timer
- ◆Two 12-bit Timer/Counter
  Timer, event counter, and pulse width measurement mode
- ◆On-screen display circuit (bar display)
  - Variable display position : horizontal 256 steps
  - 2 colors
  - 2 display bar width
- ◆3-bit A/D converter input.
  Auto frequency control signal (S-shaped curve) detection
- ◆Pulse width modulation outputs
  - 14-bit resolution 1 channel
  - 6-bit resolution 1 channel
- ◆High current outputs
  LED direct drive capability (typ. 10mA x 4bit)
- ◆Hold function
  Battery / Capacitor back-up
- ◆Real Time Emulator : BM47C337A



PIN ASSIGNMENT (TOP VIEW)



BLOCK DIAGRAM



PIN FUNCTION

PIN NAME	Input/Output	FUNCTIONS	
K03-K00	Input	4-bit input port	
R42 (DOUT0)	I/O (Input)	3-bit I/O port with latch. When used as input port, D/A converter output pin and OSD output pin, the latch must be set to"1".	OSD output
R41 ($\overline{PWM1}$)			6-bit D/A converter output
R40 ($\overline{PWM0}$)			14-bit D/A converter output
R53 (OSC2)	I/O (Output)	4-bit I/O port with latch. When used as input port, resonator connectting pin for and OSD output pin, the latch must be set to "1".	Resonator connecting pin for OSD
R52 (OSC1)	I/O (Input)		
R51 ($\overline{HD}$)	I/O (Input)		Horizontal sync signal input
R50 (DOUT1)	I/O (Output)		OSD output
R63-R60	I/O	4-bit I/O port with latch. When used as input port, the latch must be set to "1".	
R73-R71	I/O	4-bit I/O port with latch. When used as input port, AFC comparater input pin, the latch mast be set to "1".	
R70 (CIN)	I/O (Input)		AFC comparater input.
R83 (T1)	I/O (Input)	4-bit I/O port with latch. when used as input port, external interrupt and timer / counter input pin, the latch mast be set to "1".	Timer/Counter 1 input
R82 ($\overline{INT1}$)			External interrupt 1 input
R81 (T2)			Timer/Counter 2 external input
R80 ($\overline{INT2}$)			External interrupt 2 input
XIN, XOUT	Input, Output	Resonator connecting pin. For inputting external clock, XIN is used and XOUT is opened.	
RESET	Input	Reset signal input.	
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)	Hold request/release signal input	Sense input
TEST	Input	Test pin for out-going test. Be opened or fixed to low level.	
VDD	Power supply	+ 5V	
VSS		0V (GND)	

OPERATIONAL DESCRIPTION

Concerning the 47C237A, the configuration and functions of hardwares are described.
As the description is porvided with priority on those parts differing from the 47C200A, the technical data sheets for the 47C200A shall also be referred to.

Note. The 47C237A have no serial port, differing from the 47C200A.

1. SYSTEM CONFIGURATION

(1) I/O Port
(2) On-screen display (OSD) circuit
(3) AFC comparator input.
(4) D/A converter output.

2. PERIPHERAL HARDWARE FUNCTION

2.1 I/O Port

The 47C237A have 7 I/O Port(24 Pins)each as follow.

① K0 port ; 4-bit input
② R4 port ; 3-bit input/output (R42 pin is shared with OSD output. R41, R42 pins is shared by D/A converter output)
③ R5 port ; 4-bit input/output (R53, R52 pins is shared with Resonator connecting pin for OSD R51, R50 pins is shared with I/O port.)
④ R6 port ; 4-bit input/output
⑤ R7 port ; 4-bit input/output (R70 pins is shared with AFC comparater input.)
⑥ R8 port ; 4-bit input/output (shared with external interrupt input and timer/counter input)
⑦ KE port ; 1-bit sense input (shared with hold request/release signal input.)

This section describes ports of ②, ③, ⑤ which are changed from the 47C200A.
The 47C237A has no P1, P2 and R9, therefore 5-bit 8-bit data conversion instruction [OUTB @HL] can not use.

(1) Port R4 (R42-R40)
3-bit I/O port with latch. When used as input port, the latch must be set to "1". The latch is initialized to "1".
This pin is used both as R42 for OSD output, and as R40 and R41 for D/A converter output. When used for OSD output, select DOUT0 to enable OSD. To use for D/A converter, set the latch to "1".
Also, when this pin is used as R42 for OSD output, "1" is read in during the input instruction is executed. There is no R43 pin, but "1" is read in during the input instruction is executed.

(2) Port R5 (R53-R50)
4-bit I/O port with latch. When used as input port, the latch must be set to "1" and OSD must be disable for R53, R52 and R50 pins. The latch is initialized to "1".
R53, R52 pins is shared by resonator connecting pin for OSD. When used as resonator connecting pin, the latch must be set to "1" and OSD must be enable.
This pin is also used as R51 for horizontal sync. signal input. To use this pin for horizontal sync. signal input, set the latch to "1". Like the R42 pin, the R50 pin is also used for OSD output. Also, when the input instruction is executed with the OSD display enabled, "1" is read into the R50, R52 and R53 pin, and horizontal sync. signal input is read into the R51 pin.

Port R4 (Port address OP04 / IP04)

3	2	1	0
	R42 ($\overline{DOU T0}$)	R41 ($\overline{PWM1}$)	R40 ($\overline{PWM0}$)

Port R5 (Port address OP05/IP05)

3	2	1	0
R53 (OSC2)	R52 (OSC1)	R51 ($\overline{HD}$)	R50 (DOUT1)

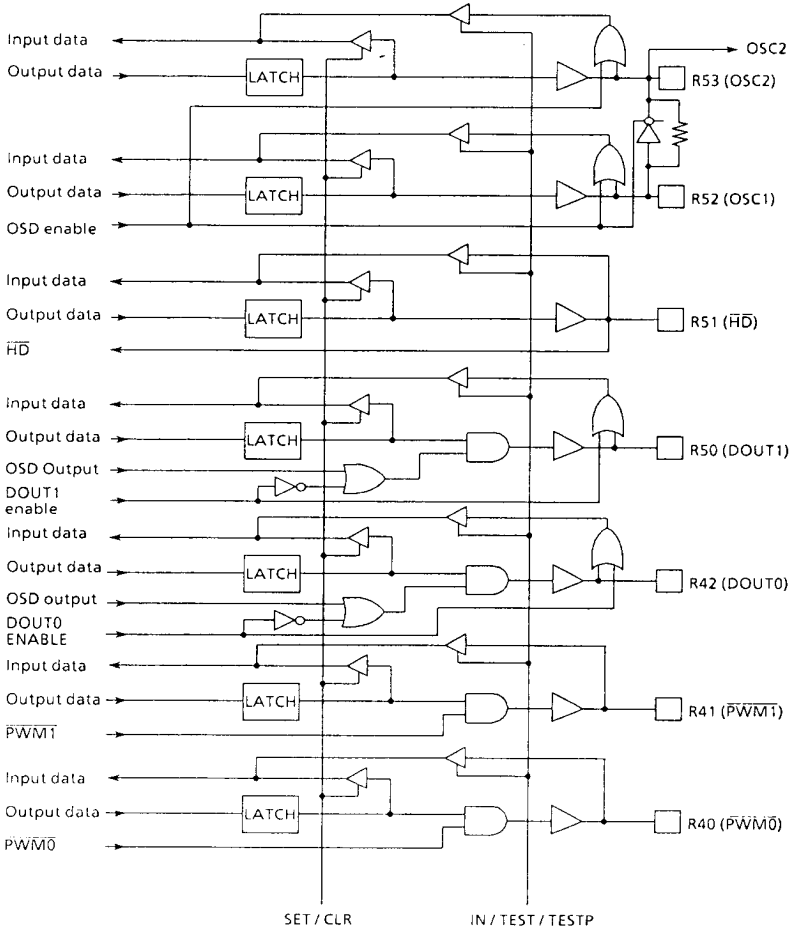


Figure 2-1. Ports R4 and R5

Port address (**)	Port		Input/output instruction						
	Input (IP**)	Output (OP**)	IN %p, A IN %p, @HL	OUT A,%p OUT @HL,%p	OUT #k, %p	OUTB @HL	SET %p, b CLR %p, b	TEST %p,b TESTP %p,b	SET @L CLR @L TEST @L
00_H	K0 input port	——	○	–	–	–	–	○	–
01	——	——	–	–	–	–	–	–	–
02	——	——	–	–	–	–	–	–	–
03	——	——	–	–	–	–	–	–	–
04	R4 input port	R4 output port	○	○	○	–	○	○	○
05	R5 input port	R5 output port	○	○	○	–	○	○	○
06	R6 input port	R6 output port	○	○	○	–	○	○	○
07	R7 input port	R7 output port	○	○	○	–	○	○	○
08	R8 input port	R8 output port	○	○	○	–	○	○	–
09	——	——	–	–	–	–	–	–	–
0A	——	OSD position lower 4-bits	–	○	○	–	–	–	–
0B	——	OSD position uper 4-bits	–	○	○	–	–	–	–
0C	——	OSD control	–	○	○	–	–	–	–
0D	——	——	–	–	–	–	–	–	–
0E	Status input	——	○	–	–	–	–	○	–
0F	Horizontal sync. signal counter control	——	○	–	–	–	–	–	–
10_H	Undefined	HOLD control	–	○	–	–	–	–	–
11	Undefined	——	–	–	–	–	–	–	–
12	Undefined	AFC comparator input control	–	○	–	–	–	–	–
13	Undefined	——	–	–	–	–	–	–	–
14	Undefined	——	–	–	–	–	–	–	–
15	Undefined	——	–	–	–	–	–	–	–
16	Undefined	——	–	–	–	–	–	–	–
17	Undefined	PWM buffer	–	○	–	–	–	–	–
18	Undefined	PWM data transfer buffer	–	○	–	–	–	–	–
19	Undefined	Interval Timer interrupt control	–	○	–	–	–	–	–
1A	Undefined	——	–	–	–	–	–	–	–
1B	Undefined	——	–	–	–	–	–	–	–
1C	Undefined	Timer/Counter 1 control	–	○	–	–	–	–	–
1D	Undefined	Timer/Counter 2 Control	–	○	–	–	–	–	–
1E	Undefined	——	–	–	–	–	–	–	–
1F	Undefined	HD counter control	–	○	–	–	–	–	–

Note 1. Port addresses with "——" mark are reserved addresses and cannot be used at user program.

Table 2-1. Port Address Assinment and Input/Output Instructions

(3) Port R7 (R73-R70)

4-bit I/O port with latch. When used as input port, the latch must be set to "1" the latch is initialized to "1".

R70 (CIN) pin is shared by A/D converter input. When used as A/D converter input, R70 output latch must be set to "1" and bit 3 of command register must be set enable. CIN input is comparator input read from bit 0 of IP07 and uses the programmable 3-bit D/A converter output as the reference voltage.

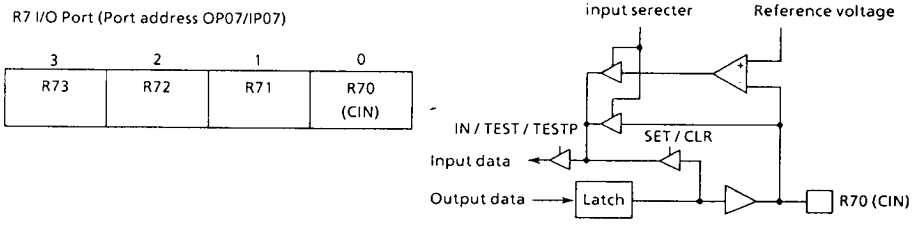


Figure 2-3. Port R7

2.2 On-Screen Display (OSD) Circuit

The 47C237A has a built-in on-screen display circuit that indicates the display position of bar displays such as channel and sound volume on the TV screen.

The lateral positons of bar displays can be changed with the data register values. Bar lengths (vertical) can also be varied by counting the horizontal sync. signals with the horizontal sync. signal counter, and then turning the display on and off.

2.2.1 Circuit Configuration

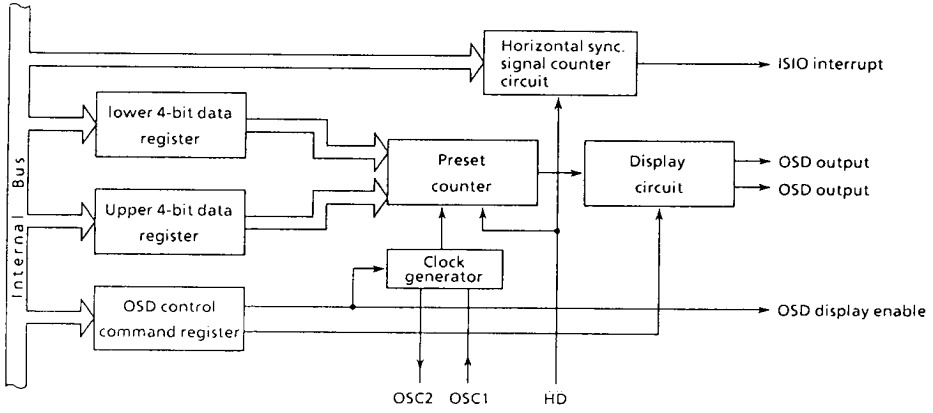


Figure 2-4. On-screen display circuit

2.2.2 Control of on-screen display circuit

On-screen display circuit is controlled by command register(OP0C),the output latch of R42 R50 pins, and data register (OP0A, OP0B).

(1) Command register OP0C

Every pin of OSD is controlled and width display bar is selected by OP0C.

On-screen display circuit control command register(Port address OP0C)

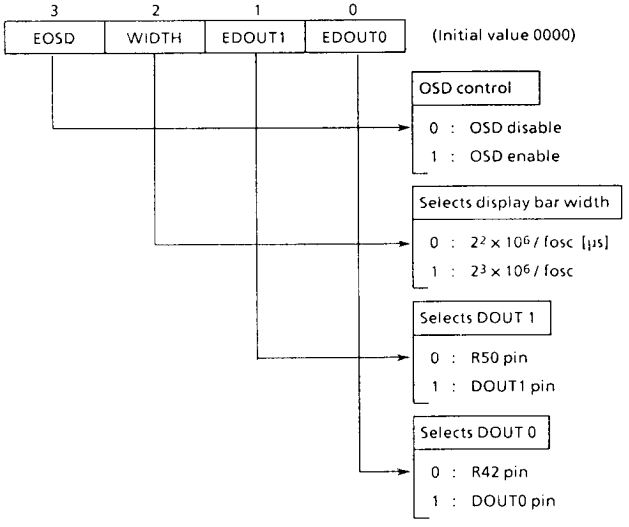


Figure 2-5. Control command register.

(2) OSD Output Control

OSD output is from the DOUT0 and DOUT 1 pins,each of which can be enabled independently. When EOSD = 1,bar display can be enabled by setting EDOUT0 and EDOUT1. Also,when not used for OSD output,EDOUT0 and EDOUT1 can be cleared and used as normal input/output pins.

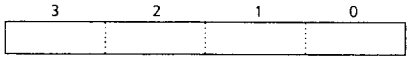
When bar display is enabled,bars are displayed continuously from the top of the TV screen to the bottom. Bar displays can be turned on and off by setting and clearing the R42 and R50 output latches;therefore,bar length(vertical)can be varied by counting the horizontal sync. signals with the horizontal sync. signal counter and then turning on and off. Width can also be used to select either of two bar widths.

(3) Display Position Setting

Bar display positions are determined by the values loaded to the data registers (OP0A, OP1B). After resetting,the display position is the upper left corner of the TV screen. The bar display position can be moved across the TV screen from left to right in 256 steps by varying the values loaded to OP0A(lower 4-bits)and OP0B(upper 4-bits)

Note. The display position is changed by accessing the OP0A data register,therefore,overwrite in the sequence OP0B,OP0A. Also,CPU operation and the horizontal sync. signal are not synchronized,so a difference in level will occur if writing is not synchronized with the vertical sync. signal.

Data register of the display position setting lower 4-bit (Port address OP0A)



Data register of the display position setting upper 4-bit (Port address OP0B)

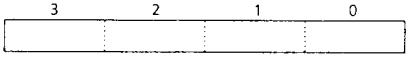


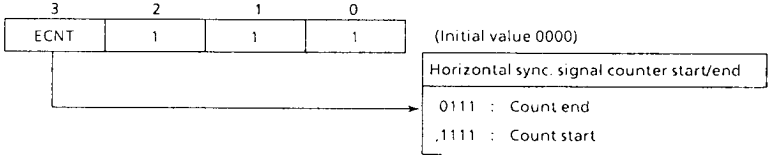
Figure 2-6. Data register of the OSD bar display position setting

2.2.3 Sync. signal counter.

This counter counts the horizontal sync. signal in units of 4 cycles and includes a built-in function for generating interrupt requests. This counter is controlled by the command register (OP1F). The horizontal sync. signal pin is also used as the R51 pin. To use for horizontal sync. signal input, set the R51 output latch to "1".

Also, the operating status can be determined from the status register (IP0E).

Command register of horizontal sync. signal counter control (Port address OP1F)



Note: When used as horizontal sync. signal counter, not only bit 3 (ECNT) of command register (OP1F) but also bit 2 through bit 0 must be set to "1".

Status register of horizontal sync. signal counter control. (Port address IP0E)

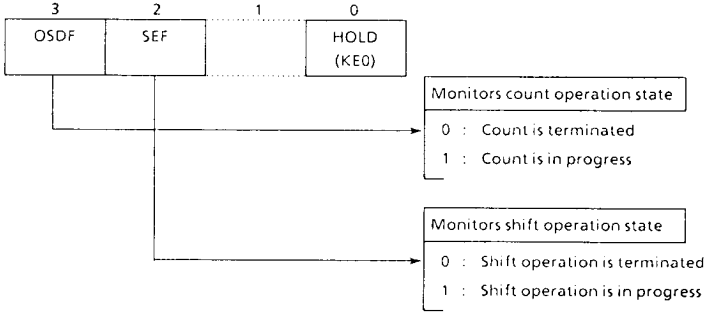


Figure 2-7. Command register/status register of horizontal sync. signal counter control

The horizontal sync. signal counter is activated when ECNT is set to "1" and an ISIO interrupt request is generated when the fourth cycls of the horizontal sync. signal has been counted. During the ISIO interrupt service program, it is possible to vary the vertical lengths (heights) of bars by setting and clearing the output latches for each DOUT pin (turning the bar display on and off). Also, ECNT setting and clearing should be synchronized with the vertical sync. signal when used; otherwise, oseillation equal to upto 8 cycles of the horizontal sync. signal will be generated. This can be corrected by inputting the vertical sync. signal ($\overline{VD}$) to the $\overline{INT1}$ pin and generating an INT1 interrupt. ISIO interrupt requests can be cleared by reading IPOF (to read in dummy data). Counting of the horizontal sync. signals will continue even after an intorrupt is generated.
Shifting of the sync. signal counter is synchronized with the horizontal sync. signal ($\overline{HD}$); therefore, IPOF must be read before the next 4 cycles are counted. If IPOF is not read, the following interrupt request will be ignored.

Note . Always read IPOF before clearing the ISIO interrupt latch. If an attempt is made to clear the interrupt latch without reading IPOF, the next ISIO interrupt will be ineffective.

Operation of the counter can be ended by setting ECNT to "0". When ECNT is cleared,operation will end when 4 cycles of the sync. signal have been counted and IPOF has been read. The program can be used to determine if counter operation has ended by sensing OSDF (bit 3 of the status register). OSDF will become "0" if counter operation has ended.
There are two methods for ending counter operation, depending on the amount of processing required of the interrupt service program.

① When processing is completed within one horizontal sync. signal cycle
When an ISIO interrupt is generated and it is possible to set ECNT to "0" before the next horizontal sync. signal arrives, the interrupt service program, which counts continuously, clears ECNT to "0"and then reads IPOF.

② When processing is not completed within one horizontal sync. signal sycle
When it is possible for the next sync. signal to arrive before ECNT is cleared by receipt of an interrupt request, the fact that SEF (bit 2 of the status register) is set to "1" is confirmed when the next to the last count is made, after which ECNT is cleared to "0" and IPOF is read. Thus, it is unnecessary for the interrupt service program to do anything in accordance with the final count operation. It is only necessary to read IPOF.

Example : The vertical length (height) is set by using the INT1 interrupt to synchronize with the $\overline{VD}$ signal and turning the bar display on and off with the ISIO interrupt (the $\overline{HD}$ count is (number of interrupts) × (4 cycles)).

INT1 interrupt service program

```
        :
LD      A, #0000B   ;  Sets data "0" to number
ST      A, 10H         of interrupt countor
LD      A, #1111B   ;  Intructs count start
OUT     A, %OP1F
        :
```

ISIO interrupt service program

```
        LD      HL, #10H    ;  Counts the number of interrupt
        INC     @HL
        B       SDINA
        :
SDINA   : LD    A, #1110B   ;  Count lower
        CMPR    A, @HL      ;  ≠
        B       SDON
SDDIS   : CLR   %OP04, 2    ;  Sets data "0" to DOUT pins output
        CLR     %OP05, 0       latch
SSEF0   : TEST  %IP0E, 2    ;  Waits until SEF = "1"
        B       SSEF0
        LD      A, #0111B   ;  ECNT ← 0
        OUT     A, %OP1F
        IN      %IP0F, A
        B       SDEND
        :
SDON    : SET   %OP04, 2    ;  Sets data "1"
        SET     %OP05, 0       to DOUT pins output latch
        IN      %IP0F, A
        :
SDEND   :
```

2.3 3-bit A/D converter (comparator) input

Comparator input consists of a comparator and a 3-bit D/A converter. AFC input voltage can be detected in 8 steps by sensing bit 0 of IP07 while changing the reference voltage (D/A converter output voltage) with the command register (OP12).

R70 pin is also used for comparator input. The comparator is initialized to disable. The latch should be set to "1" when pin R70 is used for comparator input.

2.3.1 Circuit configuration

Figure 2-8 shows the configuration of comparator circuit.

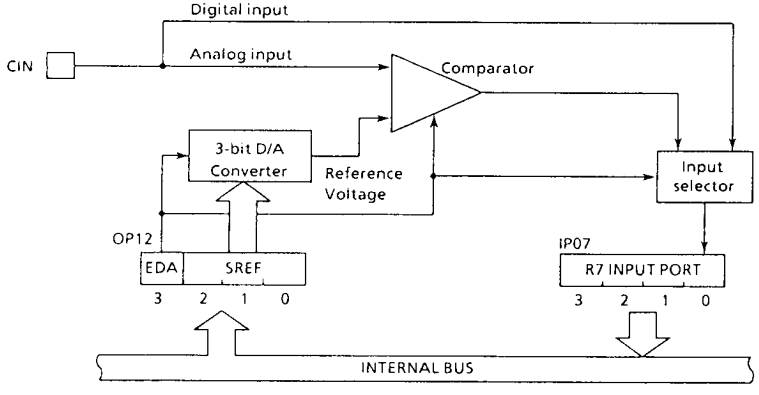


Figure 2-8. Comparator input circuit

2.3.2 Comparator input control

The reference voltage of the comparator is set using the lower 3 bits of the command register (OP12) Table 2-2 shows the reference voltage at V_{DD} = 5 V.

Comparator input control command register (port address OP12)

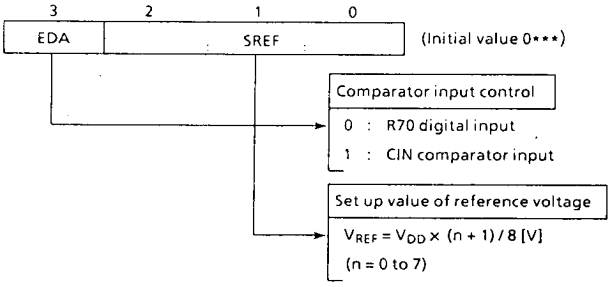


Figure 2-9. Command register

OP12 2 1 0	Reference voltage [V]
0 0 0	0.62
0 0 1	1.25
0 1 0	1.87
0 1 1	2.50
1 0 0	3.12
1 0 1	3.75
1 1 0	4.37
1 1 1	5.00

Table 2-2. Reference Voltage

2.4 D/A converter (Pulse Width Modulation) output

The 47C237A have two D/A converter ($\overline{PWM}$) output channels. PWM output can easily be obtained by connecting an external low pass filter."

$\overline{PWM}$ output is from the R40 ($\overline{PWM0}$), R41 ($\overline{PWM1}$) pins. R40 ($\overline{PWM0}$), R41 ($\overline{PWM1}$) pins are used for $\overline{PWM}$ output, the corresponding R40, R41 output latch is set to "1." The R40, R41 output latch is initialized to "1".

$\overline{PWM}$ output is controlled by the buffer selector (OP17) and the data transfer buffer (OP18). $\overline{PWM}$ data written to the data transfer buffer can be sent to the $\overline{PWM}$ data latch by writing "C_H" to the buffer selector to switch to $\overline{PWM}$ output. $\overline{PWM}$ data transferred to the $\overline{PWM}$ data latch remain intact until overwritten.

Resetting and holding clear the buffer selector, data transfer buffer and $\overline{PWM}$ data latch to "0" ($\overline{PWM}$ output is "1" level).

2.4.1 Circuit configuration

Figure 2-10 shows the pulse width modulation circuit.

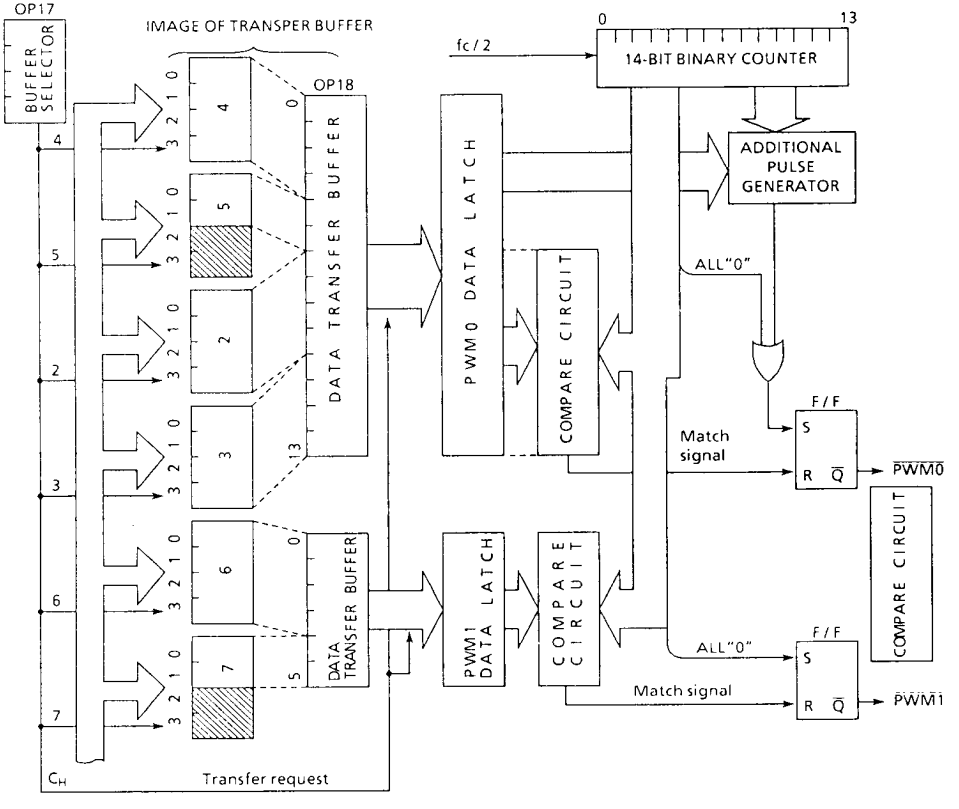


Figure 2-10. Pulse width modulation circuit

2.4.2 PWM output wave

(1) $\overline{PWM0}$ output

$\overline{PWM0}$ is a PWM output controled by 14 bits data.

The basic period of the $\overline{PWM0}$ is $T_M = 2^{15}/fc$. The higher 8 bits of 14 bits data are used to control the pulse width of the pulse output with the period of $T_S = T_M/64$, which is the sub-period of the $\overline{PWM0}$. When the 8 bits data are decimal n ($0 \leqq n \leqq 255$), this pulse width becomes n x to, where to = 2/fc.

The lower 6 bits of 14 bits data are used to control the generation of an additional to wide pulse in each T_S period. When the 6 bits data are decimal m ($0 \leqq m \leqq 63$), the additional pulse is generated in each of m periods out of 64 periods contained in a T_M period. The relationship between the 6 bits data and the position of T_S period where the additional pulse is generated is shown in Table 2-3.

Bit position of 6 bits data	Relative position of T_S where the additional (No. i of T_S is listed)
Bit 0	32
Bit 1	16, 48
Bit 2	8, 24, 40, 56
Bit 3	4, 12, 20, 28, 36, 44, 52, 60
Bit 4	2, 6, 10, 14, 18, 22, 26, 30, ·····, 58, 62
Bit 5	1, 3, 5, 7, 9, 11, 13, 15, ·····, 59, 61, 63

Table 2-3. Correspondence between 6 bits data and the additional pulse generated T_S periods

(2) $\overline{PWM1}$

$\overline{PWM1}$ is a PWM output controled by 6 bits data. The 6 period of them is $T_M = 2^7/fc$, When the 6 bits data are decimal k ($0 < k < 63$), the pulse width becomes k x to.

The waveform is also illustrated in Figure 2-11.

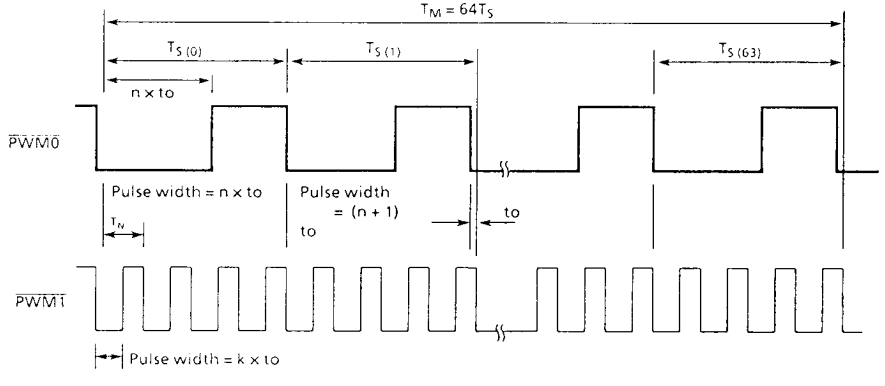


Figure 2-11. PWM Output Waveform

2.4.3 Control of PWM circuit (data transfer)

$\overline{PWM}$ output is controlled by writing the output data to the data transfer buffer (OP18). The output data are written in sections using the buffer selector (OP17). In the data transfer buffer, the respective sections of data are assigned buffer numbers and written as indicated in Table 2-4.

① The buffer number of the buffer to which the data are to be written is written to the buffer selector (OP17).
② The corresponding PWM data are written to the selected buffer.
③ The output data are written to the transfer buffer by repeating the operations in items ① and ② above.
④ When writing is completed, "C_H" is written to the buffer selector (OP17).

While the output data are being written to the transfer buffer, the previous PWM data are being output.
When "C_H" is written to the buffer selector, the output data are sent to the PWM data latch and $\overline{PWM}$ output is enabled.
The time from when "C_H" is written to the buffer selector until $\overline{PWM0}$ output is enabled is 2^{15}/fc (8192μs at 4 MHz) maximum, $\overline{PWM1}$ output is enabled is 2^9/fc (128μs at 4 MHz) maximum.

Buffer Number (OP17)	Correspondence to bit (OP18)	Mode	PWM Output
2	Bit of PWM 0 transfer buffer 9 - 6	Write	Preceding data
3	Bit of PWM 0 transfer buffer 13 - 10	Write	Preceding data
4	Bit of PWM 0 transfer buffer 3 - 0	Write	Preceding data
5	Bit of PWM 0 transfer buffer 5 - 4	Write	Preceding data
6	Bit of PWM 1 transfer buffer 3 - 0	Write	Preceding data
7	Bit of PWM 1 transfer buffer 5 - 4	Write	Preceding data
C	None	Transfer	Present data

Table 2-4. The bit and buffer number of data transfer buffer

ELECTRICAL CHARACTERISTCS

ABSOLUTE MAXMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		− 0.3 to 7	V
Input Voltage	V_{IN}		− 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT1}	Except sink open drain pin, but include R5	− 0.3 to V_{DD} + 0.3	V
	V_{OUT2}	Sink Open drain pin, Except R5 port	− 0.3 to 10	
Output Voltage(Per 1 pin)	I_{OUT1}	Port R6	10	mA
	I_{OUT2}	Ports R4, R5, R7, R8	3.2	
Output Voltage(Total)	Σ I_{OUT1}	Port R6	40	mA
Power Dissipation[Topr = 70℃]	PD		600	mW
Soldering Temperature(Time)	T_{sld}		260 (10sec)	°C
Storage Temperature	T_{stg}		− 55 to 125	°C
Operating Temperature	T_{opr}		− 20 to 70	°C

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = − 20 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		in the Normal mode	4.5	6.0	V
			in the Hold mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5V$	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5V$		$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input		0	$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5V$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	4.2	MHz
	fosc	OSC1, OSC2		2	6	

Note. Input Voltage V_{IH3}, V_{IL3} : in the HOLD mode

D.C.CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = − 20 to 70°C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		—	0.7	—	V
Input Curreut	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	—	—	± 2	μA
	I_{IN2}	Ports R (Open drain)					
Input Resistance	R_{IN1}	Port K0 with pull-up		30	70	150	KΩ
	R_{IN2}	$\overline{RESET}$		100	220	450	
Output Leak Current	I_{LO}	Open drain output ports	V_{DD} = 5.5V, V_{OUT} = 5.5V	—	—	2	μA
Output High Voltage	V_{OH}	Port R6	V_{DD} = 4.5V, I_{OH} = − 200μA	2.4	—	—	V
Output Low Voltage	V_{OL}	Excepet Xout	V_{DD} = 4.5V, I_{OL} = − 1.6mA	—	—	0.4	V
Output Low Current	I_{OL}	Port R6	V_{DD} = 4.5V, V_{OL} = 1.0V	—	10	—	mA
Suply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	—	3	6	mA
Suply Current (in the Hold mode)	I_{DDH}		V_{DD} = 5.5V	—	0.5	10	μA

Note 1. TYP. values show those at T_{opr} = 25°C, V_{DD} = 5 V.
Note 2. When the K0 port has a built-in input resistor, current by resistor is excluded.
Note 3. When K0 port has a built-in input resistor, current value is that at time of open. Further, voltage level at R port is valid.

A/D CONVERSION

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Input Voltage	V_{AIN}	CIN		V_{SS}	—	V_{DD}	V
A/D Conversion Error	—			—	—	$\pm\frac{1}{4}$	LSB

A.C.CHARACTERISTICS

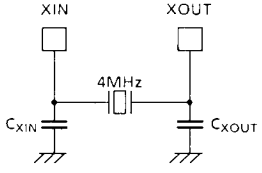
(V_{SS} = 0V, V_{DD} = 4.5 to 6.0V, T_{opr} = − 20 to 70°C)

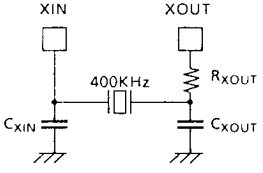
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	—	20	μs
High level Clock Pulse Width	t_{WCH}	For external clock operation	80	—	—	ns
Low level Clock Pulse Width	t_{WCL}					

RECOMMENDED OSCILLATING CONDITIONS (V_{SS} = 0 V, V_{DD} = 4.5 to 6 V, T_{opr} = – 20 to 70°C)

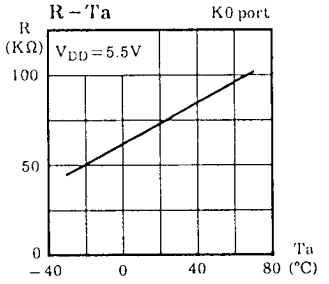
(1) 4MHz
Ceramic Resonator
CSA4.00MG (MURATA) $C_{XIN} = C_{XOUT}$ = 30pF
KBR-4.00MS (KYOCERA) $C_{XIN} = C_{XOUT}$ = 30pF
Crystal Oscillator
204B-6F 4.0000 (TOYOCOM) $C_{XIN} = C_{XOUT}$ = 20pF

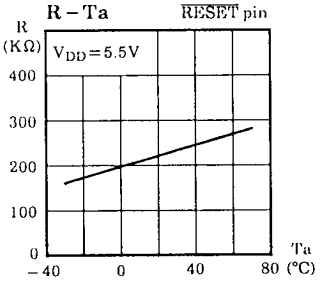
(2) 400KHz
Ceramic Resonator
CSB400B (MURATA) $C_{XIN} = C_{XOUT}$ = 220pF, R_{XOUT} = 6.8KΩ
KBR-400B (KYOCERA) $C_{XIN} = C_{XOUT}$ = 100pF, R_{XOUT} = 10KΩ

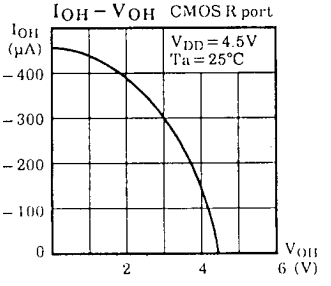


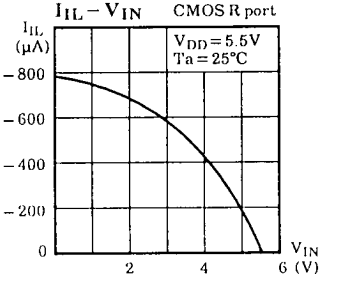


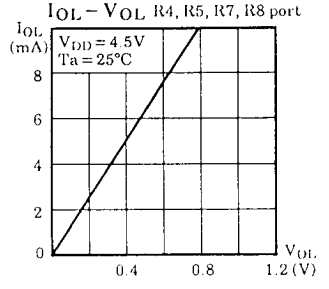
TYPICAL CHARACTERISTICS

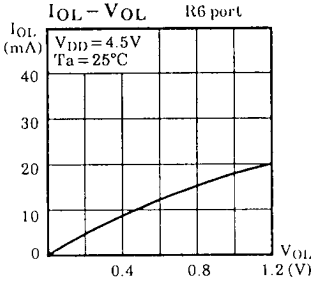


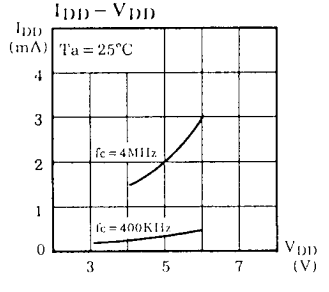


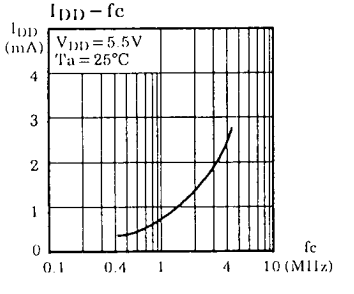








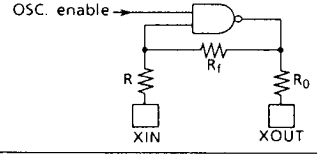
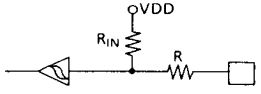
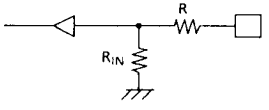
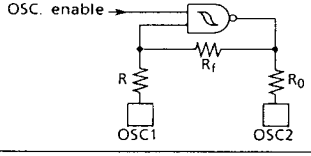




INPUT/OUTPUT CIRCUITRY

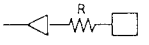
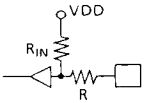
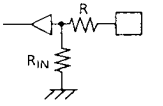
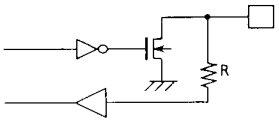
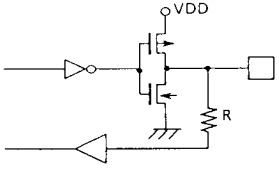
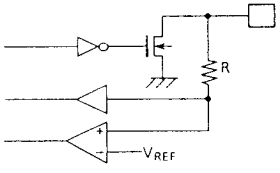
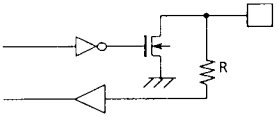
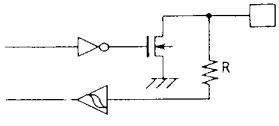
(1) Control pins

Input/Output circuitreis of the 47C237A control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins R = 1KΩ (typ.) Rf = 1.5MΩ (typ.) RO = 2KΩ (typ.)
$\overline{RESET}$	Input		Hysteresis input Contained pull-up resistor RIN = 220KΩ (typ.) R = 1KΩ (typ.)
$\overline{HOLD}$ ($\overline{KE0}$)	Input (Input)		Hysteresis input (Sence input) R = 1KΩ (typ.)
TEST	Input		Contained pull-down resistor RIN = 70KΩ (typ.) R = 1KΩ (typ.)
OSC1 OSC2	Input Output		Resonator connectting pin for OSD R = 1KΩ (typ.) Rf = 1.5MΩ (typ.) RO = 2KΩ (typ.)
$\overline{HD}$	Input		Sync signal input pin Hysteresis input R = 1KΩ (typ.)

(2) I/O port

The input/output circuitries of the 47C237A I/O port are shown below, any one of the circuitries can be chosen by a code (PD-PF) as a mask option.

PORT	I/O	INPUT/OUTPUT CIRCUITRY and CODE	REMARKS
K0	Input	PD:  PE:  PF: 	Pull-up/Pull-down resistor R_{IN} = 70kΩ (typ.) R = 1kΩ (typ.)
R4 R5	I/O		Sink open drain output Initial "Hi-Z" R = 1kΩ (typ.)
R6	I/O		Push-pull output Initial "Low" High drive current output I_{OL} = 10mA (typ.) R = 1kΩ (typ.)
R7	I/O	R70:  R71-R73: 	Sink open drain output Initial "Hi-Z" Comparater input (R70) R = 1kΩ (typ.)
R8	I/O		Sink open drain output Initial "Hi-Z" Hysteresis input R = 1kΩ (typ.)