### **INTEGRATED CIRCUITS**

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## HEF4001UB gates Quadruple 2-input NOR gate

Product specification
File under Integrated Circuits, IC04

January 1995



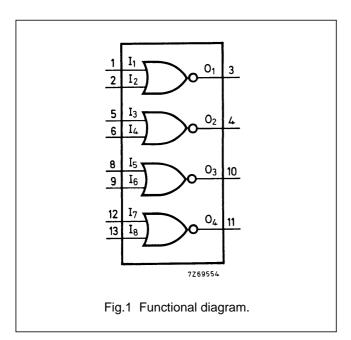


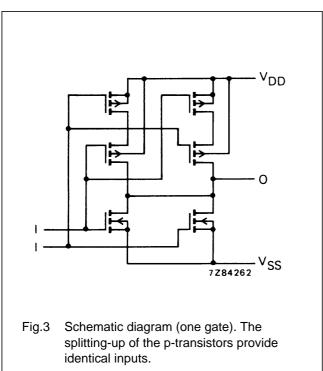
### **Quadruple 2-input NOR gate**

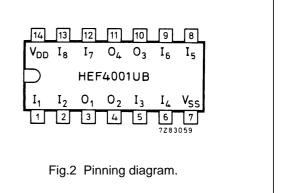
## HEF4001UB gates

#### **DESCRIPTION**

The HEF4001UB is a quadruple 2-input NOR gate. This unbuffered single stage version provides a direct implementation of the NOR function. The output impedance and output transition time depends on the input voltage and input rise and fall times applied.







HEF4001UBP(N): 14-lead DIL; plastic

(SOT27-1)

HEF4001UBD(F): 14-lead DIL; ceramic (cerdip)

(SOT73)

HEF4001UBT(D): 14-lead SO; plastic

(SOT108-1)

(): Package Designator North America

### FAMILY DATA, IDD LIMITS category GATES

See Family Specifications for  $V_{\text{IH}}/V_{\text{IL}}$  unbuffered stages

## Quadruple 2-input NOR gate

HEF4001UB gates

### **AC CHARACTERISTICS**

 $V_{SS}$  = 0 V;  $T_{amb}$  = 25 °C;  $C_L$  = 50 pF; input transition times  $\leq$  20 ns

	V <sub>DD</sub> V	SYMBOL	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays						
$I_n \to O_n$	5		65	130	ns	30 ns + (0,70 ns/pF) C <sub>L</sub>
HIGH to LOW	10	t <sub>PHL</sub>	30	60	ns	17 ns + (0,27 ns/pF) C <sub>L</sub>
	15		25	50	ns	15 ns + (0,20 ns/pF) C <sub>L</sub>
	5		40	80	ns	13 ns + (0,55 ns/pF) C <sub>L</sub>
LOW to HIGH	10	t <sub>PLH</sub>	20	40	ns	9 ns + (0,23 ns/pF) C <sub>L</sub>
	15		15	30	ns	7 ns + (0,16 ns/pF) C <sub>L</sub>
Output transition times	5		75	150	ns	15 ns + (1,20 ns/pF) C <sub>L</sub>
HIGH to LOW	10	t <sub>THL</sub>	30	60	ns	6 ns + (0,48 ns/pF) C <sub>L</sub>
	15		20	40	ns	4 ns + (0,32 ns/pF) C <sub>L</sub>
	5		60	110	ns	10 ns + (1,00 ns/pF) C <sub>L</sub>
LOW to HIGH	10	t <sub>TLH</sub>	30	60	ns	9 ns + (0,42 ns/pF) C <sub>L</sub>
	15		20	40	ns	6 ns + (0,28 ns/pF) C <sub>L</sub>
Input capacitance		C <sub>IN</sub>	_	10	pF	

	V <sub>DD</sub> V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	500 $f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	5000 $f_i + \sum (f_o C_L) \times V_{DD}^2$	f <sub>i</sub> = input freq. (MHz)
package (P)	15	$30\ 000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f <sub>o</sub> = output freq. (MHz)
			C <sub>L</sub> = load capacitance (pF)
			$\sum (f_o C_L) = \text{sum of outputs}$
			V <sub>DD</sub> = supply voltage (V)

## Quadruple 2-input NOR gate

# HEF4001UB gates

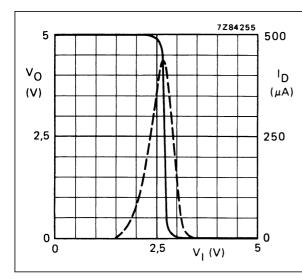


Fig.4 Typical transfer characteristics; one input, the other input connected to  $V_{SS}$ ;

$$V_O$$
;  
 $---I_D$  (drain current);  
 $I_O = 0$ ;  $V_{DD} = 5$  V.

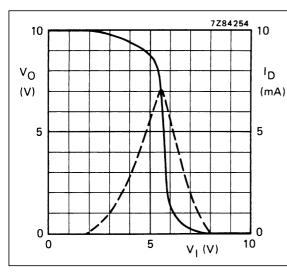


Fig.5 Typical transfer characteristics; one input, the other input connected to  $V_{SS}$ ;

$$\frac{1}{100} = \frac{1}{100} = \frac{1}$$

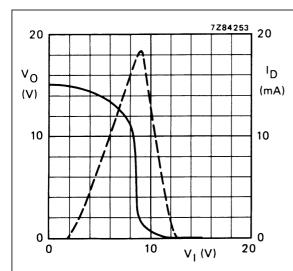


Fig.6 Typical transfer characteristics; one input, the other input connected to  $V_{SS}$ ;

## Quadruple 2-input NOR gate

# HEF4001UB gates

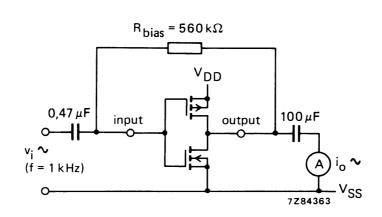
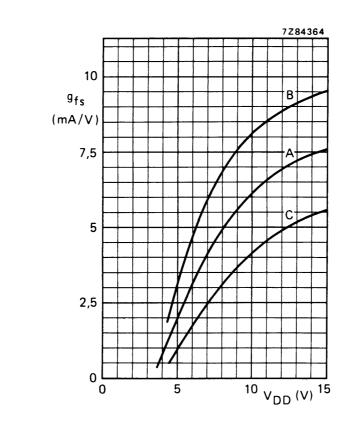


Fig.7 Test set-up for measuring forward transconductance  $g_{fs} = di_o/dv_i$  at  $v_o$  is constant (see also graph Fig.8).



A : average,

 $\,C\,$  :  $\,$  average  $-\,2$  s, in where 's' is the observed standard deviation.

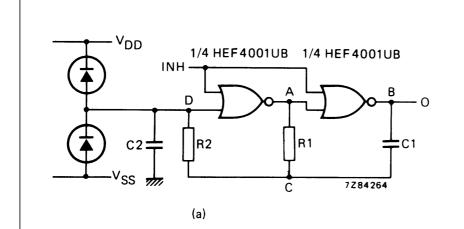
Fig.8 Typical forward transconductance  $g_{fs}$  as a function of the supply voltage at  $T_{amb}$  = 25 °C.

### Quadruple 2-input NOR gate

HEF4001UB gates

#### **APPLICATION INFORMATION**

Some examples of applications for the HEF4001UB are shown below. Because of the fact that this circuit is unbuffered, it is suitable for use in (partly) analogue circuits.



INH	0		
Н	L		
L	osc		

In Fig.9 the oscillation frequency is mainly determined by R1C1, provided R1 << R2 and R2C2 << R1C1.

The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance. The period  $T_p$  is given by  $T_p = T_1 + T_2$ , in which

$$\rm T_1 = R1C1 \; ln \frac{V_{DD} + V_{ST}}{V_{ST}} \; and \; T_2 = R1C1 \; ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}} \; where$$

 $V_{ST}$  is the signal threshold level of the gate. The period is fairly independent of  $V_{DD},\,V_{ST}$  and temperature. The duty factor, however, is influenced by  $V_{ST}.$ 

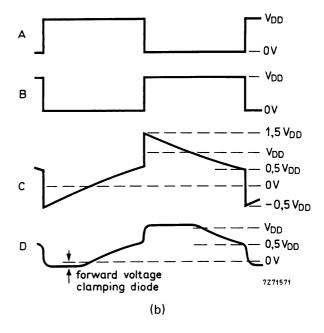
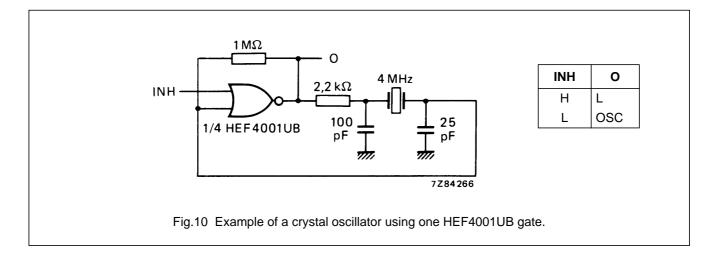


Fig.9 (a) Astable relaxation oscillator using two HEF4001UB gates; the diodes may be BAW62; C2 is a parasitic capacitance.

(b) Waveforms at the points marked A, B, C and D in the circuit diagram.

### Quadruple 2-input NOR gate

# HEF4001UB gates



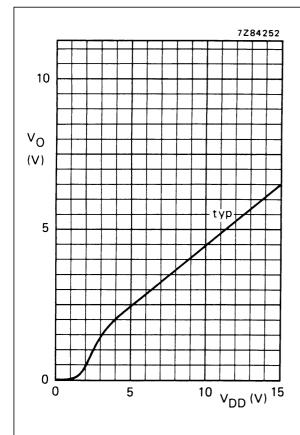


Fig.11 Output voltages as a function of supply voltage.

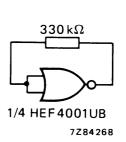


Fig.12 Test set-up for measuring graph of Fig.11. Condition: all other inputs connected to ground.

### **NOTES**

If a gate is just used as an amplifying inverter, there are two possibilities:

- Connecting the inputs together gives simpler wiring, but makes the device output not completely symmetrical.
- 2. Connecting one input to  $V_{\mbox{\footnotesize SS}}$  will give the device a symmetrical output.

### Quadruple 2-input NOR gate

# HEF4001UB gates

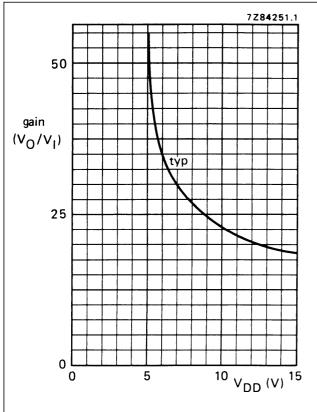


Fig.13 Voltage gain  $(V_O/V_I)$  as a function of supply voltage.

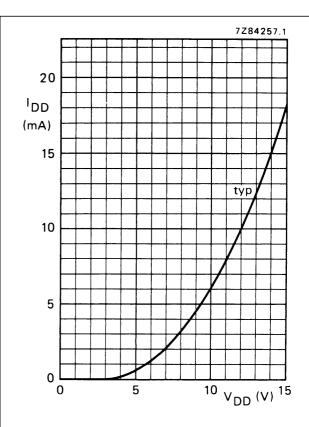


Fig.14 Supply current as a function of supply voltage.

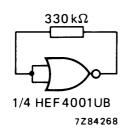


Fig.15 Test set-up for measuring graphs of Figs 13 and 14. Condition: all other inputs connected to ground.

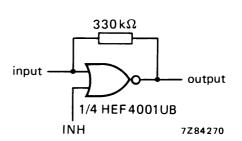


Fig.16 Example of an analogue amplifier with inhibit using one HEF4001UB gate.