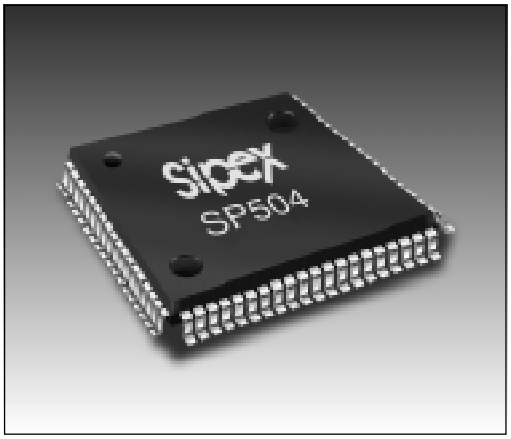
SP504

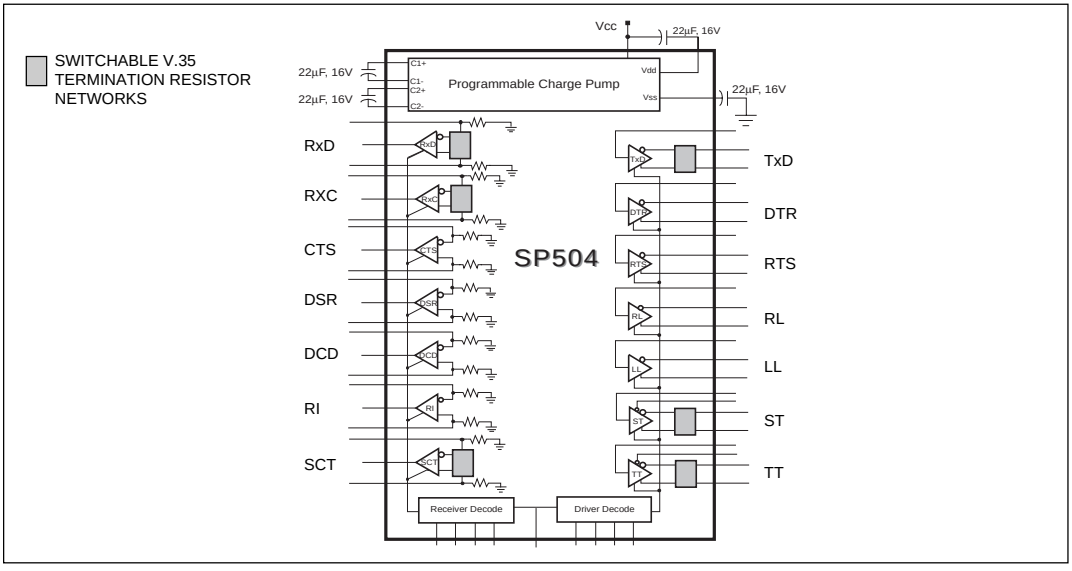
WAN Multi-Mode Serial Transceiver

- +5V Only
- Seven (7) Drivers and Seven (7) Receivers
- Driver and Receiver Tri-State Control
- Reduced V.35 Termination Network
- Pin Compatible with the SP503
- Software Selectable Interface Modes:
  - -RS-232E (V.28)
  - -RS-422A (V.11, X.21)
  - -RS-449 (V.11 & V.10)
  - -RS-485
  - -V.35
  - -EIA-530 (V.11 & V.10)
  - -EIA-530A (V.11 & V.10)
  - -V.36



DESCRIPTION...

The **SP504** is a single chip device that supports eight (8) physical serial interface standards for Wide Area Network Connectivity. The **SP504** is fabricated using a low power BiCMOS process technology, and incorporates a **Sipex** patented (5,306,954) charge pump allowing +5V only operation. Seven (7) drivers and seven (7) receivers can be configured via software for any of the above interface modes at any time. The **SP504** is suited for DTE–DCE applications. The **SP504** requires only one external resistor per V.35 driver for compliant V.35 operation.



SPECIFICATIONS

T_A = +25°C and V_{CC} = +5.0V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
LOGIC INPUTS					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
LOGIC OUTPUTS					
V_{OL}			0.4	Volts	I_{OUT}= +3.2mA
V_{OH}	2.4			Volts	I_{OUT}= –1.0mA
RS-485 DRIVER					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
HIGH Level Output			+6.0	Volts	
LOW Level Output	–0.3			Volts	
Differential Output	±1.5		±5.0	Volts	R_L=54Ω, C_L=50pF
Balance		±0.2		Volts	$\|V_T\| - \|\overline{V_T}\|$
Offset		+2.5		Volts	
Open Circuit Voltage			±6.0	Volts	
Output Current	28.0			mA	R_L=54Ω
Short Circuit Current		±250		mA	Terminated in –7V to +10V
Transition Time		20	40	ns	Rise/fall time, 10%–90%
Max. Transmission Rate	10			Mbps	R_L=54Ω; Figure 3a
Propagation Delay					T_A @ 25°C & V_{CC} = +5V only
t_{PHL}	50	80	100	ns	Figures 3a and 5; R_L=54Ω
t_{PLH}	50	80	100	ns	C_L=50pF
Differential Driver Skew		20	40	ns	$\| t_{PHL} - t_{PLH} \|$; T_A @ +25°C
RS-485 RECEIVER					
TTL Output Levels					
V_{OL}			0.4	Volts	
V_{OH}	2.4			Volts	
Input					
HIGH Threshold	+0.2		+12	Volts	(a)-(b)
LOW Threshold	–7.0		–0.2	Volts	(a)-(b)
Common Mode Range	–7.0		+12.0	Volts	
HIGH Input Current					Refer to Rec. input graph
LOW Input Current					Refer to Rec. input graph
Receiver Sensitivity			±0.2	Volts	Over –7V to +12V common mode range
Input Impedance	12			kΩ	
Max. Transmission Rate	10			Mbps	Figure 3a
Propagation Delay					T_A = 25°C & V_{CC} = +5V only
t_{PHL}	80	110	180	ns	Figures 3a and 7; A is invert-
t_{PLH}	80	110	180	ns	ing and B is non-inverting.
Differential Receiver Skew		30		ns	$\| t_{PHL} - t_{PLH} \|$; T_A @ +25°C
V.35 DRIVER					
TTL Input Levels					All outputs measured w/
V_{IL}			0.8	Volts	150Ω termination resistor
V_{IH}	2.0			Volts	connected to the non-
					inverting outputs as shown
Outputs					in Figure 18.
Differential Output	±0.44		±0.66	Volts	R_L=100Ω
Source Impedance	50	100	150	Ω	
Short-Circuit Impedance	135	150	165	Ω	V_{OUT} = –2V to +2V; A = B
Voltage Output Offset	–0.6		+0.6		
Transition Time		35	60	ns	48kbps data rate.; T_A@ 25°C
Max. Transmission Rate	10			Mbps	R_L=100Ω

SPECIFICATIONS (Continued)

T_A = +25°C and V_{CC} = +5.0V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.35 DRIVER					
Propagation Delay					T_A @ 25°C & V_{CC} = +5V only
t_{PHL}	50	80	100	ns	Figures 3b and 5
t_{PLH}	50	80	100	ns	
Differential Driver Skew		30	40	ns	$\lvert t_{PHL} - t_{PLH} \rvert$; T_A @ +25°C
V.35 RECEIVER					
TTL Output Levels					
V_{OL}			0.4	Volts	
V_{OH}	2.4			Volts	
Input					
Differential Threshold		±80		mV	
Input Impedance	90	100	110	Ω	
Short-Circuit Impedance	135	150	165	Ω	V_{IN} = +2V to –2V
Max. Transmission Rate	10			Mbps	
Propagation Delay					T_A @ 25°C & V_{CC} = +5V only
t_{PHL}	100	130	200	ns	Figure 3b and 7; A is invert-
t_{PLH}	100	130	200	ns	ing and B is non-inverting.
Differential Receiver Skew		30		ns	$\lvert t_{PHL} - t_{PLH} \rvert$; T_A @ +25°C
RS-422 DRIVER (V.11)					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Outputs					
Open Circuit Voltage,V_O			±6.0	Volts	R_L=3.9kΩ
Differential Output, V_T	±2.0		±5.0	Volts	R_L=100Ω
	0.5V_O		0.67V_O	Volts	T_A @ +25°C
Balance			±0.4	Volts	$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$
Offset			+3.0	Volts	
Short Circuit Current			±150	mA	V_{out} = 0V
Power Off Current			±100	µA	V_{cc} = 0V, V_{out} = ±0.25V
Transition Time		20	40	ns	Rise/fall time, 10%-90%
Max. Transmission Rate	10			Mbps	R_L=100Ω; Figure 3a
Propagation Delay					T_A @ 25°C & V_{CC} = +5V only
t_{PHL}	50	80	100	ns	Figure 3a and 5;
t_{PLH}	50	80	100	ns	R_{DIFF}=100Ω
Differential Driver Skew		20	40	ns	$\lvert t_{PHL} - t_{PLH} \rvert$; T_A @ +25°C
RS-422 RECEIVER (V.11)					
TTL Output Levels					
V_{OL}			0.4	Volts	
V_{OH}	2.4			Volts	
Input					
HIGH Threshold	+0.2		+6.0	Volts	(a)-(b)
LOW Threshold	–6.0		–0.2	Volts	(a)-(b)
Common Mode Range	–7.0		+7.0	Volts	
HIGH Input Current					Refer to Rec. input graph
LOW Input Current					Refer to Rec. input graph
Receiver Sensitivity			±0.3	Volts	V_{CM} = +7V to –7V
Input Impedance	4			kΩ	V_{IN} = +10V to –10V
Max. Transmission Rate	10			Mbps	
Propagation Delay					T_A @ 25°C & V_{CC} = +5V only
t_{PHL}	80	110	180	ns	Figure 3a and 7; A is invert-
t_{PLH}	80	110	180	ns	ing and B is non-inverting.
Differential Receiver Skew		30		ns	$\lvert t_{PHL} - t_{PLH} \rvert$; T_A @ +25°C
RS-232 DRIVER (V.28)					
TTL Input Level					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	

SPECIFICATIONS (Continued)

T_A = +25°C and V_{CC} = +5.0V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-232 DRIVER (V.28)					
Outputs					
HIGH Level Output	+5.0		+15	Volts	R_L=3kΩ, V_{IN}=0.8V
LOW Level Output	–15.0		–5.0	Volts	R_L=3kΩ, V_{IN}=2.0V
Open Circuit Voltage	–15		+15	Volts	
Short Circuit Current			±100	mA	V_{OUT} = 0V
Power Off Impedance	300			Ω	V_{cc} = 0V, V_{out} = ±2.0V
Slew Rate			30	V/µs	R_L=3kΩ, C_L= 50pF V_{CC} = +5.0V, T_A @ +25°C
Transition Time			1.56	µs	R_L=3kΩ, C_L=2500pF ; between ±3V, T_A @ +25°C
Max. Transmission Rate	120	230.4		kbps	R_L=3kΩ, C_L=2500pF
Propagation Delay					T_A @ 25°C & V_{CC} = +5V only
t_{PHL}	0.5	1	4	µs	Measured from 1.5V of V_{IN}
t_{PLH}	0.5	1	4	µs	to 50% of V_{OUT}; R_L=3kΩ
RS-232 RECEIVER (V.28)					
TTL Output Levels					
V_{OL}			0.4	Volts	
V_{OH}	2.4			Volts	
Input					
HIGH Threshold		1.7	3.0	Volts	
LOW Threshold	0.8	1.2		Volts	
Receiver Open Circuit Bias			+2.0	Volts	
Input Impedance	3	5	7	kΩ	V_{IN} = +15V to –15V
Max. Transmission Rate	120	230.4		kbps	
Propagation Delay					T_A @ 25°C & V_{CC} = +5V only
t_{PHL}	0.05	0.25	1	µs	Measured from 50% of V_{IN}
t_{PLH}	0.05	0.25	1	µs	to 1.5V of V_{OUT}.
RS-423 DRIVER (V.10)					
TTL Input Levels					
V_{IL}			0.8	Volts	
V_{IH}	2.0			Volts	
Output					
Open Circuit Voltage, V_O	±4.0		±6.0	Volts	R_L=3.9kΩ
HIGH Level Output, V_T	+3.6		+6.0	Volts	R_L=450Ω; $V_{OUT} \geq 0.9V_{OC}$
LOW Level Output, V_T	–6.0		–3.6	Volts	R_L=450Ω; $V_{OUT} \geq 0.9V_{OC}$
	$0.9V_{OC}$			Volts	T_A =+25˚C,, V_{CC} = +5.0V
Short Circuit Current			±150	mA	V_{OUT} = 0V, V_{CC} = +5.0V
Power Off Current			±100	µA	V_{CC} = 0V, V_{OUT}= ±0.25V
Transition Time			100	ns	Rise/fall time, between ±3V
Max. Transmission Rate	120			kbps	R_L=450Ω
Propagation Delay					T_A @ 25°C & V_{CC} = +5V only
t_{PHL}	0.05	0.5	2	µs	Measured from 1.5V of V_{IN}
t_{PLH}	0.05	0.5	2	µs	to 50% of V_{OUT}; R_L=450Ω
RS-423 RECEIVER (V.10)					
TTL Output Levels					
V_{OL}			0.4	Volts	
V_{OH}	2.4			Volts	
Input					
HIGH Threshold	+0.3		+7.0	Volts	
LOW Threshold	–7.0		–0.3	Volts	
HIGH Input Current					Refer to Rec. input graph
LOW Input Current					Refer to Rec. input graph
Receiver Sensitivity			±0.3	Volts	V_{CM} = +7V to –7V
Input Impedance	4			kΩ	V_{IN} = +10V to –10V
Max. Transmission Rate	120			kbps	

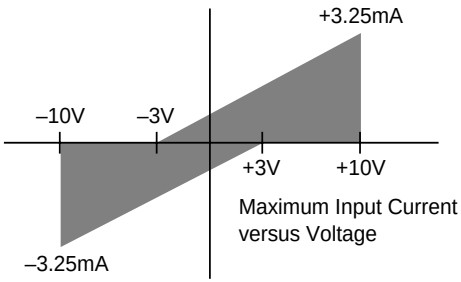
SPECIFICATIONS (Continued)

T_A = +25°C and V_{CC} = +5.0V unless otherwise noted.

	MIN.	TYP.	MAX.	UNITS	CONDITIONS
RS-423 RECEIVER (V.10)					
Propagation Delay					T_A @ 25°C & V_{CC} = +5V only
t_{PHL}	0.05	0.2	1	µs	Measured from 50% of V_{IN}
t_{PLH}	0.05	0.2	1	µs	to 1.5V of V_{OUT}
POWER REQUIREMENTS					
V_{CC}	4.75	5.00	5.25	Volts	
I_{CC} (no interface selected)		30		mA	V_{CC} =5.0V
(RS-232 Mode)		140		mA	f_{IN} = 120kbps. Drivers loaded.
(RS-422 Mode)		320		mA	f_{IN} = 2Mbps. Drivers loaded.
(RS-449 Mode)		320		mA	f_{IN} = 2Mbps. Drivers loaded.
(EIA-530 Mode)		320		mA	f_{IN} = 2Mbps. Drivers loaded.
(EIA-530A Mode)		320		mA	f_{IN} = 2Mbps. Drivers loaded.
(RS-485 Mode)		370		mA	f_{IN} = 2Mbps. Drivers loaded.
(V.35 Mode)		210		mA	f_{IN} = 2Mbps. Drivers loaded.
(V.36 Mode)		310		mA	f_{IN} = 2Mbps. Drivers loaded.
ENVIRONMENTAL AND MECHANICAL					
Operating Temperature Range	0		+70	°C	
Storage Temperature Range	–65		+150	°C	
Package		80–pin QFP			

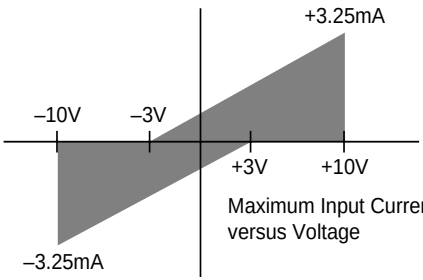
RECEIVER INPUT GRAPHS

RS-422 RECEIVER



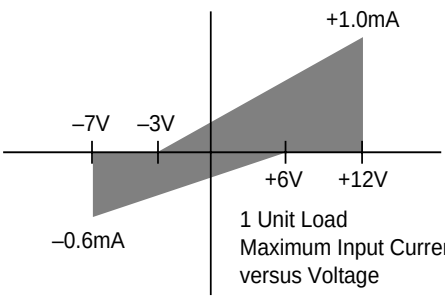
Maximum Input Current versus Voltage

RS-423 RECEIVER



Maximum Input Current versus Voltage

RS-485 RECEIVER



1 Unit Load
Maximum Input Current versus Voltage

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

V_{CC}.....+7V
Input Voltages:
Logic.....-0.3V to (V_{CC}+0.5V)
Drivers.....-0.3V to (V_{CC}+0.5V)
Receivers.....±15V
Output Voltages:
Logic.....-0.3V to (V_{CC}+0.5V)
Drivers.....±14V
Receivers.....-0.3V to (V_{CC}+0.5V)
Storage Temperature.....-65˚C to +150˚C
Power Dissipation.....2000mW

Package Derating:
$ø_{JA}$.....46 °C/W
$ø_{JC}$.....16 °C/W

STORAGE CONSIDERATIONS

Due to the relatively large package size of the 80-pin quad flat-pack, storage in a low humidity environment is preferred. Large high density plastic packages are moisture sensitive and should be stored in Dry Vapor Barrier Bags. Prior to usage, the parts should remain bagged and stored below 40°C and 60%RH. If the parts are removed from the bag, they should be used within 48 hours or stored in an environment at or below 20%RH. If the above conditions cannot be followed, the parts should be baked for four hours at 125°C in order remove moisture prior to soldering. Sipex ships the 80-pin QFP in Dry Vapor Barrier Bags with a humidity indicator card and desiccant pack. The humidity indicator should be below 30%RH.

OTHER AC CHARACTERISTICS

T_A = +70°C to 0°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
DRIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232 MODE					
t_{PZL}; Tri-state to Output LOW		0.70	5.0	µs	C_L = 100pF, Fig. 4 ; S_2 closed
t_{PZH}; Tri-state to Output HIGH		0.40	2.0	µs	C_L = 100pF, Fig. 4 ; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.20	2.0	µs	C_L = 100pF, Fig. 4 ; S_2 closed
t_{PHZ}; Output HIGH to Tri-state		0.40	2.0	µs	C_L = 100pF, Fig. 4 ; S_2 closed
RS-423 MODE					
t_{PZL}; Tri-state to Output LOW		0.15	2.0	µs	C_L = 100pF, Fig. 4 ; S_2 closed
t_{PZH}; Tri-state to Output HIGH		0.20	2.0	µs	C_L = 100pF, Fig. 4 ; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.20	2.0	µs	C_L = 100pF, Fig. 4 ; S_2 closed
t_{PHZ}; Output HIGH to Tri-state		0.15	2.0	µs	C_L = 100pF, Fig. 4 ; S_2 closed
RS-422, RS-485 MODES					
t_{PZL}; Tri-state to Output LOW		2.80	10.0	µs	C_L = 100pF, Fig. 4 & 6; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 4 & 6; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 4 & 6; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 4 & 6; S_2 closed
V.35 MODE					
t_{PZL}; Tri-state to Output LOW		2.60	10.0	µs	C_L = 100pF, Fig. 4 & 6; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 4 & 6; S_2 closed

OTHER AC CHARACTERISTICS (Continued)

T_A = +70°C to 0°C and V_{CC} = +4.75V to +5.25V unless otherwise noted.

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V.35 MODE					
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 4 & 6; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.15	2.0	µs	C_L = 15pF, Fig. 4 & 6; S_2 closed
RECEIVER DELAY TIME BETWEEN ACTIVE MODE AND TRI-STATE MODE					
RS-232 MODE					
t_{PZL}; Tri-state to Output LOW		0.12	2.0	µs	C_L = 100pF, Fig. 2 ; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 2 ; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 100pF, Fig. 2 ; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 100pF, Fig. 2 ; S_2 closed
RS-423 MODE					
t_{PZL}; Tri-state to Output LOW		0.10	2.0	µs	C_L = 100pF, Fig. 2 ; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 2 ; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 100pF, Fig. 2 ; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 100pF, Fig. 2 ; S_2 closed
RS-422/RS-485 MODES					
t_{PZL}; Tri-state to Output LOW		0.10	2.0	µs	C_L = 100pF, Fig. 2 & 8 ; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 2 & 8 ; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 2 & 8 ; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 2 & 8; S_2 closed
V.35 MODE					
t_{PZL}; Tri-state to Output LOW		0.10	2.0	µs	C_L = 100pF, Fig. 2 & 8; S_1 closed
t_{PZH}; Tri-state to Output HIGH		0.10	2.0	µs	C_L = 100pF, Fig. 2 & 8; S_2 closed
t_{PLZ}; Output LOW to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 2 & 8; S_1 closed
t_{PHZ}; Output HIGH to Tri-state		0.10	2.0	µs	C_L = 15pF, Fig. 2 & 8; S_2 closed
TRANSCEIVER TO TRANSCEIVER SKEW $[(t_{phl} - t_{plh})_{Trcvr1} - (t_{phl} - t_{plh})_{TrcvrX}]$					
RS-232 Driver		20	50	ns	V_{CC} = +5.0V, T_A @ +25°C
RS-232 Receiver		20		ns	
RS-422 Driver		20	50	ns	V_{CC} = +5.0V, T_A @ +25°C
RS-422 Receiver		20		ns	
RS-423 Driver		20	50	ns	V_{CC} = +5.0V, T_A @ +25°C
RS-423 Receiver		20		ns	
V.35 Driver		20	50	ns	V_{CC} = +5.0V, T_A @ +25°C
V.35 Receiver		20		ns	

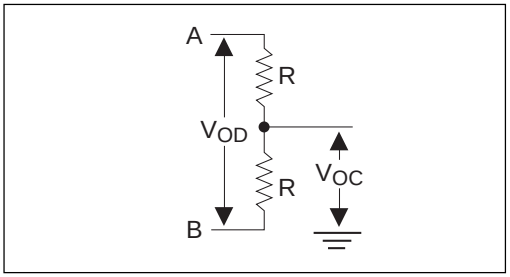


Figure 1. Driver DC Test Load Circuit

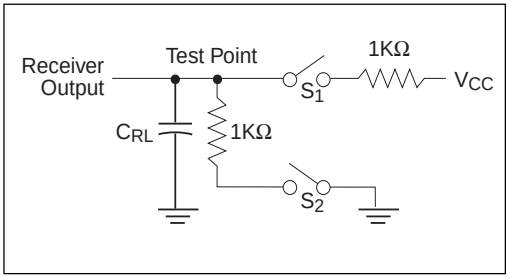


Figure 2. Receiver Timing Test Load Circuit

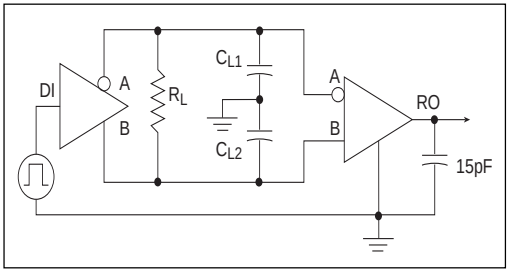


Figure 3a. Driver/Receiver Timing Test Circuit

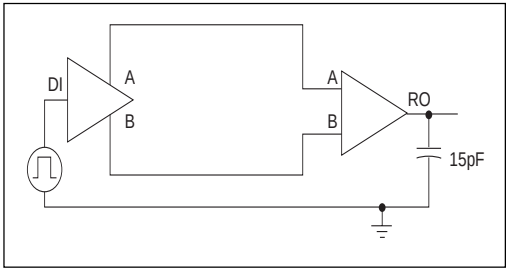


Figure 3b. Timing Test Ckt. (V.35 mode only for SP504)

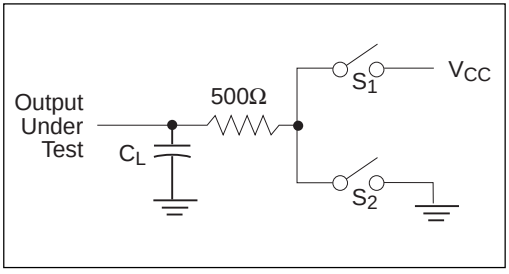


Figure 4. Driver Timing Test Load #2 Circuit

Note : Figures 3a and 3b shown above are used for evaluating maximum transmission rate. For 10Mbps transmission rate, an input signal of 5MHz is applied to the driver input. In order for a valid transmission rate, the driver output must adhere to the output electrical specifications (V_{OH} & V_{OL}) and an acceptable duty cycle for the protocol tested. The receiver outputs are checked for proper TTL/CMOS V_{OH} & V_{OL} levels and an acceptable output duty cycle.

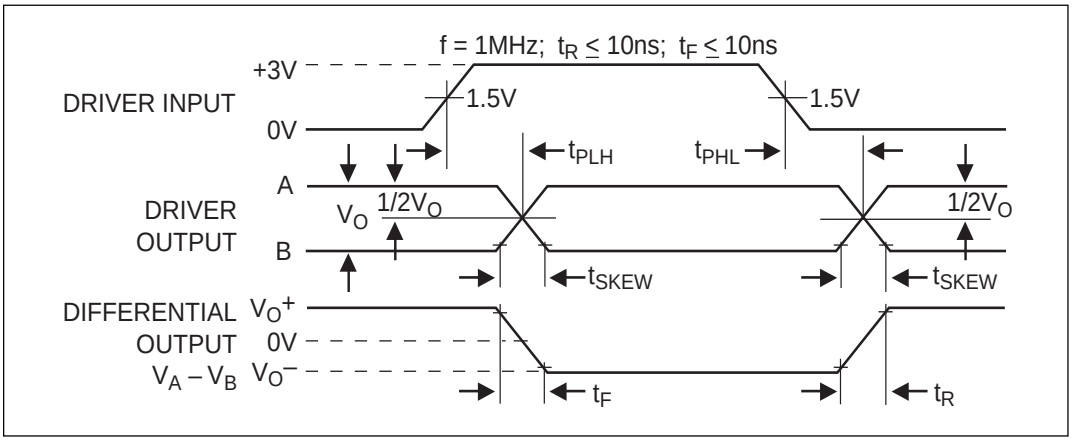


Figure 5. Driver Propagation Delays

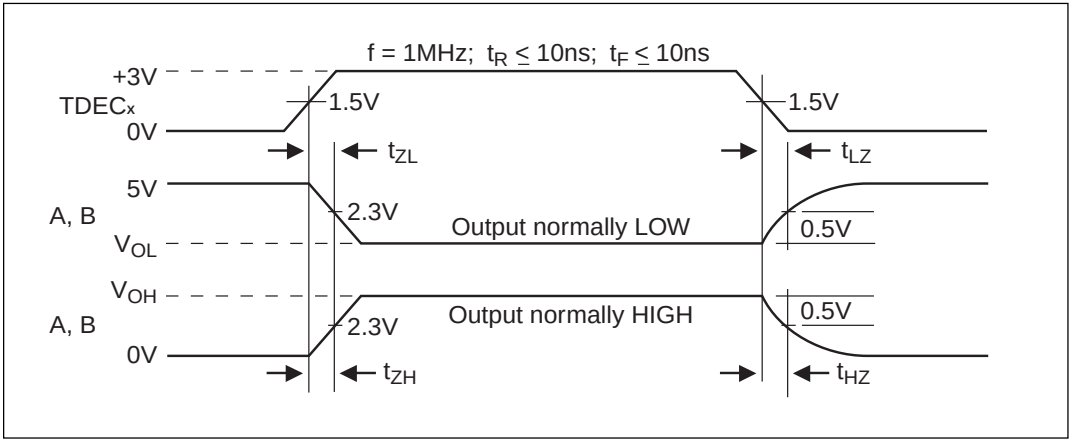


Figure 6. Driver Enable and Disable Times

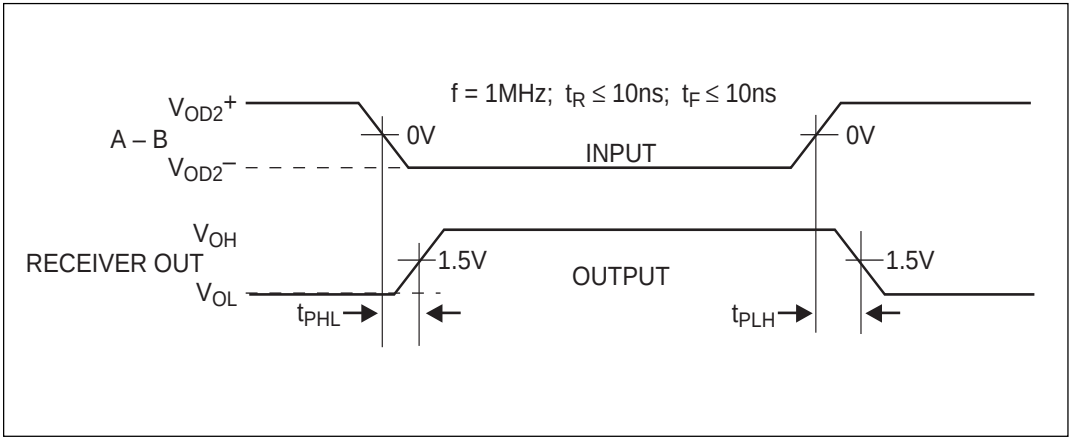


Figure 7. Receiver Propagation Delays

Note : Figures 5 and 7 shown above are corrected from the original SP504 datahseet. Both figures were incorrect on the original datasheet where the driver output from Figure 5 and the receiver output from Figure 7 are inverted signals.

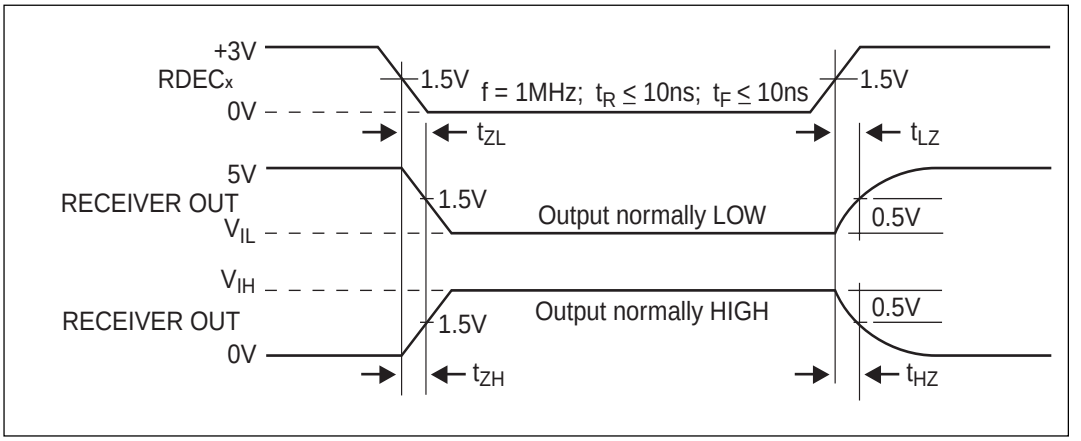


Figure 8. Receiver Enable and Disable Times

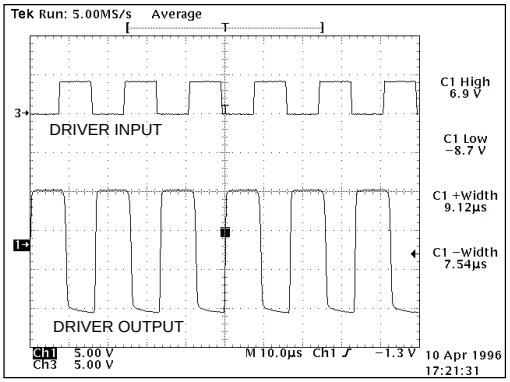


Figure 9. Typical RS-232 Driver Output Waveform

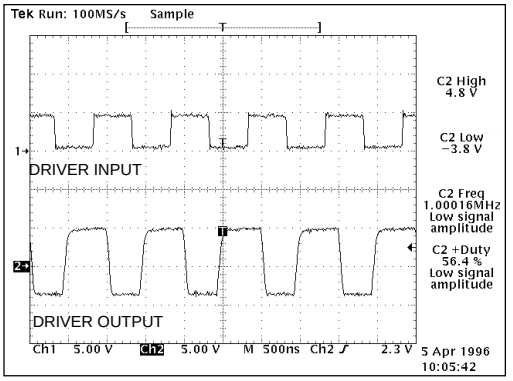


Figure 10. Typical RS-423 Driver Output Waveform

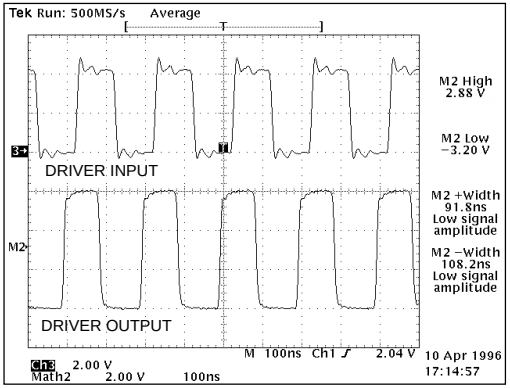


Figure 11. Typical RS-422/485 Driver Output Waveform

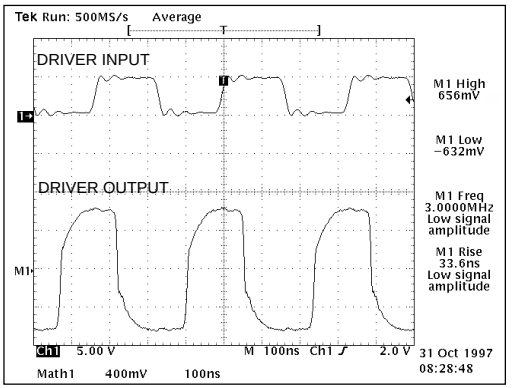
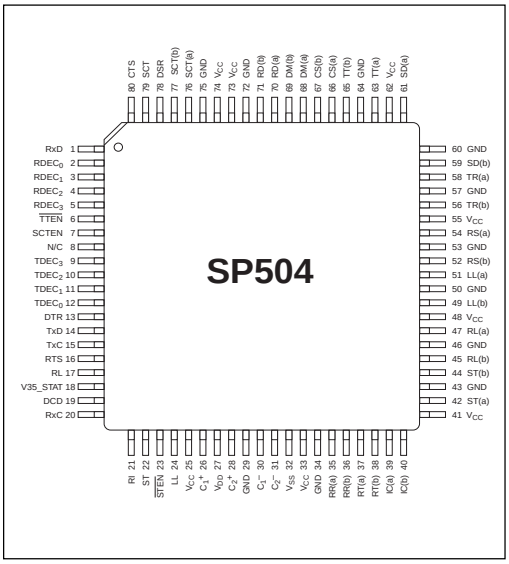


Figure 12. Typical V.35 Driver Output Waveform

PINOUT…



PIN ASSIGNMENTS…

CLOCK AND DATA GROUP

Pin 1 — RxD — Receive Data; TTL output, sourced from RD(a) and RD(b) inputs.

Pin 14 — TxD — TTL input ; transmit data source for SD(a) and SD(b) outputs.

Pin 15 — TxC — Transmit Clock; TTL input for TT driver outputs.

Pin 20 — RxC — Receive Clock; TTL output sourced from RT(a) and RT(b) inputs.

Pin 22 — ST — Send Timing; TTL input; source for ST(a) and ST(b) outputs.

Pin 37 — RT(a) — Receive Timing; analog input, inverted; source for RxC.

Pin 38 — RT(b) — Receive Timing; analog input, non-inverted; source for RxC.

Pin 42 — ST(a) — Send Timing; analog output, inverted; sourced from ST.

Pin 44 — ST(b) — Send Timing; analog output, non-inverted; sourced from ST.

Pin 59 — SD(b) — Analog Out — Send data, non-inverted; sourced from TxD.

Pin 61 — SD(a) — Analog Out — Send data, inverted; sourced from TxD.

Pin 63 — TT(a) — Analog Out — Terminal Timing, inverted; sourced from TxC

Pin 65 — TT(b) — Analog Out — Terminal Timing, non–inverted; sourced from TxC.

Pin 70 — RD(a) — Receive Data, analog input; inverted; source for RxD.

Pin 71 — RD(b) — Receive Data; analog input; non-inverted; source for RxD.

Pin 76 — SCT(a) — Serial Clock Transmit; analog input, inverted; source for SCT.

Pin 77 — SCT(b) — Serial Clock Transmit: analog input, non–inverted; source for SCT

Pin 79 — SCT — Serial Clock Transmit; TTL output; sources from SCT(a) and SCT(b) inputs.

CONTROL LINE GROUP

Pin 13 — DTR — Data Terminal Ready; TTL input; source for TR(a) and TR(b) outputs.

Pin 16 — RTS — Ready To Send; TTL input; source for RS(a) and RS(b) outputs.

Pin 17 — RL — Remote Loopback; TTL input; source for RL(a) and RL(b) outputs.

Pin 18 — V35_STAT — V.35 Status; TTL output; outputs logic high when in V.35 mode.

Pin 19 — DCD— Data Carrier Detect; TTL output; sourced from RR(a) and RR(b) inputs.

Pin 21 — RI — Ring Indicate; TTL output; sourced from IC(a) and IC(b) inputs.

Pin 24 — LL — Local Loopback; TTL input; source for LL(a) and LL(b) outputs.

Pin 35 — RR(a)— Receiver Ready; analog input, inverted; source for DCD.

Pin 36 — RR(b)— Receiver Ready; analog input, non-inverted; source for DCD.

Pin 39 — IC(a)— Incoming Call; analog input, inverted; source for RI.

Pin 40 — IC(b)— Incoming Call; analog input,non-inverted; source for RI.

Pin 45 — RL(b) — Remote Loopback; analog output, non-inverted; sourced from RL.

Pin 47 — RL(a) — Remote Loopback; analog output inverted; sourced from RL.

Pin 49— LL(b) — Local Loopback; analog output, non-inverted; sourced from LL.

Pin 51 — LL(a) — Local Loopback; analog output, inverted; sourced from LL.

Pin 52 — RS(b) — Ready To Send; analog output, non-inverted; sourced from RTS.

Pin 54 — RS(a) — Ready To Send; analog output, inverted; sourced from RTS.

Pin 56 — TR(b) — Terminal Ready; analog output, non-inverted; sourced from DTR.

Pin 58 — TR(a) — Terminal Ready; analog output, inverted; sourced from DTR.

Pin 66 — CS(a)— Clear To Send; analog input, inverted; source for CTS.

Pin 67 — CS(b)— Clear To Send; analog input, non-inverted; source for CTS.

Pin 68 — DM(a)— Data Mode; analog input, inverted; source for DSR.

Pin 69 — DM(b)— Data Mode; analog input, non-inverted; source for DSR

Pin 78 — DSR— Data Set Ready; TTL output; sourced from DM(a), DM(b) inputs.

Pin 80 — CTS— Clear To Send; TTL output; sourced from CS(a) and CS(b) inputs.

CONTROL REGISTERS

Pins 2–5 — $RDEC_0$ – $RDEC_3$ — Receiver decode register; configures receiver modes; TTL inputs.

Pin 6 — $\overline{TTEN}$ — Enables TT driver, active low; TTL input.

Pin 7 — SCTEN — Enables SCT receiver; active high; TTL input.

Pins 12–9 — $TDEC_0$ – $TDEC_3$ — Transmitter decode register; configures transmitter modes; TTL inputs.

Pin 23 — $\overline{STEN}$ — Enables ST driver; active low; TTL input.

POWER SUPPLIES

Pins 25, 33, 41, 48, 55, 62, 73, 74 — V_{CC} — +5V input.

Pins 29, 34, 43, 46, 50, 53, 57, 60, 64, 72, 75 — GND — Ground.

Pin 27 — V_{DD} +10V Charge Pump Capacitor — Connects from V_{DD} to V_{CC}. Suggested capacitor size is 22µF, 16V.

Pin 32 — V_{SS} –10V Charge Pump Capacitor — Connects from ground to V_{SS}. Suggested capacitor size is 22µF, 16V.

Pins 26 and 30 — C_1^+ and C_1^- — Charge Pump Capacitor — Connects from C_1^+ to C_1^-. Suggested capacitor size is 22µF, 16V.

Pins 28 and 31 — C_2^+ and C_2^- — Charge Pump Capacitor — Connects from C_2^+ to C_2^-. Suggested capacitor size is 22µF, 16V.

NOTE: NC pins should be left floating; internal signals may be present.

FEATURES…

The **SP504** is a highly integrated serial transceiver that allows software control of its interface modes. Similar to the SP503, the **SP504** offers the same hardware interface modes for RS-232 (V.28), RS-422A (V.11), RS-449, RS-485, V.35, EIA-530 and includes V.36 and EIA-530A. The interface mode selection is done via an 8–bit switch; four (4) bits control the drivers and four (4) bits control the receivers. The **SP504** is fabricated using low power BiCMOS process technology, and incorporates a **Sipex** patented (5,306,954) charge pump allowing +5V only operation. Each device is packaged in an 80–pin JEDEC Quad FlatPack package.

The **SP504** is ideally suited for wide area network connectivity based on the interface modes offered and the driver and receiver configurations. The **SP504** has seven (7) independent drivers and seven (7) independent receivers. In V.35 mode, the **SP504** includes the necessary components and termination resistors internal within the device for compliant V.35 operation.

THEORY OF OPERATION

The **SP504** is made up of five separate circuit blocks — the charge pump, drivers, receivers, decoder and switching array. Each of these circuit blocks is described in more detail below.

Charge–Pump

The **SP504**'s charge pump design is based on the SP503 where **Sipex**'s patented charge pump design (5,306,954) uses a four–phase voltage shifting technique to attain symmetrical ±10V power supplies. In addition, the **SP504** charge pump incorporates a "programmable" feature that produces an output of ±10V or ±5V for V_{SS} and V_{DD} depending on the mode of operation. The charge pump still requires external capacitors to store the charge. *Figure 17a* shows the waveform found on the positive side of capacitor C2, and *Figure 17b* shows the negative side of capcitor C2. There is a free–running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

The **SP504** charge pump is used for RS-232 where the output voltage swing is typically ±10V and also used for RS-423. However, RS-423 requires the voltage swing on the driver output be between ±4V to ±6V during an open circuit (no load). The charge pump would need to be regulated down from ±10V to ±5V. A typical ±10V charge pump would require external clamping such as 5V zener diodes on V_{DD} and V_{SS} to ground. The ±5V output has symmetrical levels as in the ±10V output. The ±5V is used in the following modes where RS-423 levels are used: RS-449, EIA-530, EIA-530A and V.36.

Phase 1 (±10V)

— V_{SS} charge storage — During this phase of the clock cycle, the positive side of capacitors C_1 and C_2 are initially charged to +5V. The C_1^+ is then switched to ground and the charge on C_1^- is transferred to C_2^-. Since C_2^+ is connected to +5V, the voltage potential across capacitor C_2 is now 10V.

Phase 1 (±5V)

— V_{SS} & V_{DD} charge storage and transfer — With the C_1 and C_2 capacitors initially charged to +5V, C_1^+ is then switched to ground and the charge on C_1^- is transferred to the V_{SS} storage capacitor. Simultaneously the C_2^- is switched to ground and the 5V charge on C_2^+ is transferred to the V_{DD} storage capacitor.

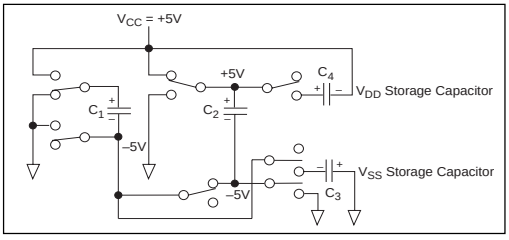


Figure 13a. Charge Pump Phase 1 for ±10V.

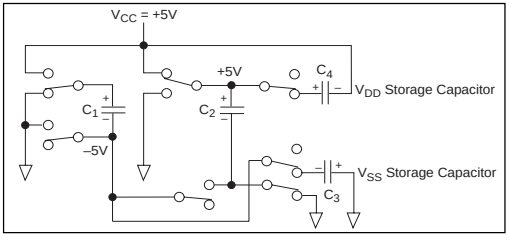


Figure 13b. Charge Pump Phase 1 for ±5V.

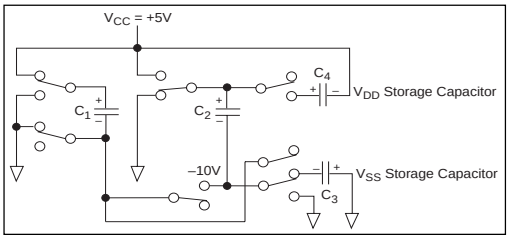


Figure 14a. Charge Pump Phase 2 for ±10V.

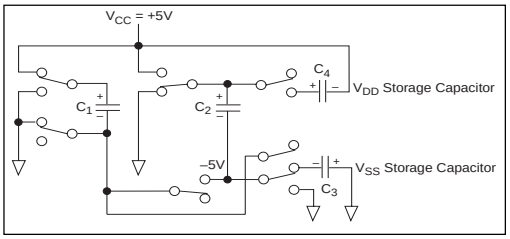


Figure 14b. Charge Pump Phase 2 for ±5V.

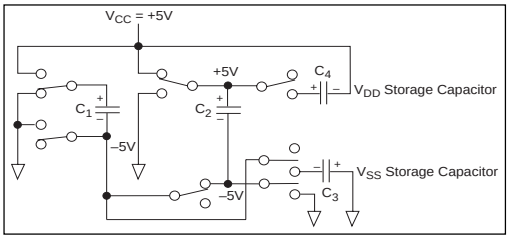


Figure 15. Charge Pump Phase 3.

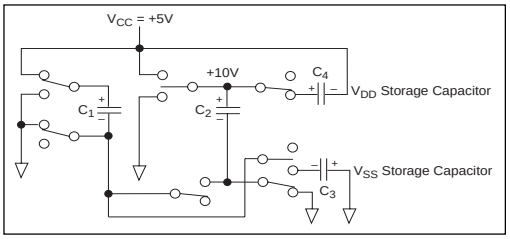


Figure 16. Charge Pump Phase 4.

Phase 2 (±10V)

— V_{SS} transfer — Phase two of the clock connects the negative terminal of C_2 to the V_{SS} storage capacitor and the positive terminal of C_2 to ground, and transfers the generated –l0V or the generated –5V to C_3. Simultaneously, the positive side of capacitor C_1 is switched to +5V and the negative side is connected to ground.

Phase 2 (±5V)

— V_{SS} & V_{DD} charge storage — C_1^+ is reconnected to V_{CC} to recharge the C_1 capacitor. C_2^+ is switched to ground and C_2^- is connected to C_3. The 5V charge from Phase 1 is now transferred to the V_{SS} storage capacitor. V_{SS} receives a continuous charge from either C_1 or C_2. With the C1 capacitor charged to 5V, the cycle begins again.

Phase 3

— V_{DD} charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C_1 produces –5V in the negative terminal of C_1, which is applied to the negative side of capacitor C_2. Since C_2^+ is at +5V, the voltage potential across C_2 is l0V. For the 5V output, C_2^+ is connected to ground so that the potential on C_2 is only +5V.

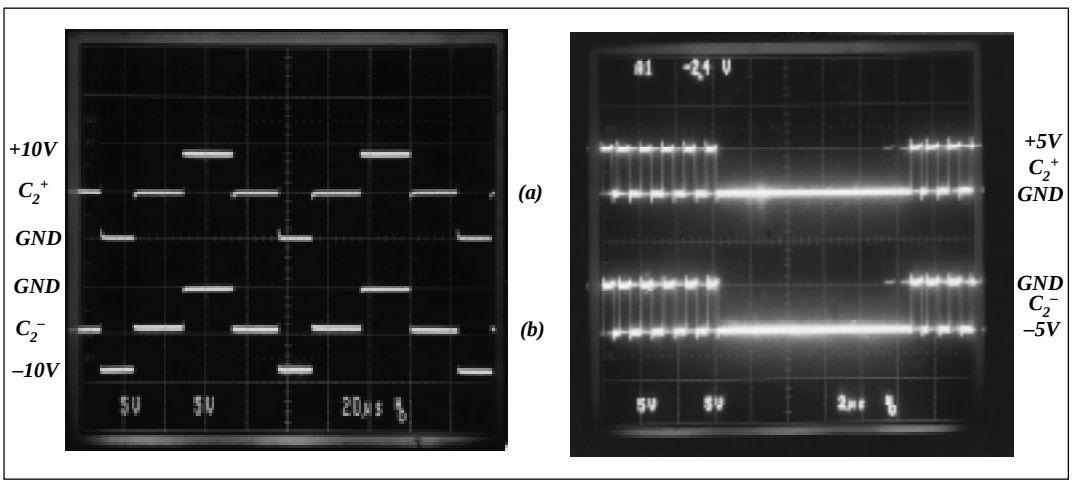


Figure 17. Charge Pump Waveforms

Since both V_{DD} and V_{SS} are separately generated from V_{CC} in a no–load condition, V_{DD} and V_{SS} will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be a minimum of 22µF with a 16V breakdown rating.

External Power Supplies

For applications that do not require +5V only, external supplies can be applied at the V+ and V^- pins. The value of the external supply voltages must be no greater than ±l0.5V. The tolerance should be ±5% from ±10V. The current drain for the supplies is used for RS-232 and RS-423 drivers. For the RS-232 driver, the current requirement will be 3.5mA per driver. The RS-423 driver worst case current drain will be 11mA per driver. Power sequencing is required for the **SP504**. The supplies must be sequenced accordingly: +10V, +5V and –10V. An external circuit would be needed for proper power supply sequencing. Consult factory for application circuitry.

Drivers

The **SP504** has seven (7) enhanced independent drivers. Control for the mode selection is done via a four–bit control word. The drivers are prearranged such that for each mode of operation, the relative position and functionality of the drivers are set up to accommodate the selected interface mode. As the mode of the drivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line signal levels. *Table 1* shows the mode of each driver in the different interface modes that can be selected.

There are four basic types of driver circuits — RS-232, RS-423, RS-485 and V.35.

The RS-232 drivers output single–ended signals with a minimum of ±5V (with 3kΩ and 2500pF loading), and can operate up to 120kbps.

The RS-232 drivers are used in RS-232 mode for all signals, and also in V.35 mode where they are used as the control line signals such as DTR and RTS.

The RS-423 drivers are also single–ended signals with a minimum voltage output of ±3.6V (with 450Ω loading) and can operate up to 120kbps. Open circuit V_{OL} and V_{OH} measurements are ±4.0V to ±6.0V. The RS-423 drivers are used in RS-449, EIA-530, EIA-530A and V.36 modes as Category II signals from each of their corresponding specifications.

The third type of driver produces a differential signal that can maintain RS-485, ±1.5V differential output levels with a worst case load of 54Ω. The signal levels and drive capability of the RS-485 drivers allow the drivers to also support RS-422 (V.11) requirements of ±2V differential output levels with 100Ω loads. The RS-422 drivers are used in RS-449, EIA-530, EIA-530A and V.36 modes as Category I signals which are used for clock and data.

The fourth type of driver is the V.35 driver. V.35 levels require ±0.55V driver output signals with a load of 100Ω. The **SP504** drivers simplify existing V.35 implementations that use external termination schemes. The drivers were specifically designed to comply with the requirements of V.35 as well as the driver output impedance values of V.35. The drivers achieve the 50Ω to 150Ω source impedance. However, an external 150Ω resistor to ground must be connected to the non-inverting outputs; SD(b), ST(b), and TT(b), in order to comply with the 135Ω to 165Ω short-circuit impedance for V.35. The V.35 driver itself is disabled and transparent when the decoder is in all other modes. All of the differential drivers; RS-485, RS-422, and V.35, can operate up to 10Mbps.

The driver inputs are both TTL or CMOS compatible. Since there are no pull-up or pull-down resistors on the driver inputs, they should be tied to a known logic state in order to define the driver output.

Receivers

The **SP504** has seven (7) independent receivers which can be programmed for the different interface modes. Control for the mode selection is done via a 4–bit control word that is independent from the driver control word. The coding for the drivers and receivers is identical. Therefore, if the modes for the drivers and receivers are supposed to be identical in the application, the control lines can be tied together.

Like the drivers, the receivers are pre-arranged for the specific requirements of the interface. As the operating mode of the receivers is changed, the electrical characteristics will change to support the requirements of clock, data, and control line receivers. *Table 2* shows the mode of each receiver in the different interface modes that can be selected.

There are three basic types of receiver circuits — RS-232, RS-423, and RS-485.

The RS-232 receiver is a single–ended input with a threshold of 0.8V to 2.4V. The RS-232 receiver has an operating voltage range of ±15V and can receive signals up to 120kbps. The input sensitivity complies with EIA-RS-232 and V.28 at +3V to -3V. The input impedance is 3kΩ to 7kΩ. RS-232 receivers are used in RS-232 mode for all data, clock and control signals. They are also used in V.35 mode for control line signals such as CTS and DSR.

The RS-423 receivers are also single–ended but have an input threshold as low as ±200mV. The input impedance is guaranteed to be greater than 4kΩ, with an operating voltage range of ±7V. The RS-423 receivers can operate up to 120kbps. RS-423 receivers are used in RS-449, EIA-530, EIA-530A and V.36 modes as Category II signals as indicated by their corresponding specifications.

The third type of receiver is a differential which supports RS-485. The RS-485 receiver has an input impedance of 15kΩ and a differential threshold of ±200mV. Since the characteristics of an RS-422 (V.11) receiver are actually subsets of RS-485, the receivers for RS-422 requirements are covered by the RS-485 receivers. RS-422 receivers are used in RS-449, EIA-530, EIA-530A and V.36 as Category I signals for receiving clock, data, and some control line signals. The differential receivers can receive data up to 10Mbps.

The RS-485 receivers are also used for the V.35 mode. Unlike the older implementations of differential or V.35 receivers, the **SP504** contains an internal resistor termination network that ensures a V.35 input impedance of 100Ω (±10Ω) and a short-circuit impedance of 150Ω (±15Ω). The traditional V.35 implementations required external termination resistors to acheive the proper V.35 impedances. The internal network is connected via low on-resistance FET switches when the decoder is changed to V.35 mode. The termination network is transparent when all other modes are selected. The V.35 receivers can operate up to 10Mbps.

All receivers include a fail-safe feature that outputs a logic HIGH when the receiver inputs are open. For single-ended RS-232 receivers, there are internal 5kΩ pull-down resistors on the inputs which produces a logic HIGH ("1") at the receiver outputs. The single-ended RS-423 receivers produce a logic LOW ("0") on the output when the inputs are open. This is due to a pull-up device connected to the input. The differential receivers have the same internal pull-up device on the non-inverting input which produces a logic HIGH ("1") at the receiver output. The three differential receivers when configured in V.35 mode (RxD, RxC & SCT) do not have fail-safe because the internal termination resistor network is connected.

Decoder

The **SP504** has the ability to change the interface mode of the drivers or receivers via an 8–bit switch. The decoder for the drivers and receivers is not latched; it is merely a combinational logic switch.

The control word can be externally latched either HIGH or LOW to write the appropriate code into the **SP504**. The codes shown in *Tables 1 and 2* are the only specified, valid modes for the **SP504**. Undefined codes may represent other interface modes not specified (consult the fac-

tory for more information). The drivers are controlled with the data bits labeled $TDEC_3$–$TDEC_0$. All of the drivers can be put into tri-state mode by writing 0000 to the driver decode switch. The three drivers TxD, ST and TxC, have a 150Ω pull-down resistor to ground connected at the (b) output. This resistor is part of the V.35 driver circuitry and should be connected when in V.35 mode. Tri-state is possible for all drivers in RS-232 mode. The receivers are controlled with data bits $RDEC_3$–$RDEC_0$; the code 0000 written to the receivers will place the outputs into tri-state mode. The 0000 decoder word will override the enable control line for the one receiver (SCT).

Using the V.35_STAT Pin

The **SP504** includes a V.35 status pin where the V35_STAT pin (pin 18) is a logic HIGH ("1") when the decoder is set to V.35 mode. The pin is a logic LOW ("0") when in all other modes including tri-state (decoder set at "0000"). Pin 18 allows the user to easily add FET switches or solid state relays to connect the external 150Ω resistor for V.35 operation. V35_STAT can be connected to the gate of the FET switches or the control of the relays so that the 150Ω resistors are connected to the non-inverting output of the three V.35 drivers. The output current of the V35_STAT pin is that of a typical TTL load of –3.2mA. The electrical specifications are similar to the **SP504** receiver outputs. This feature would reduce additional logic required by older traditional methods.

NET1/NET2 Testing and Compliancy

Many system designers are required to certify their system for use in the European public network. Electrical testing is performed in adherence to the NET (Norme Européenne de Télécommunication) which specifies the ITU Series V specifications. The **SP504** adheres to all the required physical layer testing for NET1 and NET2. Consult factory for details.

SP504 Driver Mode Selection

Pin Label	Mode:	RS232	V.35	RS422	RS485	RS449	EIA530	EIA-530A	V.36
$TDEC_3$–$TDEC_0$	0000	0010	1110	0100	0101	1100	1101	1111	0110
SD(a)	tri-state	V.28	V.35–	V.11–	RS485–	V.11–	V.11–	V.11–	V.11–
SD(b)	tri-state	tri-state	V.35+	V.11+	RS485+	V.11+	V.11+	V.11+	V.11+
TR(a)	tri-state	V.28	V.28	V.11–	RS485–	V.11–	V.11–	V.10	V.10
TR(b)	tri-state	tri-state	tri-state	V.11+	RS485+	V.11+	V.11+	tri-state	tri-state
RS(a)	tri-state	V.28	V.28	V.11–	RS485–	V.11–	V.11–	V.11–	V.10
RS(b)	tri-state	tri-state	tri-state	V.11+	RS485+	V.11+	V.11+	V.11+	tri-state
RL(a)	tri-state	V.28	V.28	V.11–	RS485–	V.10	V.10	V.11–	V.10
RL(b)	tri-state	tri-state	tri-state	V.11+	RS485+	tri-state	tri-state	V.11+	tri-state
LL(a)	tri-state	V.28	V.28	V.11–	RS485–	V.10	V.10	V.10	V.10
LL(b)	tri-state	tri-state	tri-state	V.11+	RS485+	tri-state	tri-state	tri-state	tri-state
ST(a)	tri-state	V.28	V.35–	V.11–	RS485–	V.11–	V.11–	V.11–	V.11–
ST(b)	tri-state	tri-state	V.35+	V.11+	RS485+	V.11+	V.11+	V.11+	V.11+
TT(a)	tri-state	V.28	V.35–	V.11–	RS485–	V.11–	V.11–	V.11–	V.11–
TT(b)	tri-state	tri-state	V.35+	V.11+	RS485+	V.11+	V.11+	V.11+	V.11+

Table 1. Driver Mode Selection

SP504 Receiver Mode Selection

Pin Label	Mode:	RS232	V.35	RS422	RS485	RS449	EIA530	EIA-530A	V.36
$RDEC_3$–$RDEC_0$	0000	0010	1110	0100	0101	1100	1101	1111	0110
RD(a)	>12kΩ to GND	V.28	V.35–	V.11–	RS485–	V.11–	V.11–	V.11–	V.11–
RD(b)	>12kΩ to GND	>12kΩ to GND	V.35+	V.11+	RS485+	V.11+	V.11+	V.11+	V.11+
RT(a)	>12kΩ to GND	V.28	V.35–	V.11–	RS485–	V.11–	V.11–	V.11–	V.11–
RT(b)	>12kΩ to GND	>12kΩ to GND	V.35+	V.11+	RS485+	V.11+	V.11+	V.11+	V.11+
CS(a)	>12kΩ to GND	V.28	V.28	V.11–	RS485–	V.11–	V.11–	V.11–	V.10
CS(b)	>12kΩ to GND	>12kΩ to GND	>12kΩ to GND	V.11+	RS485+	V.11+	V.11+	V.11+	>12kΩ to GND
DM(a)	>12kΩ to GND	V.28	V.28	V.11–	RS485–	V.11–	V.11–	V.10	V.10
DM(b)	>12kΩ to GND	>12kΩ to GND	>12kΩ to GND	V.11+	RS485+	V.11+	V.11+	>12kΩ to GND	>12kΩ to GND
RR(a)	>12kΩ to GND	V.28	V.28	V.11–	RS485–	V.11–	V.11–	V.11–	V.10
RR(b)	>12kΩ to GND	>12kΩ to GND	>12kΩ to GND	V.11+	RS485+	V.11+	V.11+	V.11+	>12kΩ to GND
IC(a)	>12kΩ to GND	V.28	V.28	V.11–	RS485–	V.10	V.10	V.10	V.10
IC(b)	>12kΩ to GND	>12kΩ to GND	>12kΩ to GND	V.11+	RS485+	>12kΩ to GND	>12kΩ to GND	>12kΩ to GND	>12kΩ to GND
SCT(a)	>12kΩ to GND	V.28	V.35–	V.11–	RS485–	V.11–	V.11–	V.11–	V.11–
SCT(b)	>12kΩ to GND	>12kΩ to GND	V.35+	V.11+	RS485+	V.11+	V.11+	V.11+	V.11+

Table 2. Receiver Mode Selection

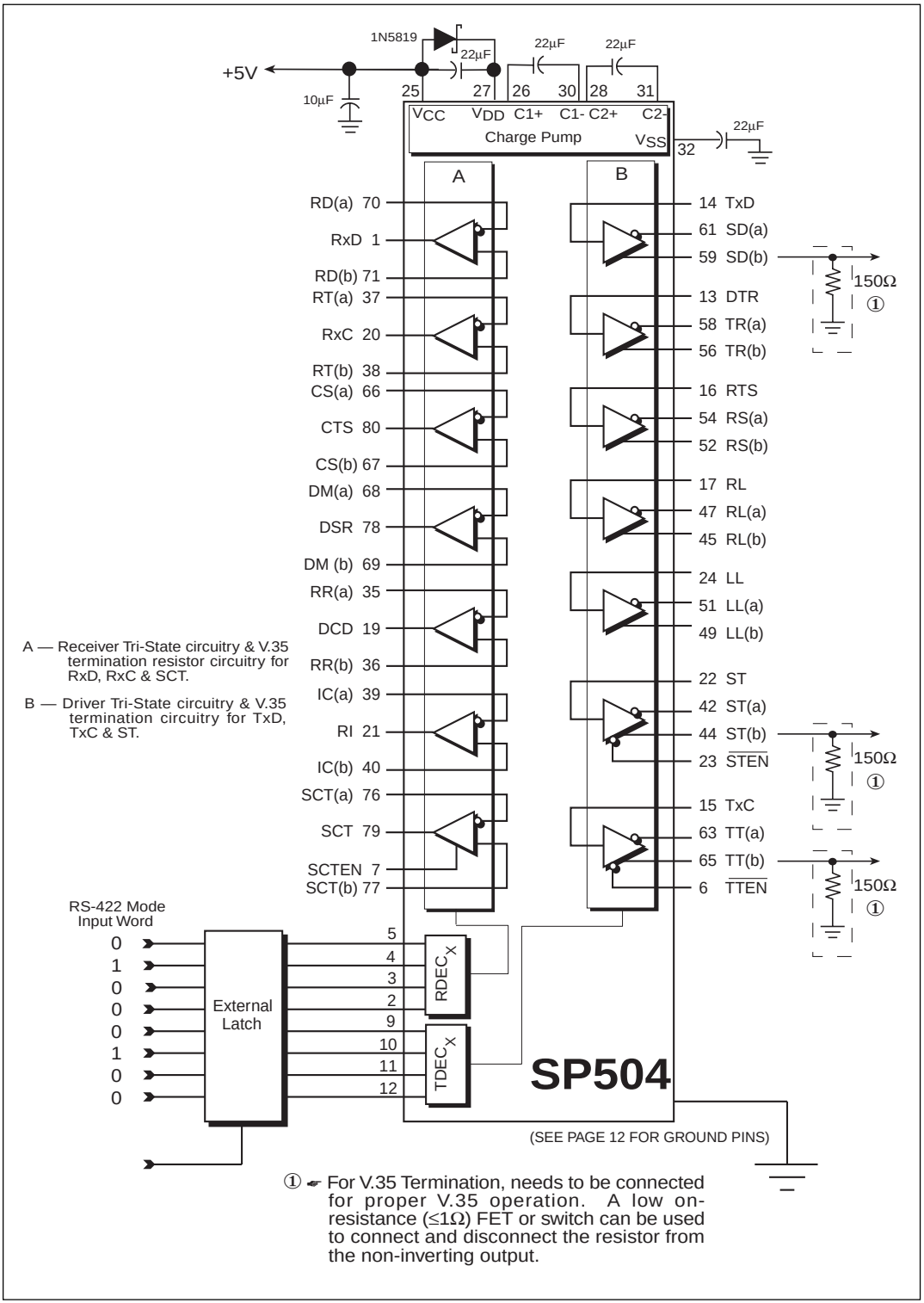
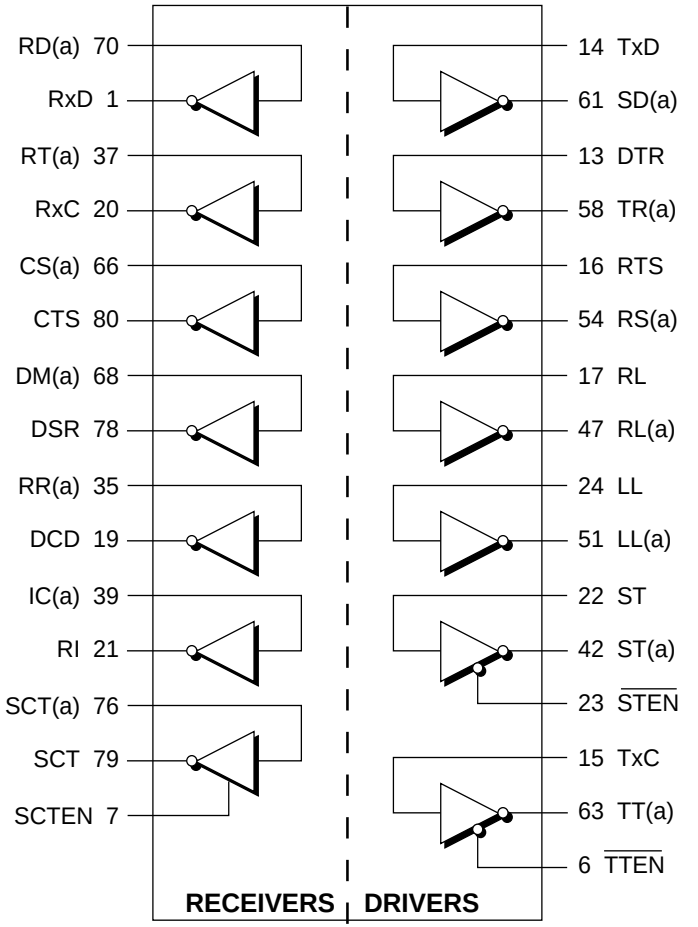


Figure 18. Typical Operation Circuit

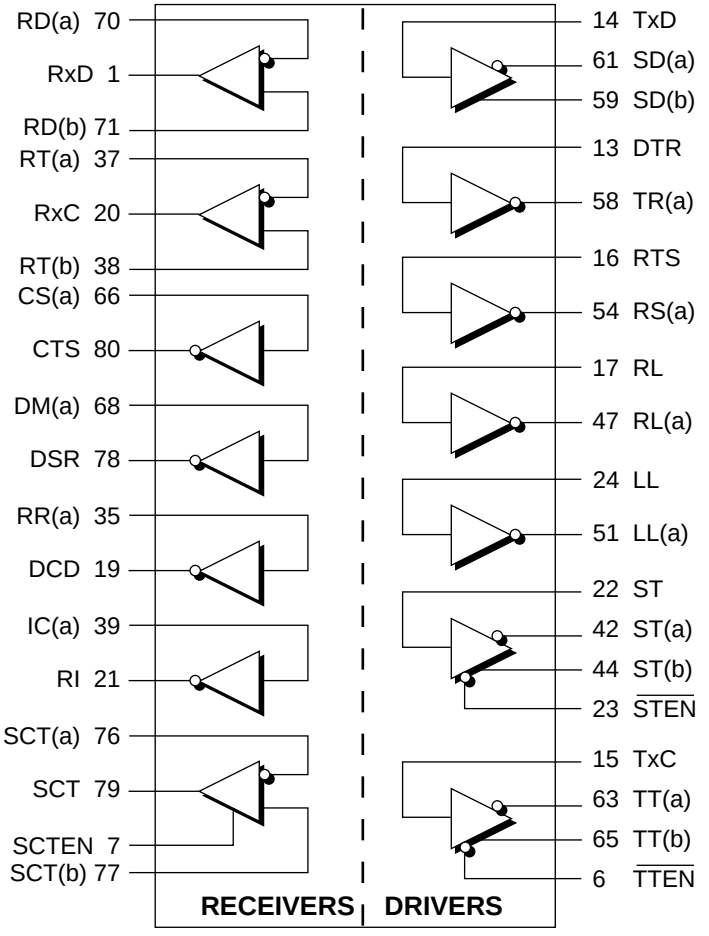
MODE: RS-232							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	0	1	0	0	0	1	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 19. Mode Diagram — RS-232

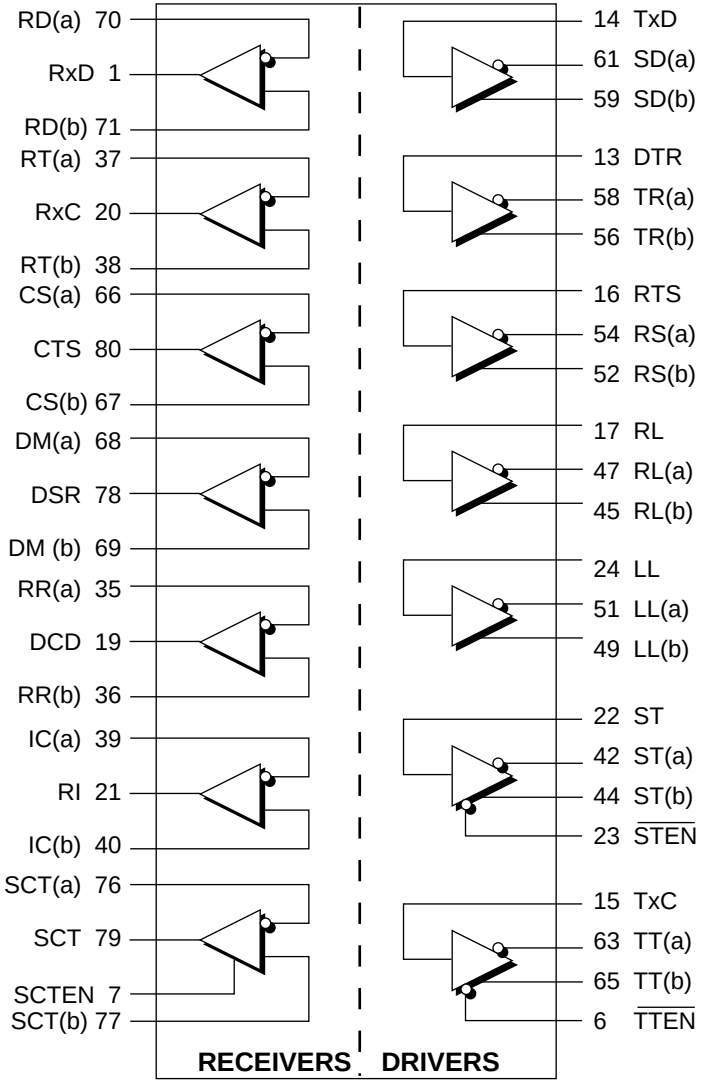
MODE: V.35							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	1	0	1	1	1	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 20. Mode Diagram — V.35

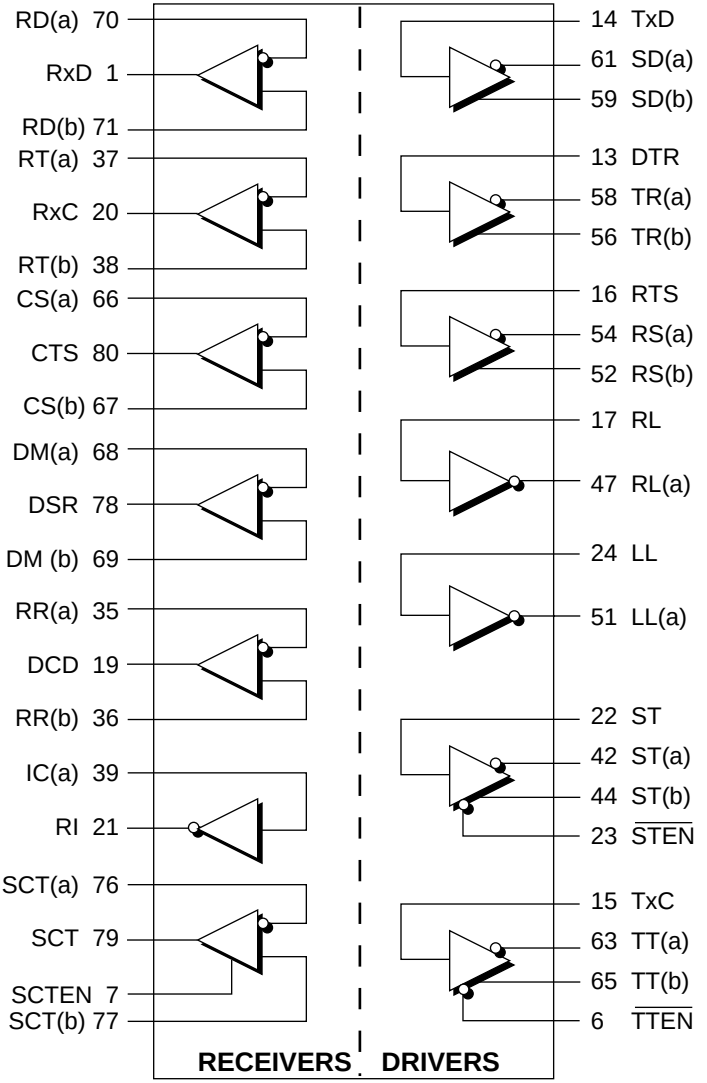
MODE: RS-422							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	0	0	0	1	0	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 21. Mode Diagram — RS-422

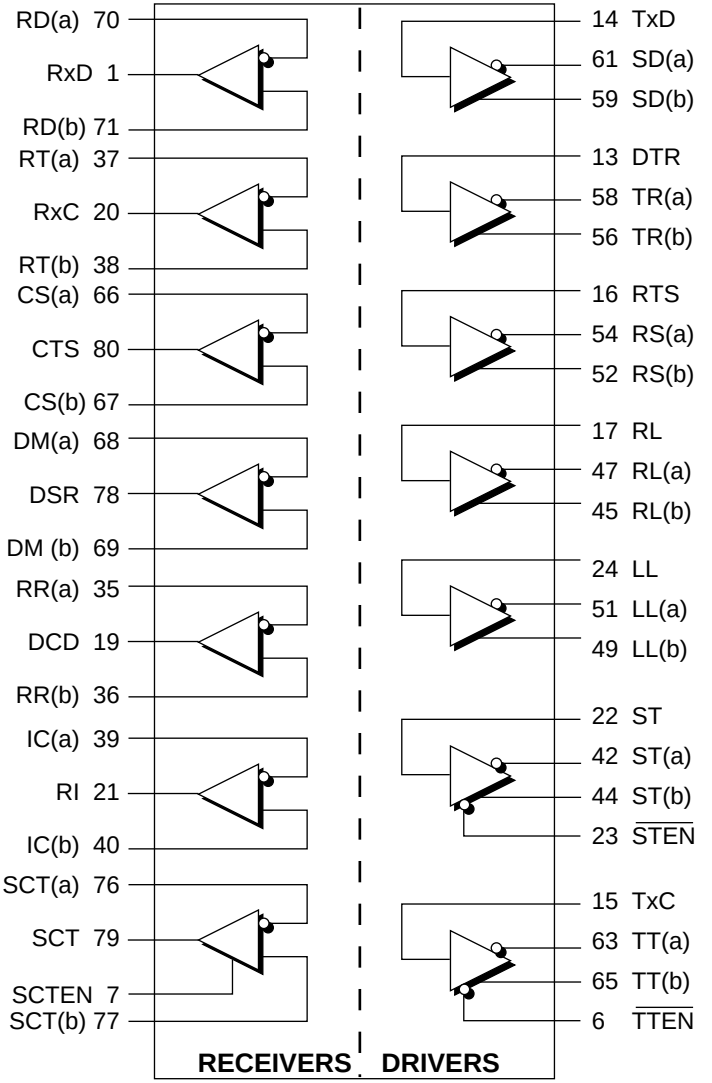
MODE: RS-449							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	0	0	1	1	0	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 22. Mode Diagram — RS-449

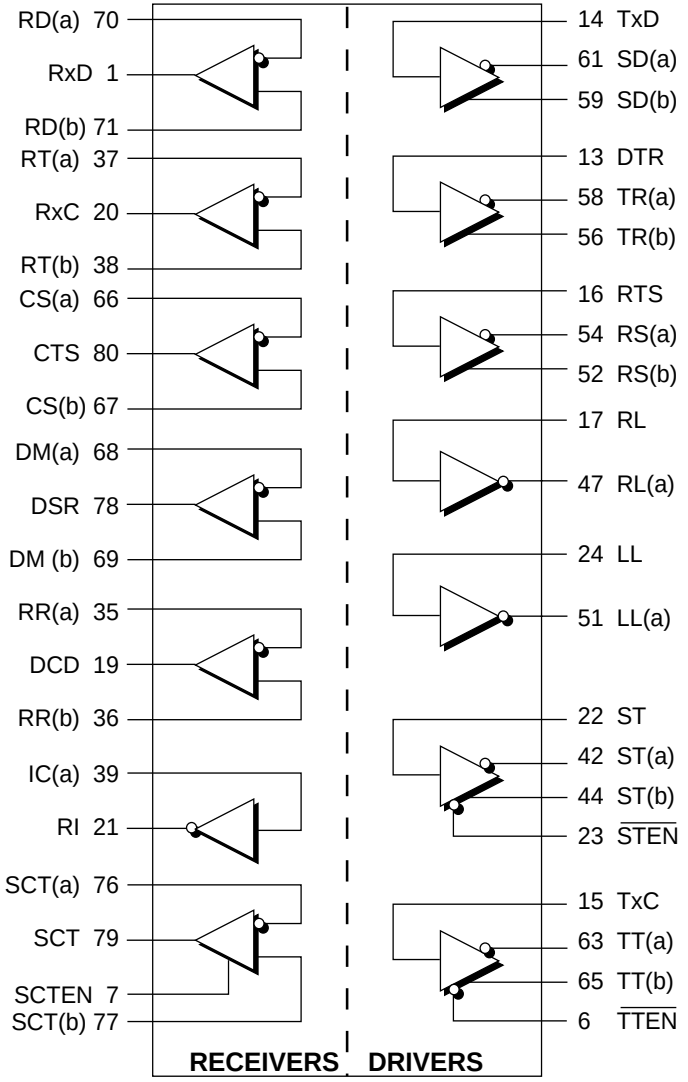
MODE: RS-485							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	0	1	0	1	0	1



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 23. Mode Diagram — RS-485

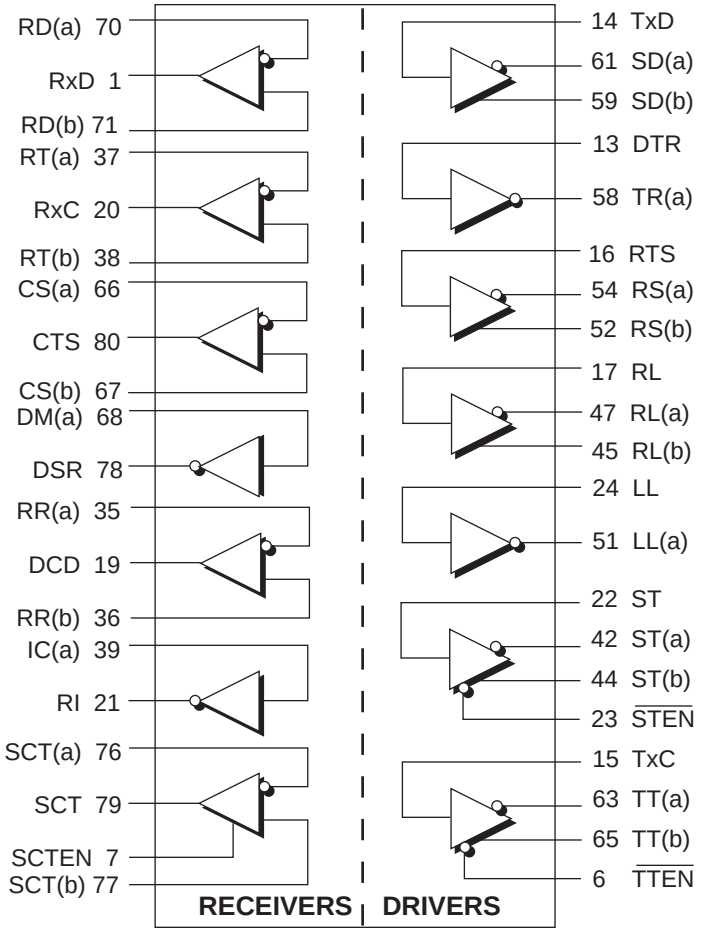
MODE: EIA-530							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	0	1	1	1	0	1



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 24. Mode Diagram — EIA-530

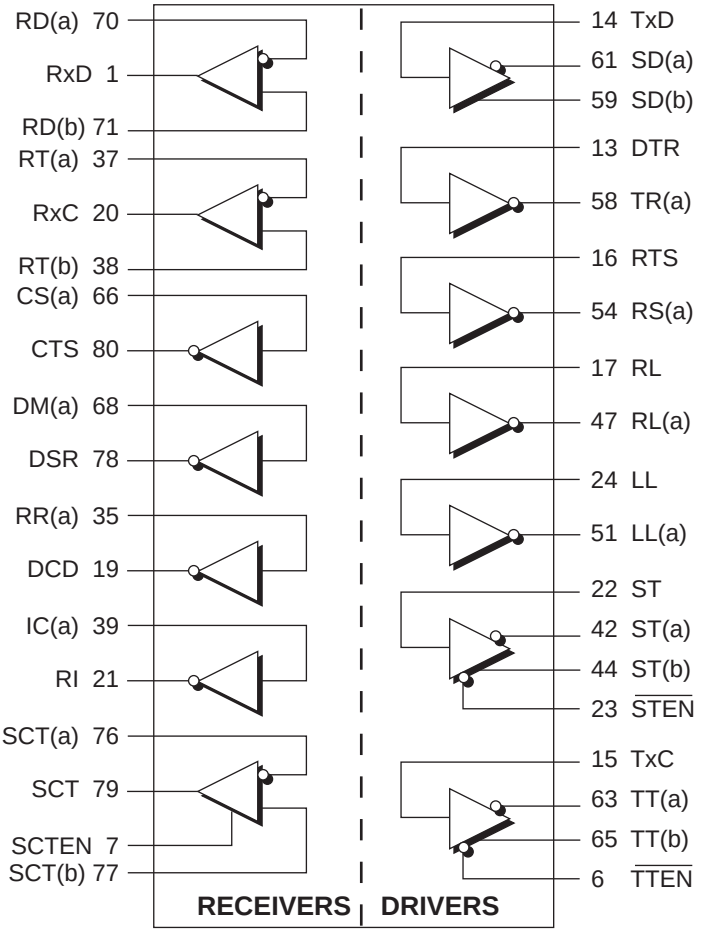
MODE: EIA-530A							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
1	1	1	1	1	1	1	1



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 25. Mode Diagram — EIA-530A

MODE: V.36							
DRIVER				RECEIVER			
$TDEC_3$	$TDEC_2$	$TDEC_1$	$TDEC_0$	$RDEC_3$	$RDEC_2$	$RDEC_1$	$RDEC_0$
0	1	1	0	0	1	1	0



$\overline{STEN}$	ST	$\overline{TTEN}$	TT	SCTEN	SCT
1	Disabled	1	Disabled	1	Enabled
0	Enabled	0	Enabled	0	Disabled

Figure 26. Mode Diagram — V.36

ADDITIONAL TRANSCEIVERS WITH THE SP504

Serial ports usually can have two data signals (SD, RD), three clock signals (TT, ST, RT), and at least eight control signals (CS, RS, etc.). EIA-RS-449 contains twenty six signal types for a DB-37 connector. A DB-37 serial port design may require thirteen drivers and fourteen receivers[1]. Although many applications do not use all these signals, some applications may need to support extra functions such as diagnostics. The **SP504** supports enough transceivers for the primary channels of data, clock and control signals. Configuring LL, RL and TM would require two additional drivers and one receiver if designing for a DTE (one driver and two receivers for a DCE).

A programmable transceiver such as the SP332 is a convenient solution in a design that requires extra single ended or differential drivers/receivers. As shown in *Figure 28*, the SP332 can be configured to four different variations.

The SP332 in *Figure 29* is configured for two single-ended drivers and one diffferential receiver. For a DTE design, the two drivers are used for LL and RL signals and the receiver is used for the TM signal. This configuration was selected because the two RS-232 drivers can be used for RS-423 by connecting a zener clamping diode to ground on the two driver outputs. The diodes will limit the voltage swing on the outputs so that the V_{OC} = ±4V to ±6V adheres to the RS-423 specification. The differential receiver can be easily configured to RS-423 by grounding the non-inverting input. The receiver will adhere to the RS-423 specifications.

CIRCUIT MNEMONIC	CIRCUIT NAME	CIRCUIT DIRECTION	CIRCUIT TYPE	
SG	SIGNAL GROUND	----------	COMMON	
SC	SEND COMMON	TO DCE		
RC	RECEIVE COMMON	FROM DCE		
IS	TERMINAL IN SERVICE	TO DCE	CONTROL	
IC	INCOMING CALL	FROM DCE		
TR	TERMINAL READY	TO DCE		
DM	DATA MODE	FROM DCE		
SD	SEND DATA	TO DCE	DATA	PRIMARY CHANNEL
RD	RECEIVE DATA	FROM DCE		
TT	TERMINAL TIMING	TO DCE	TIMING	
ST	SEND TIMING	FROM DCE		
RT	RECEIVE TIMING	FROM DCE		
RS	REQUEST TO SEND	TO DCE	CONTROL	
CS	CLEAR TO SEND	FROM DCE		
RR	RECEIVER READY	FROM DCE		
SQ	SIGNAL QUALITY	FROM DCE		
NS	NEW SIGNAL	TO DCE		
SF	SELECT FREQUENCY	TO DCE		
SR	SIGNAL RATE SELECTOR	TO DCE		
SI	SIGNAL RATE INDICATOR	FROM DCE		
SSD	SECONDARY SEND DATA	TO DCE	DATA	SECONDARY CHANNEL
SRD	SECONDARY RD	FROM DCE		
SRS	SECONDARY RS	TO DCE	CONTROL	
SCS	SECONDARY CS	FROM DCE		
SRR	SECONDARY RR	FROM DCE		
LL	LOCAL LOOPBACK	TO DCE	CONTROL	
RL	REMOTE LOOPBACK	TO DCE		
TM	TEST MODE	FROM DCE		
SS	SELECT STANDBY	TO DCE	CONTROL	
SB	STANDBY INDICATOR	FROM DCE		

[1] RS-449 Interchange Circuits Table

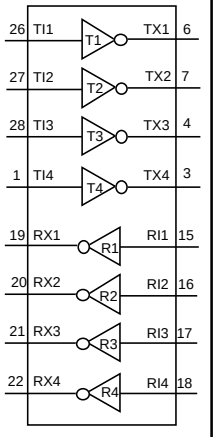
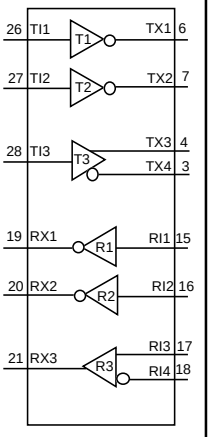
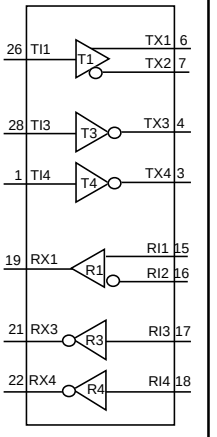
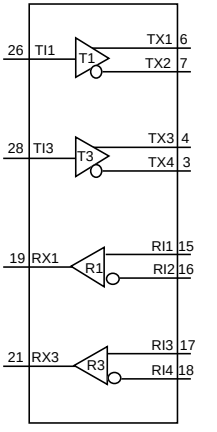
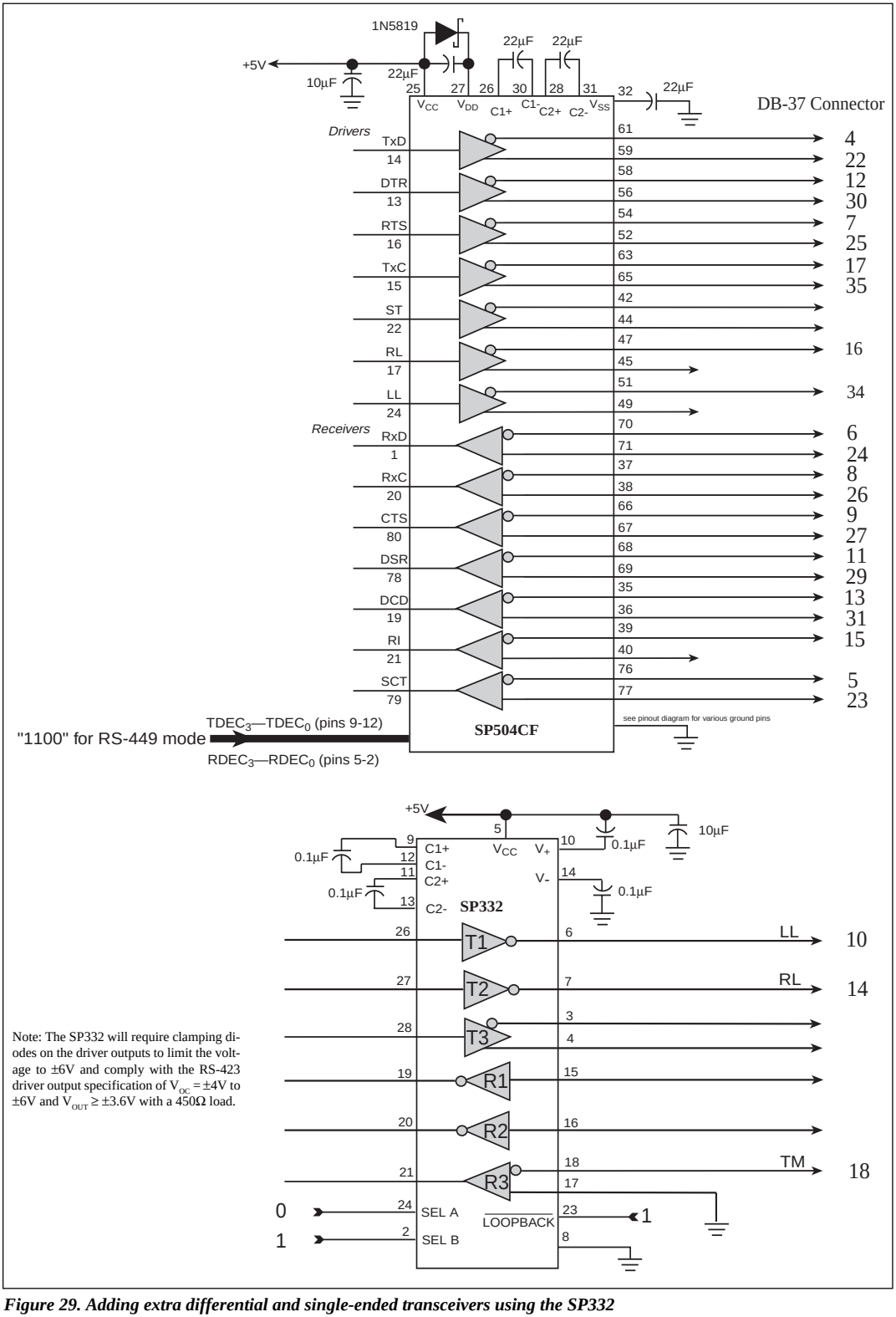
SEL A	0	0	1	1
SEL B	0	1	0	1
LOOPBACK	1	1	1	1
SHUTDOWN	0	0	0	0
				

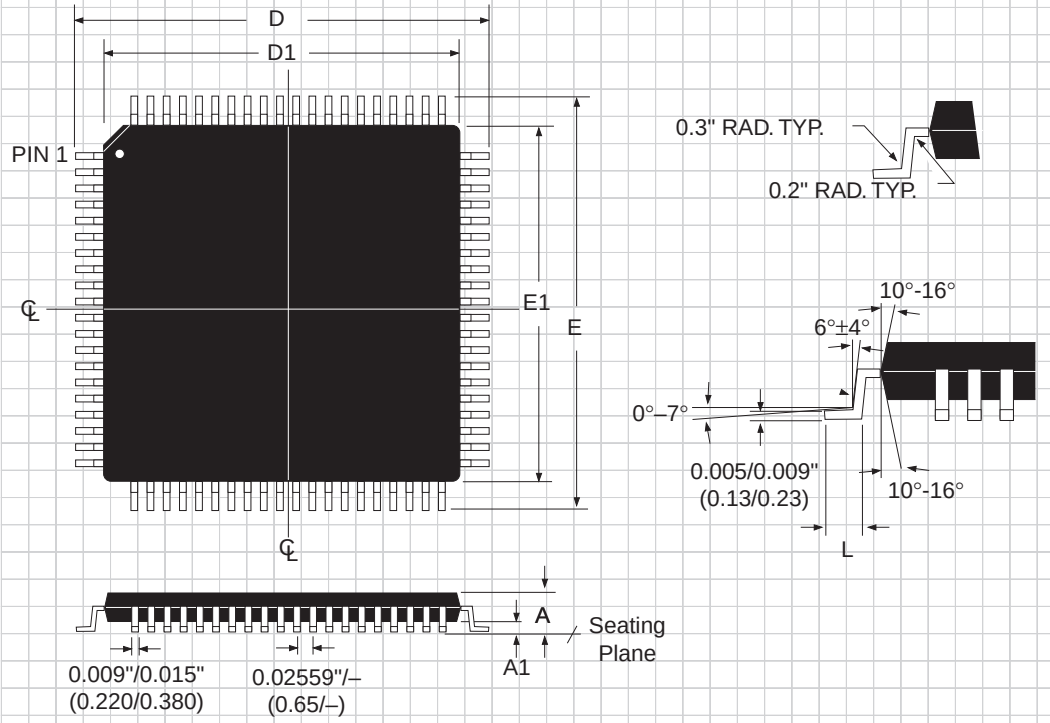
Figure 28. Mode selection for the SP332



Note: The SP332 will require clamping diodes on the driver outputs to limit the voltage to ±6V and comply with the RS-423 driver output specification of $V_{OC} = \pm 4V$ to ±6V and $V_{OUT} \geq \pm 3.6V$ with a 450Ω load.

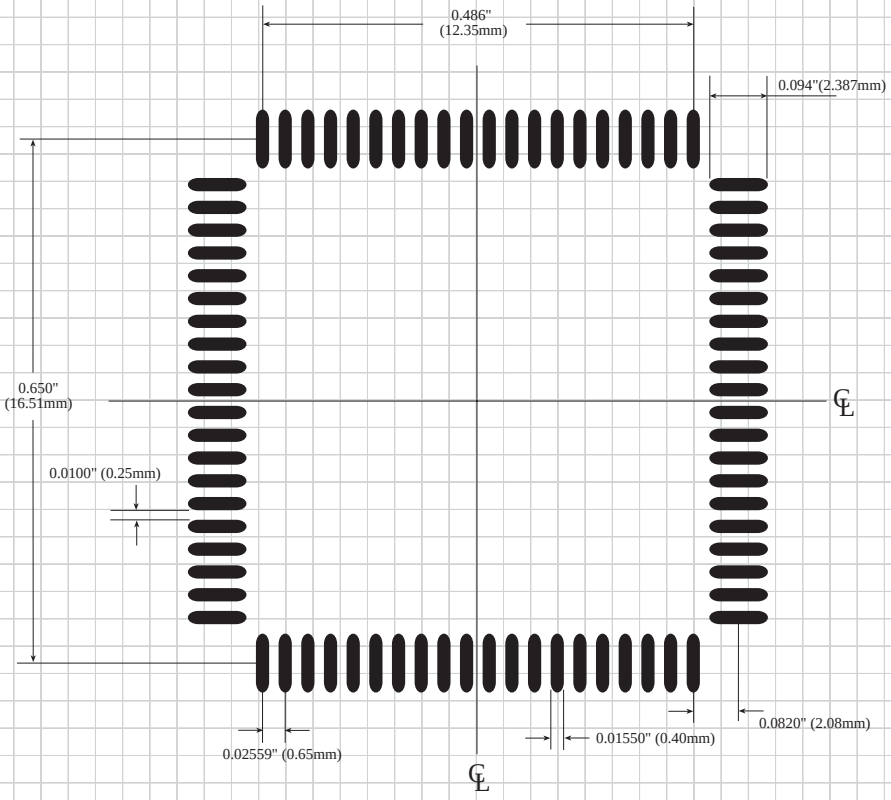
Figure 29. Adding extra differential and single-ended transceivers using the SP332

PACKAGE: QUAD FLATPACK
JEDEC "BE-2" OUTLINE



DIMENSIONS in Inches Minimum/Maximum (mm)	JEDEC BE-2 Outline 80–PIN
A	–/0.0925 (–/2.350)
A1	–/0.010 (–/0.250)
D	0.667/0.687 (16.950/17.450)
D1	0.547/0.555 (13.900/14.100)
E	0.667/0.687 (16.950/17.450)
E1	0.547/0.555 (13.900/14.100)
L	0.0255/0.0375 (0.650/0.950)

TYPICAL PCB LAYOUT FOR THE 80-PIN QFP



NOTE: THIS IS A TYPICAL PCB LAYOUT ONLY. PLEASE CHECK YOUR OWN LAYOUT RULES AND CRITERIA.

ORDERING INFORMATION

Model	Temperature Range	Package Types
SP504MCF	0°C to +70°C	80–pin JEDEC (BE-2 Outline) QFP

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