PRELIMINARY

CY7C1330

64K x 32 Synchronous-Pipelined Cache RAM

Features

- **Low (1.65 mW) standby power (f=0, L version)**
- **Supports 117-MHz bus operations with zero wait states**
- **Fully registered inputs and outputs for pipelined operation**
- **64K x 32 common I/O architecture**
- **3.3V V_{DD} and 2.5V V_{DDQ} for 2.5V I/Os**
- **Fast Clock-to-output times**
  - **5.0 ns (for 117-MHz device)**
  - **5.5ns (for 100-MHz device)**
  - **8.5ns (for 66-MHz device)**
- **User-selectable burst counter supporting interleaved or linear burst sequences**
- **Separate processor and controller address strobes**
- **Synchronous self-timed writes**
- **Asynchronous output enable**
- **JEDEC-standard 100 TQFP pinout**
- **"ZZ" Sleep Mode option**
- **Supports Stop Clock option for power conservation**

Functional Description

The CY7C1330 is 3.3V 64K by 32 synchronous-pipelined cache SRAM designed to support zero wait state secondary cache with minimal glue logic.

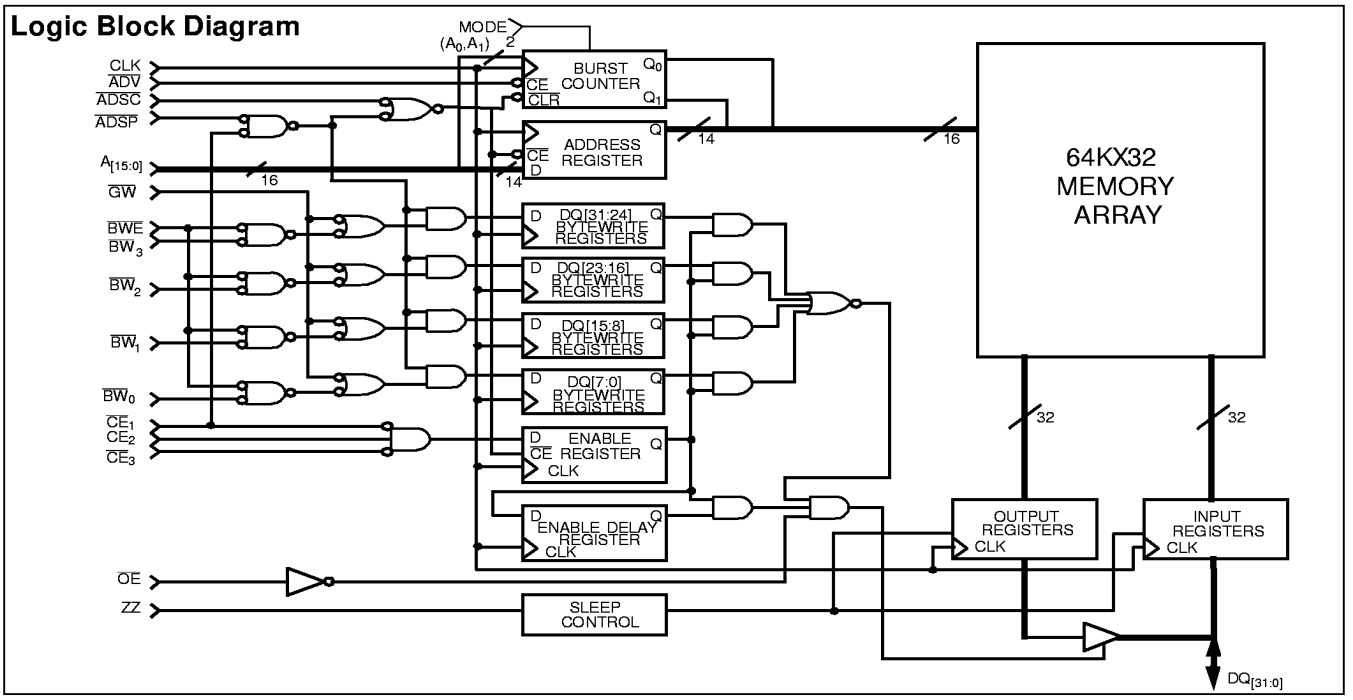
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise is 5 ns (117-MHz version). A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

The CY7C1330 supports either the interleaved burst sequence or a linear burst sequence used by processors such as the PowerPC. The burst sequence is selected through the MODE pin. Accesses can be initiated by asserting either the processor address strobe ($\overline{ADSP}$) or the controller address strobe ($\overline{ADSC}$) at clock rise. Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input.

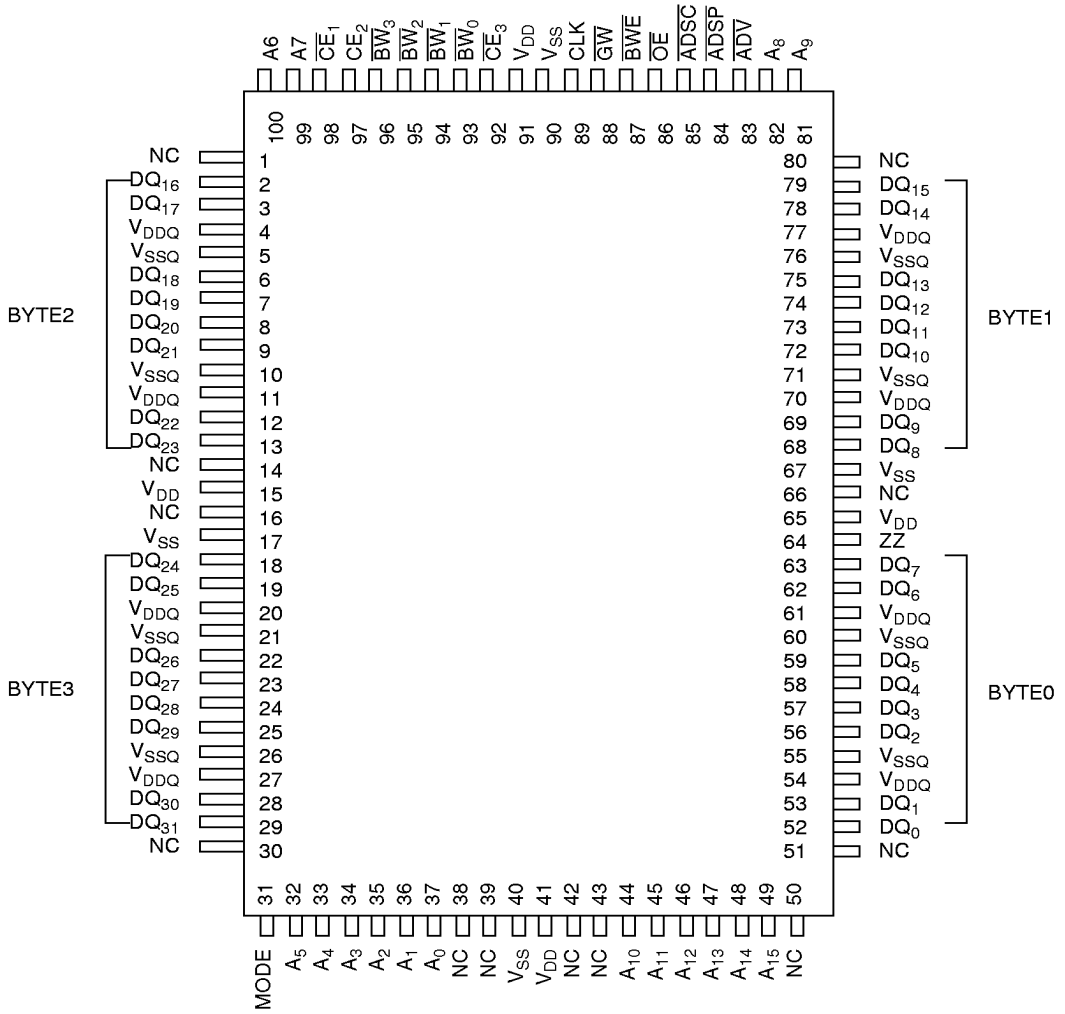
Byte write operations are qualified with the four Byte Write Select ($\overline{BW}_{[0-3]}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output three-state control. In order to provide proper data during depth expansion, $\overline{OE}$ is masked during the first clock of a read cycle when going from a deselected to a selected state.

Logic Block Diagram



Pin Configuration



Selection Guide

		7C1330-117 7C1330L-117	7C1330-100 7C1330L-100	7C1330-66 7C1330L-66
Maximum Access Time (ns)		5.0	5.5	8.5
Maximum Operating Current (mA)	Commercial	350	310	230
Maximum CMOS Standby Current (µA) (L Version only)	Commercial	500	500	500

Pin Definitions

Pin Number	Name	I/O	Description
49–44, 81,82, 99, 100, 32–37	$A_{[15:0]}$	Input-Synchronous	Address Inputs used to select one of the 64K address locations. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE}_1$, CE_2, and $\overline{CE}_3$ are sampled active. A_0 and A_1 feed the 2-bit counter.
96–93	$\overline{BW}_{[3:0]}$	Input-Synchronous	Byte Write Select Inputs, active LOW. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
88	$\overline{GW}$	Input-Synchronous	Global Write Enable Input, active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted. (ALL bytes are written, regardless of the values on $\overline{BW}_{[3:0]}$ and $\overline{BWE}$.)
87	$\overline{BWE}$	Input-Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
89	CLK	Input-Clock	Clock input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
98	$\overline{CE}_1$	Input-Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE}_3$ to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is high.
97	CE_2	Input-Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and $\overline{CE}_3$ to select/deselect the device.
92	$\overline{CE}_3$	Input-Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE}_1$ and CE_2 to select/deselect the device.
86	$\overline{OE}$	Input-Asynchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when going from a deselected to a selected state.
83	$\overline{ADV}$	Input-Synchronous	Advance Input signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
84	$\overline{ADSP}$	Input-Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK. When asserted LOW, $A_{[15:0]}$ is captured in the address registers. A_0 and A_1 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE}_1$ is deasserted HIGH.
85	$\overline{ADSC}$	Input-Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK. When asserted LOW, $A_{[15:0]}$ is captured in the address registers. A_0 and A_1 are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
64	ZZ	Input-Asynchronous	ZZ "sleep" Input. This active high input places the device in a non-time critical "sleep" condition with data integrity preserved.
29, 28, 25–22, 19, 18, 13, 12, 9–6, 3, 2, 79, 78, 75–72, 69, 68, 63, 62 59–56, 53, 52	$DQ_{[31:0]}$	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[15:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, $DQ_{[31:0]}$ are placed in a three-state condition.
15, 41, 65, 91	V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to 3.3V power supply.
17, 40, 67, 90	V_{SS}	Ground	Ground for the core of the device. Should be connected to ground of the system.
4, 11, 20, 27, 54, 61, 70, 77	V_{DDQ}	I/O Power Supply	Power supply for the I/O circuitry. Should be connected to a 2.5V power supply.
5, 10, 21, 26, 55, 60, 71, 76	V_{SSQ}	I/O Ground	Ground for the I/O circuitry. Should be connected to ground of the system.
31	MODE	Input-Static	Selects burst order. When tied to GND selects linear burst sequence. When tied to V_{DDQ} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation.
1, 14, 16, 30, 38,39, 42, 43, 49, 50, 51, 66, 80	NC	-	No Connects

Introduction

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (T_{CO}) is 5.0 ns (117-MHz device). A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

The CY7C1330 supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the processor address strobe ($\overline{ADSP}$) or the controller address strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}_{[0-3]}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous chip selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous output enable ($\overline{OE}$) provide for easy bank selection and output three-state control. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deasserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. The address presented to the address inputs (A_0–A_{15}) is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 5.0 ns (117-MHz device) if $\overline{OE}$ is active low. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always three-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output will three-state immediately.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW, and (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active. The address presented to A_0–A_{15} is loaded into the address register and the address advancement logic while being delivered to the RAM core. The write signals ($\overline{GW}$, $\overline{BWE}$ and $\overline{BW}_0$–$\overline{BW}_3$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$ triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the DQ_0–DQ_{31} inputs is written into the corresponding address location in the RAM core. If $\overline{GW}$ is HIGH, then the write operation is controlled by $\overline{BWE}$ and $\overline{BW}_{[3:0]}$ signals. The CY7C1330 provides byte write capability that is described in the write cycle description table. Asserting the Byte Write Enable input ($\overline{BWE}$) with the selected Byte Write ($\overline{BW}_0$–$\overline{BW}_3$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A Synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1330 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ_0–DQ_{31} inputs. Doing so will three-state the output drivers. As a safety precaution, DQ_0–DQ_{31} are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) $\overline{ADSP}$ is deasserted HIGH, (3) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_0$–$\overline{BW}_3$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$ triggered write accesses require a single clock cycle to complete. The address presented to A_0–A_{15} is loaded into the address register and the address advancement logic while being delivered to the RAM core. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the DQ_0–DQ_{31} is written into the corresponding address location in the RAM core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A Synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the CY7C1330 is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the DQ_0–DQ_{31} inputs. Doing so will three-state the output drivers. As a safety precaution, DQ_0–DQ_{31} are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The CY7C1330 provides a two-bit wraparound counter, fed by A_0 and A_1, that implements either an interleaved or linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
Ax+1, Ax	Ax+1, Ax	Ax+1, Ax	Ax+1, Ax
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
Ax+1, Ax	Ax+1, Ax	Ax+1, Ax	Ax+1, Ax
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation "sleep" mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the "sleep" mode are not considered valid nor is the completion of the operation guaranteed. The device should be deselected prior to entering the "sleep" mode. $\overline{CE}_1$, CE_2, $\overline{CE}_3$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns low.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
I_{CCZZ}	Snooze mode standby current	$ZZ \geq V_{DDQ} - 0.2V$		3	mA
I_{CCZZ} (L version)	Snooze mode standby current	$ZZ \geq V_{DDQ} - 0.2V$		800	µA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DDQ} - 0.2V$		$3t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$3t_{CYC}$		ns

Cycle Descriptions[1,2,3]

Next Cycle	Add. Used	ZZ	$\overline{CE}_3$	CE_2	$\overline{CE}_1$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	DQ	Write
Unselected	None	L	X	X	1	X	0	X	X	Hi-Z	X
Unselected	None	L	1	X	0	0	X	X	X	Hi-Z	X
Unselected	None	L	X	0	0	0	X	X	X	Hi-Z	X
Unselected	None	L	1	X	0	1	0	X	X	Hi-Z	X
Unselected	None	L	X	0	0	1	0	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	0	X	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	1	0	X	X	Hi-Z	read
Continue Read	Next	L	X	X	X	1	1	0	1	Hi-Z	read
Continue Read	Next	L	X	X	X	1	1	0	0	DQ	read
Continue Read	Next	L	X	X	1	X	1	0	1	Hi-Z	read
Continue Read	Next	L	X	X	1	X	1	0	0	DQ	read
Suspend Read	Current	L	X	X	X	1	1	1	1	Hi-Z	read
Suspend Read	Current	L	X	X	X	1	1	1	0	DQ	read
Suspend Read	Current	L	X	X	1	X	1	1	1	Hi-Z	read
Suspend Read	Current	L	X	X	1	X	1	1	0	DQ	read
Begin Write	Current	L	X	X	X	1	1	1	X	Hi-Z	write
Begin Write	Current	L	X	X	1	X	1	1	X	Hi-Z	write
Begin Write	External	L	0	1	0	1	0	X	X	Hi-Z	write
Continue Write	Next	L	X	X	X	1	1	0	X	Hi-Z	write
Continue Write	Next	L	X	X	1	X	1	0	X	Hi-Z	write
Suspend Write	Current	L	X	X	X	1	1	1	X	Hi-Z	write
Suspend Write	Current	L	X	X	1	X	1	1	X	Hi-Z	write
ZZ “sleep”	None	H	X	X	X	X	X	X	X	Hi-Z	X

Notes:
1. X=Don't Care, 1=HIGH, 0=LOW.
2. Write is defined by $\overline{BWE}$, $\overline{BW}$[3:0], and $\overline{GW}$. See write table.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.

Write Cycle Descriptions[4,5,6]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_3}$	$\overline{BW_2}$	$\overline{BW_1}$	$\overline{BW_0}$
Read	1	1	X	X	X	X
Read	1	0	1	1	1	1
Write Byte 0-$DQ_{[7:0]}$	1	0	1	1	1	0
Write Byte 1-$DQ_{[15:8]}$	1	0	1	1	0	1
Write Bytes 1, 0	1	0	1	1	0	0
Write Byte 2 - $DQ_{[23:16]}$	1	0	1	0	1	1
Write Bytes 2, 0	1	0	1	0	1	0
Write Bytes 2, 1	1	0	1	0	0	1
Write Bytes 2, 1, 0	1	0	1	0	0	0
Write Byte 3 - $DQ_{[31:24]}$	1	0	0	1	1	1
Write Bytes 3, 0	1	0	0	1	1	0
Write Bytes 3, 1	1	0	0	1	0	1
Write Bytes 3, 1, 0	1	0	0	1	0	0
Write Bytes 3, 2	1	0	0	0	1	1
Write Bytes 3, 2, 0	1	0	0	0	1	0
Write Bytes 3, 2, 1	1	0	0	0	0	1
Write All Bytes	1	0	0	0	0	0
Write All Bytes	0	X	X	X	X	X

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{DD} Relative to GND.....–0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[7]].....–0.5V to V_{DDQ} + 0.5V

DC Input Voltage[7].....–0.5V to V_{DDQ} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature[8]]	V_{DD}
Com'l	0°C to +70°C	3.3V ± 5%

Notes:

4. X=Don't Care, 1=Logic HIGH, 0=Logic LOW.
5. The SRAM always initiates a read cycle when $\overline{ADSP}$ asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}_{3-0}$. Writes may occur only on subsequent clocks after the $\overline{ADSP}$ or with the assertion of $\overline{ADSC}$. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to three- state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
6. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle DQ=HIGH–Z when $\overline{OE}$ is inactive or when the device is de–selected, and DQ=data when $\overline{OE}$ is active
7. Minimum voltage equals -2.0V for pulse durations of less than 20 ns.
8. T_A is the "instant on" case temperature.

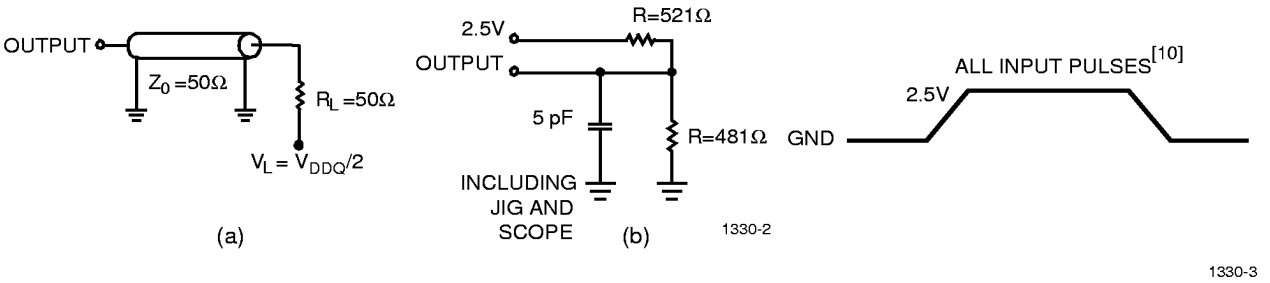
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage			3.135	3.465	V
V_{DDQ}	I/O Supply Voltage			2.375	2.9	V
V_{OH}	Output HIGH Voltage	Ioh = –100 µA		2.1		V
		Ioh = –1 mA		2.0		V
		Ioh = –2 mA		1.7		V
V_{OL}	Output LOW Voltage	Iol = 100 µA			0.2	V
		Iol = 1 mA			0.4	V
		Iol = 2 mA			0.7	V
V_{IH}	Input HIGH Voltage			1.7	V_{DDQ} + 0.3V	V
V_{IL}	Input LOW Voltage[7]			–0.3	0.7	V
I_X	Input Load Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DDQ}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DDQ}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Outputs Disabled		–5	5	µA
I_{CC}	V_{DD} Operating Supply Current	V_{DD} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	8.6 ns cycle, 117 MHz		350	mA
			10 ns cycle, 100 MHz		310	mA
			15 ns cycle, 66 MHz		230	mA
I_{SB1}	Automatic CS Power-Down Current—TTL Inputs	Max V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX} = $1/t_{CYC}$	8.6 ns cycle, 117 MHz		40	mA
			10 ns cycle, 100 MHz		35	mA
			15 ns cycle, 66 MHz		25	mA
I_{SB2}	Automatic CS Power-Down Current—CMOS Inputs	Max V_{DD}, Device Deselected, V_{IN} ≤ 0.3V, f = 0			2.5	mA
			L version		500	µA
I_{SB3}	Automatic CS Power-Down Current—CMOS Inputs	Max V_{DD}, Device Deselected, V_{IN} < 0.3V, f = f_{MAX} = $1/t_{CYC}$	8.6 ns cycle, 117 MHz		35	mA
			10 ns cycle, 100 MHz		30	mA
			15 ns cycle, 66 MHz		20	mA
I_{SB4}	Automatic CS Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0			25	mA

Capacitance[9]

Parameter	Description	Test Conditions	Min	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V. V_{DDQ} = 2.5V	2	5	pF
C_{CLK}	Clock Input Capacitance		2	5	pF
$C_{I/O}$	Input/Output Capacitance		3.5	8	pF

AC Test Loads and Waveforms



Notes:
9. Tested initially and after any design or process changes that may affect these parameters.
10. Input waveform should have a slew rate of 1V/nS and swing from 0V to 2.5V

Switching Characteristics Over the Operating Range[11,12,13]

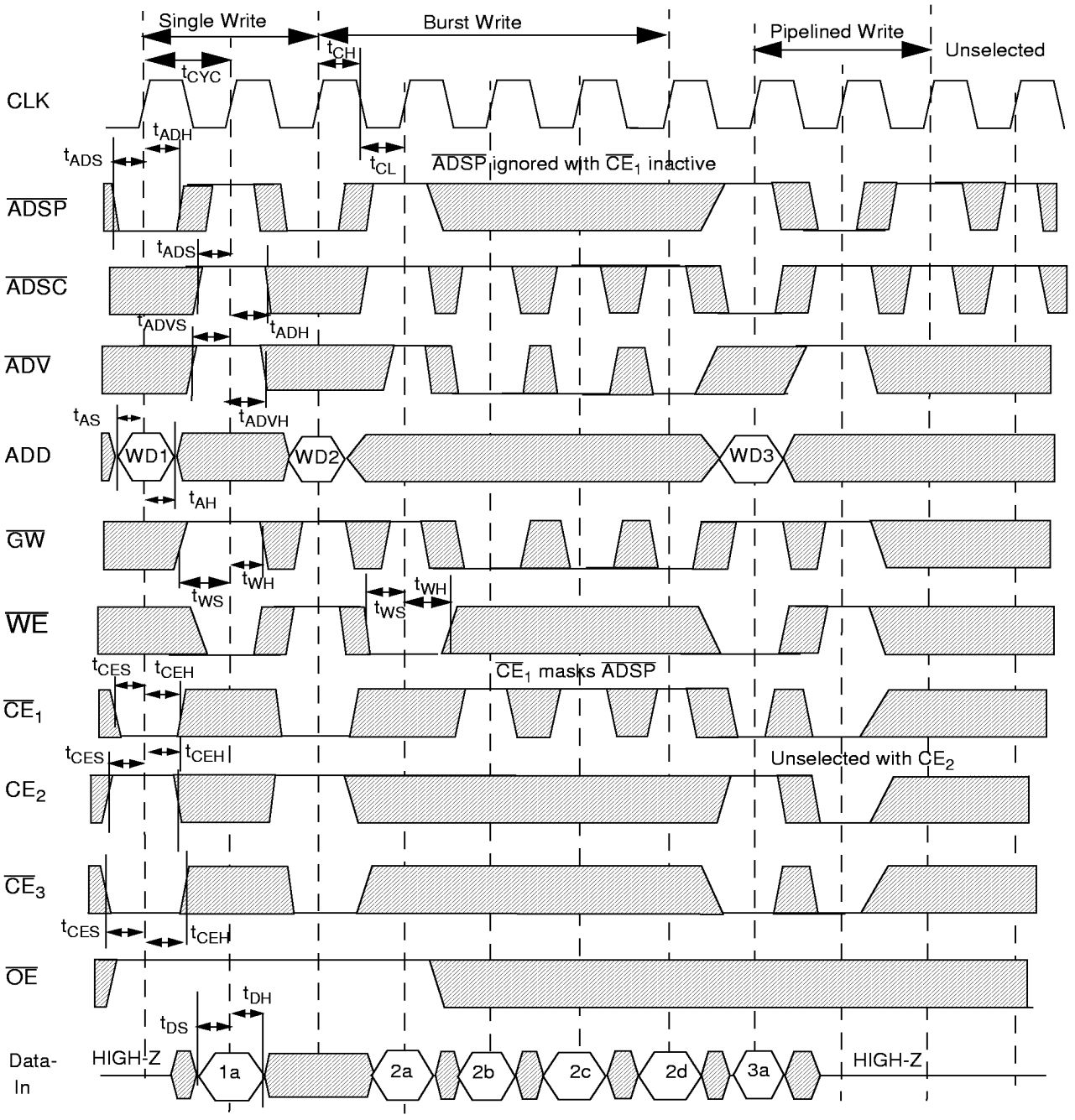
Parameter	Description	-117		-100		-66		Unit
		Min	Max	Min.	Max.	Min	Max	
t_{CYC}	Clock Cycle Time	8.6		10		15.0		ns
t_{CH}	Clock HIGH	2.5		3.2		6.0		ns
t_{CL}	Clock LOW	2.5		3.2		6.0		ns
t_{AS}	Address Set-Up Before CLK Rise	2.0		2.0		2.5		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CO}	Data Output Valid After CLK Rise		5.0		5.5		8.5	ns
t_{DOH}	Data Output Hold After CLK Rise	1.5		1.5		2.0		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.0		2.0		2.5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{WES}	$\overline{BWE}$, $\overline{GW}$, $\overline{BW}_{[3:0]}$ Set-Up Before CLK Rise	2.0		2.0		2.5		ns
t_{WEH}	$\overline{BWE}$, $\overline{GW}$, $\overline{BW}_{[3:0]}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.0		2.0		2.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.0		2.0		2.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CES}	Chip Select Set-Up	2.0		2.0		2.5		ns
t_{CEH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CHZ}	Clock to High-Z[12]	1.5	4.5	1.5	5	2.0	6.0	ns
t_{CLZ}	Clock to Low-Z[12]	0		0		0		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[12, 13]		4.8		5.5		6.0	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[12,13]	0		0		0		ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[12]		4.8		5.5		6.0	ns

Notes:

11. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.25V, input pulse levels of 0 to 2.5V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) of AC test loads.
12. t_{CHZ}, t_{CLZ}, t_{OEV}, t_{EOLZ}, and t_{EOHZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
13. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ}.

Switching Waveforms

Write Cycle Timing

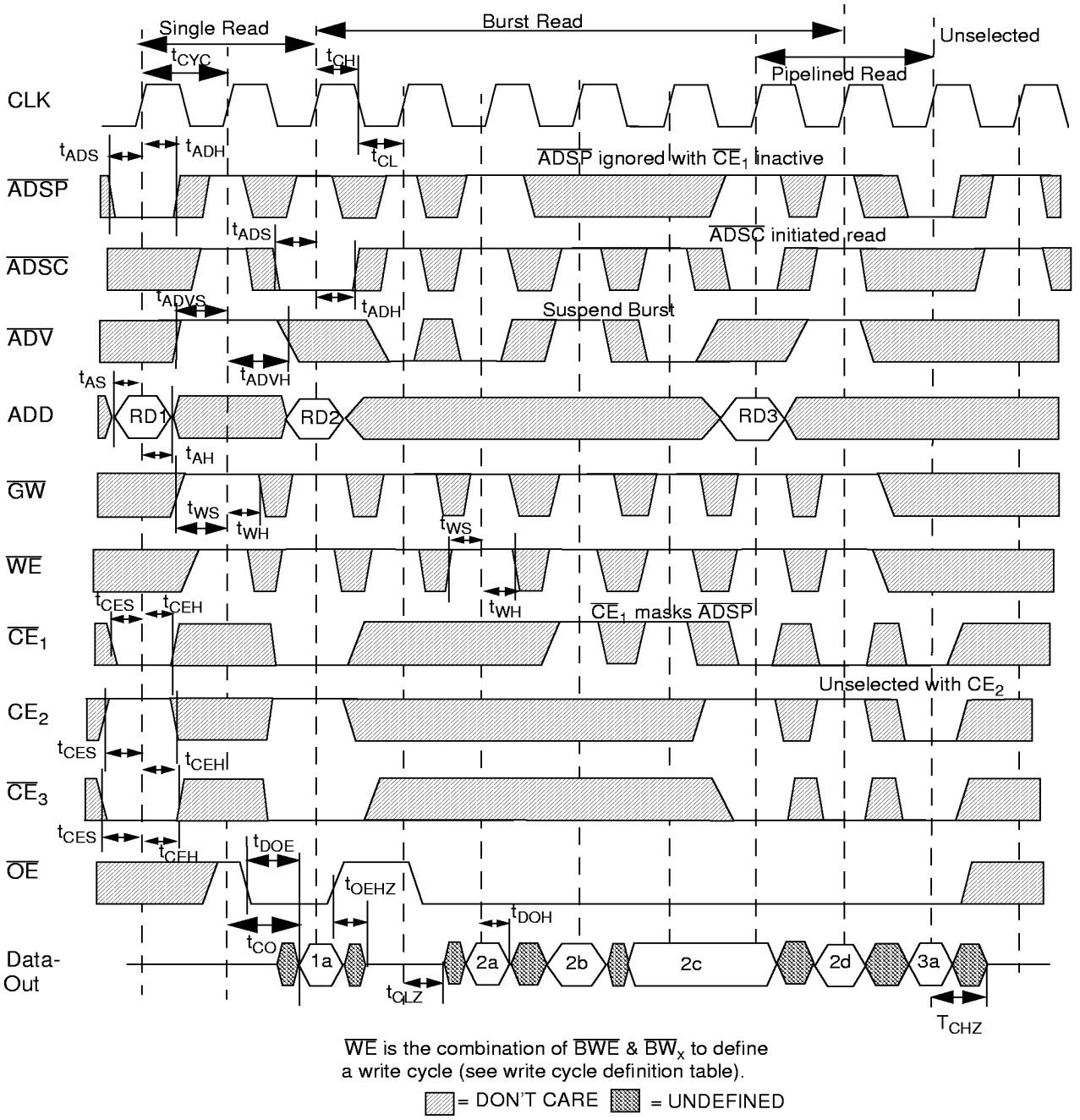


WE is the combination of BWE & BWx to define a write cycle (see write cycle definition table).

= UNDEFINED = DON'T CARE

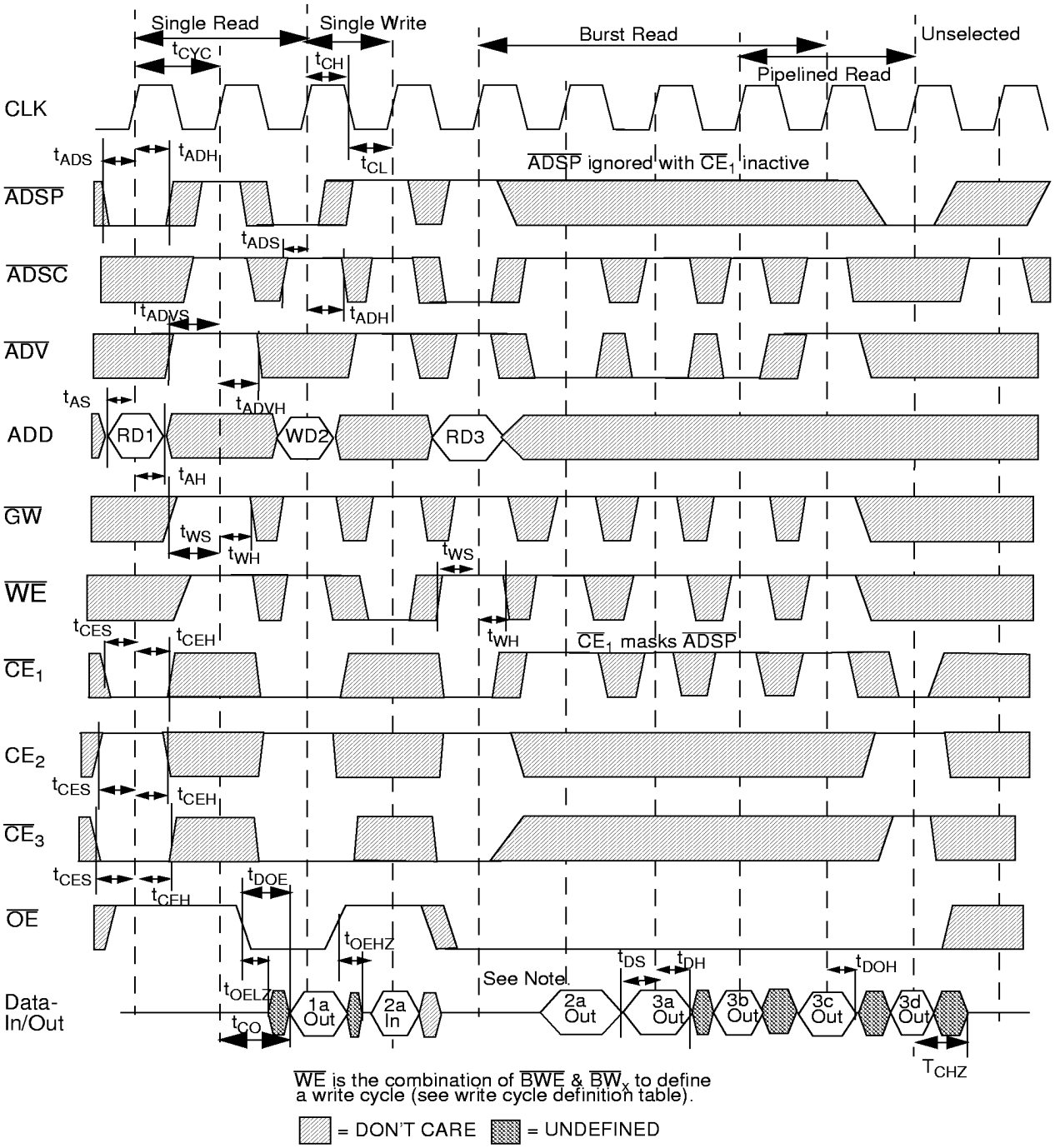
Switching Waveforms (continued)

Read Cycle Timing



Switching Waveforms (continued)

Read/Write Cycle Timing



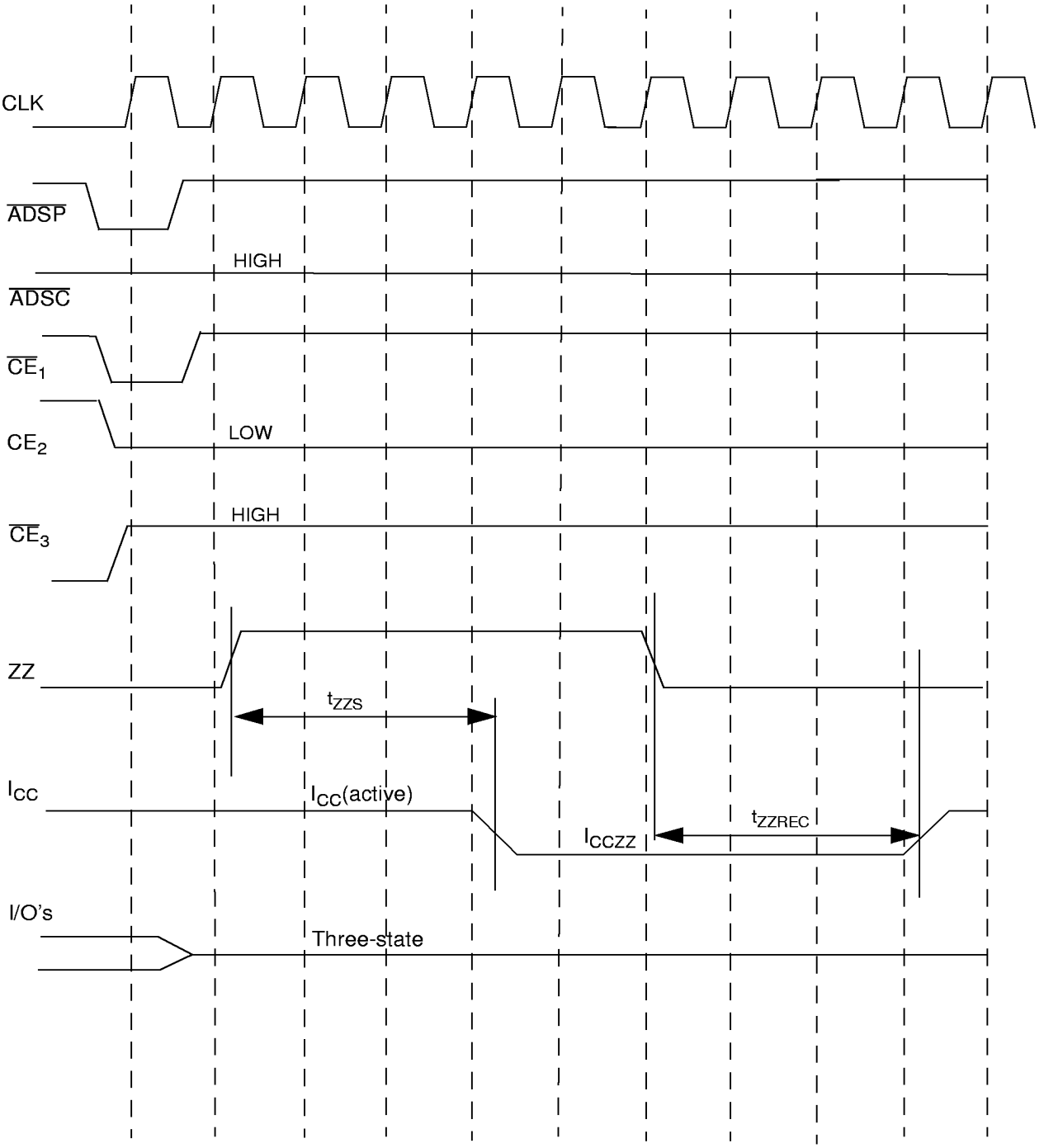
WE is the combination of BWE & BWx to define a write cycle (see write cycle definition table).

= DON'T CARE = UNDEFINED

Note: Write data forwarded to outputs on read immediately following a write

Switching Waveforms (continued)

ZZ Mode Timing [14,15]



Notes:
14. Device must be deselected when entering ZZ mode. See Cycle description for all possible signal conditions to deselect the device.
15. I/O's are in three-state when exiting ZZ sleep mode.

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
117	CY7C1330-117AC	A100	100-Lead Thin Quad Flat Pack	Commercial
100	CY7C1330-100AC	A100	100-Lead Thin Quad Flat Pack	Commercial
66	CY7C1330-66AC	A100	100-Lead Thin Quad Flat Pack	Commercial
117	CY7C1330L-117AC	A100	100-Lead Thin Quad Flat Pack	Commercial
100	CY7C1330L-100AC	A100	100-Lead Thin Quad Flat Pack	Commercial
66	CY7C1330L-66AC	A100	100-Lead Thin Quad Flat Pack	Commercial

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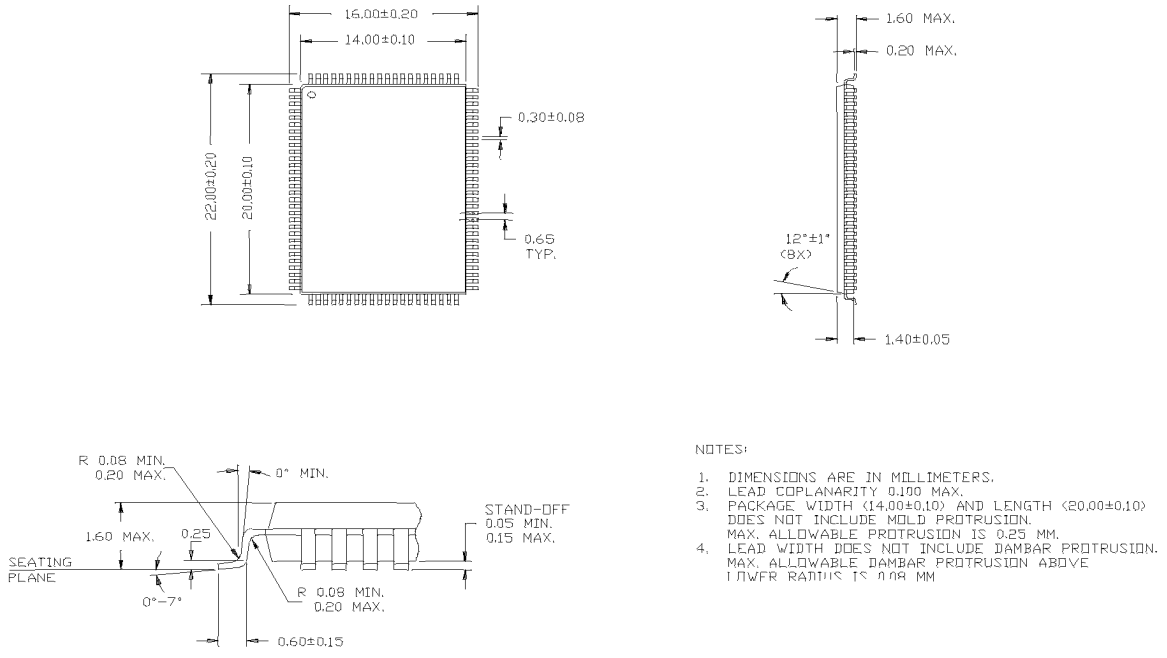
Package Diagrams

100-Lead Thin Quad Flat Pack (TQFP) A100



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. LEAD COPLANARITY 0.100 MAX.
3. PACKAGE WIDTH (14.00±0.10) AND LENGTH (20.00±0.10) DOES NOT INCLUDE MOLD PROTRUSION. MAX. ALLOWABLE PROTRUSION IS 0.25 MM.
4. LEAD WIDTH DOES NOT INCLUDE DAMBAR PROTRUSION. MAX. ALLOWABLE DAMBAR PROTRUSION ABOVE LOWER RADIUS IS 0.08 MM