LXT971A — LXT970A-to-LXT971A Migration

Application Note

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As of January 15, 2001, this document replaces the Level One document known as *AN121*.

Application Note

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1.0 Introduction

The LXT971A and LXT970A are single-port Fast Ethernet 10/100 Transceivers that support 10 Mbps and 100 Mbps networks. Both products comply with all applicable requirements of the IEEE 802.3 standard

While the LXT971A and LXT970A are similar in many respects, the LXT971A incorporates several functional enhancements for a more robust Ethernet solution. This document provides an outline of the differences between the two devices. It is intended to support design upgrades that take advantage of the LXT971A to enhance existing LXT970 designs.

1.1 Feature Comparison

Differences between the feature sets of the LXT970A and LXT971A can be grouped into four categories. These categories include:

- "External Interfaces" on page 5
- "Power Management" on page 10
- "Mode Controls and Indicators" on page 11
- "Production Support" on page 15

1.2 External Interfaces

At the top level, the LXT970A and LXT971A provide substantially similar external interfaces:

- Both the LXT970A and the LXT971A provide support for twisted-pair and fiber networks.
- Both devices support twisted-pair operations via an internal twisted-pair PMD block.
- Both devices support fiber operations via a pseudo-ECL interface to external fiber modules that perform the PMD functions for fiber networks.
- Both devices support a standard Media Independent Interface (MII) for MAC communications.

Nonetheless, there are some significant differences between the two devices with respect to these external interfaces. These differences are discussed in the following paragraphs.

1.2.1 Twisted Pair Interface

Differences in the twisted-pair interface are highlighted in Table 1 and Figure 1, and described in detail in the following paragraphs.

1.2.1.1 TP Pin Assignments

The most immediate difference between the two devices is in the pin assignments. On the LXT970A, the twisted-pair interface is entirely separate from the fiber interface - the pins are not shared. The LXT971A supports twisted-pair and fiber networks via a single set of pins. That is, the LXT971A network interface pins serve dual functions - either TP or fiber.

1.2.1.2 Transmit Termination Circuitry

The external resistor used on the LXT970A has been integrated into the LXT971A. Therefore no external load-balancing resistor is required on the twisted-pair output of the LXT971A.

1.2.1.3 Receive Termination Circuitry

The recommended receive termination for the LXT970A was a strictly resistive receive interface - a 100Ω load across the receive input pins. Recent investigations of the CDE (Cable Discharge Event) phenomenon have led to improvements in receive termination. The recommended receive termination for the LXT971A adds capacitors in series with the inputs to provide improved noise immunity.

1.2.1.4 Transmit Output Waveshaping

The LXT970A output driver was fixed to provide a balanced waveform that met IEEE 802.3 standards over a wide range of applications. The LXT971A provides additional control over the output waveform. This allows the designer to optimize the output to the specific magnetics, termination circuit and anticipated cable environment. This control is provided via a pair of “TxSlew” input pins. These inputs can also be provided via the MII Management Interface.

2.0 Migration Guide

2.1 Transmit Current Source

Both the LXT970A and the LXT971A use current-driven output stages. However, the source of that current is different. The LXT970A supplied the driver current from an output pin labeled “TREF”. This signal is not used on the LXT971A. Instead, the driver current is provided from an external source. As an additional power-saving option, the driver current may be supplied from either a 3.3V or a 2.5V source. Using a 2.5V source provides significant power savings when compared to a 3.3V source.

2.2 Fiber Interface

Fiber applications are supported via a pseudo-ECL interface to external fiber modules. Neither the LXT970 nor the LXT971A provides internal support for fiber PMD functions.

2.2.1 Fiber Pin Assignments

As with the TP interface, the most immediate difference between the two devices is in the pin assignments. The LXT971A supports twisted-pair and fiber networks via a single set of pins. That is, the LXT971A network interface pins serve dual functions - either TP or fiber. On the LXT970A, the fiber interface is entirely separate from the TP interface - the pins are not shared.

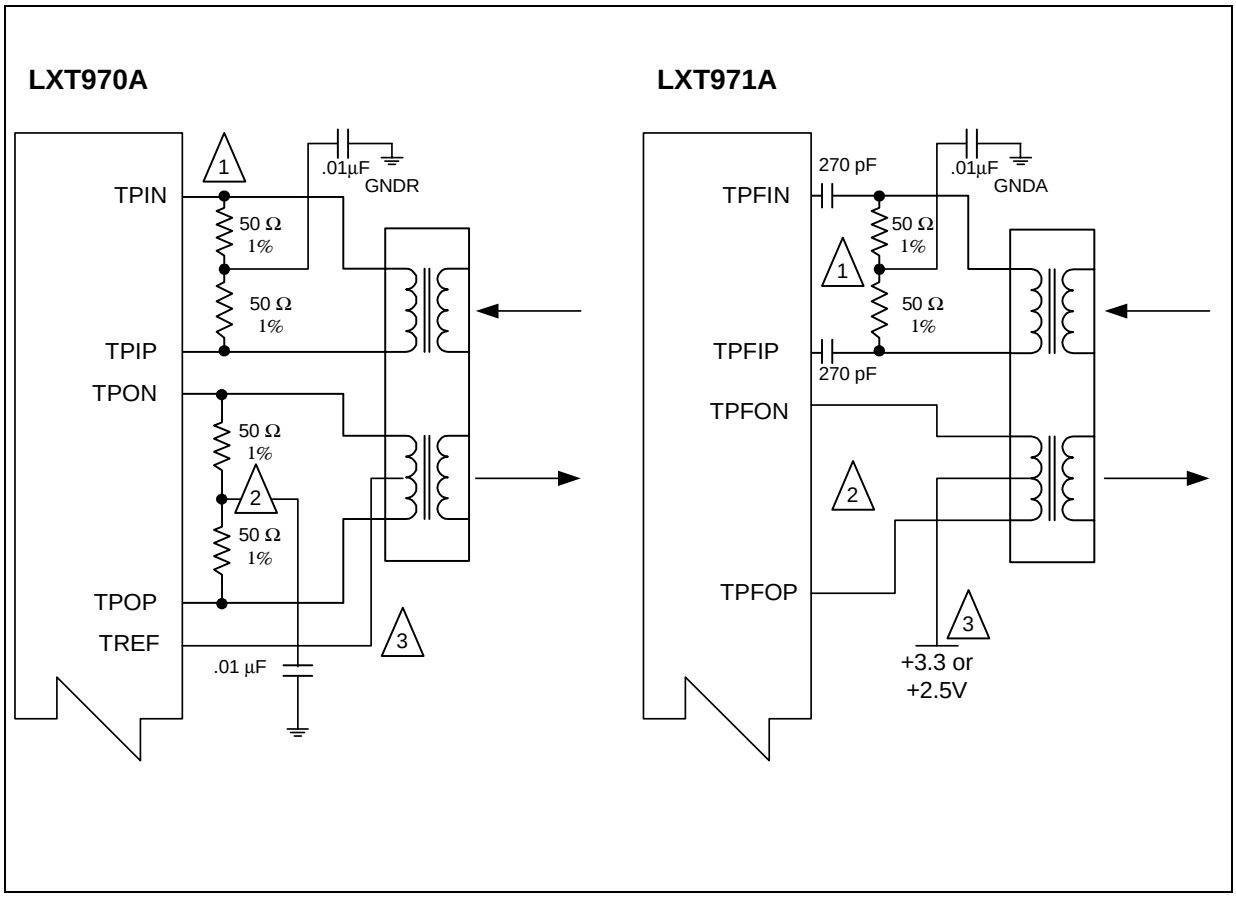
2.2.2 Signal Detect and Far End Fault Functions

The LXT970A does not support the fiber Signal Detect function. This capability has been added to the LXT971A. The Signal Detect function allows the LXT971A to support Far End Fault Indications (FEFI). This PMA layer function consists of a specific fault code that is transmitted over the fiber link. The LXT971A sends the FEFI code in response to a locally-detected signal fault reported by the fiber module over the Signal Detect line.

Table 1. Network Line Interface Comparison

Feature	LXT970A		LXT971A	
Output	2 Pairs:	TPO P/N (Twisted-Pair) FIBO P/N (Fiber)	1 Pair:	TPFO P/N (combined Twisted-Pair and Fiber)
Output Current Source	Internal Supply TREF: Device output connects to the center tap of the transmit transformer.		External Supply Transformer center-tap can be supplied with either 3.3V (standard) or 2.5V (for reduced power consumption).	
Input	2 Pairs:	TPI P/N (Twisted-Pair) FIBI P/N (Fiber)	1 Pair:	TPFI P/N (combined Twisted-Pair and Fiber)
Media Select (Twisted-Pair or Fiber)	Multi-function pin MF4 selects either TX or FX Mode.		Dual function SD/$\overline{\text{TP}}$ pins select media. When Fiber Mode is selected, these pins also provide the Signal Detect function.	
Twisted-Pair Output Waveform Adjustment	Not supported.		TxSLEW0 and TxSLEW1: These pins select the TX output slew rate (rise and fall time).	

Figure 1. Network Interface Circuit Comparison



2.3 MII Data Interface

Both the LXT970A and the LXT971A support the IEEE 802.3 MII. However, there are some minor differences in implementation.

2.3.1 Repeater Mode

The LXT970A included a Repeater mode that allowed multiple PHY devices to share a common MII bus. This was accomplished using a Tristate signal that allowed an external controller to selectively enable a single PHY while isolating all other PHYs on the bus. This mode was intended for early Fast Ethernet repeater applications that used ASIC devices to implement the repeater state machine (RSM). Modern repeater designs use integrated repeater chips (such as the Intel LXT98xx family) that include both the RSM and multiple PHY ports. Therefore, the repeater mode is not supported in the LXT971A. However, the MII tristate function is still available via the MDIO (Control register bit 0.10).

Related repeater mode functions such as the slave clock mode (where TX_CLK was an input) and 5-bit Symbol mode (bypassing the 4B/5B encoder/decoder) are also not supported by the LXT971A.

2.3.2 MII Termination Circuitry

The LXT971A incorporates various advanced features that were available only as user-selectable options on the LXT970A. The LXT970A required termination resistors on the MII data outputs unless a lower drive level was selected via the MDIO interface. This option was not available on applications that didn't use the MDIO. In most applications, the LXT971A does not require termination resistors on the MII outputs, regardless of whether or not the MDIO channel is used. The LXT971A does not include the selectable drive strength feature.

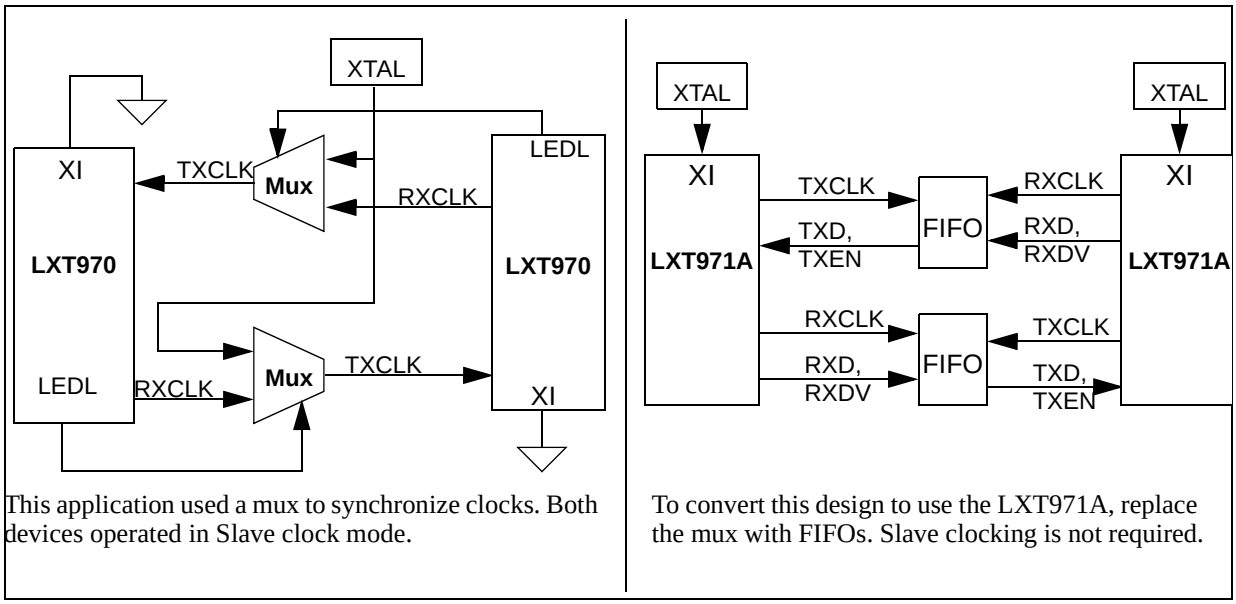
2.3.3 Special Applications

Applications where the MII data interface is used as a direct connection between two LXT970A devices (media converters, for example) typically used the Slave clock mode. This allowed the RX_CLK output from one device to drive the TX_CLK input of the other device. Since the LXT971A does not support Slave clock mode (TX_CLK is always an output), an alternative scheme is required. One approach is to use an externally-clocked FIFO to buffer the data exchange between the two LXT971As.

Table 2. MII Data Interface Comparison

Feature	LXT970A	LXT971A
Repeater Mode	Enabled repeater designs using ASIC Repeater controllers and external PHYs.	No longer required. LXT98xx devices are recommended for new repeater designs. The LXT971A does not support repeater mode.
MII Tri-State (TRSTE)	Dual-mode control (external pin or MDIO bit) enabled repeater applications.	Hardware control no longer required. Bit 0.10 provides the same isolate function as in the LXT970A. In addition, during hardware power down, all LXT971A outputs are tri-stated.
Termination Resistors	Required on MII outputs unless alternate drive strength option selected via MDIO.	Drive strength option now standard. Termination resistors are not required in most applications.

Figure 2. Back-to-Back MII Applications



This application used a mux to synchronize clocks. Both devices operated in Slave clock mode.

To convert this design to use the LXT971A, replace the mux with FIFOs. Slave clocking is not required.

2.4 Power Management

The LXT970A is a 5V device with limited power management options. The LXT971A is a 3.3V device with several features that support power management. It also simplifies the power supply aspects of application design.

2.4.1 Sleep Mode

The LXT971A supports a “Sleep” mode that was not available in the LXT970A. This mode allows the device to operate in a reduced-power mode when removed from the network, but to resume normal operation when reconnected to the network. This mode may be enabled by hardware or software. Various timing parameters are also user selectable. Refer to the LXT971A data sheet for details.

2.4.2 Power-Down Modes

Both the LXT970A and the LXT971A support a power-down mode that can be enabled via an external input pin or via the MDIO Control register. Power down functionality is essentially the same for both devices.

2.4.3 Power Supplies

The primary difference between the LXT970A and the LXT971A power circuits is the supply voltage (5V vs. 3.3V). However, there are some additional changes that are described in the following paragraphs.

2.4.3.1 Support for Lower-Voltage MACs

Both the LXT970A and the LXT971A include a power supply input labeled VCCIO. This input supports the MII interface to a MAC or other controller. Both the LXT0970A and LXT971A support applications where the MAC operates at a lower voltage than the PHY. The LXT970A requires a primary supply at +5V, but supports a 3.3V MII when VCCIO is supplied with 3.3V. The LXT971A requires a primary supply of +3.3V, but supports a 2.5V MII when VCCIO is supplied with 2.5V. In both cases, VCCIO should be supplied from the same source as the MAC. Inputs on the LXT971A MII interface are tolerant to 5V.

2.4.3.2 Transmit Driver Supply

Both the LXT970A and the LXT971A use current-driven output stages. However, the source of that current is different. The LXT970A supplied the driver current from an output pin labeled “TREF”. This signal is not used on the LXT971A. Instead, the driver current is provided from an external source. As an additional power-saving option, the driver current may be supplied from either a 3.3V or a 2.5V source. Using a 2.5V source provides significant power savings when compared to a 3.3V source.

2.4.3.3 Supply and Return Circuits

The LXT970A data sheet includes several differentiated power and ground signals. Some of these signals have been consolidated in the LXT971A. For example, the LXT970A included not only an analog power supply (VCCA), but separate supplies labeled for the receiver (VCCR) and

transmitter (VCCT). In the LXT971A these three inputs have been consolidated as VCCA. The LXT971A does not require separate handling of the power supplies for the receiver and transmitter. Ground returns have been similarly consolidated. Refer to Table 3 for details.

Table 3. Power Supply Comparison

LXT970A		LXT971A	
Pin Name	**Signal Description**	**Pin Name**	**Signal Description**
VCCIO	MII Supply (3.3V or 5V)	VCCIO	MII Power (3.3V or a 2.5V).
VCCD	Digital (5V)	VCCD	Digital (3.3V)
VCCA	Separate Analog supplies for Receive and Transmit circuits.	VCCA	The common supply for all Analog circuits.
VCCT			
VCCR			
GNDD	Separate Grounds for each supply.	GND	Common ground for all supplies.
GNDA			
GNDR			
GNDT			
GNDIO			

2.5 Mode Controls and Indicators

Both the LXT970A and the LXT971A support applications that use either Manual/Hardware control or MDIO/Software control. The LXT971A provides a simpler interface for hardware control, and a more extensive register set for software control. In either case, the design upgrade from the LXT970A to LXT971A is relatively simple.

2.5.1 Manual/Hardware Control Mode

The LXT970A used a relatively complex 4-level input scheme ($V_{MF}1$, $V_{MF}2$, $V_{MF}3$, $V_{MF}4$) for hardware control. This allowed the hardware control pins to also supply the full set of 32 PHY addresses. The LXT971A uses a simpler scheme that does not require the 4-level ‘totem-pole’ voltage divider. PHY addresses are set independently of the configuration controls. Refer to Table 4 for a comparison of typical hardware configuration settings.

2.5.1.1 MDDIS

For both the LXT970A and LXT971A, the operation of a physical interface consisting of a data line (MDIO) and clock line (MDC) is controlled by the MDDIS input pin. When MDDIS is Low, the MDIO port is enabled for both read and write operations and the Hardware Control Interface is not used. However, when MDDIS is High on the LXT970A, the MDIO is restricted to Read Only and the MF<4:0>, CFG<1:0>, and FDE pins provide continual control of their respective bits. When MDDIS is High on the LXT971A, the MDIO read and write operations are disabled and the Hardware Control Interface provides primary configuration control.

2.5.2 MDIO/Software Control Mode

Both the LXT970A and the LXT971A support the IEEE 802.3 MII, including the MDIO Management Interface. However, there are some minor differences in implementation.

2.5.2.1 Clock Speeds

Both the LXT970A and the LXT971A require an external clock (MDC) to drive the MDIO interface. In the LXT970A, the clock speed was limited to 2.5 MHz. In the LXT971A, this has been increased to 8 MHz to allow for faster control circuits.

Table 4. Hardware Configuration Settings

Desired Mode			Required Settings						
			LXT970A				LXT971A		
Auto-Neg	Speed	Duplex	MF0	CFG0	CFG1	FDE	LED/CFG1	LED/CFG2	LED/CFG3
Disabled	10	Half	$V_{MF}1$ or $V_{MF}4$	Low	-	Low	Low	Low	Low
		Full		Low	-	High	Low	Low	High
	100	Half		High	-	Low	Low	High	Low
		Full		High	-	High	Low	High	High
Enabled	100 Only	Half	$V_{MF}2$ or $V_{MF}3$	-	Low	Low	High	Low	Low
		Full		-	Low	High	High	Low	High
	10/100	Half Only		-	High	Low	High	High	Low
		Full or Half		-	High	High	High	High	High

2.5.2.2 Interrupt Functions

Both the LXT970A and LXT971A support a processor interrupt function, however the LXT971A provides a broader range of controls. For example, the LXT970A provided only a single Interrupt Enable bit with no control over the events that triggered an interrupt.

The LXT971A supports an increased number of interrupt events as well as providing an individual Mask/Enable control for each interrupt event. Interrupt events include:

LXT970A Interrupts	LXT971A Interrupts
• Link Status Change • Duplex Status Change	• Link Status Change • Duplex Status Change • Speed Change • Auto-Negotiation Completion

Both devices also support a Force Interrupt with a control bit.

The LXT970A interrupt output was multiplexed with a duplex status indication, using a pin labeled FDS/$\overline{\text{INT}}$. The LXT971A provides an exclusive Interrupt pin that is not shared with any other function. Because the LXT970A interrupt is a shared pin, the device also supports an “MDIO”

interrupt (a low-going pulse on the MDIO data line) as an alternative to the standard interrupt line. Controllers that use this MDIO interrupt are no longer in wide usage and the MDIO interrupt feature was dropped from the LXT971A.

2.5.2.3 Register Set

Table 6 provides a comparison of Register Sets and Table 7 lists the LXT970A and LXT971A register bits for various common functions.

Table 5. MII Management Interface

Feature	LXT970A	LXT971A
Management Data Clock --	2.5 MHz Maximum	8 MHz Maximum
Management Data Interrupt	**FDS/$\overline{\text{MDINT}}$**: Combination Full-Duplex Status/ Management Data Interrupt pin. **MDIO:** alternate interrupt signaling	**$\overline{\text{MDINT}}$**: Dedicated Management Data Interrupt pin. **MDIO:** interrupt not available
Management Disable	When MDDIS is High, the MDIO is restricted to Read Only.	When MDDIS is High, the MDIO is disabled from read and write operations.
Management Data Line	Standard bi-directional data line	No changes

Table 6. LXT970A-to-LXT971A Register Set Comparison

Register Address	LXT970A	LXT971A
0 through 6	**No change**	
7 and 8	**Not Supported**	Next Page Registers. These registers support the ability to transparently exchange user-defined data across the link. This feature can be used to enable a variety of applications such as IP telephony and transporting other protocols across Ethernet links.
16 (Hex 10)	Mirror Register	Port Configuration Register
17 (Hex 11)	Interrupt Enable Register	Status Register #2
18 (Hex 12)	Interrupt Status Register	Interrupt Enable Register
19 (Hex 13)	Configuration Register	Interrupt Status Register
20 (Hex 14)	Chip Status Register	LED Configuration Register
30 (Hex 1E)	**Not Supported**	**Transmit Control Register**

Table 7. LXT970A-to-LXT971A Register Bit Comparison

Function		Configuration or Status Bit		Notes
		LXT970A	LXT971A	
Status Functions	Link	20.13	17.10	1 = Link is up. 0 = Link is down
	Duplex	20.12	17.9	1 = Full-duplex. 0 = Half-duplex.
	Speed	20.11	19.4	1 = 100 Mbps. 0 = 10 Mbps.
	Auto-Negotiation	20.9	17.7	1 = Auto-negotiation process completed. 0 = Auto-negotiation process not completed.
	Page Received	20.8	6.1	1 = Page received correctly (3x). 0 = Page not received correctly (3x).
Configuration	Media/Mode Select	19.2	16.0	1 = Select Fiber mode. 0 = Select Twisted-Pair mode.
	Bypass Scrambler (100BASE-X)	19.3	16.12	1 = Bypass transmit scrambler and receive descrambler. 0 = Normal operation (scrambler and descrambler enabled).
	Jabber (10BASE-T)	19.9	16.10	1 = Disable Jabber Correction 0 = Normal operation
	SQE (10BASE-T)	19.10	16.9	1 = Enable Heart Beat 0 = Normal operation
	TP Loopback (10BASE-T)	19.11	16.8	1 = Disable TP loopback 0 = Normal operation
	Txmit Test (Force Link Pass)	19.14 (100) 19.8 (10)	16.14 (10/100)	1 = Force Link Pass (use for transmit testing) 0 = Normal operation
	Transmit Disconnect	19.0	16.13	1 = Disable Twisted-Pair transmitter. 0 = Normal operation.
	LED Programming	19.7:6	20.15:4	970A = Program bits for LEDC only. 971 = Program bits for LEDs 1, 2, and 3.
Interrupt	Interrupt Enable	17.1	18.1	1 = Enable interrupts. 0 = Disable interrupts.
	Force Interrupt	17.0	18.0	1 = Force interrupt (for test purposes). 0 = Normal operation.
	Interrupt Status	18.15	19.2	1 = MII interrupt pending. 0 = No MII interrupt pending.

2.5.3 LED Drivers

The LXT970A provided individual five LED driver outputs:

- Link
- Speed
- Transmit
- Receive
- Collision.

The LXT971A provides only three direct LED drivers, but they are all programmable. The LEDs can be programmed to indicate any of the conditions reported by the LXT970A LEDs. In addition, the LXT971A offers an option for indicating duplex status as well as various combinations of conditions. (Refer to the LXT971A data sheet for details on the 16 settings available for each LED.) Table 8 compares the differences in LED driver pins.

Table 8. Comparison of LEDs

Function	LXT970A	LXT971A
LED Drivers	5 LED Drivers. Function of each LED driver is fixed as follows: • Link • Speed • Transmit • Receive • Collision	3 LED Drivers. Function of each LED driver is selectable from the following list: • Link • Speed • Transmit • Receive • Collision • Duplex Status The LED drivers can also be programmed to display various combined status conditions. *Refer to the LED Configuration Register table in the LXT971A data sheet*.
LED Blink Frequency	No blinking	Adjustable/Programmable via MDIO Register 20.3:2
LED Pulse Stretch	Fixed	Adjustable/Programmable via MDIO Register 20.1

2.6 Production Support

The LXT971A adds several features to enhance production including JTAG Boundary Scan, new packages for portable applications and extended temperature options for more demanding environments.

2.6.1 Boundary Scan

The LXT971A implements the JTAG 1149.1 boundary scan test port. This provides direct access to every pin on the device, simplifying production test requirements. The standard requirement for ‘bed of nails’ test fixtures may be eliminated in many applications. This is particularly advantageous for applications using the BGA package.

2.6.2 Package and Temperature Options

The LXT971A is available in two packages, including a new ball-grid array (BGA). An expanded temperature rating also supports industrial applications. Table 9 lists the various options. Table 10 provides a pin-to-pin comparison to assist in design conversions.

Table 9. Packaging

	LXT970A	LXT970
Package Types	QFP & TQFP	BGA
		LQFP (Low-Profile Quad Flat Pack)
Operating Temperatures	Commercial operating temperature only	Both packages available in Industrial and Commercial operating temperatures.

Table 10. LXT970A and LXT971A QFP Pin Assignment Comparison

Pin #	Signal Name		Pin #	Signal Name		Pin #	Signal Name		Pin #	Signal Name	
	970A	971		970A	971		970A	971		970A	971
1	CRS	REFCLK/XI	17	FIBOP	RBIAS	33	CFG1	PAUSE	49	RXD1	RX_DV
2	FDS/ MDINT	XO	18	FIBON	GND	34	PWRDWN	TEST0	50	RXD0	GND
3	TRSTE	MDDIS	19	VCCT	TPFOP	35	N/C	TEST1	51	RX_DV	VCCD
4	MF4	$\overline{\text{RESET}}$	20	TREF	TPFON	36	N/C	LEDCFG3	52	GNDIO	RX_CLK
5	MF3	TXSLEW0	21	TPOP	VCCA	37	VCCR	LEDCFG2	53	VCCIO	RX_ER
6	MF2	TXSLEW1	22	GNDT	VCCA	38	LEDS	LEDCFG1	54	RX_CLK	TX_ER
7	MF1	GND	23	TPON	TPFIP	39	LEDC	PWRDWN	55	RX_ER	TX_CLK
8	MF0	VCCIO	24	VCCA	TPFIN	40	LEDL	VCCIO	56	TX_ER	TX_EN
9	VCCD	N/C	25	RBIAS	GND	41	LEDT	GND	57	TX_CLK	TXD0
10	TEST	N/C	26	GNDA	SD/$\overline{\text{TP}}$	42	LEDR	MDIO	58	TX_EN	TXD1
11	XO	GND	27	FIBIP	TDI	43	GNDD	MDC	59	TXD0	TXD2
12	XI	ADDR0	28	FIBIN	TDO	44	MDIO	N/C	60	TXD1	TXD3
13	FDE	ADDR1	29	TPIP	TMS	45	MDC	RXD3	61	TXD2	N/C
14	CFG0	ADDR2	30	TPIN	TCK	46	RXD4	RXD2	62	TXD3	COL
15	MDDIS	ADDR3	31	GNDR	$\overline{\text{TRST}}$	47	RXD3	RXD1	63	TXD4	CRS
16	RESET	ADDR4	32	N/C	SLEEP	48	RXD2	RXD0	64	COL	$\overline{\text{MDINT}}$