

1 Mbit SPI™ Bus Serial Flash

Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
25LC1024	2.5-5.5V	256 Byte	I, E	P, SM, MF
25AA1024	1.8-5.5V	256 Byte	I	P, SM, MF

Features

- Max. clock 20 MHz
- Flash and byte-level serial EEPROM operation
- Low-power CMOS technology
 - Max. Write Current: 5 mA at 5.5V, 20 MHz
 - Read Current: 10 mA at 5.5V, 20 MHz
 - Standby Current: 1µA at 5.5V (Deep power-down)
- 131,072 x 8-bit organization
- Byte and Page (256 byte page) Write Operations (5 ms max.)
- Electronic Signature for device ID
- Self-timed ERASE and WRITE cycles
 - Sector Erase (1 second/sector typical)
 - Bulk Erase (2 seconds typical)
- Sector write protection (32K byte/sector)
 - Protect none, 1/4, 1/2 or all of array
- Built-in write protection
 - Power-on/off data protection circuitry
 - Write enable latch
 - Write-protect pin
- High reliability
 - Endurance: 100,000 erase/write cycles
- Temperature ranges supported;
 - Industrial (I): -40°C to +85°C
 - Automotive (E): -40°C to +125°C
- Standard and Pb-free packages available

Pin Function Table

Name	Function
$\overline{\text{CS}}$	Chip Select Input
SO	Serial Data Output
$\overline{\text{WP}}$	Write-Protect
Vss	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{\text{HOLD}}$	Hold Input
Vcc	Supply Voltage

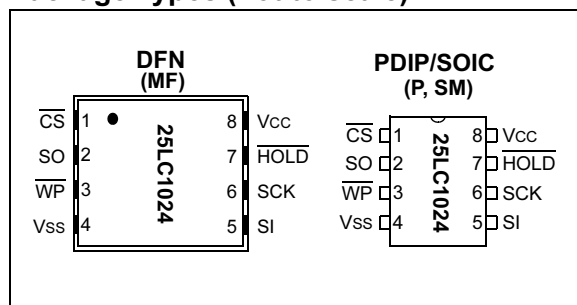
Description

The Microchip Technology Inc. 25AA1024/25LC1024 (25XX1024*) is a 1024 Kbit serial reprogrammable Flash memory with both Flash and byte-level serial EEPROM functions. The memory is accessed via a simple Serial Peripheral Interface™ (SPI™) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled by a Chip Select (CS) input.

Communication to the device can be paused via the hold pin (HOLD). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The 25XX1024 is available in standard packages including 8-lead PDIP and SOIC, and advanced 8-lead DFN package. Pb-free (Pure Sn) finish is also available.

Package Types (not to scale)



SPI is a registered trademark of Motorola Semiconductor.

*25XX1024 is used in this document as a generic part number for the 25AA1024, 25LC1024 devices.

25AA1024/25LC1024

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

V _{CC}	6.5V
All inputs and outputs w.r.t. V _{SS}	-0.6V to V _{CC} +1.0V
Storage temperature	-65°C to 150°C
Ambient temperature under bias	-40°C to 125°C
ESD protection on all pins	4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): Automotive (E):		TA = -40°C to +85°C TA = -40°C to +125°C	V _{CC} = 1.8V to 5.5V V _{CC} = 2.5V to 5.5V
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
D001	V _{IH1}	High-level input voltage	.7 V _{CC}	V _{CC} +1	V	
D002	V _{IL1}	Low-level input voltage	-0.3	0.3 V _{CC}	V	V _{CC} ≥ 2.7V
D003	V _{IL2}		-0.3	0.2 V _{CC}	V	V _{CC} < 2.7V
D004	V _{OL}	Low-level output voltage	—	0.4	V	I _{OL} = 2.1 mA
D005	V _{OL}		—	0.2	V	I _{OL} = 1.0 mA, V _{CC} < 2.5V
D006	V _{OH}	High-level output voltage	V _{CC} -0.5	—	V	I _{OH} = -400 μA
D007	I _{LI}	Input leakage current		±1	μA	$\overline{CS}$ = V _{CC} , V _{IN} = V _{SS} TO V _{CC}
D008	I _{LO}	Output leakage current		±1	μA	$\overline{CS}$ = V _{CC} , V _{OUT} = V _{SS} TO V _{CC}
D009	C _{INT}	Internal capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, CLK = 1.0 MHz, V _{CC} = 5.0V (Note)
D010	I _{CC} Read	Operating current	—	10	mA	V _{CC} = 5.5V; F _{CLK} = 20.0 MHz; SO = Open
			—	5	mA	V _{CC} = 2.5V; F _{CLK} = 10.0 MHz; SO = Open
D011	I _{CC} Write		—	5	mA	V _{CC} = 5.5V
			—	3	mA	V _{CC} = 2.5V
D012	I _{CCS}	Standby current	—	20	μA	$\overline{CS}$ = V _{CC} = 5.5V, Inputs tied to V _{CC} or V _{SS} , 125°C
			—	10	μA	$\overline{CS}$ = V _{CC} = 5.5V, Inputs tied to V _{CC} or V _{SS} , 85°C
D13	I _{CCSPD}	Deep power-down current	—	1	μA	$\overline{CS}$ = V _{CC} = 5.5V, Inputs tied to V _{CC} or V _{SS}

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): Automotive (E):		TA = -40°C to +85°C TA = -40°C to +125°C	VCC = 1.8V TO 5.5V VCC = 2.5V to 5.5V
Param. No.	Sym	Characteristic	Min	Max	Units	Conditions
1	FCLK	Clock frequency	—	20	MHz	4.5 ≤ VCC ≤ 5.5
			—	10	MHz	2.5 ≤ VCC < 4.5
			—	2	MHz	1.8 ≤ VCC < 2.5
2	Tcss	CS setup time	25	—	ns	4.5 ≤ VCC ≤ 5.5
			50	—	ns	2.5 ≤ VCC < 4.5
			250	—	ns	1.8 ≤ VCC < 2.5
3	TCSH	CS hold time	50	—	ns	4.5 ≤ VCC ≤ 5.5
			100	—	ns	2.5 ≤ VCC < 4.5
			500	—	ns	1.8 ≤ VCC < 2.5 (Note 3)
4	TcSD	CS disable time	50	—	ns	
5	Tsu	Data setup time	5	—	ns	4.5 ≤ VCC ≤ 5.5
			10	—	ns	2.5 ≤ VCC < 4.5
			50	—	ns	1.8 ≤ VCC < 2.5
6	THD	Data hold time	10	—	ns	4.5 ≤ VCC ≤ 5.5
			20	—	ns	2.5 ≤ VCC < 4.5
			100	—	ns	1.8 ≤ VCC < 2.5
7	TR	CLK rise time	—	20	ns	(Note 1)
8	TF	CLK fall time	—	20	ns	(Note 1)
9	THI	Clock high time	25	—	ns	4.5 ≤ VCC ≤ 5.5
			50	—	ns	2.5 ≤ VCC < 4.5
			250	—	ns	1.8 ≤ VCC < 2.5
10	TLO	Clock low time	25	—	ns	4.5 ≤ VCC ≤ 5.5
			50	—	ns	2.5 ≤ VCC < 4.5
			250	—	ns	1.8 ≤ VCC < 2.5
11	TCLD	Clock delay time	50	—	ns	
12	TCLE	Clock enable time	50	—	ns	
13	TV	Output valid from clock low	—	25	ns	4.5 ≤ VCC ≤ 5.5
			—	50	ns	2.8 ≤ VCC < 4.5
			—	250	ns	1.8 ≤ VCC < 2.5
14	THO	Output hold time	0	—	ns	(Note 1)
15	TDis	Output disable time	—	25	ns	4.5 ≤ VCC ≤ 5.5
			—	50	ns	2.5 ≤ VCC < 4.5
			—	250	ns	1.8 ≤ VCC < 2.5 (Note 1)
16	THS	HOLD setup time	10	—	ns	4.5 ≤ VCC ≤ 5.5
			20	—	ns	2.5 ≤ VCC < 4.5
			100	—	ns	1.8 ≤ VCC < 2.5
17	THH	HOLD hold time	10	—	ns	4.5 ≤ VCC ≤ 5.5
			20	—	ns	2.5 ≤ VCC < 4.5
			100	—	ns	1.8 ≤ VCC < 2.5

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from our web site.

3: Includes THi time.

25AA1024/25LC1024

TABLE 1-2: (CONTINUED) AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C				VCC = 1.8V to 5.5V VCC = 2.5V to 5.5V
Param. No.	Sym	Characteristic	Min	Max	Units	Conditions	
18	Thz	HOLD low to output High-Z	15 30 150	— — —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5 (Note 1)	
19	Thv	HOLD high to output valid	15 30 150	— — —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	
20	Trel	CS High to Standby mode	—	1.6	μs	VCC = 1.8V to 5.5V	
21	Tpd	CS High to Deep power-down	—	1.6	μs	VCC = 1.8V to 5.5V	
22	Tce	Chip erase cycle time	—	4	s	VCC = 1.8V to 5.5V	
23	Tse	Sector erase cycle time	—	2	s	VCC = 1.8V to 5.5V	
24	Twc	Internal write cycle time	—	5	ms	Byte or Page mode	
25	—	Endurance	100K	—	E/W Cycles	(Note 2)	

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from our web site.

3: Includes THi time.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
VLO = 0.2V	—
VHI = VCC - 0.2V	(Note 1)
VHI = 4.0V	(Note 2)
CL = 100 pF	—
Timing Measurement Reference Level	
Input	0.5 VCC
Output	0.5 VCC

Note 1: For VCC ≤ 4.0V

2: For VCC > 4.0V

FIGURE 1-1: HOLD TIMING

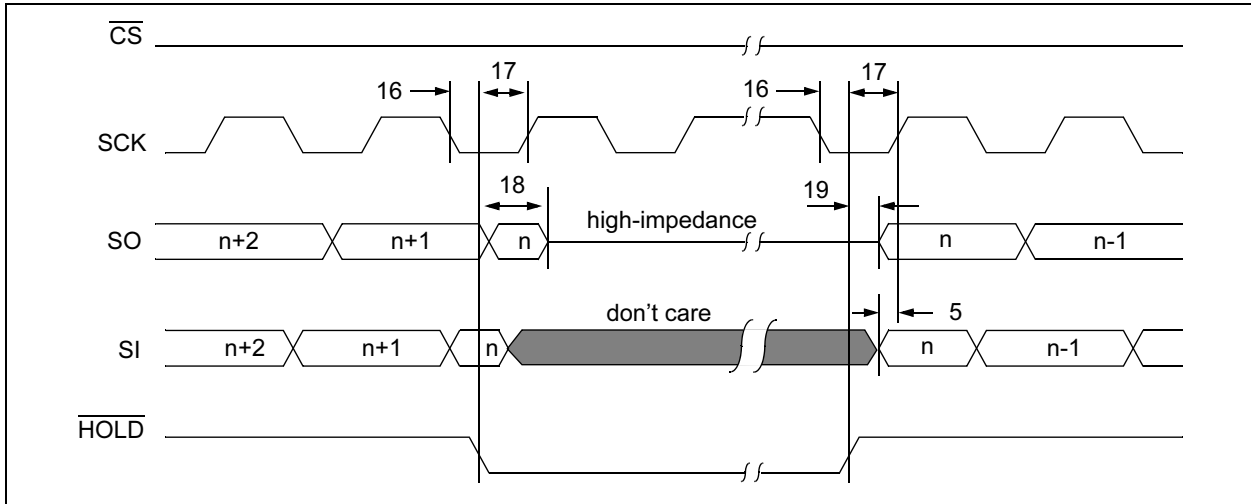


FIGURE 1-2: SERIAL INPUT TIMING

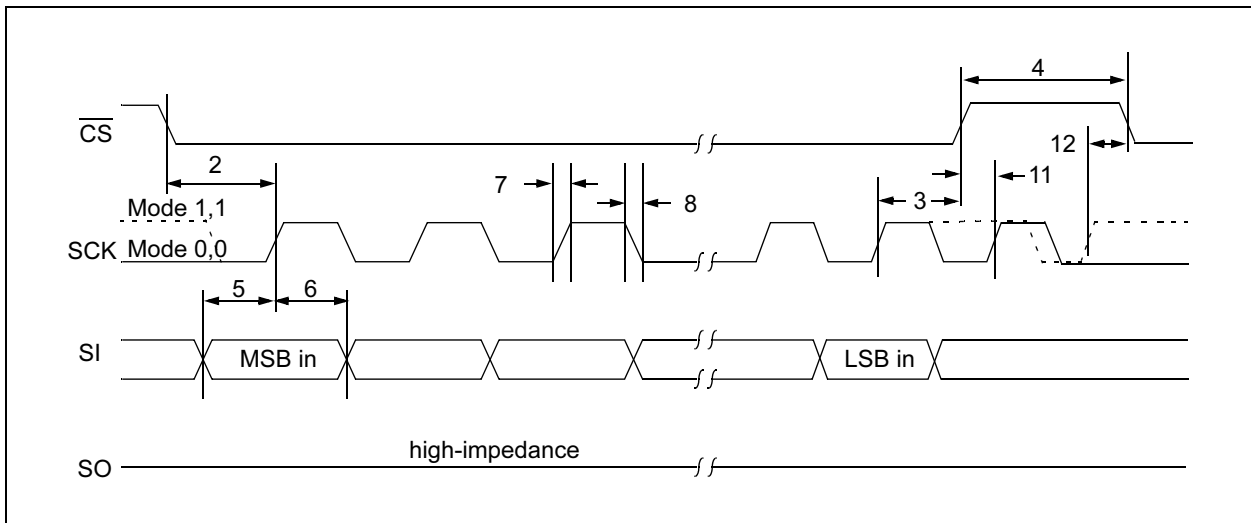
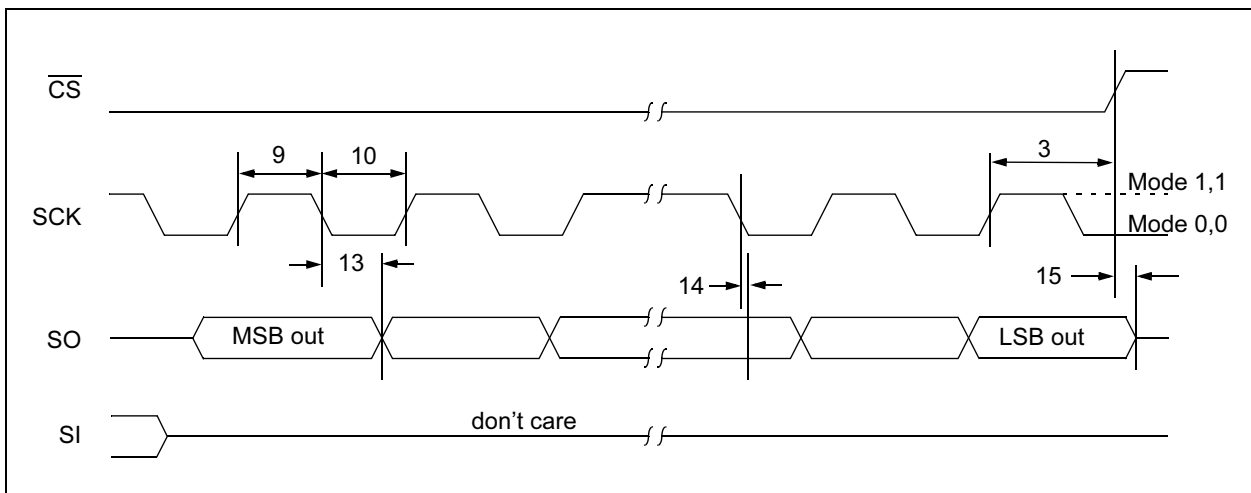


FIGURE 1-3: SERIAL OUTPUT TIMING



25AA1024/25LC1024

2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 25XX1024 is a 131,072 byte Serial Flash designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PICMicro® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

The 25XX1024 contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the HOLD pin must be high for the entire operation.

Table 2-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSB first, LSB last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input and place the 25XX1024 in 'HOLD' mode. After releasing the HOLD pin, operation will resume from the point when the HOLD was asserted.

2.2 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit read instruction is transmitted to the 25XX1024 followed by the 24-bit address, with seven MSBs of the address being don't care bits. After the correct read instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses. The internal address pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (1FFFFh), the address counter rolls over to address 00000h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin (Figure 2-1).

2.3 Write Sequence

Prior to any attempt to write data to the 25XX1024, the write enable latch must be set by issuing the WREN instruction (Figure 2-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25XX1024. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

Once the write enable latch is set, the user may proceed by setting the $\overline{CS}$ low, issuing a WRITE instruction, followed by the 24-bit address, with seven MSBs of the address being don't care bits, and then the data to be written. Up to 256 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page.

Note: Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size'), and end at addresses that are integer multiples of page size - 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 2-2 and Figure 2-3 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the Status Register may be read to check the status of the WPEN, WIP, WEL, BP1 and BP0 bits (Figure 2-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

25AA1024/25LC1024

FIGURE 2-2: BYTE WRITE SEQUENCE

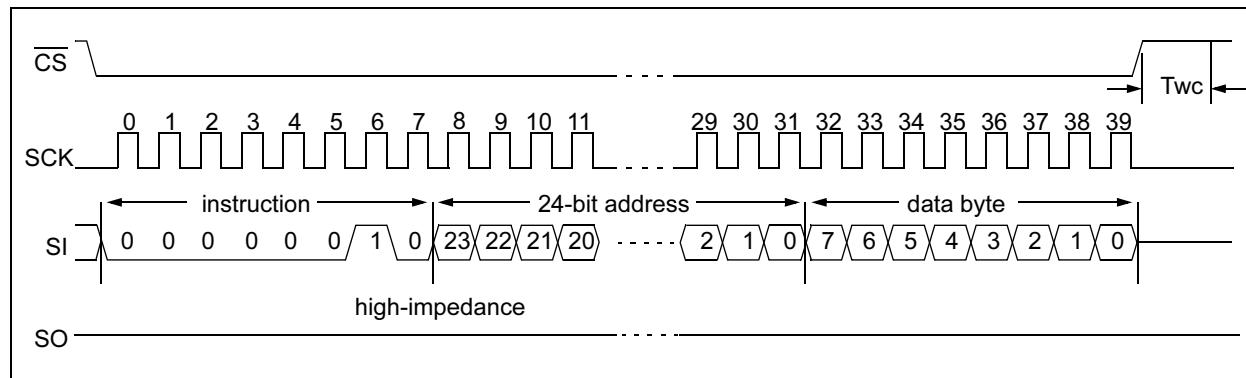
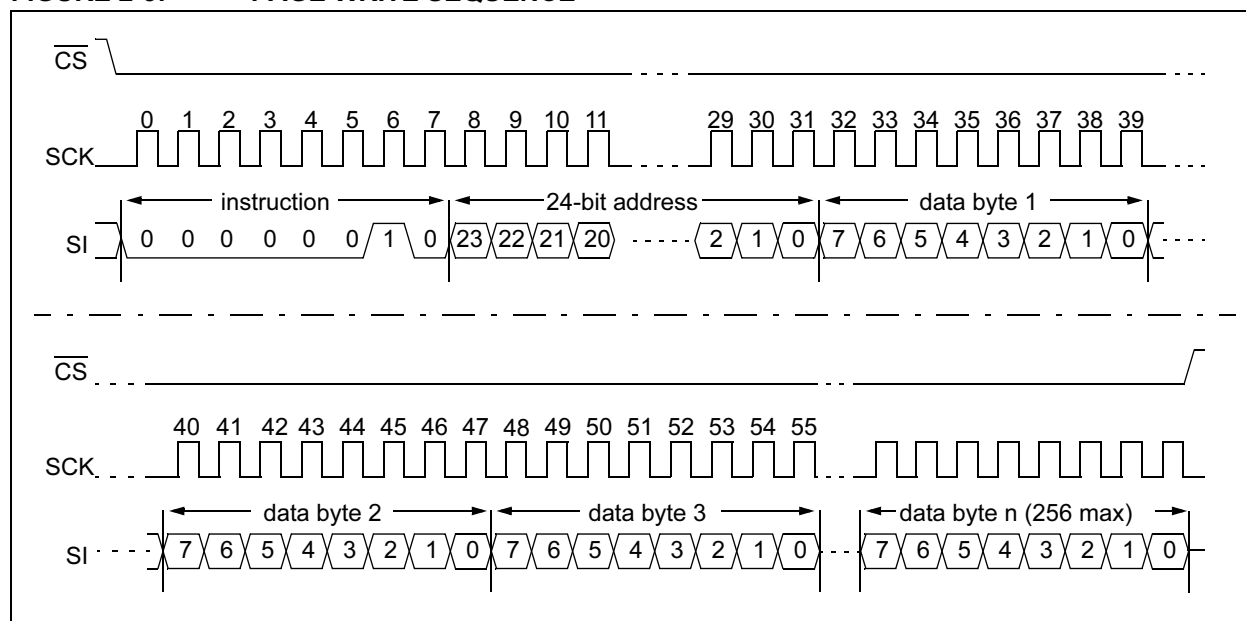


FIGURE 2-3: PAGE WRITE SEQUENCE



2.4 Write Enable (WREN) and Write Disable (WRDI)

The 25XX1024 contains a write enable latch. See Table 2-4 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed

FIGURE 2-4: WRITE ENABLE SEQUENCE (WREN)

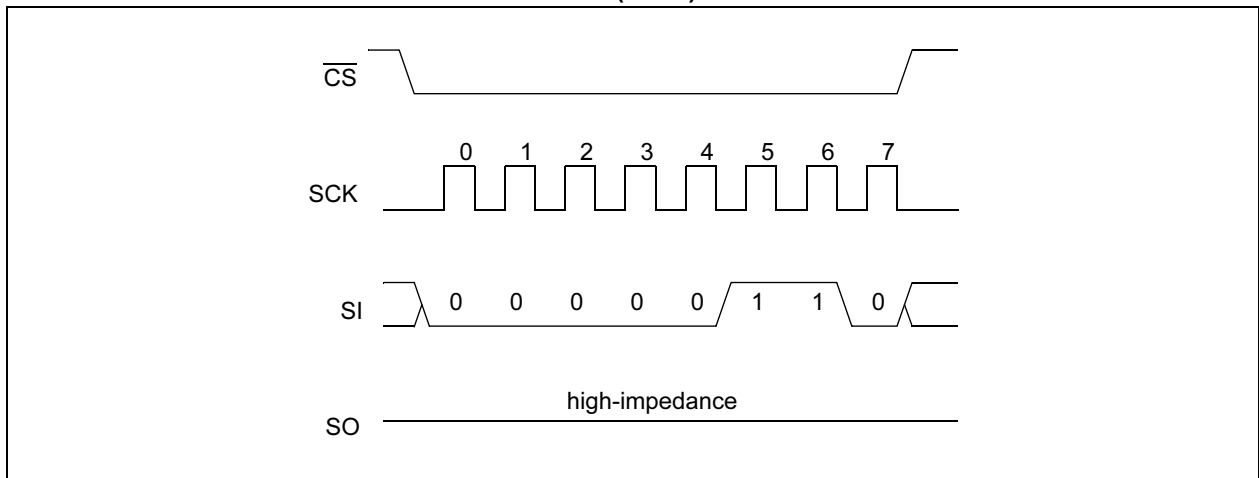
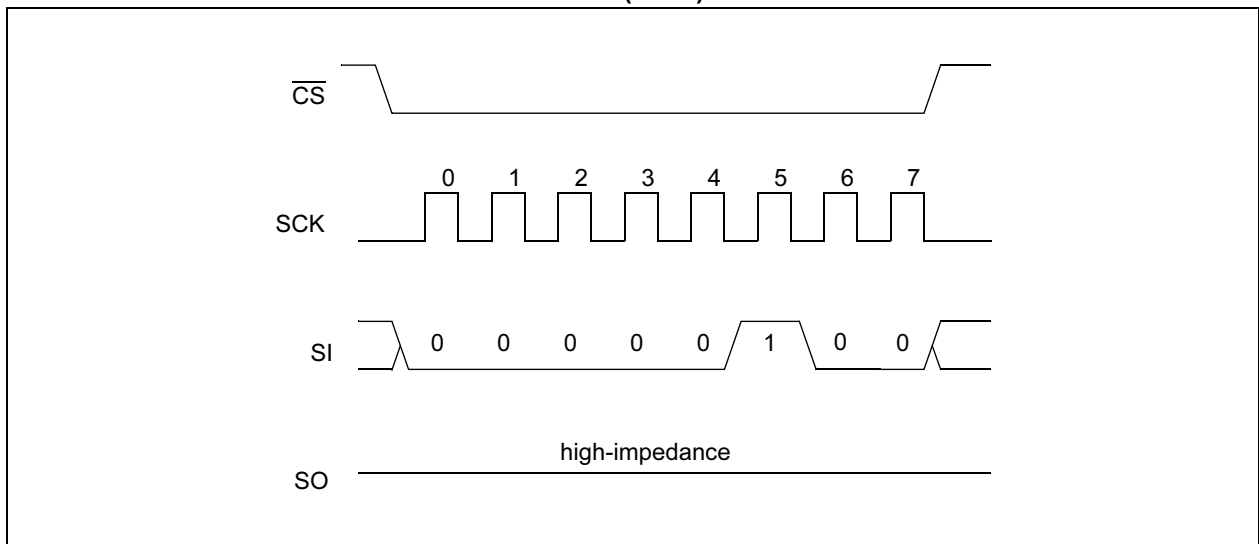


FIGURE 2-5: WRITE DISABLE SEQUENCE (WRDI)



25AA1024/25LC1024

2.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the Status Register. The Status Register may be read at any time, even during a write cycle. The Status Register is formatted as follows:

TABLE 2-2: STATUS REGISTER

7	6	5	4	3	2	1	0
W/R	–	–	–	W/R	W/R	R	R
WPEN	X	X	X	BP1	BP0	WEL	WIP
W/R = writable/readable. R = read-only.							

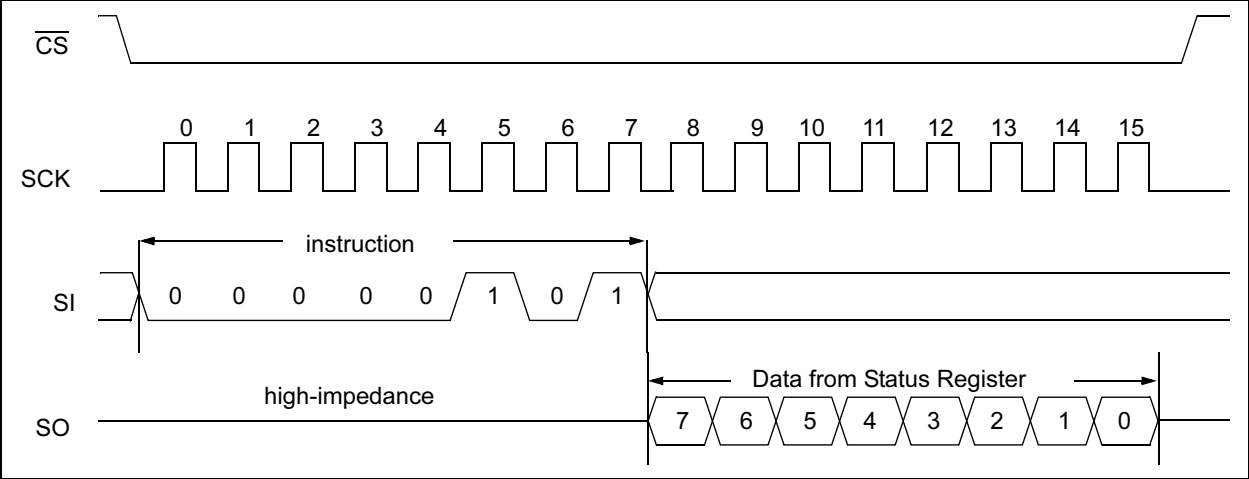
The **Write-In-Process (WIP)** bit indicates whether the 25XX1024 is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the Status Register. These commands are shown in Figure 2-4 and Figure 2-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction. These bits are nonvolatile, and are shown in Table 2-3.

See Figure 2-6 for the RDSR timing sequence.

FIGURE 2-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



2.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the Status Register as shown in Table 2-2. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the Status Register. The array is divided up into four segments. The user has the ability to write-protect none, one, two or all four of the segments of the array. The partitioning is controlled as shown in Table 2-3.

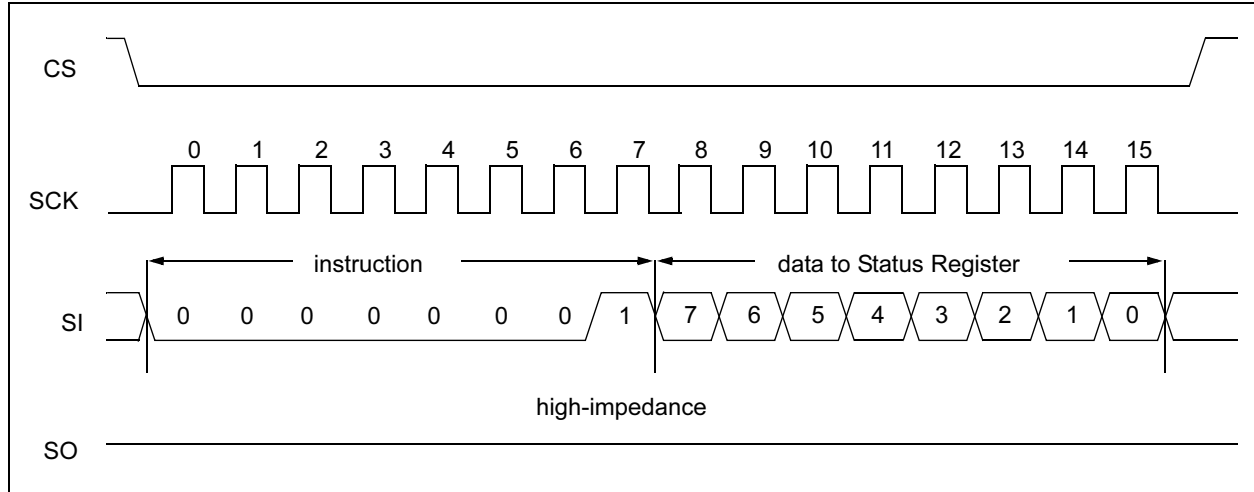
The Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write-Protect ($\overline{WP}$) pin and the Write-Protect Enable (WPEN) bit in the Status Register control the programmable hardware write-protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write-protected, only writes to nonvolatile bits in the Status Register are disabled. See Table 2-4 for a matrix of functionality on the WPEN bit.

See Figure 2-7 for the WRSR timing sequence.

TABLE 2-3: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected	Array Addresses Unprotected
0	0	none	All (Sectors 0, 1, 2 & 3) (00000h - 1FFFFh)
0	1	Upper 1/4 (Sector 3) (18000h - 1FFFFh)	Lower 3/4 (Sectors 0, 1 & 2) (00000h - 17FFFh)
1	0	Upper 1/2 (Sectors 2 & 3) (10000h - 1FFFFh)	Lower 1/2 (Sectors 0 & 1) (00000h - 0FFFFh)
1	1	All (Sectors 0, 1, 2 & 3) (00000h - 1FFFFh)	none

FIGURE 2-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



25AA1024/25LC1024

2.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or Status Register write, the write enable latch is reset
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

2.8 Power-On State

The 25XX1024 powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS} = 1$)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{CS}$ is required to enter active state

TABLE 2-4: WRITE-PROTECT FUNCTIONALITY MATRIX

WEL (SR bit 1)	WPEN (SR bit 7)	$\overline{WP}$ (pin 3)	Protected Blocks	Unprotected Blocks	Status Register
0	x	x	Protected	Protected	Protected
1	0	x	Protected	Writable	Writable
1	1	0 (low)	Protected	Writable	Protected
1	1	1 (high)	Protected	Writable	Writable

x = don't care

2.9 PAGE ERASE

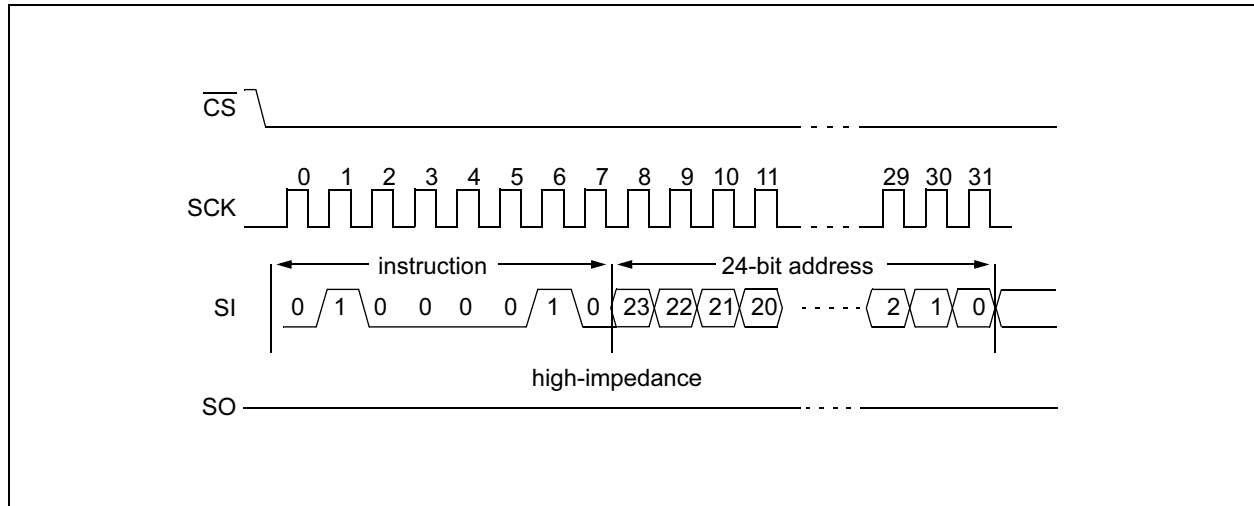
The Page Erase function will erase all bits (FFh) inside the given page. A Write Enable (WREN) instruction must be given prior to attempting a Page Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25XX1024. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

The Page Erase function is entered by driving $\overline{CS}$ low, followed by the instruction code Figure 2-8, and three address bytes. Any address inside the page to be erased is a valid address.

$\overline{CS}$ must then be driven high after the last bit if the address or the Page Erase will not execute. Once the $\overline{CS}$ is driven high the self-timed Page Erase cycle is started. The WIP bit in the Status Register can be read to determine when the Page Erase cycle is complete.

If a Page Erase function is given to an address that has been protected by the Block Protect bits (BP0, BP1) then the sequence will be aborted and no erase will occur.

FIGURE 2-8: PAGE ERASE SEQUENCE



25AA1024/25LC1024

2.10 SECTOR ERASE

The Sector Erase function will erase all bits (FFh) inside the given sector. A Write Enable (WREN) instruction must be given prior to attempting a Sector Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25XX1024. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

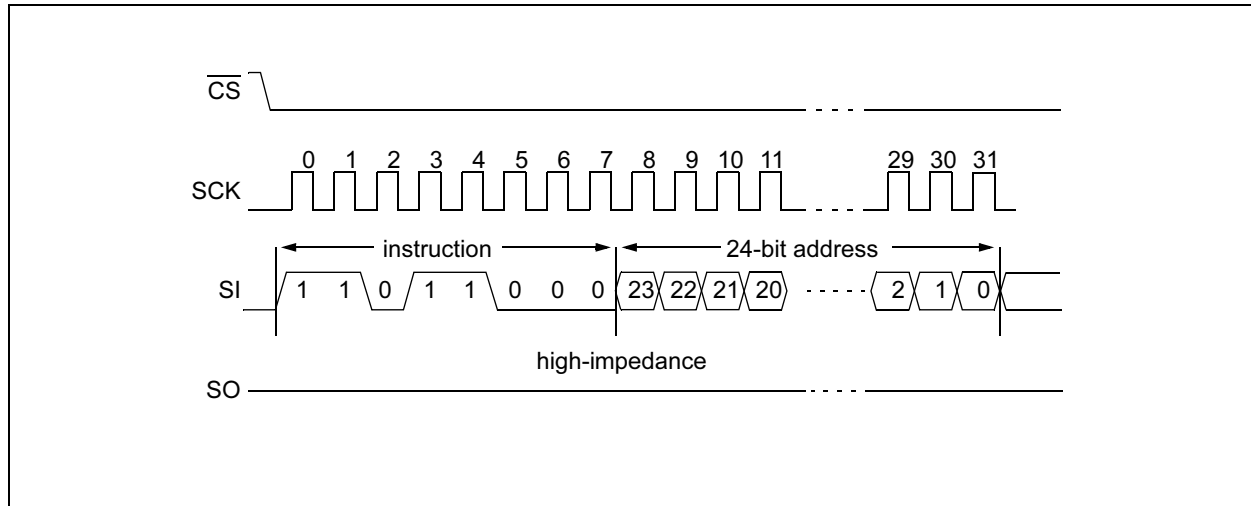
The Sector Erase function is entered by driving $\overline{CS}$ low, followed by the instruction code Figure 2-9, and three address bytes. Any address inside the sector to be erased is a valid address.

$\overline{CS}$ must then be driven high after the last bit if the address or the Sector Erase will not execute. Once the $\overline{CS}$ is driven high the self-timed Sector Erase cycle is started. The WIP bit in the Status Register can be read to determine when the Sector Erase cycle is complete.

If a Sector Erase instruction is given to an address that has been protected by the Block Protect bits (BP0, BP1) then the sequence will be aborted and no erase will occur.

See Table 2-3 for Sector Addressing.

FIGURE 2-9: SECTOR ERASE SEQUENCE



2.11 CHIP ERASE

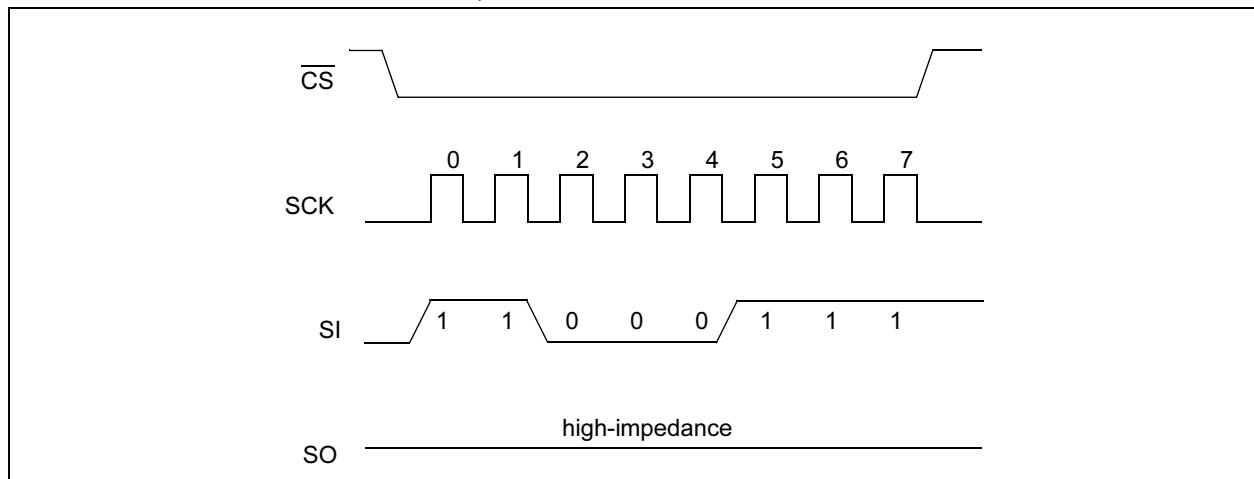
The Chip Erase function will erase all bits (FFh) in the array. A Write Enable (WREN) instruction must be given prior to executing a Chip Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the 25XX1024. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

The Chip Erase function is entered by driving the $\overline{CS}$ low, followed by the instruction code (Figure 2-10) onto the SI line.

The $\overline{CS}$ pin must be driven high after the eighth bit of the instruction code has been given or the Chip Erase function will not be executed. Once the $\overline{CS}$ pin is driven high the self-timed Chip Erase function begins. While the device is executing the Chip Erase function the WIP bit in the Status Register can be read to determine when the Chip Erase function is complete.

The Chip Erase function is ignored if either of the Block Protect bits (BP0, BP1) are not 0, meaning 1/4, 1/2, or all of the array is protected.

FIGURE 2-10: CHIP ERASE SEQUENCE



2.12 DEEP POWER-DOWN MODE

Deep Power-down Mode of the 25XX1024 is its lowest power consumption state. The device will not respond to any of the read or write commands while in Deep Power-down mode, and therefore it can be used as an additional software write protection feature.

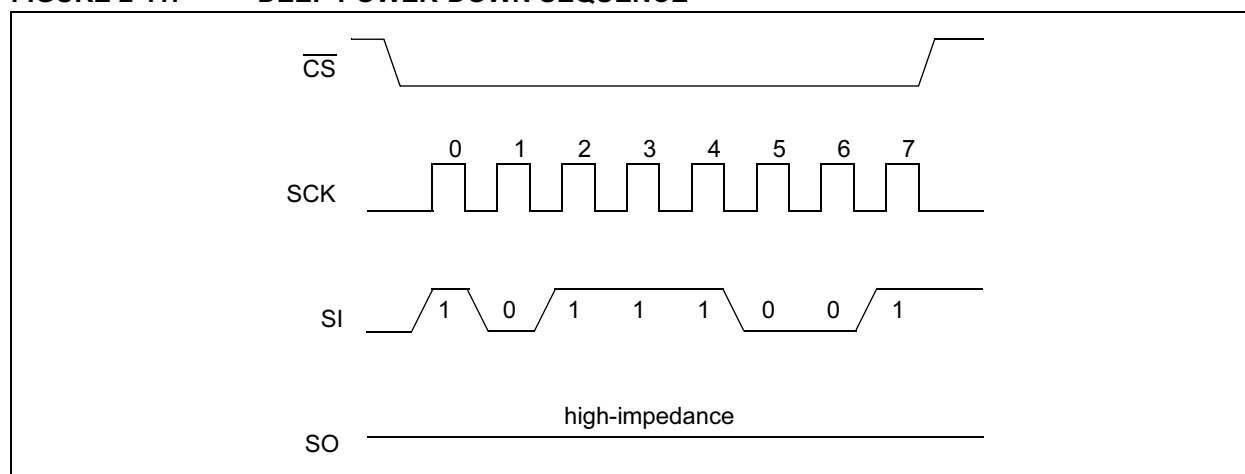
The Deep Power-down mode is entered by driving $\overline{\text{CS}}$ low, followed by the instruction code (Figure 2-11) onto the SI line, followed by driving $\overline{\text{CS}}$ high.

If the $\overline{\text{CS}}$ pin is not driven high after the eighth bit of the instruction code has been given, the device will not execute Deep power-down. Once the $\overline{\text{CS}}$ line is driven high there is a delay (T_{DP}) before the current settles to its lowest consumption.

All instructions given during Deep Power-down mode are ignored except the Read Electronic Signature Command (RDID). The RDID command will release the device from Deep power-down and outputs the electronic signature on the SO pin, and then returns the device to Standby mode after delay (T_{REL}).

Deep Power-down mode automatically releases at device power-down. Once power is restored to the device it will power-up in the Standby mode.

FIGURE 2-11: DEEP POWER-DOWN SEQUENCE



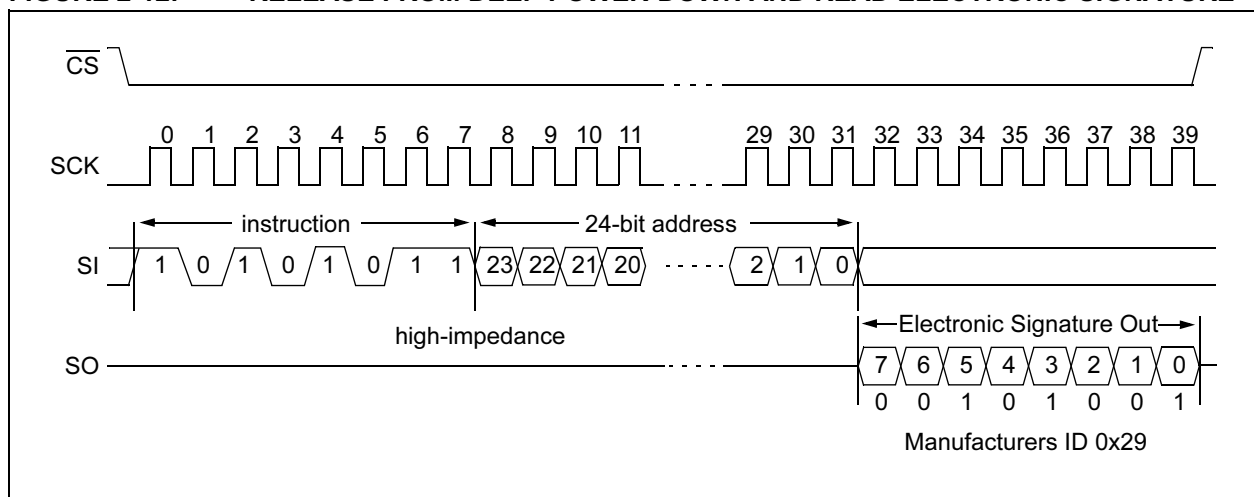
2.13 RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE

Once the device has entered Deep Power-down mode all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature command. This command can also be used when the device is not in Deep Power-down to read the electronic signature out on the SO pin unless another command is being executed such as Erase, Program or Write Status Register.

Release from Deep Power-down mode and Read Electronic Signature is entered by driving $\overline{CS}$ low, followed by the RDID instruction code (Figure 2-12) and then a dummy address of 24 bits (A23-A0). After the last bit of the dummy address is clock in, the 8-bit Electronic signature is clocked out on the SO pin.

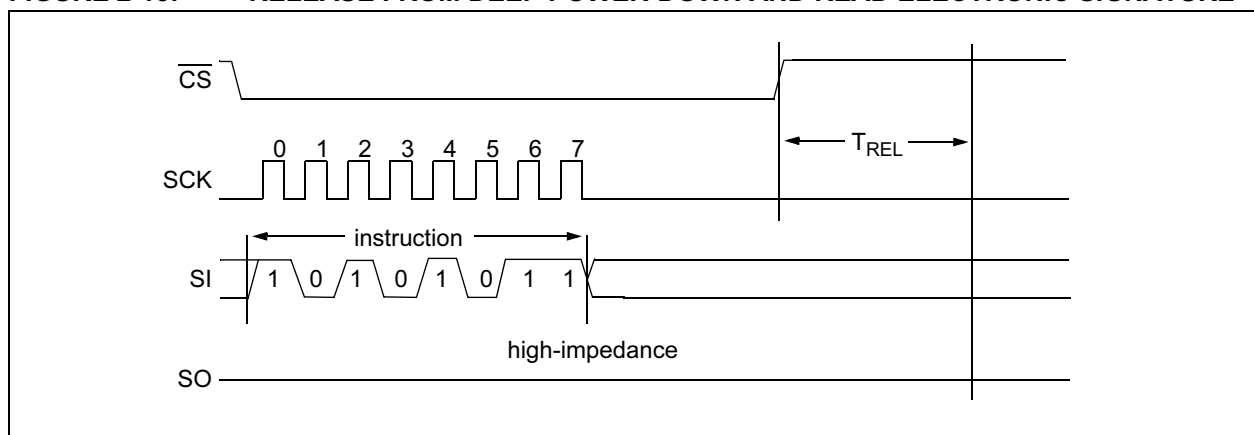
After the signature has been read out at least once, the sequence can be terminated by driving $\overline{CS}$ high. The device will then return to Standby mode and will wait to be selected so it can be given new instructions. If additional clock cycles are sent after the electronic signature has been read once, it will continue to output the signature on the SO line until the sequence is terminated.

FIGURE 2-12: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE



Driving $\overline{CS}$ high after the 8-bit RDID command but before the Electronic Signature has been transmitted will still ensure the device will be taken out of Deep Power-down mode. However, there is a delay T_{REL} that occurs before the device returns to Standby mode (I_{CCS}), as shown in Figure 2-13.

FIGURE 2-13: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE



3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	Pin Number	Function
$\overline{\text{CS}}$	1	Chip Select Input
SO	2	Serial Data Output
$\overline{\text{WP}}$	3	Write-Protect Pin
Vss	4	Ground
SI	5	Serial Data Input
SCK	6	Serial Clock Input
HOLD	7	Hold Input
Vcc	8	Supply Voltage

3.1 Chip Select ($\overline{\text{CS}}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{\text{CS}}$ input signal. If $\overline{\text{CS}}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{\text{CS}}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{\text{CS}}$ is required prior to any sequence being initiated.

3.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25XX1024. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

3.3 Write-Protect ($\overline{\text{WP}}$)

This pin is used in conjunction with the WPEN bit in the Status Register to prohibit writes to the nonvolatile bits in the Status Register. When $\overline{\text{WP}}$ is low and WPEN is high, writing to the nonvolatile bits in the Status Register is disabled. All other operations function normally. When $\overline{\text{WP}}$ is high, all functions, including writes to the nonvolatile bits in the Status Register, operate normally. If the WPEN bit is set, $\overline{\text{WP}}$ low during a Status Register write sequence will disable writing to the Status Register. If an internal write cycle has already begun, $\overline{\text{WP}}$ going low will have no effect on the write.

The $\overline{\text{WP}}$ pin function is blocked when the WPEN bit in the Status Register is low. This allows the user to install the 25XX1024 in a system with $\overline{\text{WP}}$ pin grounded and still be able to write to the Status Register. The $\overline{\text{WP}}$ pin functions will be enabled when the WPEN bit is set high.

3.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

3.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25XX1024. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

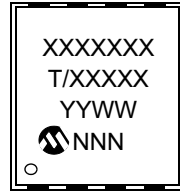
3.6 Hold (HOLD)

The HOLD pin is used to suspend transmission to the 25XX1024 while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the HOLD pin may be pulled low to pause further serial communication without resetting the serial sequence. The HOLD pin must be brought low while SCK is low, otherwise the HOLD function will not be invoked until the next SCK high-to-low transition. The 25XX1024 must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, HOLD must be brought high while the SCK pin is low, otherwise serial communication will not resume. Pulling the HOLD line low at any time will tri-state the SO line.

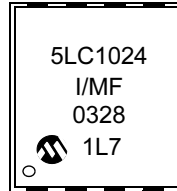
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

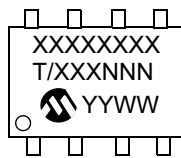
8-Lead DFN



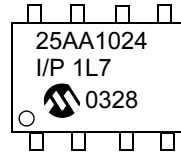
Example:



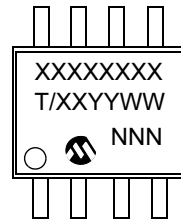
8-Lead PDIP



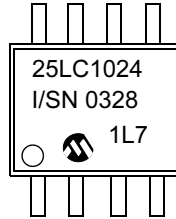
Example:



8-Lead SOIC



Example:

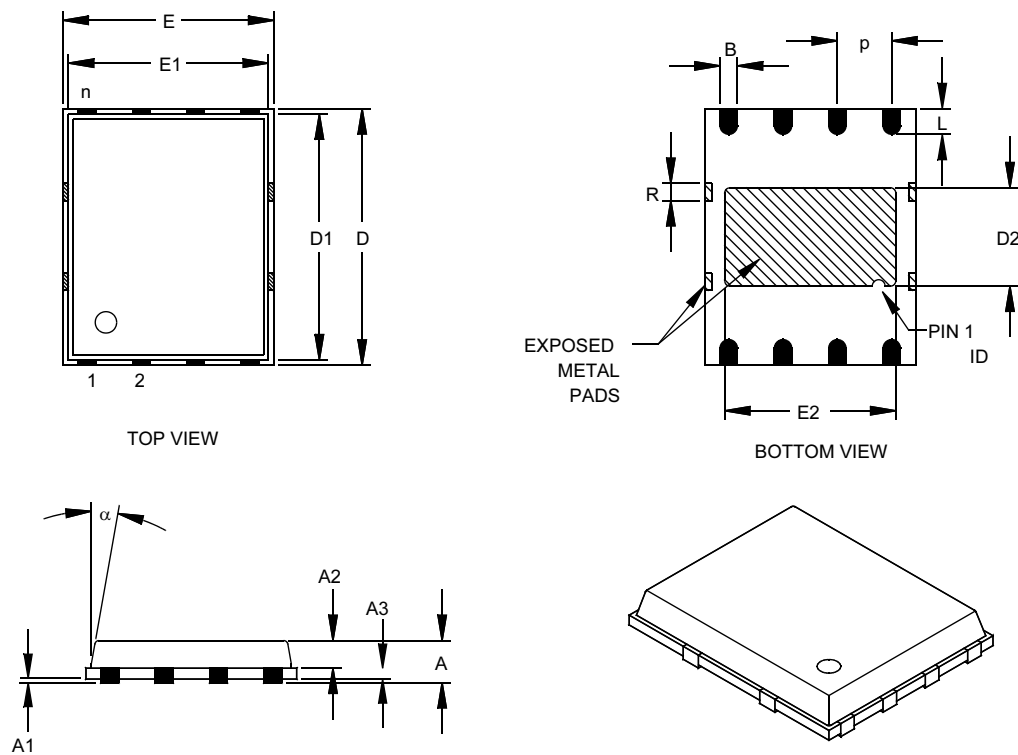


Legend:	XX...X	Part number
	T	Temperature (I,E)
	Blank	Commercial
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code

Note: Custom marking available.

25AA1024/25LC1024

8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p	.050 BSC			1.27 BSC		
Overall Height	A		.033	.039		0.85	1.00
Molded Package Thickness	A2		.026	.031		0.65	0.80
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05
Base Thickness	A3	.008 REF.			0.20 REF.		
Overall Length	E	.194 BSC			4.92 BSC		
Molded Package Length	E1	.184 BSC			4.67 BSC		
Exposed Pad Length	E2	.152	.158	.163	3.85	4.00	4.15
Overall Width	D	.236 BSC			5.99 BSC		
Molded Package Width	D1	.226 BSC			5.74 BSC		
Exposed Pad Width	D2	.085	.091	.097	2.16	2.31	2.46
Lead Width	B	.014	.016	.019	0.35	0.40	0.47
Lead Length	L	.020	.024	.030	0.50	0.60	0.75
Tie Bar Width	R		.014			.356	
Mold Draft Angle Top	α			12°			12°

*Controlling Parameter

Notes:

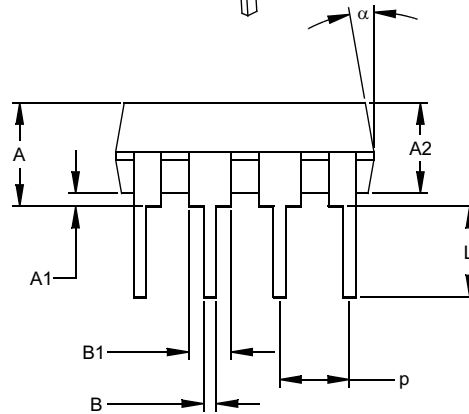
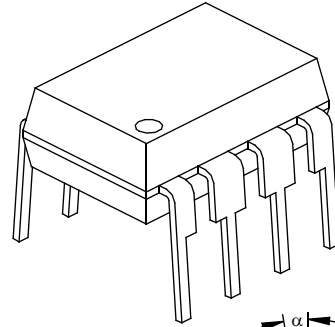
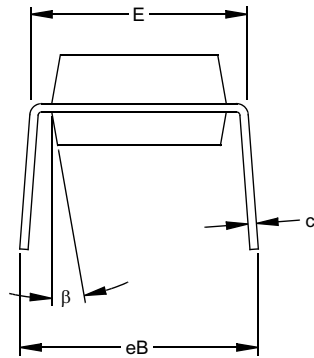
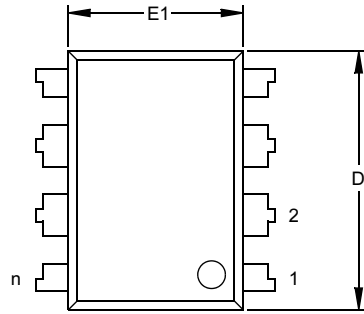
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC equivalent: pending

Drawing No. C04-113

25AA1024/25LC1024

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

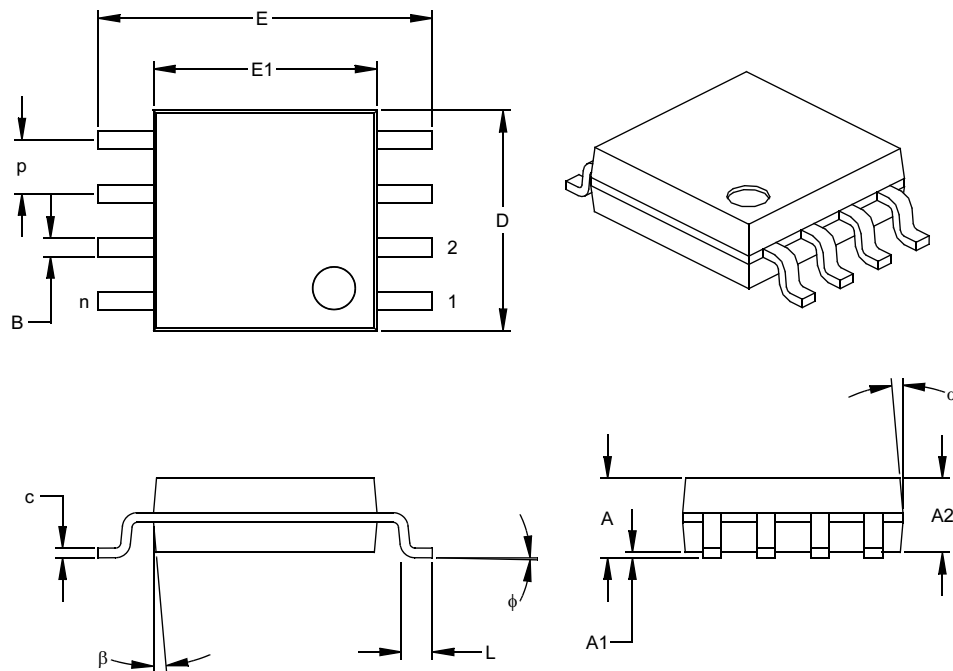
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

25AA1024/25LC1024

8-Lead Plastic Small Outline (SM) – Medium, 208 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.070	.075	.080	1.78	1.97	2.03
Molded Package Thickness	A2	.069	.074	.078	1.75	1.88	1.98
Standoff §	A1	.002	.005	.010	0.05	0.13	0.25
Overall Width	E	.300	.313	.325	7.62	7.95	8.26
Molded Package Width	E1	.201	.208	.212	5.11	5.28	5.38
Overall Length	D	.202	.205	.210	5.13	5.21	5.33
Foot Length	L	.020	.025	.030	0.51	0.64	0.76
Foot Angle	φ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.014	.017	.020	0.36	0.43	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

Drawing No. C04-056

ON-LINE SUPPORT

Microchip provides on-line support on the Microchip World Wide Web site.

The web site is used by Microchip as a means to make files and information easily available to customers. To view the site, the user must have access to the Internet and a web browser, such as Netscape® or Microsoft® Internet Explorer. Files are also available for FTP download from our FTP site.

Connecting to the Microchip Internet Web Site

The Microchip web site is available at the following URL:

www.microchip.com

The file transfer site is available by using an FTP service to connect to:

<ftp://ftp.microchip.com>

The web site and file transfer site provide a variety of services. Users may download files for the latest Development Tools, Data Sheets, Application Notes, User's Guides, Articles and Sample Programs. A variety of Microchip specific business information is also available, including listings of Microchip sales offices, distributors and factory representatives. Other data available for consideration is:

- Latest Microchip Press Releases
- Technical Support Section with Frequently Asked Questions
- Design Tips
- Device Errata
- Job Postings
- Microchip Consultant Program Member Listing
- Links to other useful web sites related to Microchip Products
- Conferences for products, Development Systems, technical information and more
- Listing of seminars and events

SYSTEMS INFORMATION AND UPGRADE HOT LINE

The Systems Information and Upgrade Line provides system users a listing of the latest versions of all of Microchip's development systems software products. Plus, this line provides information on how customers can receive the most current upgrade kits. The Hot Line Numbers are:

1-800-755-2345 for U.S. and most of Canada, and

1-480-792-7302 for the rest of the world.

042003

READER RESPONSE

It is our intention to provide you with the best documentation possible to ensure successful use of your Microchip product. If you wish to provide your comments on organization, clarity, subject matter, and ways in which our documentation can better serve you, please FAX your comments to the Technical Publications Manager at (480) 792-4150.

Please list the following information, and use this outline to provide us with your comments about this document.

To: Technical Publications Manager
RE: Reader Response
Total Pages Sent _____
From: Name _____
Company _____
Address _____
City / State / ZIP / Country _____
Telephone: (____) _____ - _____ FAX: (____) _____ - _____

Application (optional):

Would you like a reply? ___Y ___N

Device: 25AA1024/25LC1024

Literature Number: DS21836A

Questions:

1. What are the best features of this document?

2. How does this document meet your hardware and software development needs?

3. Do you find the organization of this document easy to follow? If not, why?

4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>-</u>	<u>X</u>	<u>/XX</u>	<u>X</u>
Device	Tape & Reel		Temp Range	Package	Lead Finish
Device	25AA1024		1 Mbit, 1.8V, 256-Byte Page SPI Serial Flash		
	25LC1024		1 Mbit, 2.5V, 256-Byte Page SPI Serial Flash		
Tape & Reel	Blank	=	Standard packaging (tube)		
	T	=	Tape & Reel		
Temperature Range	I	=	-40°C to+85°C		
	E	=	-40°C to+125°C		
Package	MF	=	Micro Lead Frame (6 x 5 mm body), 8-lead		
	P	=	Plastic DIP (300 mil body), 8-lead		
	SM	=	Plastic SOIC (207 mil body), 8-lead		
Lead Finish	Blank	=	Standard 63% / 37% Sn/Pb		
	G	=	Matte Tin (Pure Sn)		

Examples:

- a) 25AA1024-I/SMG = 1 Mbit, 1.8V Serial Flash, Industrial temp., SOIC package, Pb-free
- b) 25AA1024T-I/SM = 1 Mbit, 1.8V Serial Flash, Industrial temp., Tape & Reel, SOIC package
- c) 25AA1024T-I/MF = 1 Mbit, 1.8V Serial Flash, Industrial temp., Tape & Reel, DFN package
- d) 25LC1024-I/SMG = 1 Mbit, 2.5V Serial Flash, Industrial temp., SOIC package, Pb-free
- e) 25LC1024-I/P = 1 Mbit, 2.5V Serial Flash, Industrial temp., P-DIP package
- f) 25LC1024T-E/MF = 1 Mbit, 2.5V Serial Flash, Extended temp., Tape & Reel, DFN package

Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

1. Your local Microchip sales office
2. The Microchip Corporate Literature Center U.S. FAX: (480) 792-7277
3. The Microchip Worldwide Site (www.microchip.com)

Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

New Customer Notification System

Register on our web site (www.microchip.com/cn) to receive the most current information on our products.

25AA1024/25LC1024

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELoQ, MPLAB, PIC, PICmicro, PICSTART, PRO MATE and PowerSmart are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AmpLab, FilterLab, microID, MXDEV, MXLAB, PICMASTER, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

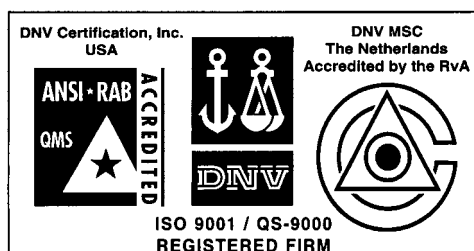
Application Maestro, dsPICDEM, dsPICDEM.net, ECAN, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, PICKit, PICDEM, PICDEM.net, PowerCal, PowerInfo, PowerMate, PowerTool, rLAB, rfPIC, Select Mode, SmartSensor, SmartShunt, SmartTel and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2003, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999 and Mountain View, California in March 2002. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, non-volatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Atlanta

3780 Mansell Road, Suite 130
Alpharetta, GA 30022
Tel: 770-640-0034
Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848
Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071
Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423
Fax: 972-818-2924

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo

2767 S. Albright Road
Kokomo, IN 46902
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888
Fax: 949-263-1338

Phoenix

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966
Fax: 480-792-4338

San Jose

2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950
Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Australia

Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing

Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100
Fax: 86-10-85282104

China - Chengdu

Rm. 2401-2402, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200
Fax: 86-28-86766599

China - Fuzhou

Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506
Fax: 86-591-7503521

China - Hong Kong SAR

Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Shanghai

Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700
Fax: 86-21-6275-5060

China - Shenzhen

Rm. 1812, 18/F, Building A, United Plaza
No. 5022 Binhe Road, Futian District
Shenzhen 518033, China
Tel: 86-755-82901380
Fax: 86-755-8295-1393

China - Shunde

Room 401, Hongjian Building
No. 2 Fengxiangnan Road, Ronggui Town
Shunde City, Guangdong 528303, China
Tel: 86-765-8395507 Fax: 86-765-8395571

China - Qingdao

Rm. B505A, Fullhope Plaza,
No. 12 Hong Kong Central Rd.
Qingdao 266071, China
Tel: 86-532-5027355 Fax: 86-532-5027205

India

Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaughnessy Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5932 or
82-2-558-5934

Singapore

200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Kaohsiung Branch
30F - 1 No. 8
Min Chuan 2nd Road
Kaohsiung 806, Taiwan
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan

Taiwan Branch
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Austria

Durisolstrasse 2
A-4600 Wels
Austria
Tel: 43-7242-2244-399
Fax: 43-7242-2244-393

Denmark

Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45-4420-9895 Fax: 45-4420-9910

France

Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany

Steinheilstrasse 10
D-85737 Ismaning, Germany
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy

Via Quasimodo, 12
20025 Legnano (MI)
Milan, Italy
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands

P. A. De Biesbosch 14
NL-5152 SC Drunen, Netherlands
Tel: 31-416-690399
Fax: 31-416-690340

United Kingdom

505 Eskdale Road
Wokingham
Berkshire, England RG41 5TU
Tel: 44-118-921-5869
Fax: 44-118-921-5820

07/28/03