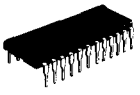
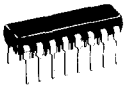
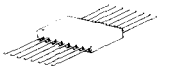
MC10,100/10,200 Series (-30 to +85°C)
MC10,500/10,600 Series (-55 to +125°C)

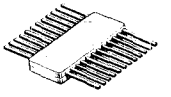
MECL 10,000 has an excellent speed-power product, has relatively slow rise and fall times, and transmission-line drive capability. The combination of versatile logic functions and the 2.0 ns propagation delay make MECL 10,000 a versatile family for data handling and processing systems.

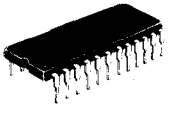
Circuit design with MECL 10,000 is unusually convenient. The differential amplifier input and emitter-follower output permit high fanout, the wired-OR option, and complementary outputs. MECL III is directly compatible with MECL 10,000, and can be used to extend the speed capability of the MECL 10,000 series.

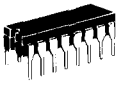

L SUFFIX
CERAMIC PACKAGE
CASE 623

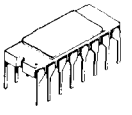

P SUFFIX
PLASTIC PACKAGE
CASE 648


F SUFFIX
CERAMIC PACKAGE
CASE 650


F SUFFIX
CERAMIC PACKAGE
CASE 652


P SUFFIX
PLASTIC PACKAGE
CASE 649


L SUFFIX
CERAMIC PACKAGE
CASE 620


AL SUFFIX
CERAMIC PACKAGE
CASE 690

FUNCTIONS AND CHARACTERISTICS (V_{CC} = 0, V_{EE} = -5.2 V, T_A = 25°C)

Function	Type① -30 to +85°C	Type① -55 to +125°C	Propagation Delay ns typ	Power Dissipation mW typ/pkg*	Case
Quad 2-Input NOR Gate With Strobe	MC10100	–	2.0	100	620
Quad OR/NOR Gate	MC10101	MC10501	2.0	100	620,648,650
Quad 2-Input NOR Gate	MC10102	MC10502	2.0	100	620,648,650
Quad 2-Input OR Gate	MC10103	–	2.0	100	620
Quad 2-Input AND Gate	MC10104	MC10504	2.7	140	620,648,650
Triple 2-3-2-Input OR/NOR Gate	MC10105	MC10505	2.0	90	620,648,650
Triple 4-3-3-Input NOR Gate	MC10106	MC10506	2.0	90	620,648,650
Triple 2-Input Exclusive OR/Exclusive NOR	MC10107	MC10507	2.5	110	620,648,650
Dual 4-5-Input OR/NOR Gate	MC10109	MC10509	2.0	60	620,648,650
Dual 3-Input 3-Output OR Gate	MC10110	–	2.4	160	620,648
Dual 3-Input 3-Output NOR Gate	MC10111	–	2.4	160	620,648
Quad Exclusive OR Gate	MC10113	–	2.5	175	620
Triple Line Receiver	MC10114	MC10514	2.4	145	620,648,650
Quad Line Receiver	MC10115	MC10515	2.0	110	620,648,650
Triple Line Receiver	MC10116	MC10516	2.0	85	620,648,650
Dual 2-Wide 2-3-Input OR-AND/OR-AND-INVERT Gate	MC10117	MC10517	2.3	100	620,648,650
Dual 2-Wide 3-Input OR-AND Gate	MC10118	MC10518	2.3	100	620,648,650
4-Wide 4-3-3-3-Input OR-AND Gate	MC10119	MC10519	2.3	100	620,648,650
4-Wide OR-AND/OR-AND-INVERT Gate	MC10121	MC10521	2.3	100	620,648,650
Triple 4-3-3-Input Bus Driver	MC10123	–	3.0	310	620
Quad MTTL to MECL Translator	MC10124	MC10524	3.5	380	620,648,650
Quad MECL to MTTL Translator	MC10125	MC10525	4.5	380	620,648,650
Dual MECL to MOS Translator	MC10127	–	–	–	620
Bus Driver	MC10128	–	12.0	700	620
Quad Bus Receiver	MC10129	–	10.0	750	620
Dual Latch	MC10130	MC10530	2.5	155	620,648,650
Dual Type D Master-Slave Flip-Flop	MC10131	MC10531	f = 160 MHz	235	620,648,650
Dual Multiplexer With Latch and Common Reset	MC10132	–	3.0	225	620,648
Quad Latch	MC10133	MC10533	4.0	310	620,648,650
Multiplexer with Latch	MC10134	–	3.0	225	620,648
Dual J-K Master-Slave Flip-Flop	MC10135	MC10535	f = 140 MHz	280	620,648,650
Universal Hexadecimal Counter	MC10136	MC10536	f = 150 MHz	625	620,650

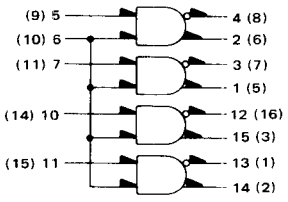
① L suffix denotes Dual In-Line Ceramic Package, P suffix denotes Dual In-Line Plastic Package, F suffix denotes flat package (i.e., MC10100L = Ceramic Dual In-Line Package, MC10100P = Plastic Dual In-Line Package and MC10500F = Ceramic Flat Package.)

*External Load Power not included.

2

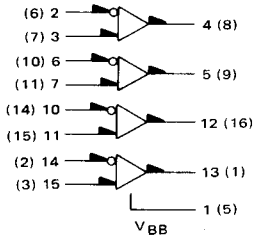
TRANSLATORS

MC10124
MC10525
Quad MTTL to MECL Translator



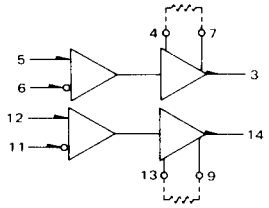
P_D = 380 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ

MC10125
MC10525
Quad MECL to MTTL Translator



P_D = 380 mW typ/pkg (No Load)
t_{pd} = 4.5 ns typ (50% to +1.5 Vdc out)

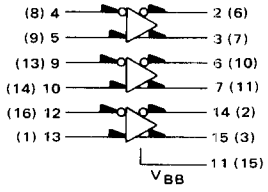
MC10127
Dual MECL to MOS Translator



V_{CC} = Gnd = Pins 1, 2, 15, 16
V_{EE} = Pin 8
V_{SS} = Pins 7, 9

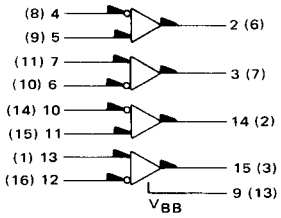
RECEIVERS

MC10114
MC10514
Triple Line Receiver



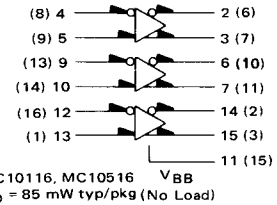
t_{pd} = 2.4 ns typ (Single Ended Input)
t_{pd} = 2.0 ns typ (Differential Input)
P_D = 145 mW typ/pkg (No Load)

MC10115
MC10515
Quad Line Receiver



P_D = 110 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ

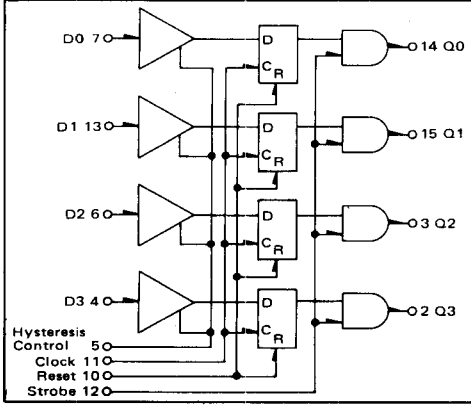
MC10116, MC10516
MC10216, MC10616
Triple Line Receiver



MC10116, MC10516
P_D = 85 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ

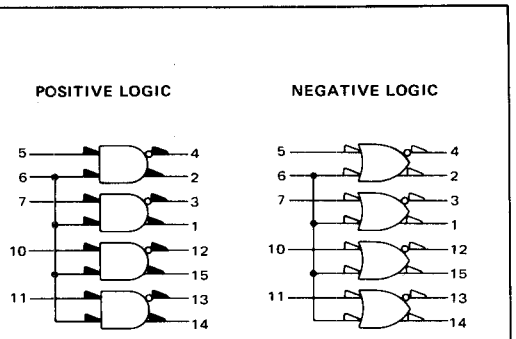
MC10216, MC10616
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 1.8 ns typ

MC10129
Quad Bus Receiver



P_D = 750 mW typ/pkg (No Load)
t_{pd} = 10 ns typ

MC10124



Gnd = Pin 16
V_{CC} (+5.0 Vdc) = Pin 9
V_{EE} (-5.2 Vdc) = Pin 8

The MC10124 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MC10124 has MTTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

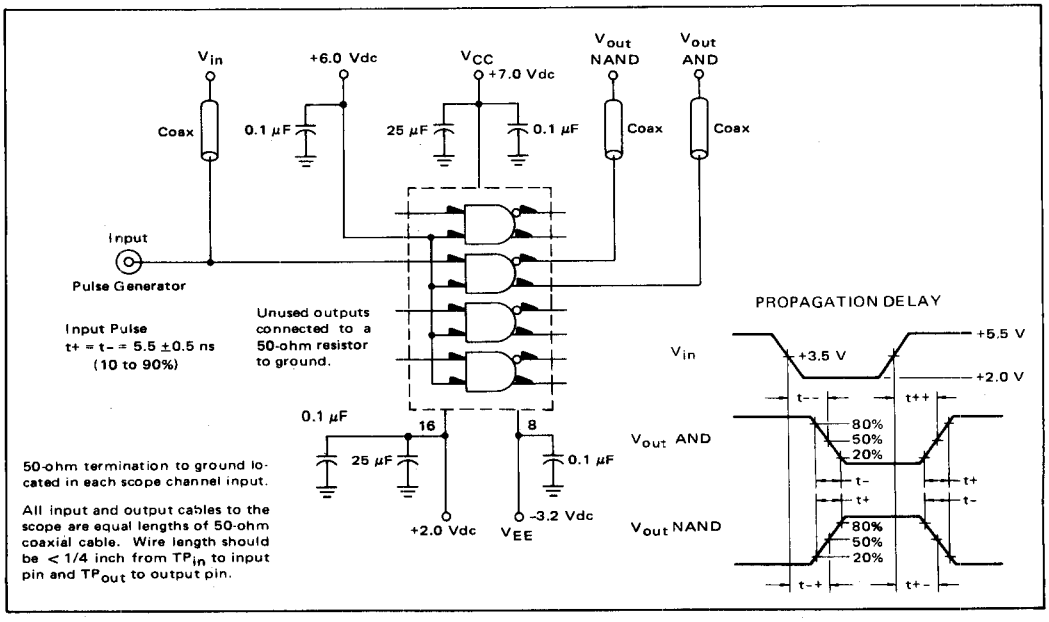
Power supply requirements are ground, +5.0 Volts, and -5.2 Volts. Propagation delay of the MC10124 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that MTTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the MC10115 or MC10116 differential line receivers. The MC10124 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communications systems.

P_D = 380 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ (+1.5 Vdc in to 50% out)
Output Rise, Fall Times;
2.5 ns typ (20% to 80%)

3

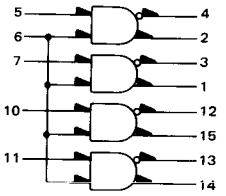
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

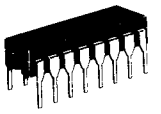


See General Information section for packaging.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one translator. The other translators are tested in the same manner.





L SUFFIX
CERAMIC PACKAGE
CASE 620

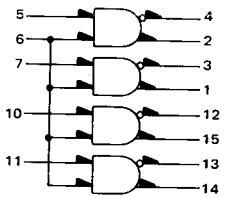
@ Test Temperature	V_{IH}	$V_{IL\ max}$	V_{IHA}	V_{ILA}	V_F	V_R	V_{CC}	V_{EE}	I_I	I_{in}
	Volts								mA	
-30°C	+4.0	+0.40	+2.00	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+25°C	+4.0	+0.40	+1.80	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+85°C	+4.0	+0.40	+1.80	+0.90	+0.40	+2.40	+5.00	-5.2	-10	+1.0

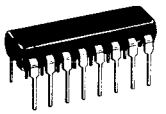
Characteristic	Symbol	Pin Under Test	MC10124L Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH}	$V_{IL\ max}$	V_{IHA}	V_{ILA}	V_F	V_R	V_{CC}	V_{EE}	I_I	I_{in}	Gnd
Negative Power Supply Drain Current	I_E	8	–	–	–	–	-66	–	–	mAdc	–	–			–	–	9	8	–	–	16
Positive Power Supply Drain Current	I_{CCH}	9	–	–	–	–	16	–	–	mAdc	5,6,7,10,11		–	–	–		9	8	–		16
	I_{CCL}	9	–	–	–	–	25	–	–	mAdc	–	–	–				9	8			5,6,7,10,11,16
Reverse Current	I_R	6	–	–	–	–	200	–	–	μAdc	–	–	–	–	5,7,10,11	6	9	8			16
		7	–	–	–	–	50	–	–	μAdc	–	–	–	–	6	7	9	8			16
Forward Current	I_F	6	–	–	–	–	-12.8	–	–	mAdc	5,7,10,11	–	–	–	6	–	9	8	–	–	16
		7	–	–	–	–	-3.2	–	–	mAdc	6	–	–	–	7	–	9	8			16
Input Breakdown Voltage	BV_{in}	6			5.5	–	–		–	Vdc				–	–	–	9	8		6	5,7,10,11,16
		7	–	–	5.5	–	–	–	–	Vdc				–	–	–	9	8		7	6,16
Clamp Input Voltage	V_I	6	–	–	–	–	-1.5			Vdc		–	–	–	–	–	9	8	6	–	16
		7	–	–	–	–	-1.5			Vdc	–		–	–	–	–	9	8	7	–	16
High Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960		-0.810	-0.890	-0.700	Vdc	6,7	–					9	8	–		16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc		6,7					9	8	–		16
Low Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	6,7		–	–	–	9	8		–	16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6,7	–		–	–	–	9	8	–	–	16
High Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6		7	–	–	–	9	8	–	–	16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6		–	7	–	–	9	8	–	–	16
Low Threshold Voltage	V_{OLA}	1		-1.655		–	-1.630	–	-1.595	Vdc	6	–	–	7		–	9	8			16
		3	–	-1.655		–	-1.630	–	-1.595	Vdc	6	–	7	–	–	–	9	8	–	–	16
Switching Time (50-Ω load)											**+6.0 Vdc**	**Pulse In**	**Pulse Out**				**+7.0 Vdc**	**-3.2 Vdc**			**+2.0 Vdc**
Propagation Delay (+3.5 Vdc to 50%)①	t_{6+1+}	1	1.5	6.8	1.5	3.5	6.0	1.0	6.0	ns	7	6	1			–	9	8	–	–	16
	t_{6-1-}		1.0	6.0				1.5	6.8		7	6		–	–	–					
	t_{7+1+}		1.5	6.8				1.0	6.0		6	7		–	–	–			–	–	
	t_{7-1-}		1.0	6.0				1.5	6.8					–	–	–			–	–	
	t_{7+3-}	3	1.5	6.8				1.0	6.0				3	–		–			–		
	t_{7-3+}	3	1.0	6.0				1.5	6.8				3							–	
Rise Time (20% to 80%)	t_{1+}	1	1.0	4.2	1.1	2.5	3.9	1.1	4.3				1			–			–	–	
Fall Time (80% to 20%)	t_{1-}	1	1.0	4.2	1.1	2.5	3.9	1.1	4.3				1						–	–	

① See switching time test circuit. Propagation delay for this circuit is specified from +1.5 Vdc in to the 50% point on the output waveform. The +3.5 Vdc is shown here because all logic and supply levels are shifted 2 volts positive.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one translator. The other translators are tested in the same manner.





P SUFFIX
PLASTIC PACKAGE
CASE 648

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IH}	$V_{IL\ max}$	$V_{IHA'}$	$V_{ILA'}$	V_F	V_R	V_{CC}	V_{EE}	(mA) I_I	I_{in}
-30°C	+4.0	+0.40	+2.00	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+25°C	+4.0	+0.40	+1.80	+1.10	+0.40	+2.40	+5.00	-5.2	-10	+1.0
+85°C	+4.0	+0.40	+1.80	+0.90	+0.40	+2.40	+5.00	-5.2	-10	+1.0

Characteristic	Symbol	Pin Under Test	MC10124P Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IH}	$V_{IL\ max}$	$V_{IHA'}$	$V_{ILA'}$	V_F	V_R	V_{CC}	V_{EE}	I_I	I_{in}	Gnd
Negative Power Supply Drain Current	I_E	8	–	–	–	–	-66	–	–	mAdc	–	–	–	–	–	–	9	8	–	–	16
Positive Power Supply Drain Current	I_{CCH}	9	–	–	–	–	16	–	–	mAdc	5,6,7,10,11	–	–	–	–	–	9	8	–	–	16
	I_{CCL}	9	–	–	–	–	25	–	–	mAdc	–	–	–	–	–	–	9	8	–	–	5,6,7,10,11,16
Reverse Current	I_R	6	–	–	–	–	200	–	–	μAdc	–	–	–	–	5,7,10,11	6	9	8	–	–	16
		7	–	–	–	–	50	–	–	μAdc	–	–	–	–	6	7	9	8	–	–	16
Forward Current	I_F	6	–	–	–	–	-12.8	–	–	mAdc	5,7,10,11	–	–	–	6	–	9	8	–	–	16
		7	–	–	–	–	-3.2	–	–	mAdc	6	–	–	–	7	–	9	8	–	–	16
Input Breakdown Voltage	BV_{in}	6	–	–	5.5	–	–	–	–	Vdc	–	–	–	–	–	–	9	8	–	6	5,7,10,11,16
		7	–	–	5.5	–	–	–	–	Vdc	–	–	–	–	–	–	9	8	–	7	6,16
Clamp Input Voltage	V_I	6	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	–	9	8	6	–	16
		7	–	–	–	–	-1.5	–	–	Vdc	–	–	–	–	–	–	9	8	7	–	16
High Output Voltage	V_{OH}	1	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	6,7	–	–	–	–	–	9	8	–	–	16
		3	-1.060	-0.890	-0.960	–	-0.810	-0.890	-0.700	Vdc	–	6,7	–	–	–	–	9	8	–	–	16
Low Output Voltage	V_{OL}	1	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	–	6,7	–	–	–	–	9	8	–	–	16
		3	-1.890	-1.675	-1.850	–	-1.650	-1.825	-1.615	Vdc	6,7	–	–	–	–	–	9	8	–	–	16
High Threshold Voltage	V_{OHA}	1	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6	–	7	–	–	–	9	8	–	–	16
		3	-1.080	–	-0.980	–	–	-0.910	–	Vdc	6	–	–	7	–	–	9	8	–	–	16
Low Threshold Voltage	V_{OLA}	1	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	–	7	–	–	9	8	–	–	16
		3	–	-1.655	–	–	-1.630	–	-1.595	Vdc	6	–	7	–	–	–	9	8	–	–	16
Switching Time (50-Ω load)											+6.0 Vdc	Pulse In	Pulse Out				+7.0 Vdc	-3.2 Vdc			+2.0 Vdc
Propagation Delay (+3.5 Vdc to 50%)①	t_{6+1+}	1	–	–	1.0	3.5	6.0	–	–	ns	7	6	1	–	–	–	9	8	–	–	16
	t_{6-1-}	↓	–	–	↓	↓	↓	–	–	↓	7	6	↓	–	–	–	↓	↓	–	–	↓
	t_{7+1+}		–	–				–	–		6	7		–	–	–			–	–	
	t_{7-1-}		–	–				–	–		↓	↓		–	–	–			–	–	
	t_{7+3-}	3	–	–				–	–				3	–	–	–			–	–	
	t_{7-3+}	3	–	–	↓	↓	↓	–	–				3	–	–	–			–	–	
Rise Time (20% to 80%)	t_{1+}	1	–	–	1.1	2.5	3.9	–	–				1	–	–	–			–	–	
Fall Time (80% to 20%)	t_{1-}	1	–	–	1.1	2.5	3.9	–	–	↓	↓	↓	1	–	–	–	↓	↓	–	–	↓

① See switching time test circuit. Propagation delay for this circuit is specified from +1.5 Vdc in to the 50% point on the output waveform. The +3.5 Vdc is shown here because all logic and supply levels are shifted 2 volts positive.)