



## N-Channel Enhancement-Mode Vertical DMOS FET

### Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low  $C_{iss}$  and fast switching speeds
- ▶ Excellent thermal stability
- ▶ Integral source-drain diode
- ▶ High input impedance and high gain

### Applications

- ▶ Motor controls
- ▶ Converters
- ▶ Amplifiers
- ▶ Switches
- ▶ Power supply circuits
- ▶ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

### General Description

This enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Ordering Information

Device	Package	$BV_{DSS}/BV_{DGS}$ (V)	$R_{DS(ON)}$ (max) ( $\Omega$ )	$I_{D(ON)}$ (min) (mA)
	TO-92			
VN10K	VN10KN3-G	60	5.0	750

For packaged products, -G indicates package is RoHS compliant ('Green').

Consult factory for die / wafer form part numbers.

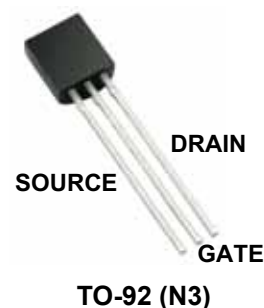
Refer to Die Specification VF21 for layout and dimensions.

### Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	$BV_{DSS}$
Drain-to-gate voltage	$BV_{DGS}$
Gate-to-source voltage	$\pm 30V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

### Pin Configuration



### Product Marking



YY = Year Sealed  
WW = Week Sealed  
\_\_\_\_\_ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)

## Thermal Characteristics

Package	$I_D$ (continuous) <sup>†</sup> (mA)	$I_D$ (pulsed) (A)	Power Dissipation @ $T_c = 25^\circ\text{C}$ (W)	$\theta_{jc}$ ( $^\circ\text{C/W}$ )	$\theta_{ja}$ ( $^\circ\text{C/W}$ )	$I_{DR}^{\dagger}$ (mA)	$I_{DRM}$ (A)
TO-92	310	1.0	1.0	125	170	310	1.0

### Notes:

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_j$ . (VN0106N3 can be used if an  $I_D$  (continuous) of 500mA is needed.)

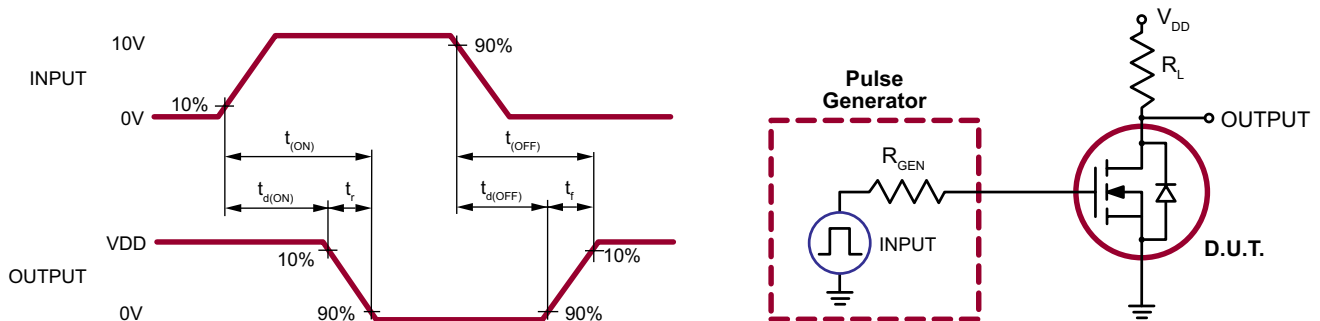
## Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$BV_{DSS}$	Drain-to-source breakdown voltage	60	-	-	V	$V_{GS} = 0V, I_D = 100\mu A$
$V_{GS(th)}$	Gate threshold voltage	0.8	-	2.5	V	$V_{GS} = V_{DS}, I_D = 1.0mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-3.8	-	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1.0mA$
$I_{GSS}$	Gate body leakage	-	-	100	nA	$V_{GS} = 15V, V_{DS} = 0V$
$I_{DSS}$	Zero gate voltage drain current	-	-	10	$\mu A$	$V_{GS} = 0V, V_{DS} = 45V$
		-	-	500		$V_{GS} = 0V, V_{DS} = 45V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	0.75	-	-	A	$V_{GS} = 10V, V_{DS} = 10V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	7.5	$\Omega$	$V_{GS} = 5.0V, I_D = 200mA$
		-	-	5.0		$V_{GS} = 10V, I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	0.7	-	%/ $^\circ\text{C}$	$V_{GS} = 10V, I_D = 500mA$
$G_{FS}$	Forward transconductance	100	-	-	mmho	$V_{DS} = 10V, I_D = 500mA$
$C_{ISS}$	Input capacitance	-	48	60	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz$
$C_{OSS}$	Common source output capacitance	-	16	25		
$C_{RSS}$	Reverse transfer capacitance	-	2.0	5.0		
$t_{(ON)}$	Turn-on time	-	-	10	ns	$V_{DD} = 15V, I_D = 600mA, R_{GEN} = 25\Omega$
$t_{(OFF)}$	Turn-off time	-	-	10		
$V_{SD}$	Diode forward voltage drop	-	0.8	-	V	$V_{GS} = 0V, I_{SD} = 500mA$
$t_{rr}$	Reverse recovery time	-	160	-	ns	$V_{GS} = 0V, I_{SD} = 500mA$

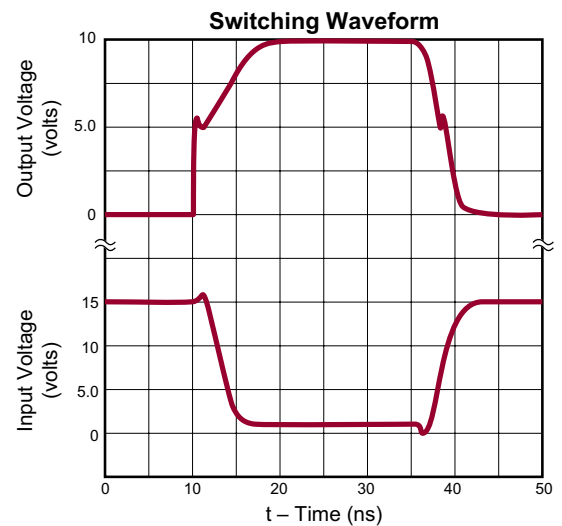
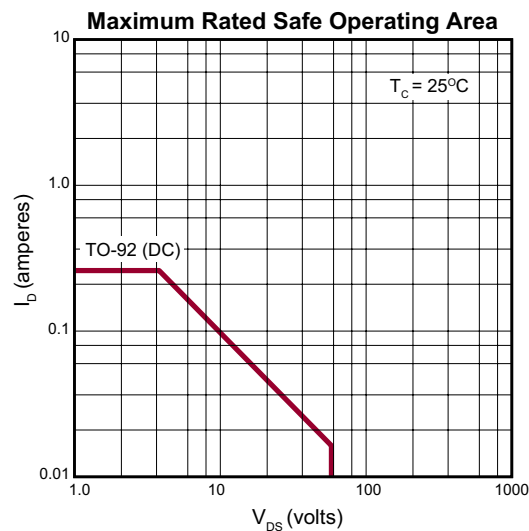
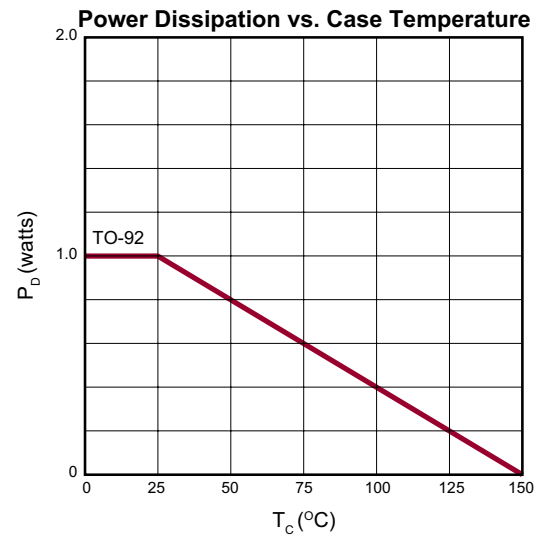
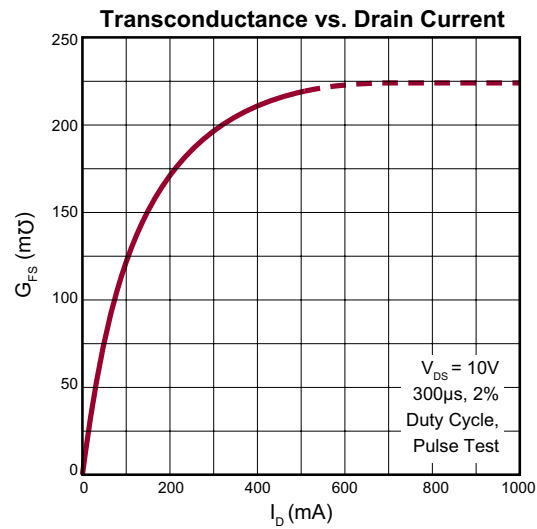
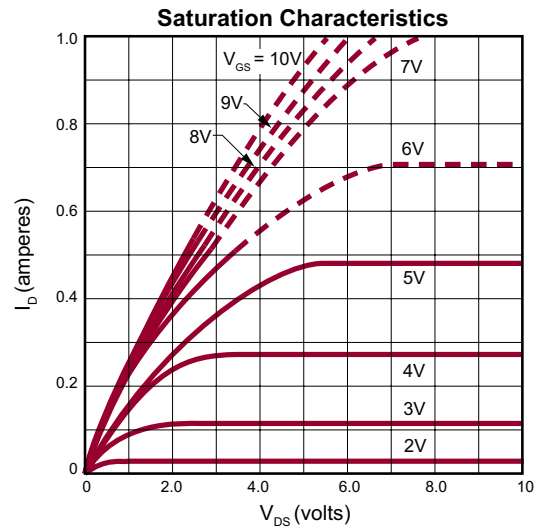
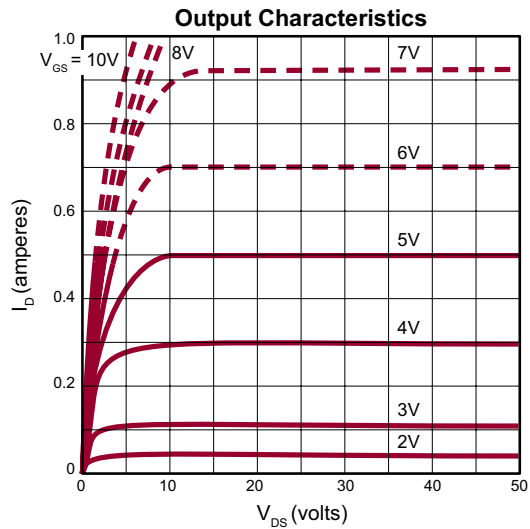
### Notes:

1. All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test: 300 $\mu s$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

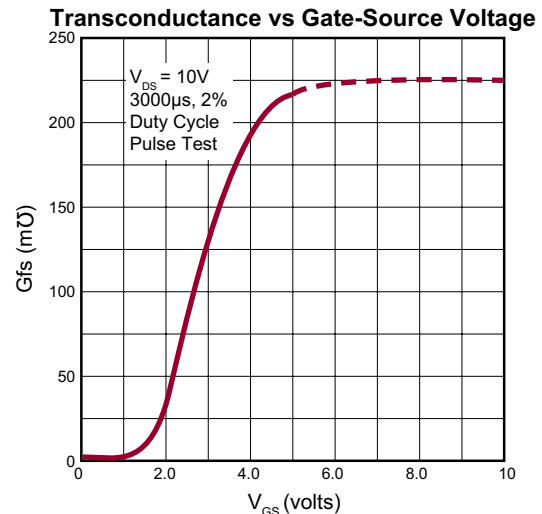
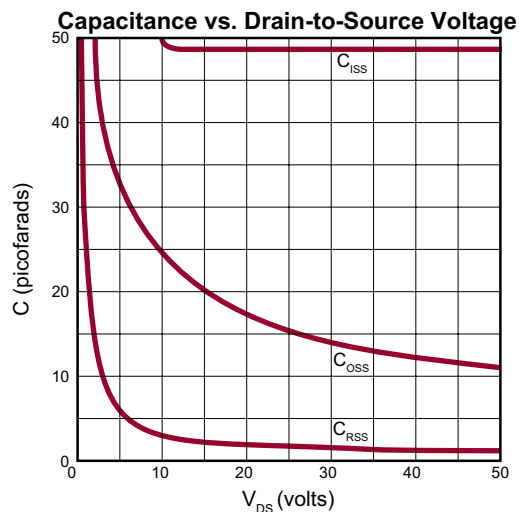
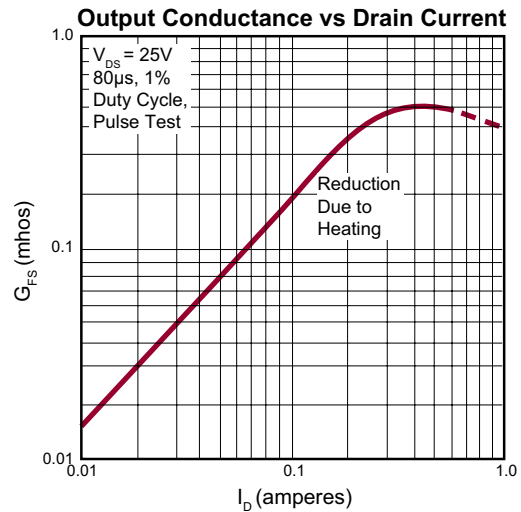
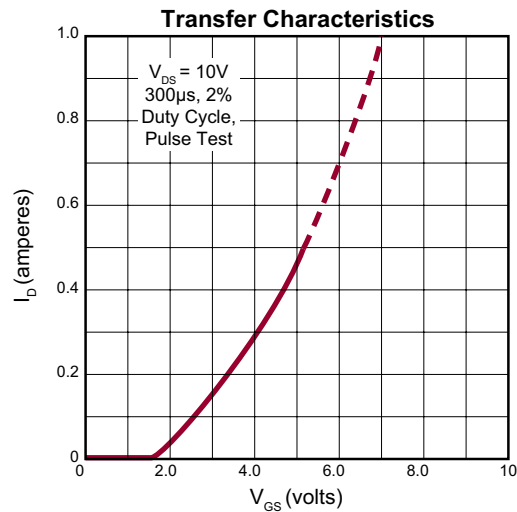
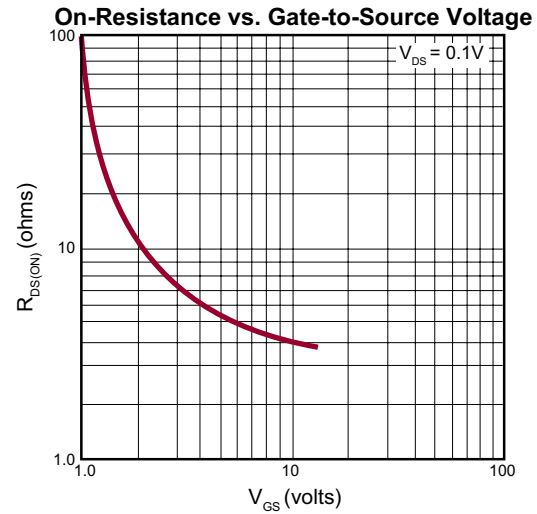
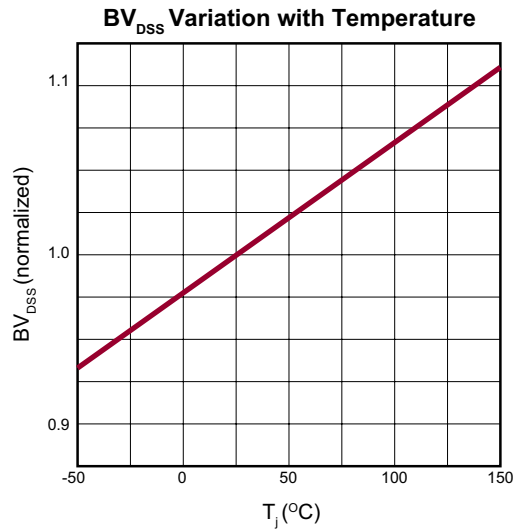
## Switching Waveforms and Test Circuit



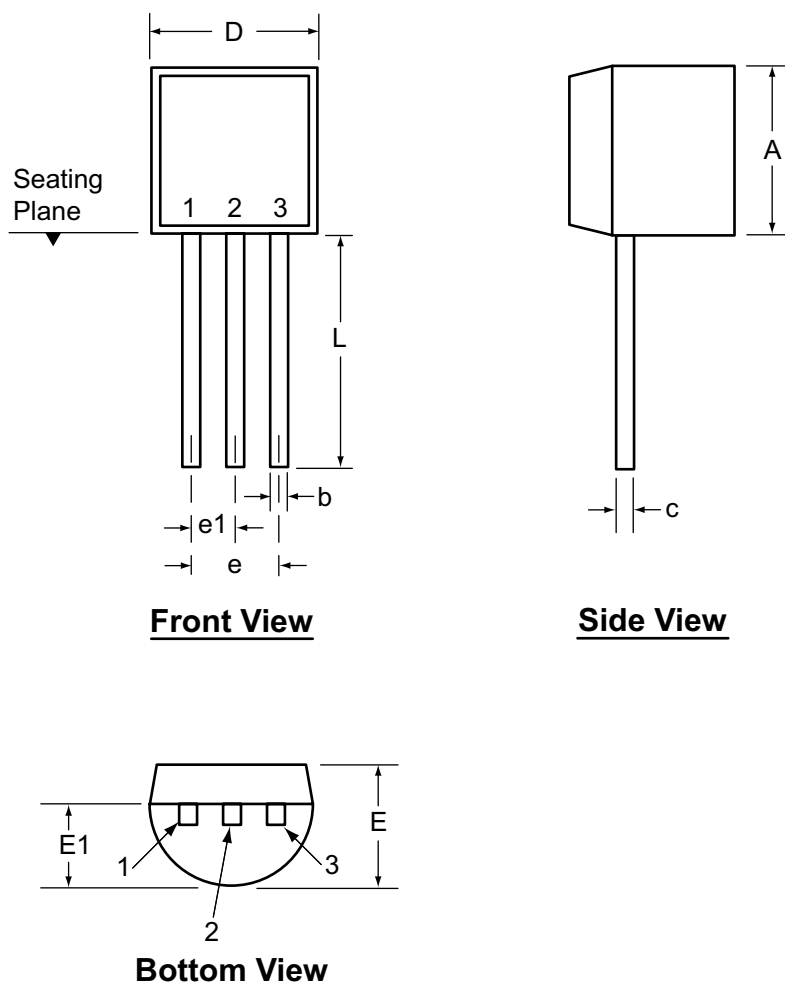
## Typical Performance Curves



## Typical Performance Curves (cont.)



### 3-Lead TO-92 Package Outline (N3)



Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014 <sup>†</sup>	.014 <sup>†</sup>	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 <sup>†</sup>	.022 <sup>†</sup>	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc.#:** DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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