

1 Gbps to 4.25 Gbps Limiting Amplifier With LOS and RSSI

FEATURES

- Multi-Rate Operation from 1 Gbps up to 4.25 Gbps
- 89-mW Power Consumption
- Input Offset Cancellation
- High Input Dynamic Range
- Output Disable
- CML Data Outputs
- Receive Signal Strength Indicator (RSSI)
- Loss of Signal Detection

- Polarity Select

- Single 3.3-V Supply

- Surface Mount Small Footprint 3-mm × 3-mm 16-Pin QFN Package

APPLICATIONS

- Cable Driver and Receiver
- 1.0625 Gbps, 2.125 Gbps, and 4.25 Gbps Fibre Channel Receivers
- Gigabit Ethernet Receivers

DESCRIPTION

The ONET4251PA is a versatile high-speed limiting amplifier for copper cable and fiber optic applications with data rates up to 4.25 Gbps.

This device provides a gain of about 50 dB, which ensures a full 800-mV_{p-p} differential output swing over its wide input signal dynamic range.

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as 1200 mV_{p-p}.

The ONET4251PA comprises a loss of signal detection as well as a received signal strength indicator.

The part is available in a small footprint 3-mm × 3-mm 16-pin QFN package. It requires a single 3.3-V supply.

This power efficient limiting amplifier dissipates less than 89 mW typical. It is characterized for operation from -40°C to 85°C .

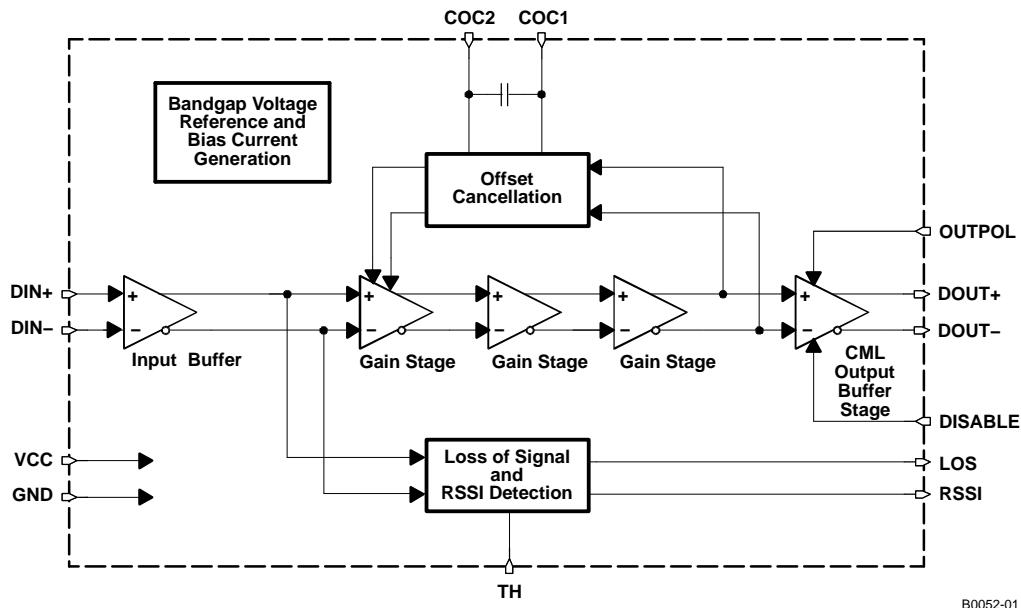
BLOCK DIAGRAM

A simplified block diagram of the ONET4251PA is shown in [Figure 1](#).

This compact 3.3 V, low power 4.25 Gbps limiting amplifier consists of a high-speed data path with offset cancellation block, a loss of signal and RSSI detection block, and a bandgap voltage reference and bias current generation block.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



B0052-01

Figure 1. Simplified Block Diagram of the ONET4251PA

HIGH SPEED DATA PATH

The high-speed data signal is applied to the data path by means of the input signal pins **DIN+/*DIN*-**. The data path consists of the input stage with $2 \times 50\text{-}\Omega$ on-chip line termination to **VCC**, three gain stages, which provide the required typical gain of about 50 dB, and a CML output stage. The amplified data output signal is available at the output pins **DOUT+/*DOUT*-**, which provide $2 \times 50\text{-}\Omega$ back-termination to **VCC**. The output stage also includes a data polarity switching function, which is controlled by the **OUTPOL** input, and a disable function, controlled by the signal applied to the **DISABLE** input pin.

An offset cancellation compensates for internal offset voltages and thus ensures proper operation even for very small input data signals.

The low frequency cutoff is typically as low as 50 kHz with the built-in filter capacitor.

For applications which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the **COC1/COC2** pins.

LOSS OF SIGNAL AND RSSI DETECTION

The output signal of the input buffer is monitored by the loss of signal and RSSI detection circuitry. In this block, a signal is generated that is linear proportional to the input amplitude over a wide input voltage range. This signal is available at the **RSSI** output pin.

Furthermore, this circuit block compares the input signal to a threshold which can be programmed by means of an external resistor connected to the **TH** pin. If the input signal falls below the specified threshold, a loss of signal is indicated at the **LOSS** pin.

The relation between the **LOSS** assert voltage V_{AST} (in $\text{mV}_{\text{p-p}}$) and the external resistor R_{TH} (in $\text{k}\Omega$) connected to the **TH** pin can be approximated as given below:

$$R_{TH} \approx \frac{22.4 \text{ k}\Omega}{\left(V_{AST}/\text{mV}_{p-p} - 1\right)} + 560 \Omega \quad (1)$$

$$V_{AST} \approx \frac{22.4 \text{ mV}_{p-p}}{R_{TH}/\text{k}\Omega - 0.56} + 1 \text{ mV}_{p-p} \quad (2)$$

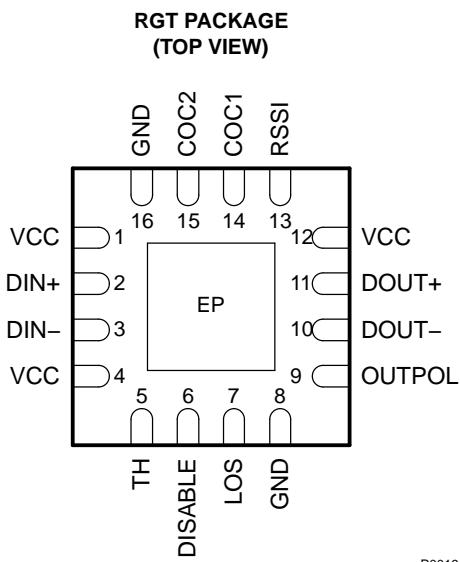
BANDGAP VOLTAGE AND BIAS GENERATION

The ONET4251PA limiting amplifier is supplied by a single 3.3-V $\pm 10\%$ supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

An on-chip bandgap voltage circuitry generates a supply voltage independent reference from which all other internally required voltages and bias currents are derived.

PACKAGE

For the ONET4251PA a small footprint 3-mm \times 3-mm 16-pin QFN package, with a lead pitch of 0.5 mm is used. The pin out is shown in [Figure 2](#).



P0019-01

Figure 2. Pinout of ONET4251PA in a 3 mm x 3 mm 16-Pin QFN Package (Top View)

TERMINAL FUNCTIONS

| TERMINAL | TYPE | DESCRIPTION |
|-----------|---------|-------------|
| NO. | | |
| 1, 4, 12 | VCC | supply |
| 2 | DIN+ | analog-in |
| 3 | DIN- | analog-in |
| 5 | TH | analog-in |
| 6 | DISABLE | CMOS-in |
| 7 | LOS | CMOS-out |
| 8, 16, EP | GND | supply |
| 9 | OUTPOL | CMOS-in |
| 10 | DOUT- | CML-out |
| 11 | DOUT+ | CML-out |

TERMINAL FUNCTIONS (continued)

| TERMINAL NO. | NAME | TYPE | DESCRIPTION |
|-----------------|------|------------|--|
| 13 | RSSI | analog-out | Analog output voltage proportional to the input data amplitude. Indicates the strength of the received signal (RSSI). |
| 14 | COC1 | analog | Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC2 (pin 15). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15). |
| 15 | COC2 | analog | Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 14). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15). |

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | VALUE/UNIT |
|--|--|-----------------|
| V_{CC} | Supply voltage ⁽²⁾ | −0.3 V to 4 V |
| V_{DIN+}, V_{DIN-} | Voltage at DIN+, DIN− ⁽²⁾ | 0.5 V to 4 V |
| $V_{TH}, V_{DISABLE}, V_{LOS}, V_{OUTPOL}, V_{DOUT+}, V_{DOUT-}, V_{RSSI}, V_{COC1}, V_{COC2}$ | Voltage at TH, DISABLE, LOS, OUTPOL, DOUT+, DOUT−, RSSI, COC1, COC2 ⁽²⁾ | −0.3 V to 4 V |
| $V_{COC,DIFF}$ | Differential voltage between COC1 and COC2 | ±1 V |
| $V_{DIN,DIFF}$ | Differential voltage between DIN+ and DIN− | ±2.5 V |
| I_{LOS} | Current into LOS | −1 to 9 mA |
| $I_{DIN+}, I_{DIN-}, I_{DOUT+}, I_{DOUT-}$ | Continuous current at inputs and outputs | −25 mA to 25 mA |
| ESD | ESD rating at all pins | 2 kV (HBM) |
| $T_{J(max)}$ | Maximum junction temperature | 125°C |
| T_{STG} | Storage temperature range | −65 to 85°C |
| T_A | Characterized free-air operating temperature range | −40 to 85°C |
| T_{LEAD} | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | TYP | MAX | UNIT |
|----------|--------------------------------|-----|-----|-----|------|
| V_{CC} | Supply voltage | 3.0 | 3.3 | 3.6 | V |
| T_A | Operating free-air temperature | −40 | | 85 | °C |
| V_{IH} | CMOS input high voltage | 2.1 | | | V |
| V_{IL} | CMOS input low voltage | | | 0.6 | V |

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|--|--|-----------|-----|------------|
| V_{CC} | Supply voltage | 3 | 3.3 | 3.6 | V |
| I_{VCC} | Supply current | <i>DISABLE</i> = low (excludes CML output current) | 27 | 40 | mA |
| V_{OD} | Differential data output voltage swing | <i>DISABLE</i> = high | 0.25 | 10 | mV_{p-p} |
| | | <i>DISABLE</i> = low | 600 | 760 | |
| R_{IN}, R_{OUT} | Data input/output resistance | Single-ended | 50 | | Ω |
| V_{RSSI} | RSSI output voltage | Input = 8 mV_{p-p} , $R_{RSSI} \geq 10 k\Omega$ | 180 | | mV |
| | | Input = 80 mV_{p-p} , $R_{RSSI} \geq 10 k\Omega$ | 1900 | | |
| RSSI Linearity | | $8 mV_{p-p} \leq V_{IN} \leq 80 mV_{p-p}$ | $\pm 3\%$ | | |
| $V_{IN(MIN)}$ | Minimum data input voltage | | | 50 | mV_{p-p} |
| $V_{IN(MAX)}$ | Data input overload | | 1200 | | mV_{p-p} |
| LOS high voltage | $I_{SOURCE} = 30 \mu A$ | | 2.4 | | V |
| LOS low voltage | $I_{SINK} = 1 mA$ | | | 0.4 | V |

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted), typical operating condition is at $V_{CC} = 3.3$ V and $T_A = 25^\circ C$

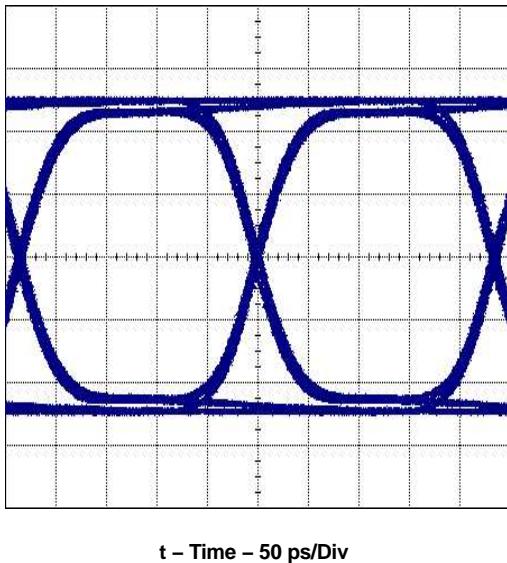
| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|-----------------------------------|---|-----|-----|---------------|
| Low frequency -3 dB bandwidth | $C_{OC} = \text{open}$ | | 50 | | kHz |
| | $C_{OC} = 0.1 \mu F$ | | 0.8 | | |
| Data rate | | 4.25 | | | Gb/s |
| V_{NI} | Input referred noise | | 230 | | μV_{RMS} |
| DJ | K28.5 pattern at 4.25 Gbps | 6 | 19 | | ps_{p-p} |
| | K28.5 pattern at 2.125 Gbps | 8 | 22 | | |
| | K28.5 pattern at 1.0625 Gbps | 11 | 28 | | |
| RJ | Random jitter | Input = 50 mV_{pp} | 1 | | ps_{RMS} |
| t_r | Output rise time | 20% to 80% | 35 | 70 | ps |
| t_f | Output fall time | 20% to 80% | 35 | 70 | ps |
| LOS hysteresis | | K28.5 pattern at 4.25 Gbps | 2.5 | 4.5 | dB |
| R_{TH} | LOS threshold adjustment resistor | See (1) | | 4 | $k\Omega$ |
| V_{AST} | LOS assert voltage | $R_{TH} = 4 k\Omega$ K28.5 pattern at 4.25 Gbps | 3 | 7 | mV_{p-p} |
| V_{DEA} | LOS deassert voltage | $R_{TH} = 4 k\Omega$ K28.5 pattern at 4.25 Gbps | | 11 | mV_{p-p} |
| t_{LOS} | LOS assert/deassert time | | 2 | 100 | μs |
| t_{DIS} | Disable response time | | | 20 | ns |

(1) For a given external resistor connected to the TH pin, the LOS assert voltage value may vary due to part-to-part variations. If high precision is required, adjustment of this resistor for each device is mandatory.

TYPICAL CHARACTERISTICS

Typical operating condition is at $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$ (unless otherwise noted).

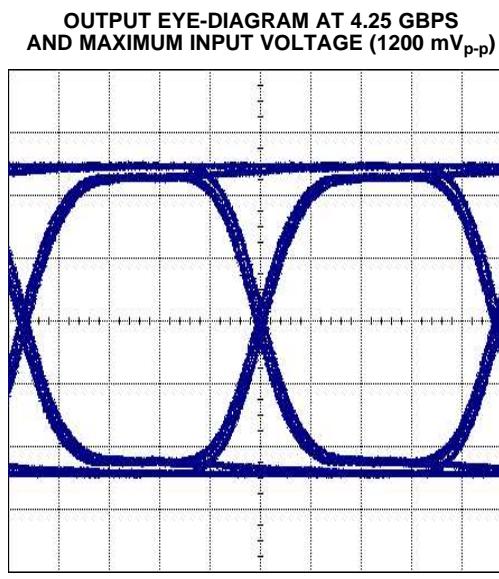
V_{OD} – Differential Output Voltage – 160 mV/Div



G005

Figure 3.

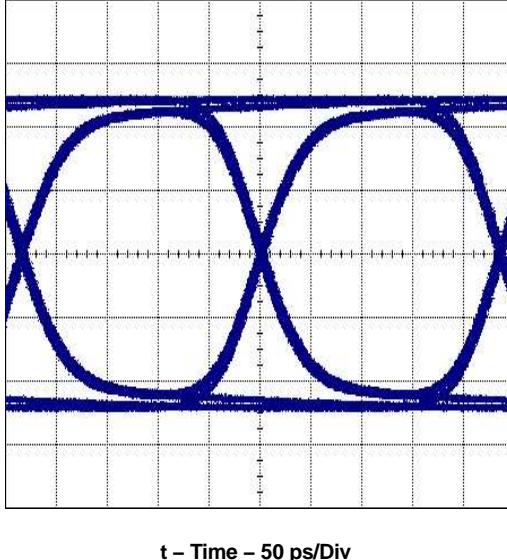
V_{OD} – Differential Output Voltage – 160 mV/Div



G006

Figure 4.

V_{OD} – Differential Output Voltage – 160 mV/Div

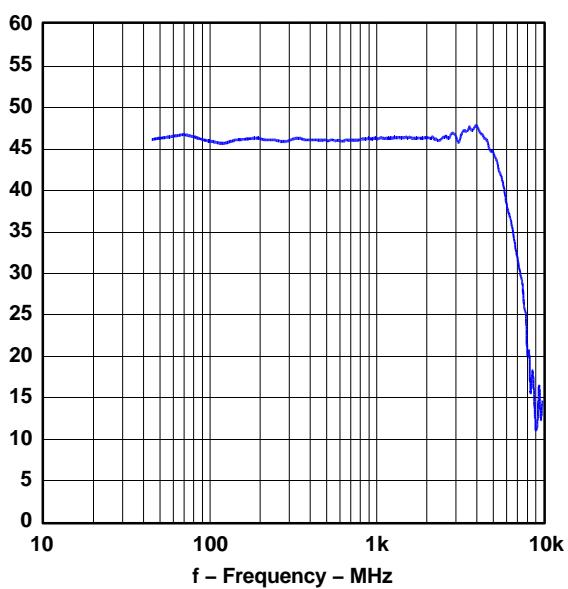


G007

Figure 5.

FREQUENCY RESPONSE

Small Signal Gain – dB



G004

Figure 6.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$ (unless otherwise noted).

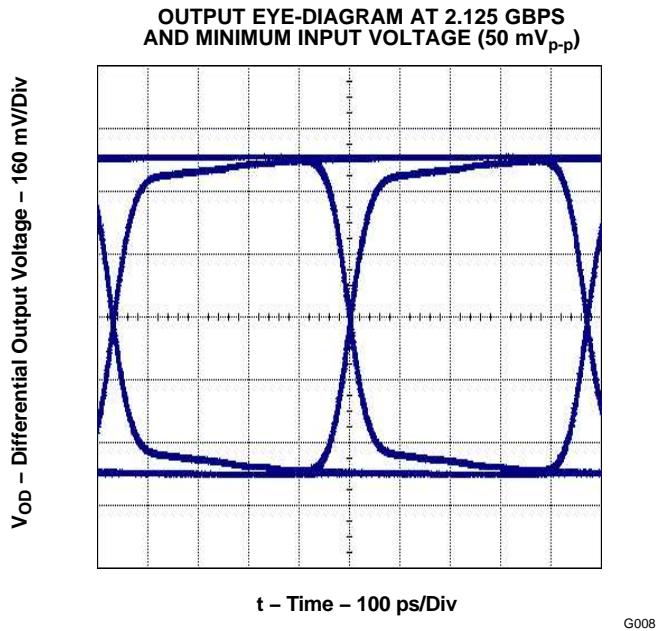


Figure 7.

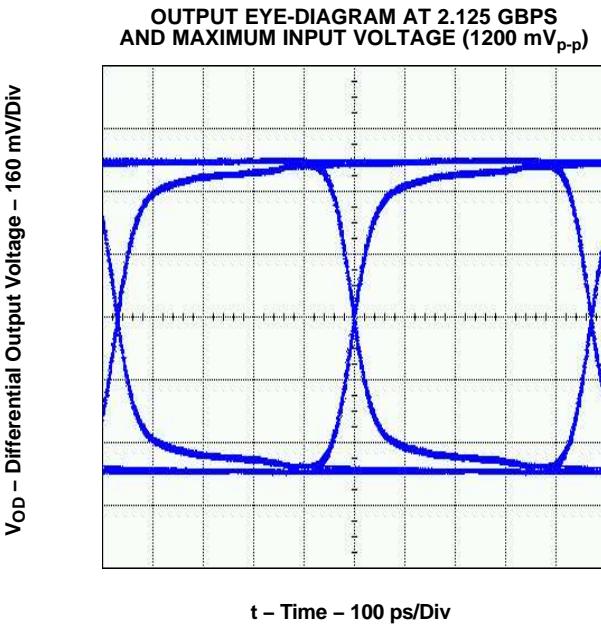


Figure 8.

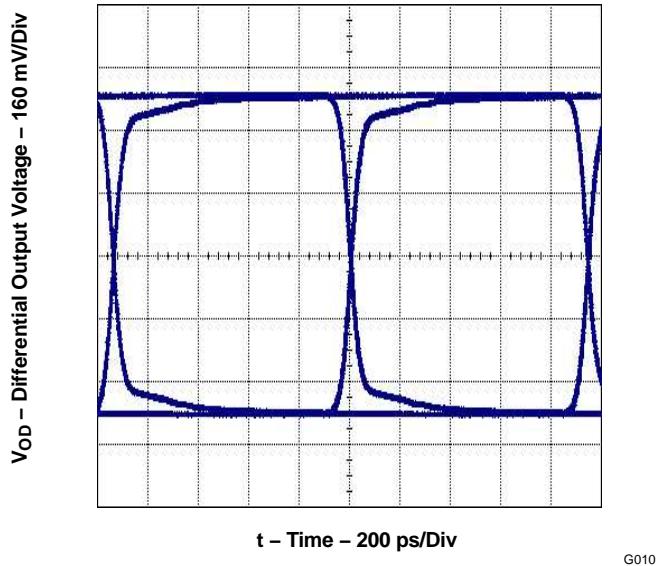


Figure 9.

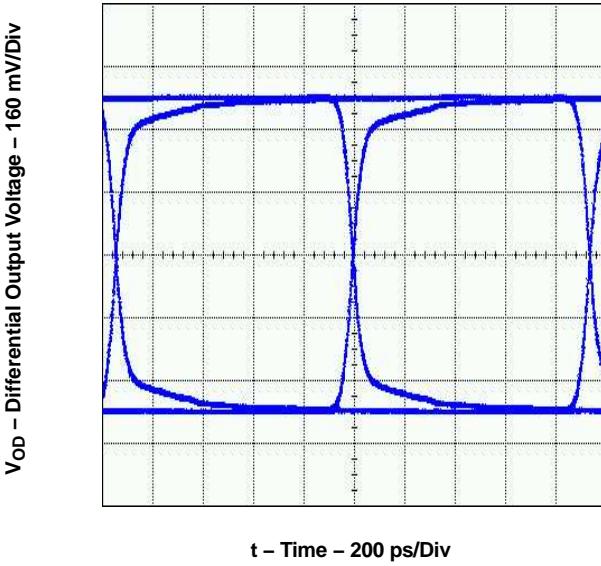


Figure 10.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$ (unless otherwise noted).

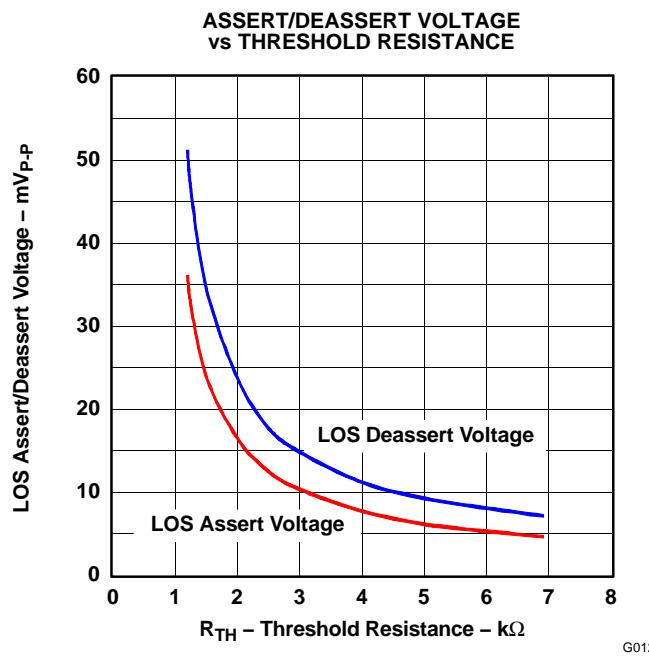


Figure 11.

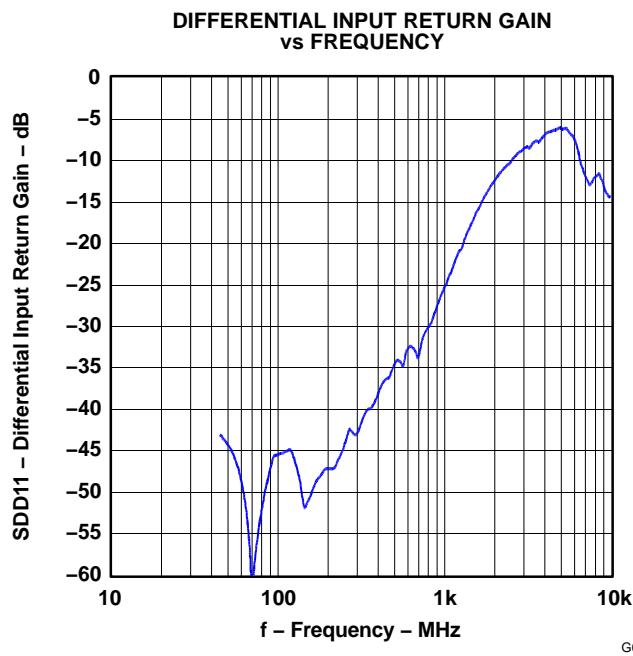


Figure 12.

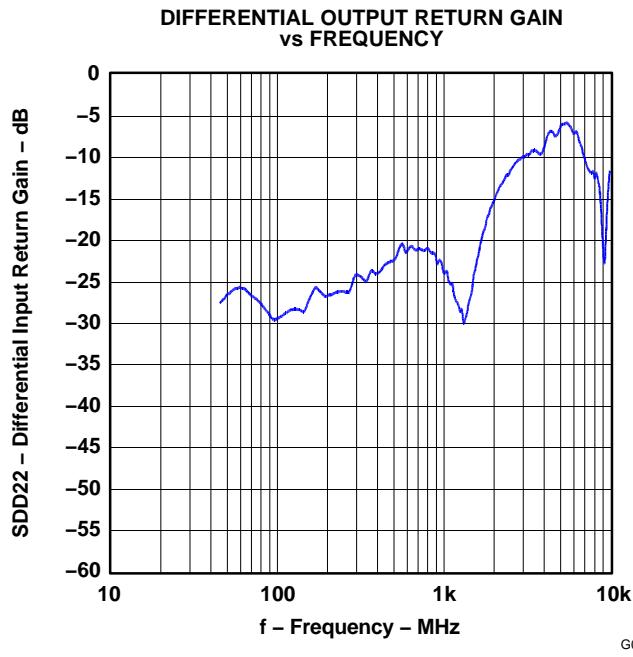


Figure 13.

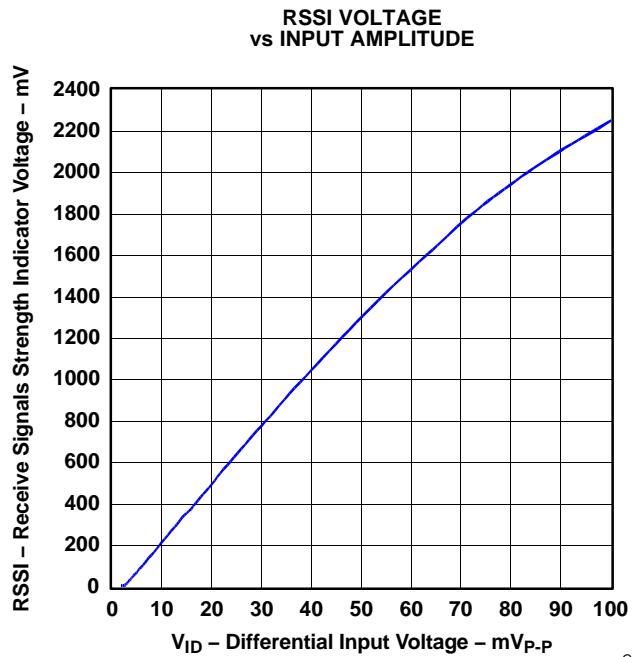


Figure 14.

APPLICATION INFORMATION

Figure 15 shows the ONET4251PA connected with an ac-coupled interface to the data signal source as well as to the output load.

Besides the ac-coupling capacitors C_1 through C_4 in the input and output data signal lines, the only required external component is the LOS threshold setting resistor R_{TH} . In addition, if a low cutoff frequency is required, as an option, an external filter capacitor C_{OC} may be used.

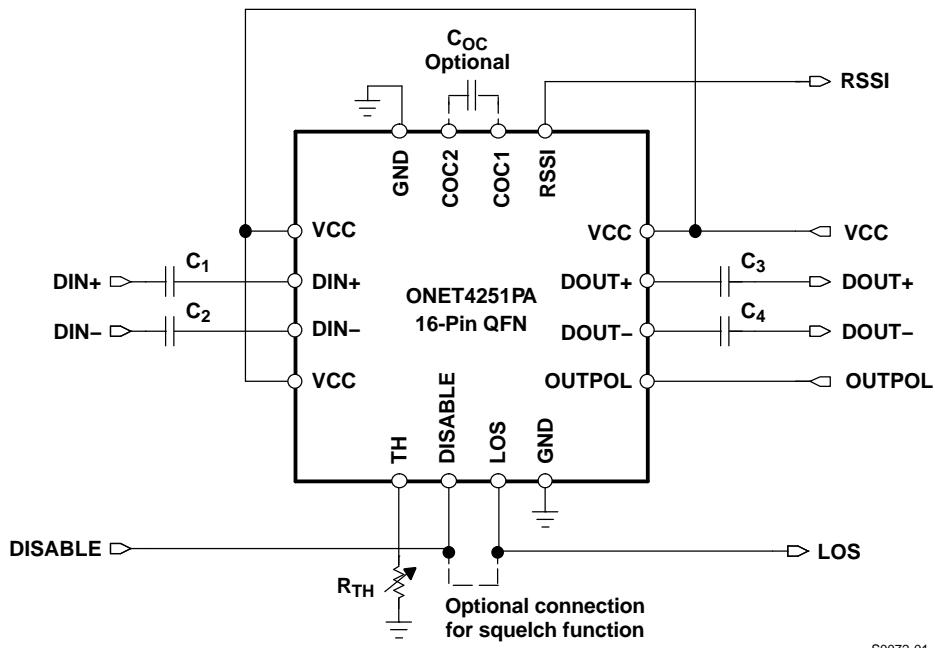


Figure 15. Basic Application Circuit With AC Coupled I/Os

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|---|
| ONET4251PARGTR | ACTIVE | QFN | RGT | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 451P | Samples |
| ONET4251PARGTRG4 | ACTIVE | QFN | RGT | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 451P | Samples |
| ONET4251PARGTT | ACTIVE | QFN | RGT | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 451P | Samples |
| ONET4251PARGTTG4 | ACTIVE | QFN | RGT | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 451P | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

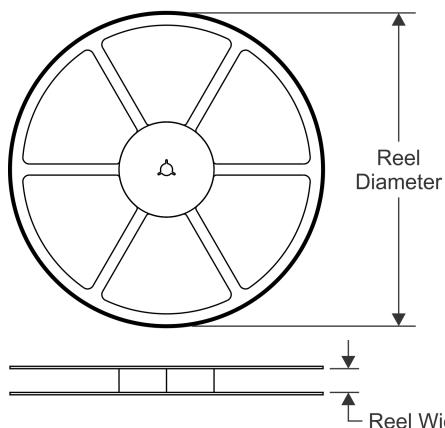
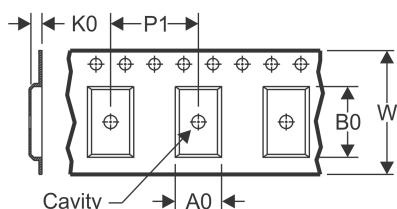
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



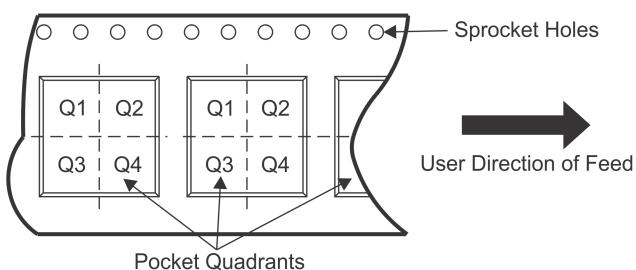
www.ti.com

PACKAGE OPTION ADDENDUM

11-Apr-2013

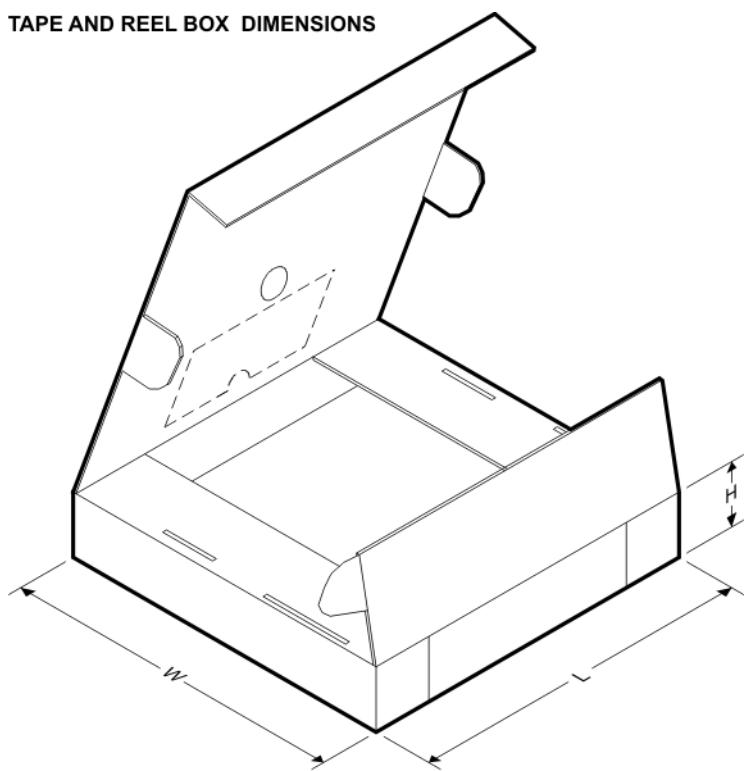
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ONET4251PARGTR | QFN | RGT | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| ONET4251PARGTT | QFN | RGT | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

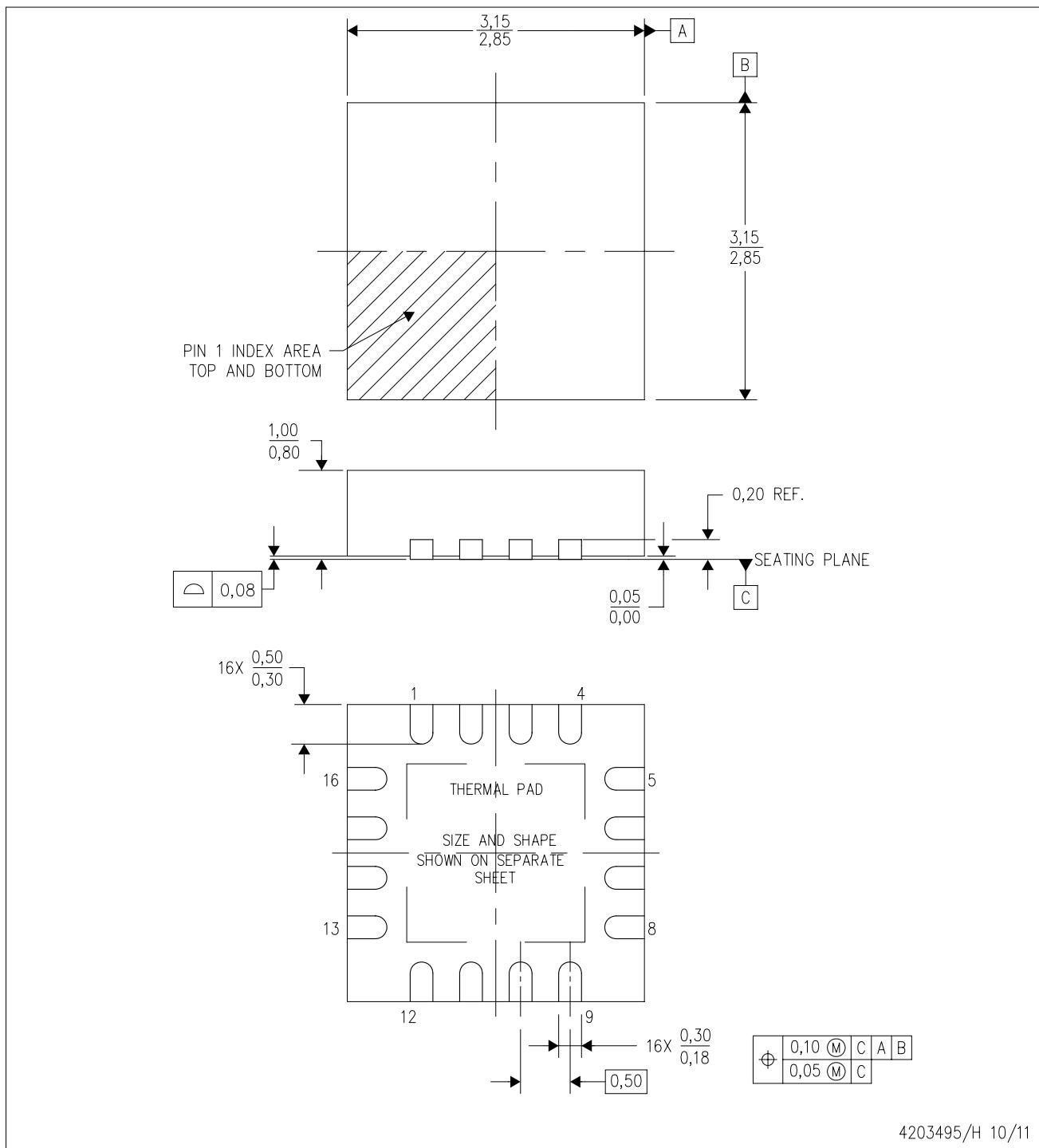
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ONET4251PARGTR | QFN | RGT | 16 | 3000 | 338.1 | 338.1 | 20.6 |
| ONET4251PARGTT | QFN | RGT | 16 | 250 | 338.1 | 338.1 | 20.6 |

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

RGT (S-PVQFN-N16)

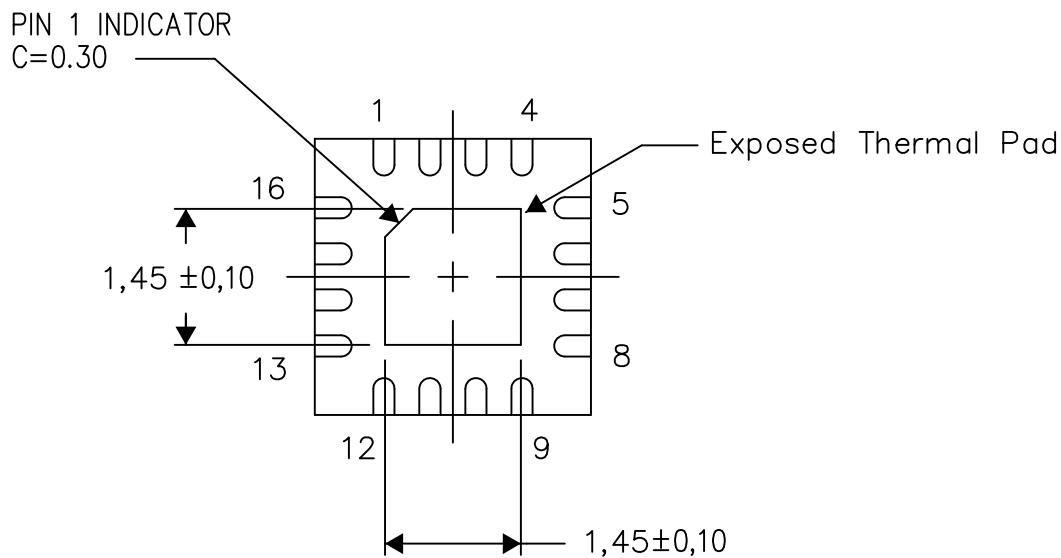
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

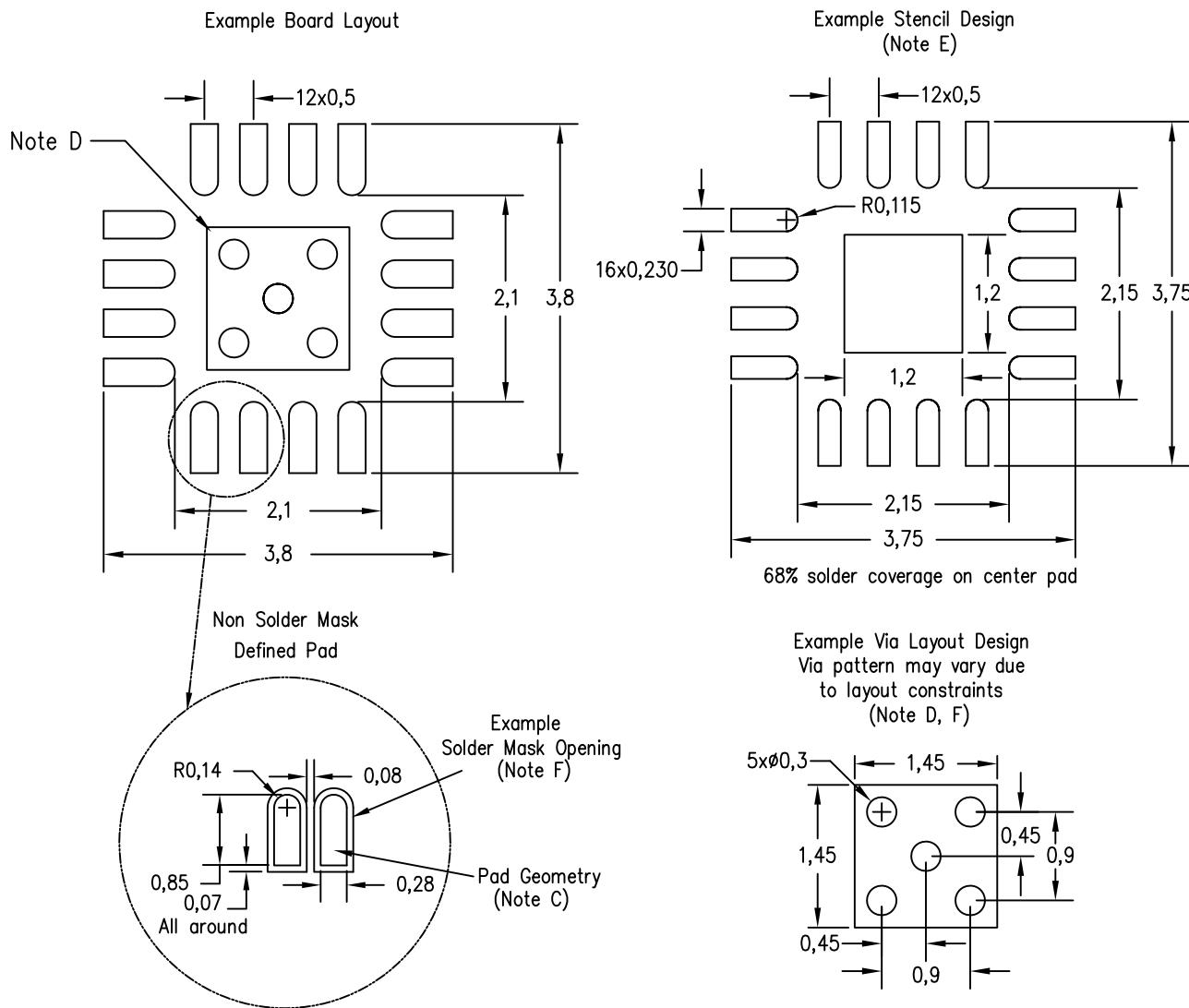
Exposed Thermal Pad Dimensions

4206349-2/U 09/13

NOTE: All linear dimensions are in millimeters

RGT (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208050-4/J 09/13

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

| Products | Applications |
|------------------------------|--|
| Audio | www.ti.com/audio |
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| OMAP Applications Processors | www.ti.com/omap |
| Wireless Connectivity | www.ti.com/wirelessconnectivity |
| | TI E2E Community |
| | e2e.ti.com |