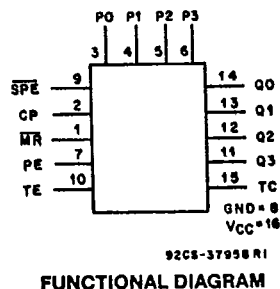


Advance Information

CD54/74AC161, CD54/74AC163

CD54/74ACT161, CD54/74ACT163

T-45-23-05



Synchronous Presettable Binary Counters

CD54/74AC/ACT 161 - Asynchronous Reset

CD54/74AC/ACT163 - Synchronous Reset

Type Features:

- Buffered inputs
- Typical propagation delay:
7.8 ns @ $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

The RCA CD54/74AC161 and CD54/74AC163 and the CD54/74ACT161 and CD54/74ACT163 synchronous presettable binary counters use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT161 are asynchronously reset; the CD54/74AC/ACT163 devices are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

A LOW level on the Synchronous Parallel Enable input, SPE, disables the counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for SPE are met).

The counters are reset with a LOW level on the Master Reset input, MR. In the CD54/74AC/ACT163 counter (synchronous reset), the requirements for setup and hold time with respect to the clock must be met.

Two count enables, PE and TE, in each counter are provided for n-bit cascading. Reset action occurs regardless of the level of the SPE, PE, and TE inputs (and the clock input, CP, in the CD54/74AC/ACT161).

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be HIGH to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count, the terminal count (TC) output goes HIGH for one clock period. This TC pulse is used to enable the next cascaded stage.

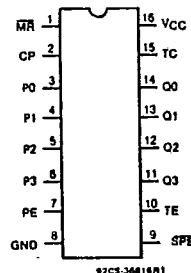
The CD74AC/ACT161 and CD74AC/ACT163 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to $+85^\circ\text{C}$); and Extended Industrial/Military (-55 to $+125^\circ\text{C}$).

The CD54AC/ACT161 and CD54AC/ACT163, available in chip form (H suffix), are operable over the -55 to $+125^\circ\text{C}$ temperature range.

Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$ output drive current
 - Fanout to 15 FAST* ICs
 - Drives 50-ohm transmission lines

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.



TERMINAL ASSIGNMENT

File Number 1959

155

Technical Data

CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163

T-45-23-05

MODE SELECT — FUNCTION TABLE (AC/ACT161)

OPERATING MODE	INPUTS						OUTPUTS	
	MR	CP	PE	TE	SPE	P _n	Q _n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H		X	X	L	L	L	L
	H		X	X	L	h	H	(a)
Count	H		h	h	h	x	count	(a)
Inhibit	H	X	L	X	h	X	q _n	(a)
	H	X	X	L	h	X	q _n	L

MODE SELECT — FUNCTION TABLE (AC/ACT163)

OPERATING MODE	INPUTS						OUTPUTS	
	MR	CP	PE	TE	SPE	P _n	Q _n	TC
Reset (Clear)	L		X	X	X	X	L	L
Parallel Load	h		X	X	L	L	L	L
	h		X	X	L	h	H	(a)
Count	h		h	h	h	X	count	(a)
Inhibit	h	X	L	X	h	X	q _n	(a)
	h	X	X	L	h	X	q _n	L

H = HIGH voltage level steady state.

L = LOW voltage level steady state.

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.

X = Don't care.

q = Lowercase letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.

 = LOW-to-HIGH clock transition.

NOTE:

(a) The TC output is HIGH when TE is HIGH and the counter is at Terminal Count (HHHH).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (V _{cc})	-0.5 to 6 V
DC INPUT DIODE CURRENT, I _{IK} (for V _i < -0.5 V or V _i > V _{cc} + 0.5 V)	±20 mA
DC OUTPUT DIODE CURRENT, I _{OK} (for V _o < -0.5 V or V _o > V _{cc} + 0.5 V)	±50 mA
DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I _o (for V _o > -0.5 V or V _o < V _{cc} + 0.5 V)	±50 mA
DC V _{cc} or GROUND CURRENT (I _{cc} or I _{GND})	±100 mA*
POWER DISSIPATION PER PACKAGE (P _D):	
For T _A = -55 to +100°C (PACKAGE TYPE E)	500 mW
For T _A = +100 to +125°C (PACKAGE TYPE E)	Derate Linearly at 8 mW/°C to 300 mW
For T _A = -55 to +70°C (PACKAGE TYPE M)	400 mW
For T _A = +70 to +125°C (PACKAGE TYPE M)	Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T _A)	-55 to +125°C
STORAGE TEMPERATURE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum	+265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only	+300°C

*For up to 4 outputs per device; add ± 25 mA for each additional output.

T-45-23-05

CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163
RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V_{CC} †: (For T_A = Full Package-Temperature Range) AC Types ACT Types	1.5 4.5	5.5 5.5	V V
DC Input or Output Voltage, V_i , V_o	0	V_{CC}	V
Operating Temperature, T_A	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv at 1.5 V to 3 V (AC Types) at 3.6 V to 5.5 V (AC Types) at 4.5 V to 5.5 V (ACT Types)	0 0 0	50 20 10	ns/V ns/V ns/V

†Unless otherwise specified, all voltages are referenced to ground.

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C						UNITS
				+25		-40 to +85		-55 to +125		
	V_I (V)	I_O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
High-Level Input Voltage V_{IH}			1.5 3 5.5	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	1.2 2.1 3.85	— — —	V
Low-Level Input Voltage V_{IL}			1.5 3 5.5	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	— — —	0.3 0.9 1.65	V
High-Level Output Voltage V_{OH}	V_{IH} or V_{IL} # , * {	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
		-0.05	3	2.9	—	2.9	—	2.9	—	
		-0.05	4.5	4.4	—	4.4	—	4.4	—	
		-4	3	2.58	—	2.48	—	2.4	—	
		-24	4.5	3.94	—	3.8	—	3.7	—	
		-75	5.5	—	—	3.85	—	—	—	
		-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V_{OL}	V_{IH} or V_{IL} # , * {	0.05	1.5	—	0.1	—	0.1	—	0.1	V
		0.05	3	—	0.1	—	0.1	—	0.1	
		0.05	4.5	—	0.1	—	0.1	—	0.1	
		12	3	—	0.36	—	0.44	—	0.5	
		24	4.5	—	0.36	—	0.44	—	0.5	
		75	5.5	—	—	—	1.65	—	—	
		50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I_i	V_{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA
Quiescent Supply Current, MSI I_{CC}	V_{CC} or GND	0	5.5	—	8	—	80	—	160	μA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

Technical Data

CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163

T-45-23-05

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS		TEST CONDITIONS		V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C						UNITS	
					+25		-40 to +85		-55 to +125			
		V _I (V)	I _O (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V _{IH}			4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V _{IL}			4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V _{OH}	V _{IH} or V _{IL} #, *	-0.05	4.5	4.4	—	4.4	—	4.4	—	V	
			-24	4.5	3.94	—	3.8	—	3.7	—		
			-75	5.5	—	—	3.85	—	—	—		
			-50	5.5	—	—	—	—	3.85	—		
Low-Level Output Voltage	V _{OL}	V _{IH} or V _{IL} #, *	0.05	4.5	—	0.1	—	0.1	—	0.1	V	
			24	4.5	—	0.36	—	0.44	—	0.5		
			75	5.5	—	—	—	1.65	—	—		
			50	5.5	—	—	—	—	—	1.65		
Input Leakage Current	I _I	V _{CC} or GND		5.5	—	±0.1	—	±1	—	±1	μA	
Quiescent Supply Current, MSI	I _{CC}	V _{CC} or GND	0	5.5	—	8	—	80	—	160	μA	
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load		ΔI _{CC}	V _{CC} -2.1		4.5 to 5.5	—	2.4	—	2.8	—	3	mA

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
Pn	0.13
CP	1
MR, TE	0.83
SPĒ	0.67
PE	0.5

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163

PREREQUISITE FOR SWITCHING: AC Series

T-45-a3-05

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. CP Frequency	f _{max}	1.5 3.3* 5†	8 73 103	— — —	7 64 90	— — —	MHz
CP Pulse Width SPE HIGH (Count)	t _w	1.5 3.3 5	61 6.8 4.8	— — —	69 7.7 5.5	— — —	ns
SPE LOW (Load)	t _w	1.5 3.3 5	61 6.8 4.8	— — —	69 7.7 5.5	— — —	ns
MR Pulse Width (161)	t _w	1.5 3.3 5	55 6.1 4.4	— — —	63 7 5	— — —	ns
Setup Time Pn to CP	t _{su}	1.5 3.3 5	55 6.1 4.4	— — —	63 7 5	— — —	ns
PE or TE to CP	t _{su}	1.5 3.3 5	55 6.1 4.4	— — —	63 7 5	— — —	ns
SPE or MR to CP (163)	t _{su}	1.5 3.3 5	66 7.4 5.3	— — —	75 8.4 6	— — —	ns
Hold Time Pn to CP	t _H	1.5 3.3 5	0 0 0	— — —	0 0 0	— — —	ns
PE or TE to CP	t _H	1.5 3.3 5	0 0 0	— — —	0 0 0	— — —	ns
SPE or MR to CP (163)	t _H	1.5 3.3 5	0 0 0	— — —	0 0 0	— — —	ns
Recovery Time MR to CP (161)	t _{REC}	1.5 3.3 5	66 7.4 5.3	— — —	75 8.4 6	— — —	ns

*3.3 V: min. is @ 3 V

†5 V: min is @ 4.5 V

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Technical Data

CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163

T-45-23-05

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn (SPE HIGH)	t _{PLH} t _{PHL}	1.5 3.3* 5†	— 5.9 4.2	188 21 15	— 5.8 4.1	207 23.1 16.5	ns
CP to Qn (SPE LOW)	t _{PLH} t _{PHL}	1.5 3.3 5	— 5.9 4.2	188 21 15	— 5.8 4.1	207 23.1 16.5	ns
CP to TC	t _{PLH} t _{PHL}	1.5 3.3 5	— 6 4.3	190 21 15.2	— 5.9 4.2	209 23.4 16.7	ns
TE to TC	t _{PLH} t _{PHL}	1.5 3.3 5	— 3.7 2.7	117 13.1 9.4	— 3.6 2.6	129 14.4 10.3	ns
MR to Qn (161)	t _{PLH} t _{PHL}	1.5 3.3 5	— 5.9 4.2	188 21 15	— 5.8 4.1	207 23.1 16.5	ns
MR to TC (161)	t _{PLH} t _{PHL}	1.5 3.3 5	— 5.9 4.2	188 21 15	— 5.8 4.1	207 23.1 16.5	ns
Power Dissipation Capacitance	C _{PD} §	—	66 Typ.		66 Typ.		pF
Input Capacitance	C _I	—	—	10	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§ C_{PD} is used to determine the dynamic power consumption, per flip-flop.

$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where
 f_i = input frequency
 f_o = output frequency
 C_L = output load capacitance
 V_{CC} = supply voltage.

CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163

PREREQUISITE FOR SWITCHING: ACT Series

T-45-23-05

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. CP Frequency	f _{max}	5*	91	—	80	—	MHz
CP Pulse Width	t _w	5	5.4	—	6.2	—	ns
SPE HIGH (Count)		5	5.4	—	6.2	—	ns
SPE LOW (Load)		5	5.3	—	6	—	ns
MR Pulse Width (161)	t _w	5	5.3	—	6	—	ns
Setup Time	t _{su}	5	4.4	—	5	—	ns
Pn to CP		5	5.3	—	6	—	
PE or TE to CP		5	6.6	—	7.5	—	
SPE or MR to CP (163)							
Hold Time	t _h	5	0	—	0	—	ns
Pn to CP		5	0	—	0	—	
PE or TE to CP		5	0	—	0	—	
SPE or MR to CP (163)							
Recovery Time	t _{rec}	5	5.3	—	6	—	ns
MR to CP (161)							

*5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: ACT Series; t_i, t_r = 3 ns, C_L = 50 pF

CHARACTERISTICS	SYMBOL	V _{CC} (V)	AMBIENT TEMPERATURE (T _A) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: CP to Qn (SPE HIGH)	t _{PLH} t _{PHL}	5*	4.2	15	4.1	16.5	ns
CP to Qn (SPE LOW)		5	4.2	15	4.1	16.5	ns
CP to TC		5	4.3	15.2	4.2	16.7	ns
TE to TC		5	2.8	9.8	2.7	10.8	ns
MR to Qn (161)		5	4.2	15	4.1	16.5	ns
MR to TC (161)		5	4.2	15	4.1	16.5	ns
Power Dissipation Capacitance		C _{PD} §	—	66 Typ.		66 Typ.	
Input Capacitance	C _I	—	—	10	—	10	pF

*5 V: min. is @ 5.5 V
max. is @ 4.5 V

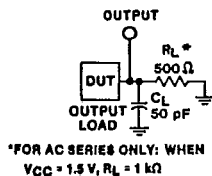
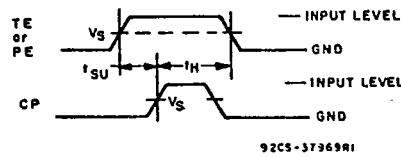
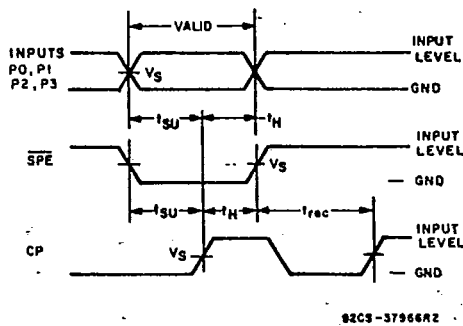
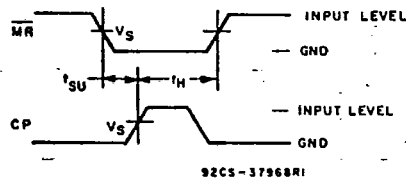
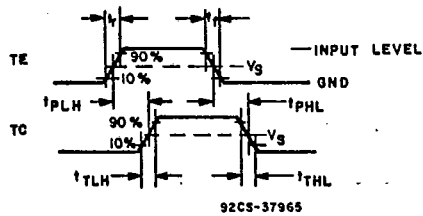
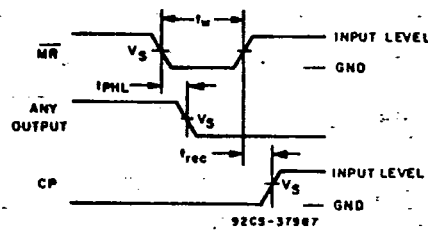
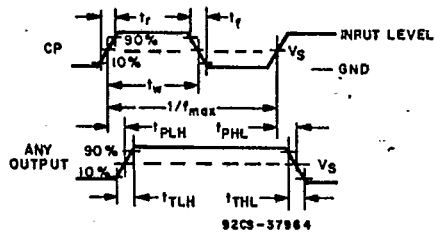
§C_{PD} is used to determine the dynamic power consumption, per flip-flop.

P_D = C_{PD}V_{CC}² f_i + Σ (C_LV_{CC}² f_o) + V_{CC}ΔI_{CC} where f_i = input frequency
f_o = output frequency
C_L = output load capacitance
V_{CC} = supply voltage.

Technical Data

CD54/74AC161, CD54/74AC163
CD54/74ACT161, CD54/74ACT163

T-45-23-05



	CD54/74AC	CD54/74ACT
Input Level	V_{CC}	3 V
Input Switching Voltage, V_S	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, V_S	$0.5 V_{CC}$	$0.5 V_{CC}$

Fig. 1 - Propagation delay times, setup, hold, and recovery times, and test circuit.

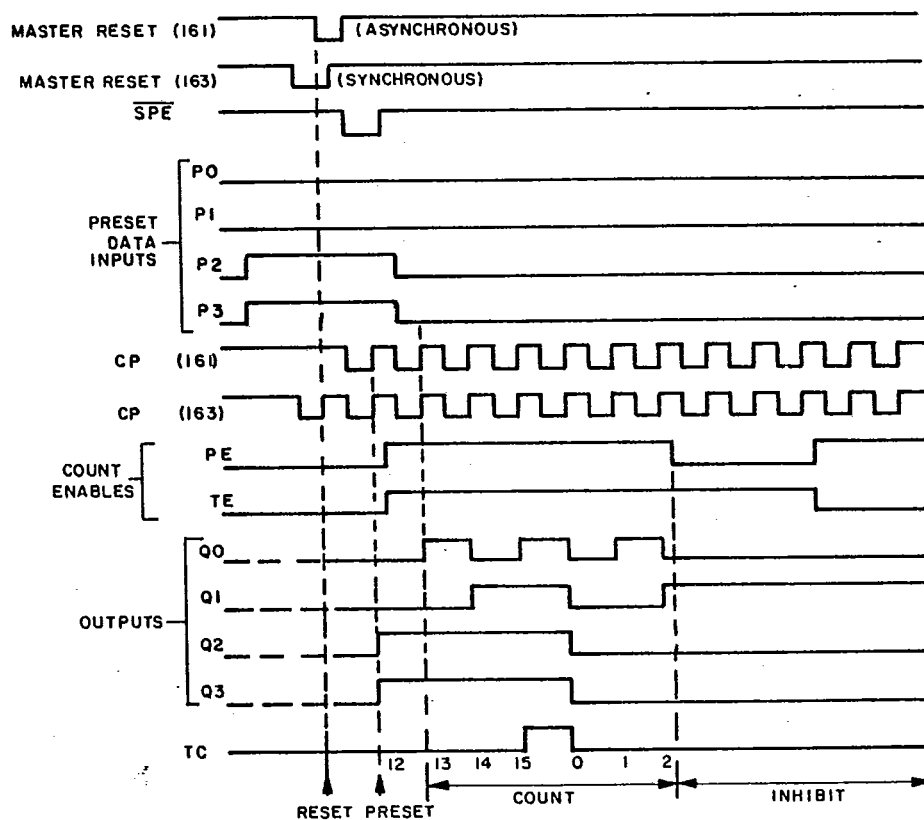
CD54/74AC161, CD54/74AC163

CD54/74ACT161, CD54/74ACT163

T-45-23-05

Sequence illustrated in waveforms

1. Reset outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.

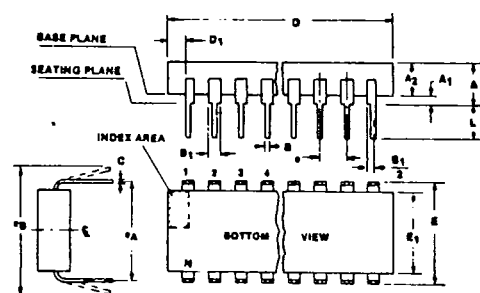


92CM-37962

Fig. 2 - Timing diagrams for the CD54/74AC/ACT 161 and 163.

Dual-In-Line Plastic Packages

T-90-20

(E) Suffix (JEDEC MS-001-AC)
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

92CS-39901

(E) Suffix (JEDEC MS-001-AA)
16-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

92CS-39900

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

$$1, N, \frac{N}{2}, \frac{N}{2} + 1.$$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E₁ does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead lip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D₁ at the left end of the package must equal dimension D₁ at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

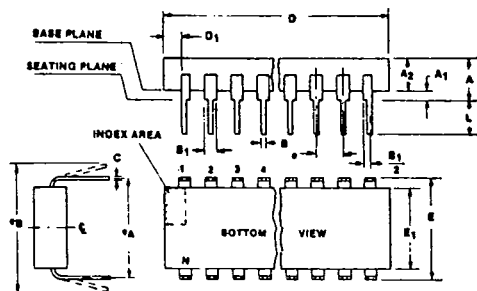
(E) Suffix (JEDEC MS-001-AE)
20-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.925	1.060	23.5	26.9	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	20		20		11

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Dual-In-Line Plastic Packages

T-90-20

(E) Suffix (JEDEC MS-001-AF)
24-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A ₁	0.015	—	0.39	—	9
A ₂	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B ₁	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	1.125	1.275	28.6	32.3	4
D ₁	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E ₁	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e _A	0.300 BSC		7.62 BSC		9
e _B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

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Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

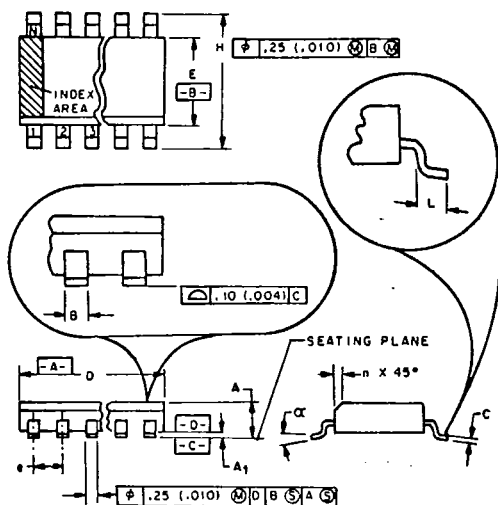
$$1, N, \frac{N}{2}, \frac{N}{2} + 1.$$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E₁ does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around

center line shown in end view.

8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D₁ at the left end of the package must equal dimension D₁ at the right end of the package within 0.030 in. (0.76 mm).
13. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

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Dual-In-Line Small-Outline Plastic Packages



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "D" is a reference datum.
4. "A" and "B" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

T-90-20

M Suffix (JEDEC MS-012AB)

14-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A ₁	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

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M Suffix (JEDEC MS-012AC)

16-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A ₁	0.0040	0.0098	0.10	0.25	
B	0.0138	0.020	0.35	0.508	
C	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38925R2

M Suffix (JEDEC MS-013AC)

20-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A ₁	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.4861	0.5118	12.60	13.00	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38926R2

M Suffix (JEDEC MS-013AD)

24-Lead Dual-In-Line Small-Outline (SO) Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A ₁	0.0040	0.0118	0.10	0.30	
B	0.0138	0.020	0.35	0.508	
C	0.0091	0.0125	0.23	0.32	
D	0.5985	0.6141	15.20	15.60	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-39037R2