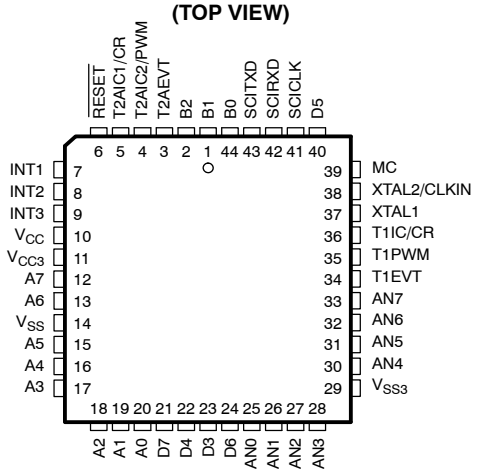
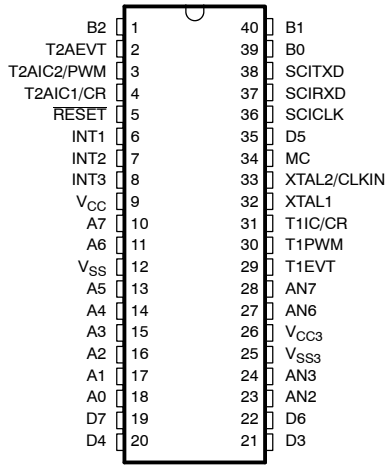
SPNS016C – NOVEMBER 1992 – REVISED FEBRUARY 1997

- CMOS/EEPROM/EPROM Technologies on a Single Device
  - Mask-ROM Devices for High Volume Production
  - One-Time-Programmable (OTP) Devices for Low-Volume Production
  - Reprogrammable EPROM Devices for Prototyping Purposes
- Flexible Operating Features
  - Low-Power Modes: STANDBY and HALT
  - Commercial, Industrial, and Automotive Temperature Ranges
  - Clock Options:
    - Divide-by-1 (2 MHz–5 MHz SYSCLK) Phase-Locked Loop (PLL)
    - Divide-by-4 (0.5 MHz–5 MHz SYSCLK)
  - Voltage (V_{CC}) 5 V ± 10%
- Internal System Memory Configurations
  - On-Chip Program Memory Versions
    - ROM: 4K Bytes or 8K Bytes
    - EPROM: 8K Bytes
  - Data EEPROM: 256 Bytes
  - Static RAM: 256 Bytes Usable as Registers
- Two 16-Bit General-Purpose Timers
  - Software Configurable as Two 16-Bit Event Counters, or Two 16-Bit Pulse Accumulators, or Three 16-Bit Input Capture Functions, or Four Compare Registers, or Two Self-Contained Pulse-Width-Modulation (PWM) Functions
- Serial Communications Interface 1 (SCI1)
  - Asynchronous and Isosynchronous† Modes
  - Full Duplex, Double Buffered RX and TX
  - Two Multiprocessor Communications Formats
- CMOS/Package/TTL Compatible I/O Pins
  - All Peripheral Function Pins Software Configurable for Digital I/O
  - 40-Pin Plastic and Ceramic Dual-In-Line Packages/27 Bidirectional, 5 Input Pins
  - 44-Pin Plastic and Ceramic Leaded Chip Carrier Packages/27 Bidirectional, 9 Input Pins
- On-Chip 24-Bit Watchdog Timer

FN AND FZ PACKAGES
(TOP VIEW)



JC, JD, N, AND NJ PACKAGES
(TOP VIEW)



- Eight-Bit ADC1
  - Four Channels in 40-Pin Packages
  - Eight Channels in 44-Pin Packages
- Flexible Interrupt Handling
- TMS370 Series Compatibility
- Workstation/PC-Based Development System
  - C Compiler Support
  - Real-Time In-Circuit Emulation
  - C Source Debug
  - Extensive Breakpoint/Trace Capability
  - Software Performance Analysis
  - Multi-Window User Interface
  - EEPROM/EPROM Programming

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† Isosynchronous = Isochronous

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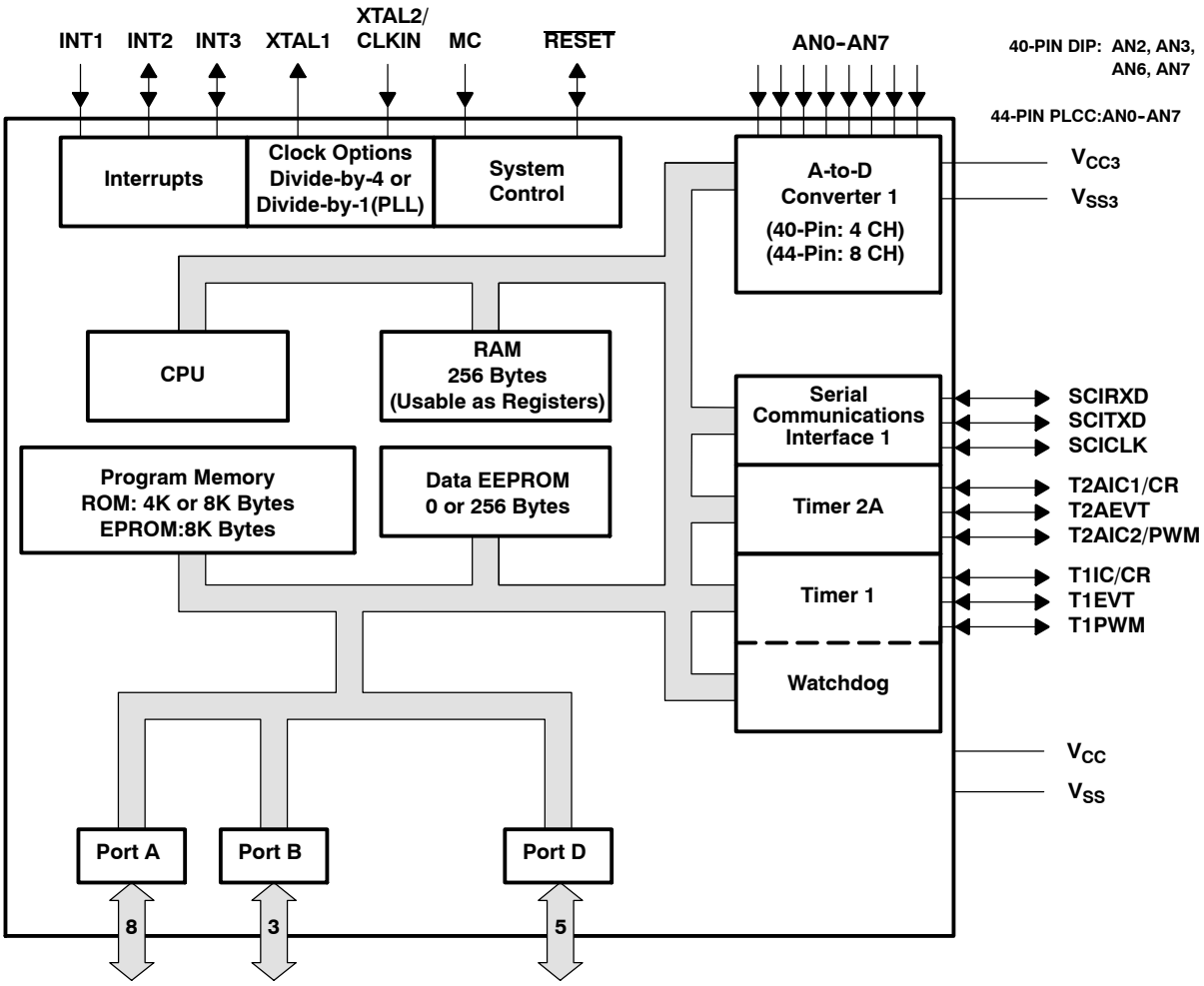
Pin Descriptions

PIN			TYPE†	DESCRIPTION
	NO.			
	DIP (40)	LCC (44)		
A0	18	20	I/O	Port A pins are general-purpose bidirectional I/O ports.
A1	17	19		
A2	16	18		
A3	15	17		
A4	14	16		
A5	13	15		
A6	11	13		
A7	10	12		
B0	39	44	I/O	Port B pins are general-purpose bidirectional I/O ports.
B1	40	1		
B2	1	2		
D3	21	23	I/O	Port D pins are general-purpose bidirectional I/O ports. D3 is also configurable as SYSCLK.
D4	20	22		
D5	35	40		
D6	22	24		
D7	19	21		
AN0/E0	—	25	I	Analog-to-digital converter 1 (ADC1) analog input channels or positive reference pins; any ADC1 channel can be programmed as general-purpose input pin (E port) if not used as an analog input or reference channel.
AN1/E1	—	26		
AN2/E2	23	27		
AN3/E3	24	28		
AN4/E4	—	30		
AN5/E5	—	31		
AN6/E6	27	32		
AN7/E7	28	33		
V_{CC3}	26	11		ADC1 converter positive supply voltage and optional positive reference input pin
V_{SS3}	25	29		ADC1 converter ground supply and low reference input pin
INT1	6	7	I	External (non-maskable or maskable) interrupt/general-purpose input pin
INT2	7	8	I/O	External maskable interrupt input/general-purpose bidirectional pin
INT3	8	9	I/O	External maskable interrupt input/general-purpose bidirectional pin
T1IC/CR	31	36	I/O	Timer 1 input capture/counter reset input pin/general-purpose bidirectional pin
T1PWM	30	35		Timer 1 pulse-width-modulation output pin/general-purpose bidirectional pin
T1EVT	29	34		Timer 1 external event input pin/general-purpose bidirectional pin
T2AIC1/CR	4	5	I/O	Timer 2A input capture/counter reset input pin/general-purpose bidirectional pin
T2AIC2/PWM	3	4		Timer 2A input capture 2/PWM output pin/general-purpose bidirectional pin
T2AEVT	2	3		Timer 2A external event input pin/general-purpose bidirectional pin
SCITXD	38	43	I/O	SCI transmit data output pin/general-purpose bidirectional pin ‡
SCIRXD	37	42		SCI receive data input pin/general-purpose bidirectional pin
SCICLK	36	41		SCI bidirectional serial clock pin/general-purpose bidirectional pin
$\overline{\text{RESET}}$	5	6	I/O	System reset bidirectional pin. As input, $\overline{\text{RESET}}$ initializes microcontroller; as open-drain output, $\overline{\text{RESET}}$ indicates detection of an internal fault by the watchdog or oscillator fault circuit.
MC	34	39	I	Mode control input pin; enables the EEPROM write-protection-override (WPO) mode, also EPROM V_{PP}.
XTAL1	32	37	I	Internal-oscillator output for crystal
XTAL2/CLKIN	33	38	O	Internal-oscillator crystal input/external clock source input
V_{CC}	9	10		Positive supply voltage
V_{SS}	12	14		Ground reference

† I = input, O = output

‡ The three-pin configuration SCI is referred to as SCI1.

functional block diagram



description

The TMS370C040A, TMS370C042A, TMS370C340A, TMS370C342A, TMS370C742A, and SE370C742A devices are members of the TMS370 family of single-chip 8-bit microcontrollers. Unless otherwise noted, the term TMS370Cx4x refers to these devices. TMS370 family provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations.

The TMS370Cx4x family is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technology. The low-operating power, wide-operating temperature range, and noise immunity of CMOS technology coupled with the high performance and extensive on-chip peripheral functions make the TMS370Cx4x devices attractive in system designs for automotive electronics, industrial motor, computer peripheral control, telecommunications, and consumer applications.

The TMS370Cx4x devices contain the following on-chip peripheral modules:

- Eight-channel (for 44 pin device) or four-channel (for 40-pin device) 8-bit analog-to-digital converter 1 (ADC1)
- Serial communications interface 1 (SCI1)
- Two 16-bit general-purpose timers (one with an 8-bit prescaler)

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description (continued)

- One 24-bit general-purpose watchdog timer

Table 1 provides an overview of the various memory configurations of the TMS370Cx4x devices.

Table 1. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		DATA MEMORY (BYTES)		PACKAGES 44 PIN/PLCC/CLCC OR 40 PIN PDIP/CDIP/PSDIP/CSDIP
	ROM	EPROM	RAM	EEPROM	
TMS370C040A	4K	—	256	256	FN-PLCC N-PDIP NJ-PSDIP†
TMS370C042A	8K	—	256	256	FN-PLCC N-PDIP NJ-PSDIP†
TMS370C340A	4K	—	256	—	FN-PLCC N-PDIP NJ-PSDIP†
TMS370C342A	8K	—	256	—	FN-PLCC N-PDIP NJ-PSDIP†
TMS370C742A	—	8K	256	256	FN-PLCC N-PDIP NJ-PSDIP†
SE370C742A‡	—	8K	256	256	FZ-CLCC JD-CDIP JC-CSDIP

† The NJ designator for the 40-pin plastic shrink DIP package was known formerly as the N2. The mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

‡ System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

The suffix letter (A) appended to the device name (shown in the first column of Table 1) indicates the configuration of the device. ROM and EPROM devices have different configurations as indicated in Table 2. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 2. Suffix Letter Configuration

DEVICE	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (standard oscillator)	Enabled
ROM A	Standard	Divide-by-4 (standard oscillator) or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		

The 4K bytes and 8K bytes of mask-programmable ROM in the TMS370C040A, TMS370C042A, TMS370C340A and TMS370C342A are replaced in the TMS370C742 with 8K bytes of EPROM while all other available memory and on-chip peripherals are identical, with the exception of no data EEPROM on the TMS370C340A and TMS370C342A devices. The OTP (TMS370C742A) device and the reprogrammable device (SE370C742A) are available.

TMS370C742A (OTP) devices are available in plastic packages. This microcontroller is effective to use for immediate production updates for other members of the TMS370Cx4x family or for low-volume production runs when the mask charge or cycle time for the low-cost mask ROM devices is not practical.

description (continued)

The SE370C742A has a windowed ceramic package to allow reprogramming of the program EPROM memory during the development/prototyping phase of design. The SE370C742A device allows quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx4x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all central processing unit (CPU) activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx4x features advanced register-to-register architecture that allows arithmetic and logical operations without requiring an accumulator (e.g., ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx4x family is fully instruction-set-compatible, allowing easy transition between members of the TMS370 8-bit microcontroller family.

The TMS370Cx4x family offers an 8-channel ADC1 with 8-bit accuracy for the 44-pin PLCC packages and also offers a 4-channel ADC1 for the 40-pin DIP packages. The 33-μs conversion time at 5-MHz SYSCLK and the variable sample period, combined with selectable positive reference voltage sources, turn analog signals into digital data.

The serial communications interface 1 (SCI1) module is a built-in serial interface that can be programmed to be asynchronous or isosynchronous to give two methods of serial communications. The SCI allows standard RS-232-C communications with other common data transmission equipment. The CPU takes no part in serial communications except to write data to be transmitted to a register and to read data received from a register.

The TMS370Cx4x family provides the system designer with very economical, efficient solutions to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370Cx4x into an ever-increasing number of complex applications. The application source code can be written in assembly and C languages, and the output code can be generated by the linker. The TMS370 family XDS communicates through a standard RS-232-C interface with a personal computer, allowing use of the personal computer editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive use of menus and screen windowing so that a system designer with minimal training can begin developing software. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation, as well as reduced time-to-market cycle.

The TMS370Cx4x family together with the TMS370 family XDS, CDT370, starter kit, software tools, the SE370C742A reprogrammable devices, comprehensive product documentation, and customer support provide a complete solution for the needs of the system designer.

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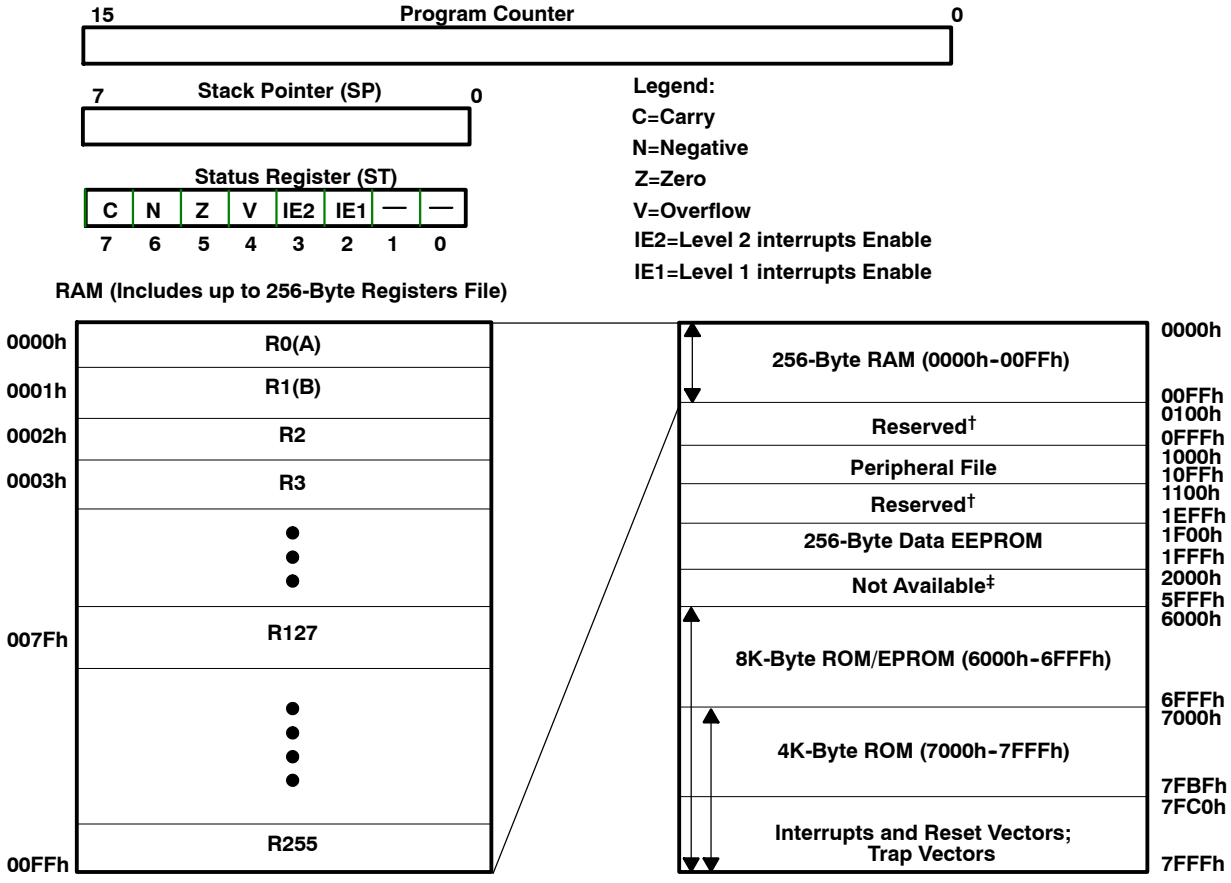
central processing unit (CPU)

The CPU used on the TMS370Cx4x device is the high-performance 8-bit TMS370 CPU module. The ’x4x implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete ’x4x instruction map is shown in Table 17 in the TMS370Cx4x instruction set overview section.

The ’370Cx4x CPU architecture provides the following components:

- CPU registers:
  - A stack pointer (SP) that points to the last entry in the memory stack
  - A status register (ST) that monitors the operation of the instructions and contains the global-interrupt-enable bits
  - A program counter (PC) that points to the memory location of the next instruction to be executed

Figure 1 illustrates the CPU registers and memory blocks.



† Reserved means the address space is reserved for future expansion.
‡ Not available means the address space is not accessible.

Figure 1. Programmer’s Model

central processing unit (CPU) (continued)

- A memory map that includes:
  - 256-byte general-purpose RAM that can be used for data memory storage, program instructions, general-purpose registers, or the stack
  - A peripheral file that provides access to all internal peripheral modules, system-wide control functions and EEPROM/EPROM programming control
  - 256-byte EEPROM module that provides in-circuit programmability and data retention in power-off conditions
  - 4K- or 8K-byte ROM or 8K-byte EPROM program memory

stack pointer (SP)

The SP is an 8-bit CPU register. The stack operates as a last-in, first-out, read/write memory. The stack is used typically to store the return address on subroutine calls as well as the status-register contents during interrupt sequences.

The SP points to the last entry or top of the stack. The SP is incremented automatically before data is pushed onto the stack and decremented after data is popped from the stack. The stack can be placed anywhere in the on-chip RAM memory.

status register (ST)

The ST monitors the operation of the instructions and contains the global interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional jump instructions) use the status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST register, status-bit notation, and status-bit definitions are shown in Table 3.

Table 3. Status Registers

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most significant byte (MSbyte) and least significant byte (LSbyte) of a 16-bit address.

The contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter during reset. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of memory locations 7FFEh and 7FFFh (reset vector).

program counter (PC) (continued)

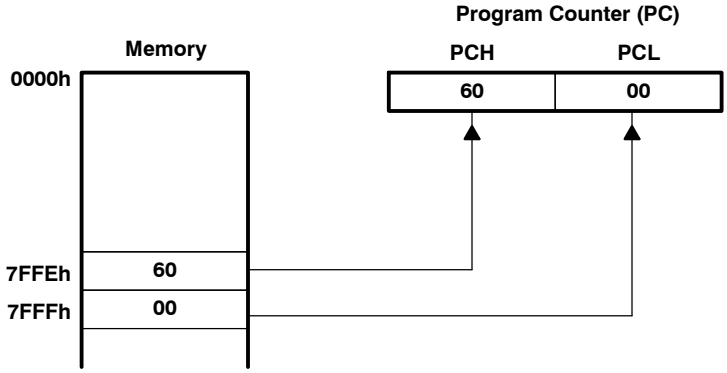


Figure 2. Program Counter After Reset

memory map

The TMS370Cx4x family architecture is based on the Von Neumann architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. As shown in Figure 3, the TMS370Cx4x family provides memory-mapped RAM, ROM, data EEPROM, EPROM, input/output pins, peripheral functions, and system interrupt vectors.

The peripheral file contains all input/output port control, peripheral status and control, EPROM and EEPROM memory programming, and system-wide control functions. The peripheral file is located between 1010h and 107Fh and is logically divided into seven peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed.

memory map (continued)

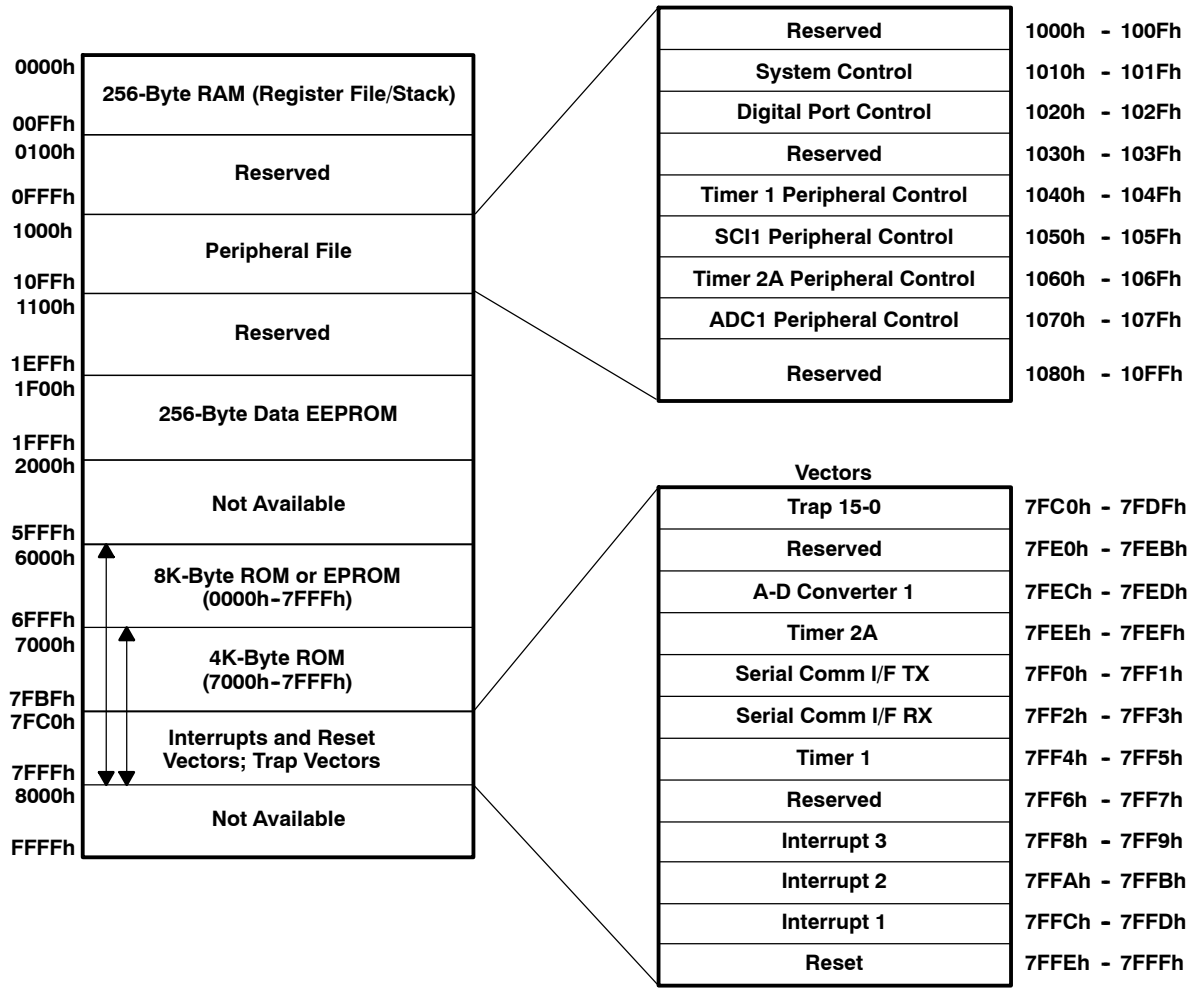


Figure 3. TMS370Cx4x Memory Map

RAM/register file (RF)

Locations within the RAM address space can serve as the RF, general-purpose read/write memory, program memory, or the stack instructions. The TMS370Cx4x devices contain 256 bytes of internal RAM memory mapped beginning at location 0000h (R0) and continuing through location 00FFh (R255).

The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx4x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 4 shows the TMS370Cx4x PF address map.

peripheral file (PF) (continued)

Table 4. TMS370Cx4x Peripheral File Address Map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h–100Fh	P000–P00F	Reserved for factory test
1010h–101Fh	P010–P01F	System and EPROM/EEPROM control registers
1020h–102Fh	P020–P02F	Digital I/O port control registers
1030h–103Fh	P030–P03F	Reserved
1040h–104Fh	P040–P04F	Timer 1 registers
1050h–105Fh	P050–P05F	Serial communications interface 1 registers
1060h–106Fh	P060–P06F	Timer 2A registers
1070h–107Fh	P070–P07F	Analog-to-digital converter 1 registers
1080h–10FFh	P080–P0FF	Reserved

data EEPROM

The TMS370Cx4x devices, containing 256 bytes of data EEPROM, have memory mapped beginning at location 1F00h and continuing through location 1FFFh. Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
  - Bit-, byte-, and block-write/erase modes
  - Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
  - Control register: Data EEPROM programming is controlled by the DEECTL located in the PF frame beginning at location P01A (see Table 5).
  - In-circuit programming capability. There is no need to remove the device to program it.
- Write protection. Writes to the data EEPROM are disabled during the following conditions.
  - Reset. All programming of the data EEPROM module is halted.
  - Write protection active. There is one write-protect bit per 32-byte EEPROM block.
  - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 5. Data EEPROM and PROGRAM EPROM Control Register Memory Map

ADDRESS	SYMBOL	NAME
P01A	DEECTL	DATA EEPROM Control Register
P01B	—	Reserved
P01C	EPCTL	Program EPROM Control Register

program EPROM

The TMS370C742A device contains 8K bytes of EPROM mapped, beginning at location 6000h and continuing through location 7FFFh. Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments (TI™), and memory addresses 7FECh through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh. Reading the program EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPROM control register (EPCTL). The program EPROM module features include:

- Programming
  - In-circuit programming capability if V_{PP} is applied to MC
  - Control register: EPROM programming is controlled by the EPROM control register (EPCTL) located in the peripheral file (PF) frame at location P01C as shown in Table 5.
- Write protection: writes to the program EPROM are disabled under the following conditions:
  - Reset: All programming to the EPROM module is halted.
  - Low-power modes
  - 13 V not applied to MC

program ROM

The program ROM consists of 4K or 8K bytes of mask-programmable read-only memory. The program ROM is used for permanent storage of data or instructions. Memory addresses 7FE0h through 7FEBh are reserved for TI, and memory addresses 7FECh through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions, are located between addresses 7FC0h and 7FDFh. Programming of the mask ROM is performed at the time of device fabrication.

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx4x CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are generated internally, while one ($\overline{\text{RESET}}$ pin) is controlled externally. These actions are as follows:

- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout . See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside of the recommended operating range. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.
- External $\overline{\text{RESET}}$ pin. A low level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 Family User's Guide* (literature number SPNU127) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x4x device to reset external system components. Additionally, if a cold start (V_{CC} is off for several hundred milliseconds) condition or oscillator failure occurs or the $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator-fault flag (OSC FLT FLAG, SCCR0.4), the cold-start flag (COLD START, SCCR0.7) and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 6 lists the reset sources.

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system reset (continued)

Table 6. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers are initialized: ST = 00h, SP = 01h (reset state).
2. Registers A and B are initialized to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state.

interrupts

The TMS370 family software-programmable interrupt structure supports flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 4. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be independently enabled by the global-interrupt enable bits (IE1 and IE2) of the status register.

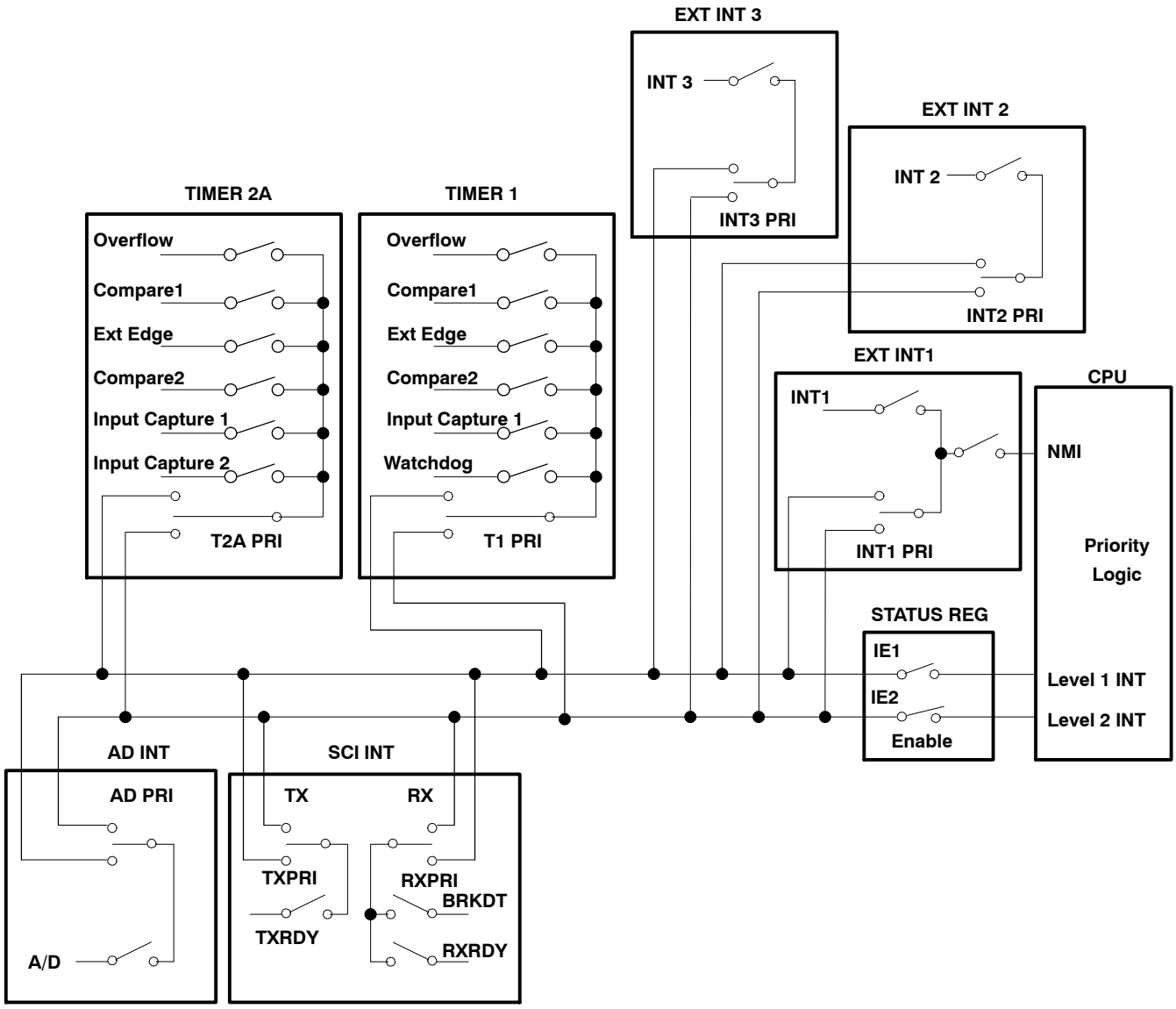

Figure 4. Interrupt Control

Each system interrupt is configured independently on either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is configured selectively on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority

interrupts (continued)

chains is performed within the peripheral modules to support interrupt expansion to future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx4x has eight hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 7. Each system interrupt has a dedicated interrupt vector located in program memory through which control is passed to the interrupt service routines. A system interrupt can have multiple interrupt sources (e.g., SCI RXNT has two interrupt sources). All of the interrupt sources are individually maskable by local interrupt-enable control bits in the associated peripheral file. Each interrupt source FLAG bit is individually readable for software polling or for determining which interrupt source generated the associated system interrupt.

Five of the system interrupts are generated by on-chip peripheral functions, and three external interrupts are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in peripheral file frame 1. Each external interrupt is individually software-configurable for input polarity (rising or falling) for ease of system interface. External interrupt INT1 is software-configurable as either a maskable or non-maskable interrupt. When INT1 is configured as non-maskable, it cannot be masked by the individual- or global-enable mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software-configured as general-purpose input/output pins if the interrupt function is not required (INT1 can be configured similarly as an input pin).

Table 7. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY†
External $\overline{\text{RESET}}$ Watchdog Overflow Oscillator Fault Detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	$\overline{\text{RESET}}$‡	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1‡	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2‡	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3†	7FF8h, 7FF9h	4
Timer 1 Overflow Timer 1 Compare 1 Timer 1 Compare 2 Timer 1 External Edge Timer 1 Input Capture Watchdog Overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC INT FLAG WD OVRFL INT FLAG	T1INT§	7FF4h, 7FF5h	5
SCI RX Data Register Full SCI RX Break Detect	RXRDY FLAG BRKDT FLAG	RXINT‡	7FF2h, 7FF3h	6
SCI TX Data Register Empty	TXRDY FLAG	TXINT	7FF0h, 7FF1h	7
Timer 2A Overflow Timer 2A Compare 1 Timer 2A Compare 2 Timer 2A External Edge Timer 2A Input Capture 1 Timer 2A Input Capture 2	T2A OVRFL INT FLAG T2AC1 INT FLAG T2AC2 INT FLAG T2AEDGE INT FLAG T2AIC1 INT FLAG T2AIC2 INT FLAG	T2AINT	7FEEh, 7FEFh	8
A-D Conversion Complete	AD INT FLAG	ADINT	7FECh, 7FEDh	9

† Relative priority within an interrupt level.
‡ Releases microcontroller from STANDBY and HALT low-power modes.
§ Releases microcontroller from STANDBY low-power mode.

privileged operation and EEPROM write-protection override

The TMS370Cx4x family has significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once defined for an end application. Following a hardware reset, the TMS370Cx4x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) is set to 1, entering the nonprivileged mode and disabling write operations to specific configuration control bits within the peripheral file. The system-configuration bits listed in Table 8 are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

Table 8. Privilege Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCR0	P010.5 P010.6	PF AUTO WAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
SCIPRI	P05F.4 P05F.5 P05F.6 P05F.7	SCI ESPEN SCI RX PRIORITY SCI TX PRIORITY SCI STEST
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST
T2APRI	P06F.6 P06F.7	T2A PRIORITY T2A STEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD STEST

† The privileged bits are shown in a bold typeface in the peripheral file frames of the following sections.

The WPO mode provides an external hardware method for overriding the write protection registers (WPR) of data EEPROM on the TMS370Cx4x. Applying a 12-V input to the MC pin after the $\overline{\text{RESET}}$ pin input goes high causes the device to enter WPO mode. The high voltage on the MC pin during the WPO mode is not the programming voltage for the data EEPROM or program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system level capability to modify the content of data EEPROM while the device remains in the application but only while requiring a 12-V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx4x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time the mask is manufactured.

low-power and IDLE modes (continued)

The STANDBY and HALT low-power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls which low-power mode is entered.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, Timer 1, and the receive start-bit-detection circuit of the SCI1 remain active. System processing is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$, external interrupt on INT1, INT2, INT3, Timer 1 interrupt, or a low level on the receive pin of the serial communications interface 1) is detected.

In the HALT mode (HALT/STANDBY=1), the TMS370Cx4x is placed in its lowest power-consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$ external interrupt on INT1, INT2, INT3, or low level on the receive pin of the SCI1) is detected. The power-down mode selection bits are sumarized in Table 9.

Table 9. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X	IDLE

X = don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6–7 bits is ignored. In addition, if an idle instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is automatically enabled as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is always generated, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU-instruction processing is stopped during the STANDBY and HALT modes, the clocking of the WD timer is inhibited.

clock modules

The 'x4x family provides two clock options that are referred to as divide-by-1 (phase-locked loop) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The 'x4x ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. The '742A EPROM has only the divide-by-4.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 clock module option provides a one-to-one match of the external resonator frequency (CLKIN) to the internal system clock (SYSCLK) frequency. The divide-by-4 option produces a SYSCLK which is one-fourth of the frequency of the external resonator. Inside of the divide-by-1 module, the frequency of the external resonator is multiplied by four, and the clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency.

clock modules (continued)

These are formulated as follows:

$$\text{Divide-by-4}: \text{SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1}: \text{SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the reduction of EMI. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 option provides the capability of reducing the resonator speed by four times, resulting in a steeper decay of emissions produced by the oscillator.

system configuration registers

Table 10 contains system configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface.

Table 10. Peripheral File Frame 1: System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	**OSC POWER**	**PF AUTO WAIT**	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011	—	—	—	**AUTOWAIT DISABLE**	—	**MEMORY DISABLE**	—	—	SCCR1
P012	**HALT/ STANDBY**	**PWRDWN/ IDLE**	—	**BUS STEST**	**CPU STEST**	—	**INT1 NMI**	**PRIVILEGE DISABLE**	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D P01E P01F	Reserved								

digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 11 and Table 12 detail the specific addresses, registers, and control bits within the peripheral file frame.

Table 11. Peripheral File Frame 2: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	—	—	—	—	—	Port B Control Register 2 (must be 0)			BPORT2
P026	—	—	—	—	—	Port B Data			BDATA
P027	—	—	—	—	—	Port B Direction			BDIR
P028 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0)†					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR

† To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 12. Port Configuration Register Setup

PORT	PIN	abcd 00q1	abcd 00y0
A	0 – 7	Data Out q	Data In y
B	0 – 2	Data Out q	Data In y
D	3 – 7	Data Out q	Data In y
a = Port × Control Register 1 b = Port × Control Register 2 c = Data d = Direction			

timer 1 module

The programmable Timer 1 (T1) module of the TMS370Cx4x provides the designer with the enhanced timer resources required to perform real-time system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers, T1 and WD, allow program selection of input clock sources (real-time, external event, or pulse accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The T1 module includes three external device pins that can be used for multiple counter functions (operation-mode dependent), or used as general-purpose I/O pins. The T1 module block diagram is shown in Figure 5.

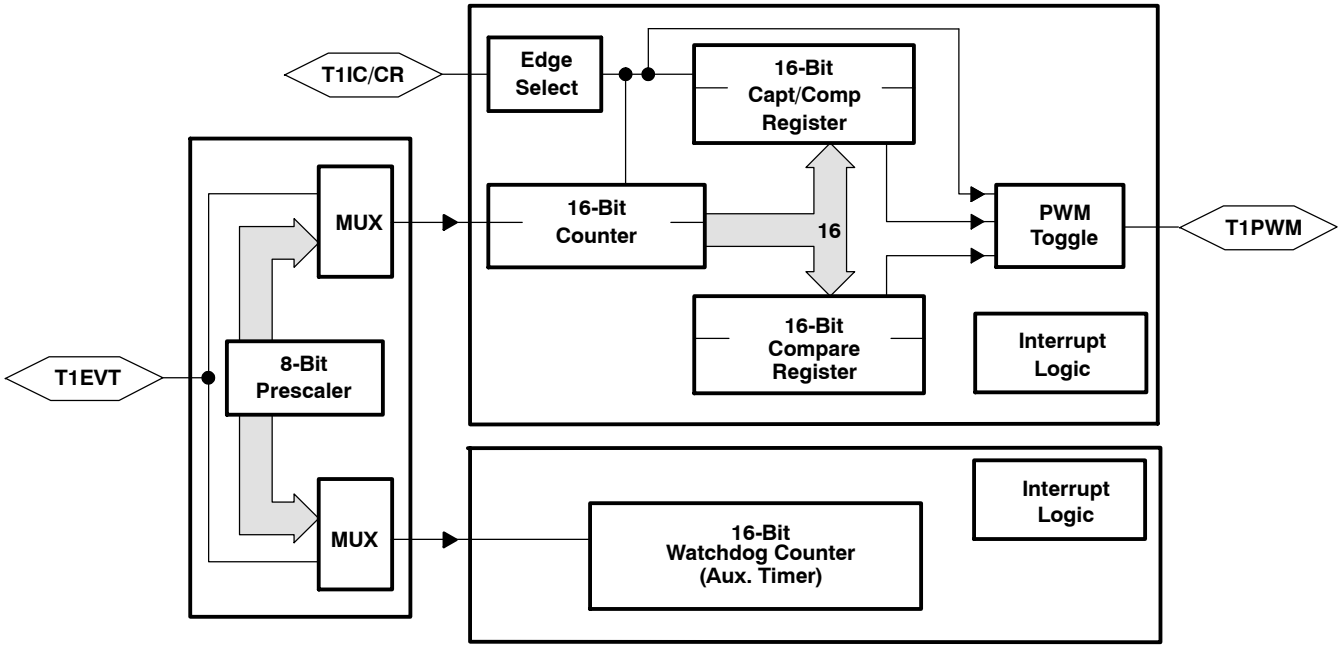

Figure 5. Timer 1 Block Diagram

- Three T1 I/O pins
  - T1IC/CR: T1 input capture / counter-reset input pin, or general-purpose bidirectional I/O pin
  - T1PWM: T1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
  - T1EVT: T1 event input pin, or general-purpose bidirectional I/O pin
- Two operational modes:
  - Dual-compare mode: Provides PWM signal
  - Capture/compare mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register.
- One 16-bit WD counter can be used as an event counter, a pulse accumulator, or an interval timer if WD feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer

timer 1 module (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR)
- Interrupts that can be generated on the occurrence of:
  - A capture
  - A compare equal
  - A counter overflow
  - An external edge detection
- Sixteen T1 module control registers located in the PF frame, beginning at address P040

The T1 module control registers are illustrated in Table 13.

timer 1 module (continued)

Table 13. Timer 1 Module Registers Memory Map†

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	Modes: Dual-Compare and Capture/Compare								
P040	Bit 15			T1 Counter MSB				Bit 8	T1CNTR
P041	Bit 7			T1 Counter LSB				Bit 0	
P042	Bit 15			Compare Register MSB				Bit 8	T1C
P043	Bit 7			Compare Register LSB				Bit 0	
P044	Bit 15			Capture/Compare Register MSB				Bit 8	T1CC
P045	Bit 7			Capture/Compare Register LSB				Bit 0	
P046	Bit 15			Watchdog Counter MSB				Bit 8	WDCNTR
P047	Bit 7			Watchdog Counter LSB				Bit 0	
P048	Bit 7			Watchdog Reset Key				Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1INPUT SELECT2	T1INPUT SELECT1	T1INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
	Mode: Dual-Compare								
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
	Mode: Capture/Compare								
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
	Modes: Dual-Compare and Capture/Compare								
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	**T1 STEST**	**T1 PRIORITY**	—	—	—	—	—	—	T1PRI

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

timer 1 module (continued)

Figure 6 shows the T1 dual-compare mode block diagram. The annotations on the diagram identify the register and the bits in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

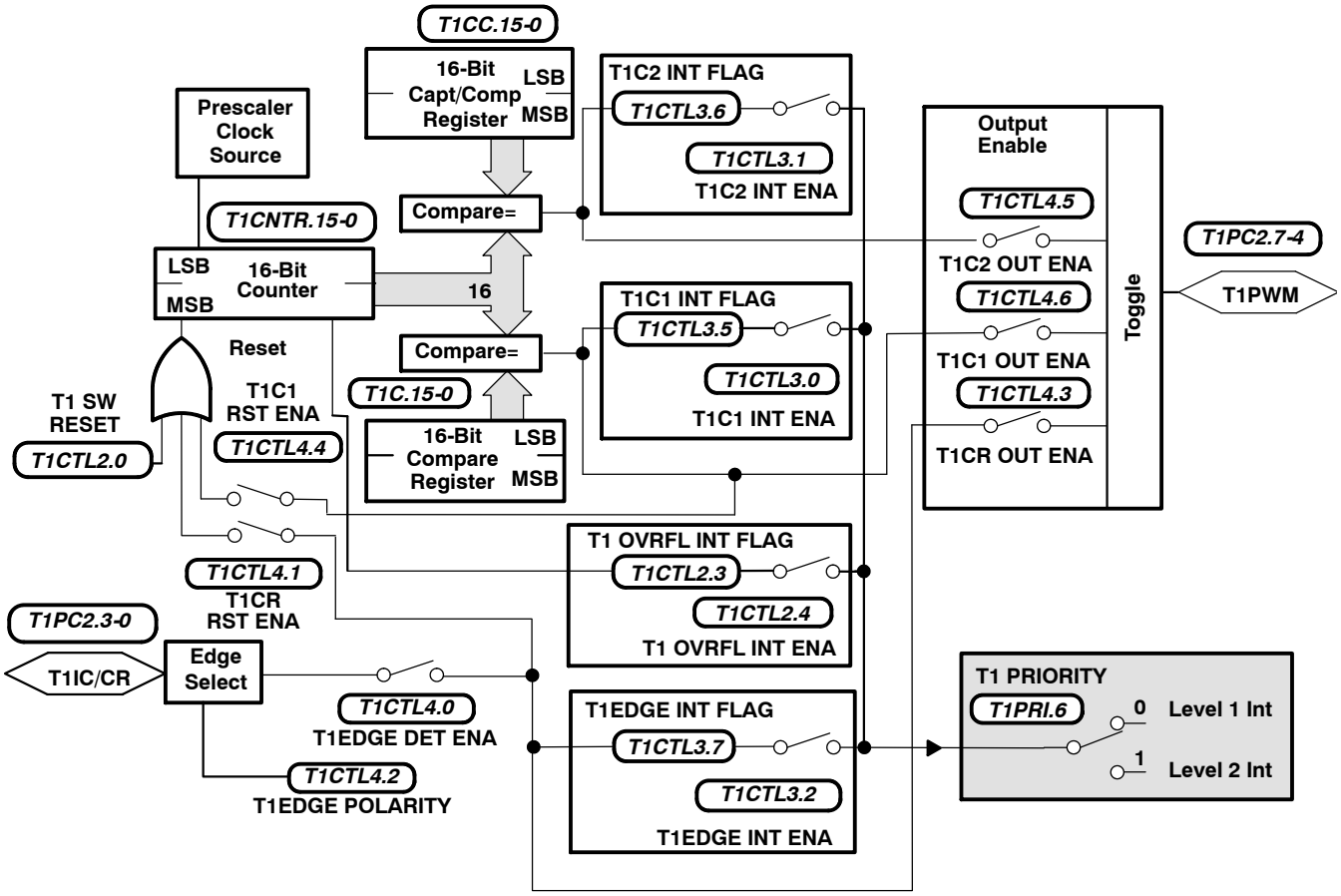

Figure 6. Timer 1: Dual-Compare Mode

timer 1 module (continued)

Figure 7 shows the T1 capture/compare mode block diagram. The annotations on the diagram identify the register and the bits in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

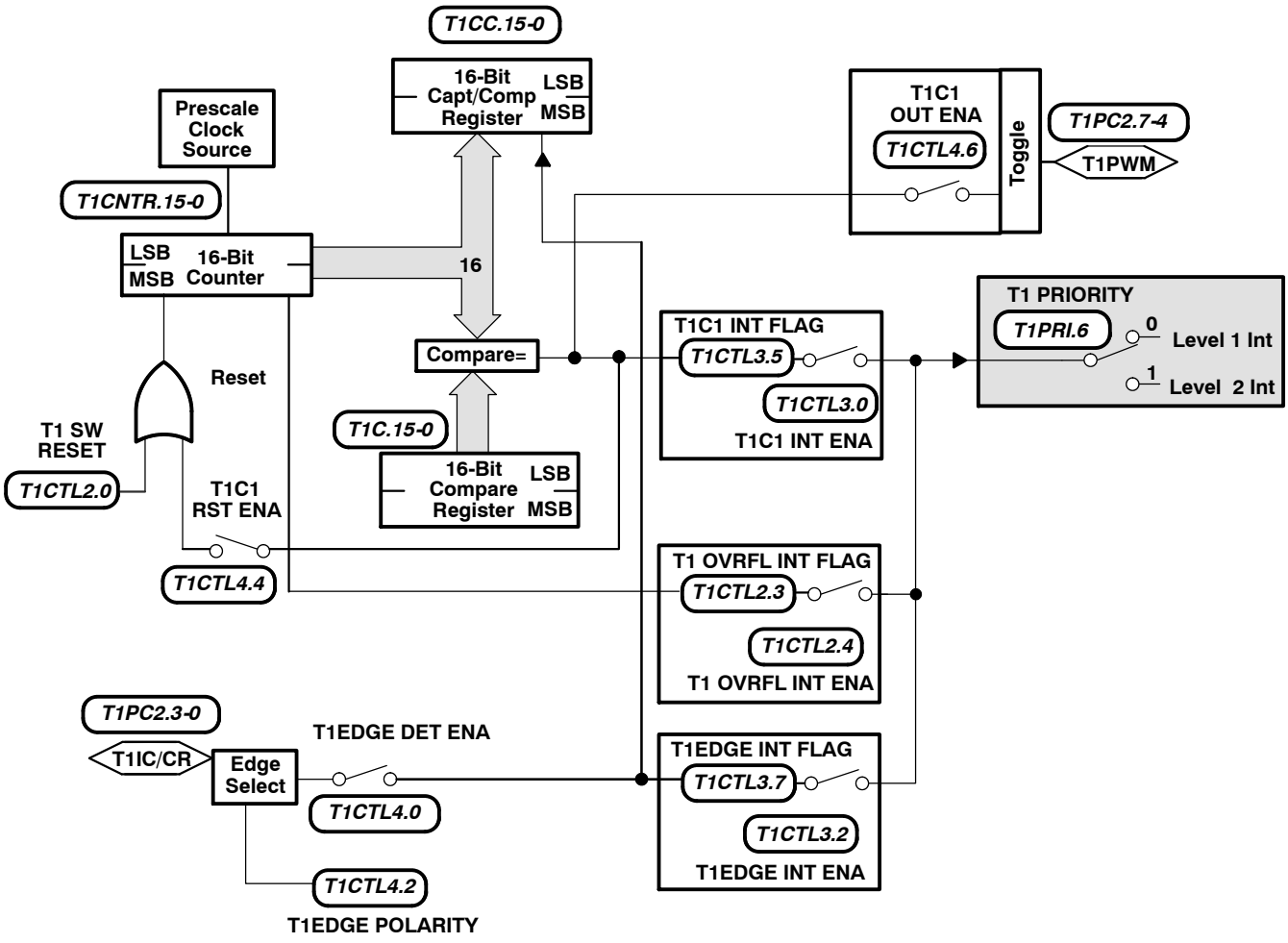

Figure 7. Timer 1: Capture/Compare Mode

timer 1 module (continued)

The TMS370Cx4x device includes a 24-bit WD timer, contained in the T1 module, which can be programmed as an event counter, pulse accumulator, or interval timer if the WD function is not used. The WD function is to monitor software and hardware operation and to implement a system reset when the WD counter is not properly serviced (WD counter overflow or WD counter is re-initialized by an incorrect value). The WD can be configured as one of three mask options as follows:

- Standard WD configuration (see Figure 8) for ’C742A EPROM and mask-ROM devices:
  - Watchdog mode
    - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCLK
    - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written
    - Generates a system reset if an incorrect value is written to the WD reset key or if the counter overflows
    - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
  - Non-watchdog mode
    - Watchdog timer can be configured as an event counter, pulse accumulator, or an interval timer

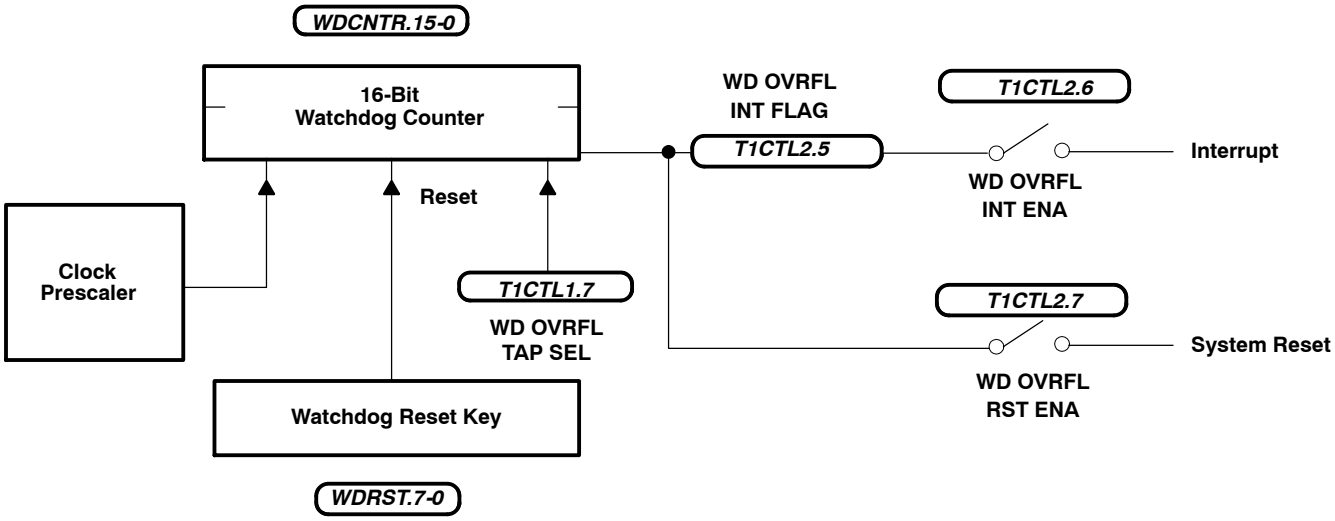

Figure 8. Standard Watchdog

timer 1 module (continued)

- Hard watchdog configuration (see Figure 9) for mask-ROM devices only:
  - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCLK
  - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
  - Generates a system reset if an incorrect value is written to the WDRST or if the counter overflows
  - A WD overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
  - Automatic activation of the WD timer upon power-up reset
  - INT1 is enabled as a nonmaskable interrupt during low power modes.

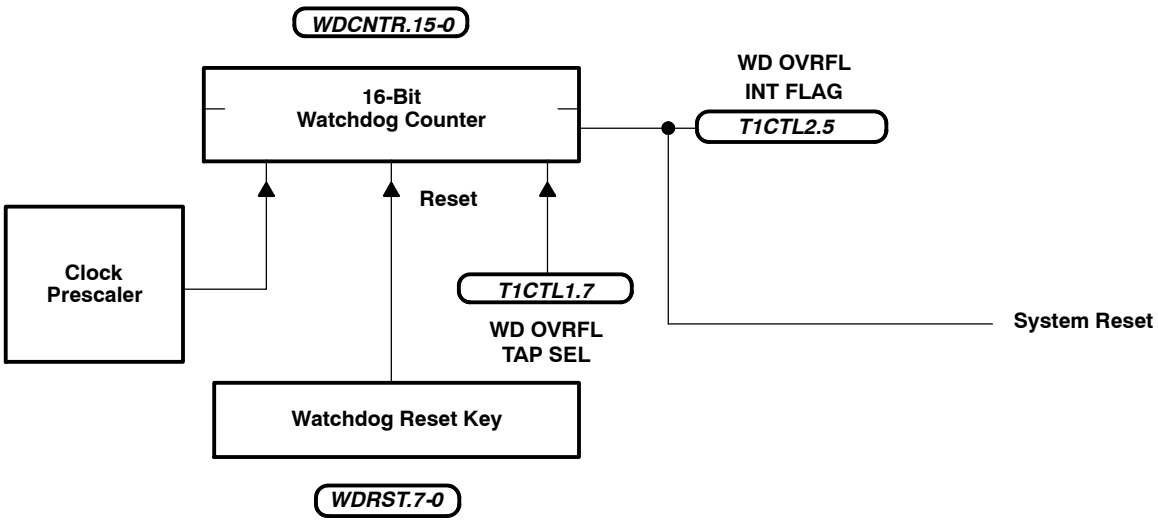

Figure 9. Hard Watchdog

timer 1 module (continued)

- Simple counter configuration (see Figure 10) for mask-ROM devices only
  - Simple counter can be configured as an event counter, pulse accumulator, or an internal timer.

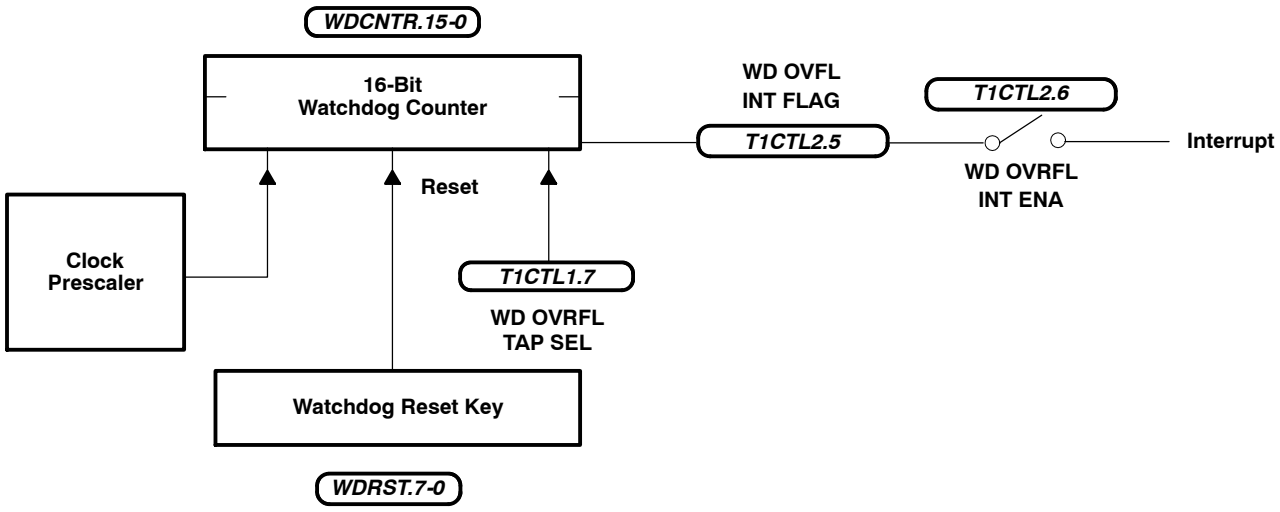

Figure 10. Simple Counter

timer 2A module

The 16-bit general-purpose timer 2A (T2A) module is composed of a 16-bit resettable counter, 16-bit compare register with associated compare logic, 16-bit capture register, and a 16-bit register that functions as a capture register in one mode and as a compare register in the other mode. The T2A module adds an additional timer that provides an event count, input capture, and compare function. The T2A module includes three external device pins that can be dedicated as timer functions or used as general-purpose I/O pins. The T2A module is shown in Figure 11.

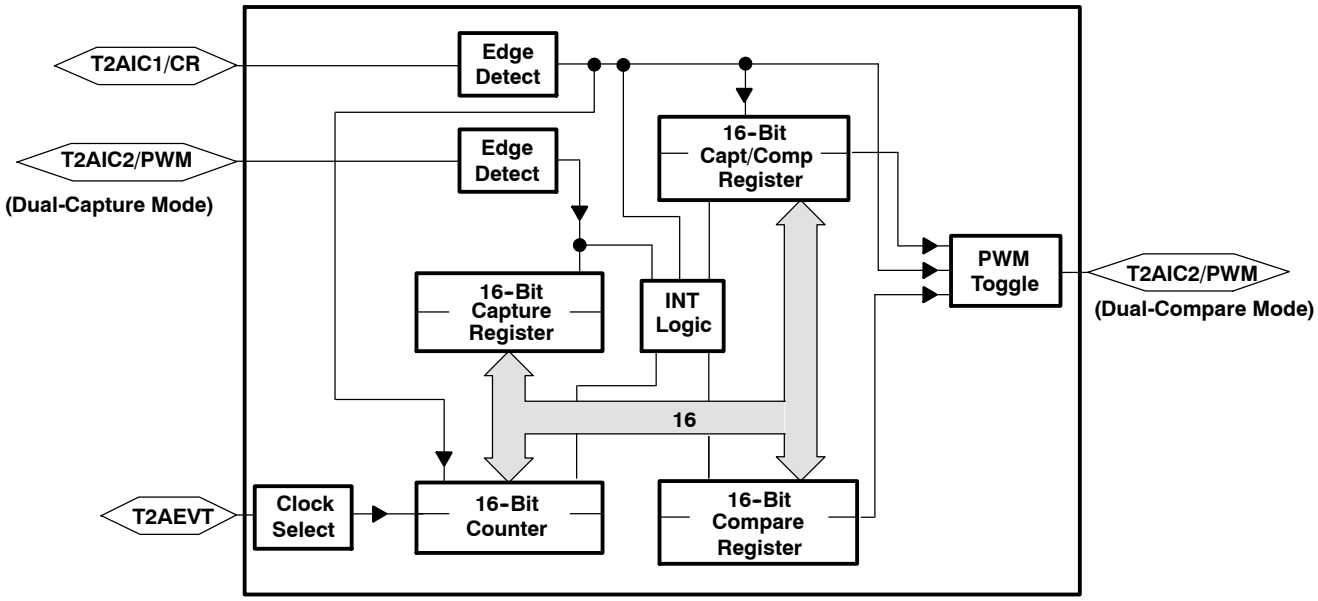

Figure 11. Timer 2A Module Block Diagram

The T2A module features include the following:

- Three T2A I/O pins:
  - T2AIC1/CR: T2A input-capture 1/counter-reset input pin, or general-purpose bidirectional I/O pin
  - T2AIC2/PWM: T2A input-capture 2/pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
  - T2AEVT: Timer 2A event-input pin, or general-purpose bidirectional I/O pin
- Two operational modes:
  - Dual-compare mode: Provides PWM signal
  - Dual-capture mode: Provides input-capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture register with associated capture logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register

timer 2A module (continued)

- T2A clock sources can be any of the following:
  - System clock
  - No clock (the counter is stopped)
  - External clock synchronized to the system clock (event counter)
  - System clock while external input is high (pulse accumulation)
- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T2AIC1/CR)
- Interrupts that can be generated on the occurrence of:
  - A compare equal to dedicated-compare register
  - A compare equal to capture-compare register
  - A counter overflow
  - An external edge 1 detection
  - An external edge 2 detection
- Fourteen T2A module-control registers: Located in the PF frame beginning at address P060

timer 2A module (continued)

The T2A module-control registers are shown in Table 14.

Table 14. T2A Module Register Memory Map†

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	Modes: Dual-Compare and Dual-Capture								
P060	Bit 15			T2A Counter MSB				Bit 8	T2ACNTR
P061	Bit 7			T2A Counter LSB				Bit 0	
P062	Bit 15			Compare Register MSB				Bit 8	T2AC
P063	Bit 7			Compare Register LSB				Bit 0	
P064	Bit 15			Capture/Compare Register MSB				Bit 8	T2ACC
P065	Bit 7			Capture/Compare Register LSB				Bit 0	
P066	Bit 15			Capture Register 2 MSB				Bit 8	T2AIC
P067	Bit 7			Capture Register 2 LSB				Bit 0	
P068 P069	Reserved								
P06A	—	—	—	T2A OVRFL INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
	Mode: Dual-Compare								
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC1 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
	Mode: Dual-Capture								
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
	Modes: Dual-Compare and Dual-Capture								
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	**T2A STEST**	**T2A PRIORITY**	—	—	—	—	—	—	T2APRI

† Privileged bits are shown in bold typeface.

timer 2A module (continued)

The T2A dual-compare mode block diagram is illustrated in Figure 12. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

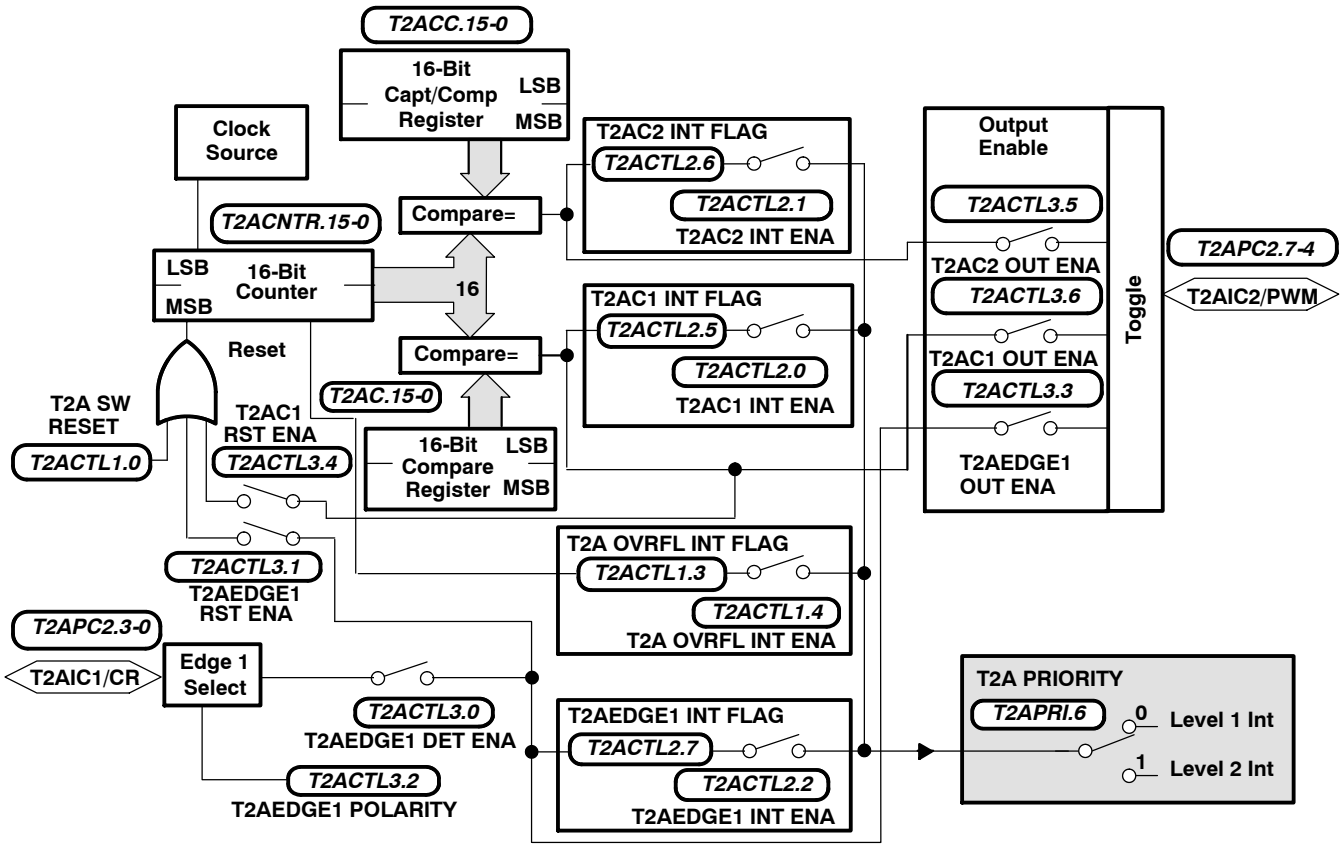

Figure 12. Timer 2A: Dual-Compare Mode

timer 2A module (continued)

The T2A dual-capture mode block diagram is illustrated in Figure 13. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

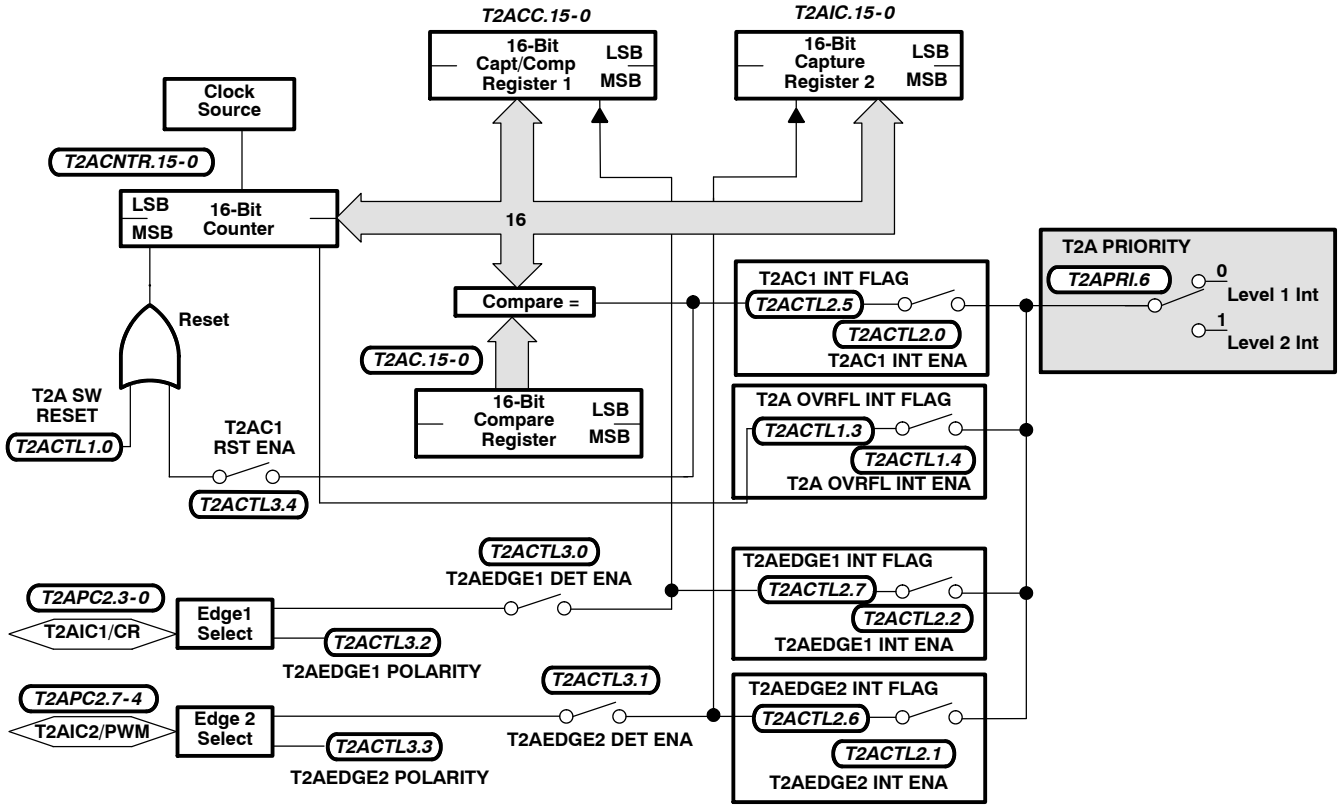

Figure 13. Timer 2A: Dual-Capture Mode

serial communications interface 1 (SCI1)

The TMS370Cx4x devices include a serial communications interface 1 (SCI1) module. The SCI1 module supports digital communications between the TMS370 devices and other asynchronous peripherals and uses the standard non return-to-zero format (NRZ) format. The SCI1's receiver and transmitter are double buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full duplex mode. To ensure data integrity, the SCI1 checks received data for break detection, parity, overrun, and framing errors. The bit rate (baud) is programmable to over 65,000 different rates through a 16-bit baud-select register.

Features of the SCI1 module include:

- Three external pins:
  - SCITXD: SCI transmit-output pin or general purpose bidirectional I/O pin.
  - SCIRXD: SCI receive-input pin or general purpose bidirectional I/O pin.
  - SCICLK: SCI bidirectional serial-clock pin, or general-purpose bidirectional I/O pin.
- Two communications modes: asynchronous and isosynchronous
- Baud rate: 64K different programmable rates
  - Asynchronous mode: 3 bps to 156K bps at 5 MHz SYSCLK

$$\text{Asynchronous Baud} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 32}$$

  - Isosynchronous mode: 39 bps to 2.5 Mbps at 5 MHz SYSCLK

$$\text{Isosynchronous Baud} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 2}$$

- Data word format:
  - One start bit
  - Data word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: Idle-line and address bit
- Half or full-duplex operation
- Double-buffered receiver and transmitter operations
- Transmitter and receiver operations can be accomplished through either interrupt-driven or polled-algorithms with status flags:
  - Transmitter: TXRDY flag (transmitter buffer register is ready to receive another character) and TX EMPTY flag (Transmitter shift register is empty)
  - Receiver: RXRDY flag (receive buffer register ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR monitoring four interrupt conditions
  - Separate enable bits for transmitter and receiver interrupts
  - NRZ (non return-to-zero) format
- Eleven SCI1 module control registers, located in control register frame beginning at address P050h

serial communications interface 1 (SCI1) (continued)

Table 15 lists the SCI1 module control registers.

Table 15. SCI1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNC/ ISOSYNC	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	RESERVED								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	**SCI STEST**	**SCITX PRIORITY**	**SCIRX PRIORITY**	**SCI ESPEN**	—	—	—	—	SCIPRI

serial communications interface 1 (SCI1) (continued)

Figure 14 shows the SCI1 module block diagram.

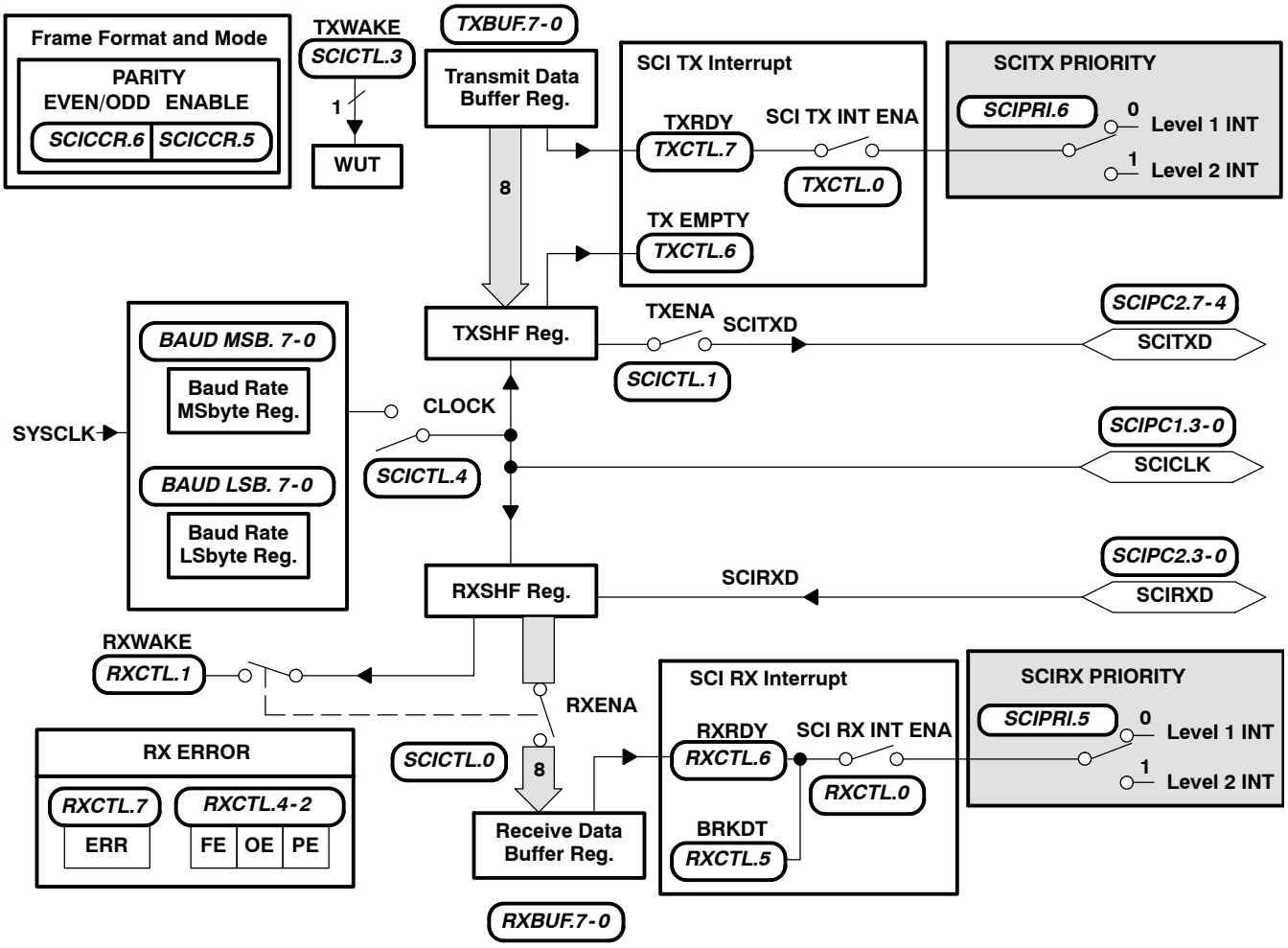

Figure 14. SCI1 Block Diagram

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analog-to-digital converter 1 (ADC1) module

The analog-to-digital converter 1 (ADC1) module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has eight multiplexed analog input channels for the 44-pin device and four multiplexed analog input channels for the 40-pin device that allow the processor to convert the voltage levels from up to eight different sources. The ADC1 module features include the following:

- Minimum conversion time: 32.8 μs at 5-MHz SYSCLK
- Up to ten external pins:
  - Four (AN2, AN3, AN6, AN7) or eight (AN0-AN7) analog input channels, any of which can be software configured as digital inputs (E2, E3, E6, E7) or (E0–E7), respectively, if not needed as analog channels
  - AN1–AN7 can also be configured as positive-input voltage reference.
  - V_{CC3}: ADC1 module high-voltage reference input
  - V_{SS3}: ADC1 module low-voltage reference input
- The ADDATA register, which contains the digital result of the last A/D conversion
- A/D operations can be accomplished through either interrupt driven or polled algorithms.
- Six ADC1 module control registers are located in the control-register frame beginning at address 1070h.

The ADC1 module control registers are illustrated in Table 16.

Table 16. ADC1 Module Control Register Memory Map†

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	**AD STEST**	**AD PRIORITY**	**AD ESPEN**	—	—	—	—	—	ADPRI

† Privileged bits are shown in bold typeface.

analog-to-digital converter 1 (ADC1) module (continued)

The ADC1 module block diagram is illustrated in Figure 15.

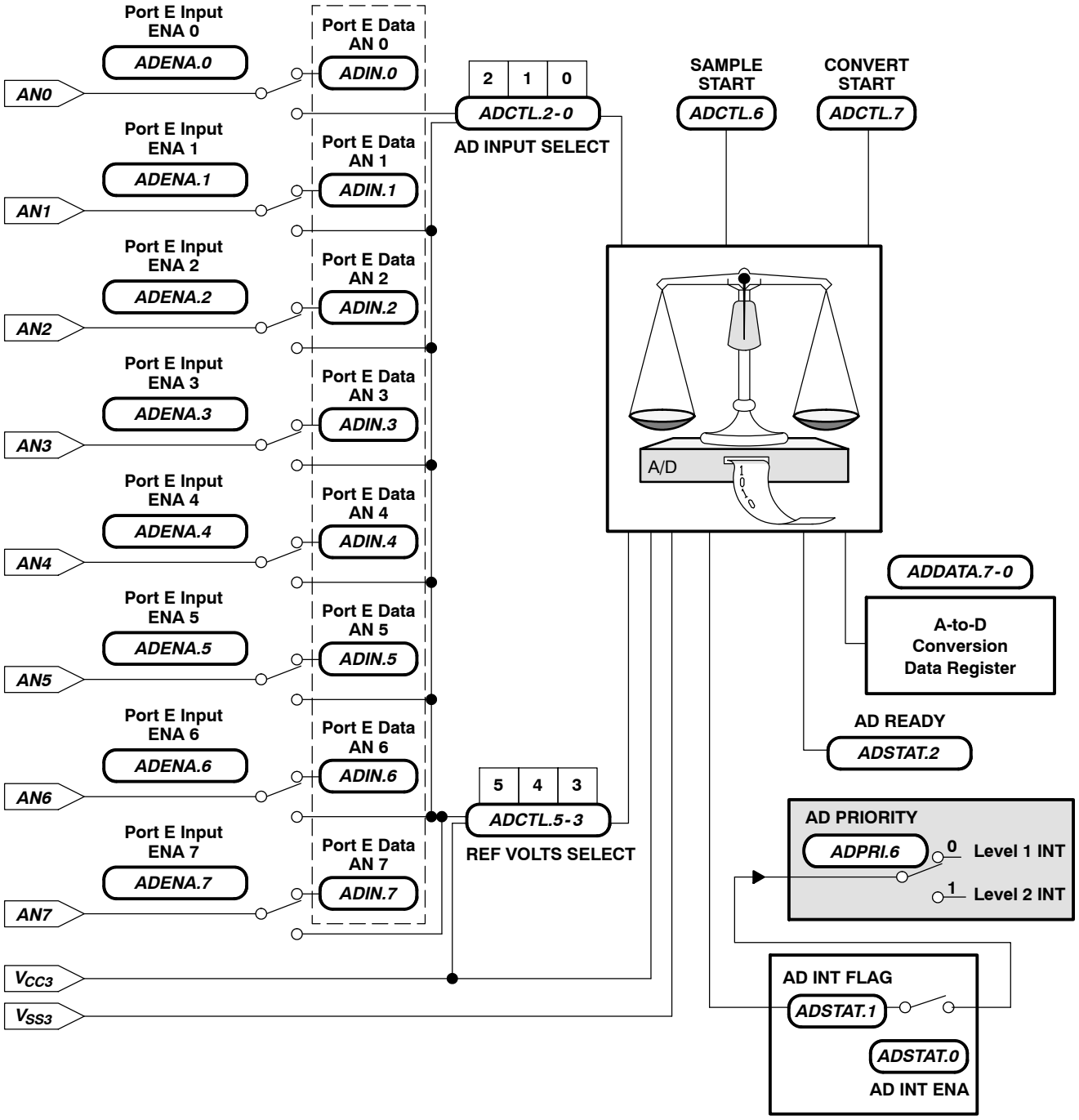

Figure 15. ADC1 Converter Block Diagram

instruction set overview

Table 17 provides an opcode-to-instruction cross-reference of all 73 instructions and 274 opcodes of the ‘370Cx4x instruction set. The numbers at the top of this table represent the most significant nibble (MSN) of the opcode while the numbers at the left side of the table represent the least significant nibble (LSN). The instructions for these two opcode nibbles contain the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

Table 17. TMS370 Family Opcode/Instruction Map†

LSN \ MSN	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8			CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1	JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7
2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7
3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8
4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes
5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14	
6	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6
7	JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10
8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7
9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9
A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12
B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8

† All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

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Table 17. TMS370 Family Opcode/Instruction Map† (Continued)

LSN \ MSN	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):

F4	8	MOVW *n[Rn] 4/15	DIV Rn.A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn],A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn],A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

Legend:

*	=	Indirect addressing operand prefix
&	=	Direct addressing operand prefix
#	=	immediate operand
#16	=	immediate 16-bit number
lab	=	16-label
n	=	immediate 8-bit number
Pd	=	Peripheral register containing destination type
Pn	=	Peripheral register
Ps	=	**Peripheral register containing source byte**
ra	=	Relative address
Rd	=	Register containing destination type
Rn	=	**Register file**
Rp	=	Register pair
Rpd	=	Destination register pair
Rps	=	Source Register pair
Rs	=	Register containing source byte

† All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, an in-circuit emulator (XDS/22), compact development tool (CDT) and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850-02 for PC)
  - — Includes extensive macro capability
  - — Provides high-speed operation
  - — Offers format conversion utilities available for popular formats
- ANSI C compiler (Part No. TMDS3740855-02 for PC, Part No. TMDS3740555-09 for HP700™, Sun-3™ or Sun-4™)
  - — Generates assembly code of the TMS370 that can be inspected easily
  - — Improves code execution speed and reduces code size with optional optimizer pass
  - — Enables the user to directly reference the TMS370's port registers by using a naming convention
  - — Provides flexibility in specifying the storage for data objects
  - — Interfaces C functions and assembly functions easily
  - — Includes assembler and linker
- CDT370 (compact development tool) real-time in-circuit emulation
  - – Base (Part Number EDSCDT370 – for PC, requires cable)
    - – Cable for 44-pin PLCC (Part No. EDSTRG44PLCC)
    - – Cable for 40-pin DIP (Part No. EDSTRG40DIL)
    - – Cable for 40-pin SDIP (Part No. EDSTRG40SDIL)
  - – Provides EEPROM and EPROM programming support
  - – Allows inspection and modification of memory locations
  - – Allows uploading anddownloading of program and data memory
  - – Provides capability to execute programs and software routines
  - – Includes 1024-sample trace buffer
  - – Includes single-step executable instructions
  - – Allows uses of software breakpoints to halt program execution at selected address
- XDS/22 (extended development support) in-circuit emulator
  - — Base (Part No. TMDS3762210 For PC, requires cable)
    - – Cable for 44-pin PLCC, 40-pin DIP, or shrink DIP (Part No. TMDS3788844)
  - — Contains all the features of the CDT370 described above but does not have the capability to program the data EEPROM and program EPROM
  - — Contains sophisticated breakpoint trace and timing hardware that provides up to 2047 qualified trace samples with symbolic disassembly
  - — Allows breakpoints to be qualified by address and/or data on any type of memory acquisition. Up to four levels of events can be combined to cause a breakpoint.

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development system support (continued)

- — Provides timers for analyzing total and average time in routines
- — Contains an eight-line logic probe for adding external signal visibility to the breakpoint qualifier and to the trace display

- Microcontroller programmer
  - — Base (Part No. TMDS3760500A – For PC, requires programming head)
    - – Single unit head for 44-pin PLCC (Part No. TMDS3780510A)
    - – Single unit head for 40-pin DIP or shrink DIP (Part No. TMDS3780511A)
  - — PC-based, window/function-key oriented user interface for ease of use and a rapid learning environment
- Starter kit (Part No. TMDS37000 – For PC)
  - – Includes TMS370 Assembler diskette and documentation
  - – Includes TMS370 Simulator
  - – Includes programming adapter board and programming software
  - – Does not include – (to be supplied by the user):
    - – + 5 V power supply

      ZIF sockets

      9-pin RS-232 cable

device numbering conventions

Figure 16 illustrates the numbering and symbol nomenclature for the TMS370Cx4x family.

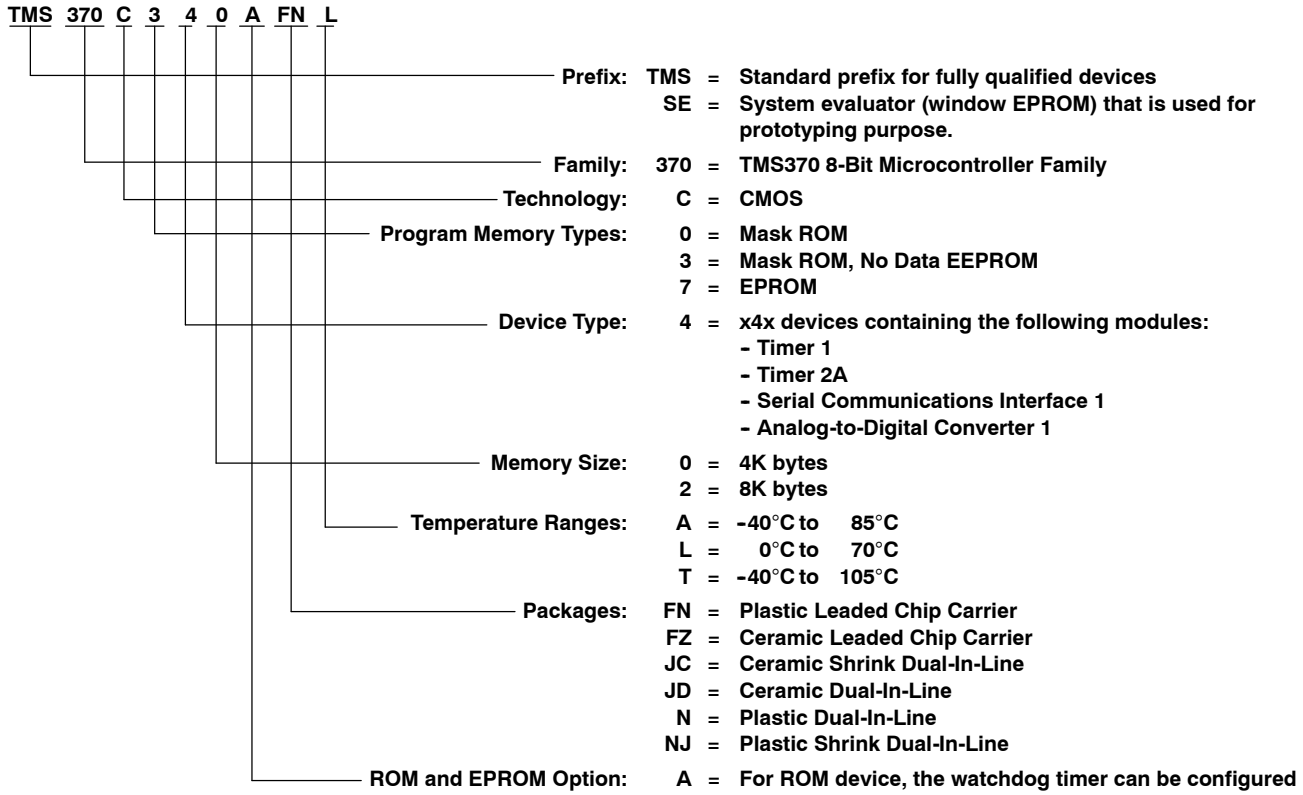


Figure 16. TMS370Cx4x Family Nomenclature

device part numbers

Table 18 lists all the ‘x4x devices available at present. The device part-number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number, but also the clock and watchdog timer options desired. Each device can have only one of the possible three watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 18. Device Part Numbers

DEVICE PART NUMBERS FOR 44 PINS (LCC)	DEVICE PART NUMBERS FOR 40 PINS (DIP)	DEVICE PART NUMBERS FOR 40 PINS (SDIP)
TMS370C040AFNA TMS370C040AFNL TMS370C040AFNT	TMS370C040ANA TMS370C040ANL TMS370C040ANT	TMS370C040ANJA† TMS370C040ANJL† TMS370C040ANJT†
TMS370C042AFNA TMS370C042AFNL TMS370C042AFNT	TMS370C042ANA TMS370C042ANL TMS370C042ANT	TMS370C042ANJA† TMS370C042ANJL† TMS370C042ANJT†
TMS370C340AFNA TMS370C340AFNL TMS370C340AFNT	TMS370C340ANA TMS370C340ANL TMS370C340ANT	TMS370C340ANJA† TMS370C340ANJL† TMS370C340ANJT†
TMS370C342AFNA TMS370C342AFNL TMS370C342AFNT	TMS370C342ANA TMS370C342ANL TMS370C342ANT	TMS370C342ANJA† TMS370C342ANJL† TMS370C342ANJT†
TMS370C742AFNT	TMS370C742ANT	TMS370C742ANJT†
SE370C742AFZT‡	SE370C742AJDT‡	SE370C742AJCT‡

† The NJ designator for the 40-pin plastic shrink DIP package was known formerly as the N2. The mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

‡ System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

new code release form

Figure 17 shows a sample of the new code release form.

NEW CODE RELEASE FORM
TEXAS INSTRUMENTS
TMS370 MICROCONTROLLER PRODUCTS

DATE: _____

To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information:

1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media)
2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.

Company Name: _____
Street Address: _____
Street Address: _____
City: _____ State _____ Zip _____

Customer Part Number: _____
Customer Application: _____

TMS370 Device: _____

TI Customer ROM Number: _____
(provided by Texas Instruments)

OSCILLATOR FREQUENCY

	MIN	TYP	MAX
[] External Drive (CLKIN)			
[] Crystal			
[] Ceramic Resonator			

[] Supply Voltage MIN: _____ MAX: _____
(std range: 4.5V to 5.5V)

TEMPERATURE RANGE
[] 'L': 0° to 70°C (standard)
[] 'A': –40° to 85°C
[] 'T': –40° to 105°C

SYMBOLIZATION
[] TI standard symbolization
[] TI standard w/customer part number
[] Customer symbolization
(per attached spec, subject to approval)

Contact Mr./Ms.: _____
Phone: (_____) _____ Ext.: _____

Customer Purchase Order Number: _____

Customer Print Number *Yes: ____ # _____
No: ____ (Std. spec to be followed)
*If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.

CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS

Low Power Modes	Watchdog counter	Clock Type
[] Enabled	[] Standard	[] Standard (/4)
[] Disabled	[] Hard Enabled	[] PLL (/1)
	[] Simple Counter	

NOTE:
Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B).

PACKAGE TYPE
[] 'N' 28-pin PDIP
[] "FN" 28-pin PLCC
[] "N" 40-pin PDIP
[] "NJ" 40-pin PSDIP (formerly known as N2)
[] "FN" 44-pin PLCC
[] "FN" 68-pin PLCC
[] "NM" 64-pin PSDIP

BUS EXPANSION
[] YES [] NO

NON-STANDARD SPECIFICATIONS:
ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.

RELEASE AUTHORIZATION:
This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.

1. Customer: _____ Date: _____

2. TI: Field Sales: _____
Marketing: _____
Prod. Eng.: _____
Proto. Release: _____

Figure 17. Sample New Code Release Form

Table 19 is a collection of all the peripheral file frames using the ’Cx4x (provided for a quick reference).

Table 19. Peripheral File Frame Compilation

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	SYSTEM CONFIGURATION REGISTERS								
P010	COLD START	**OSC POWER**	**PF AUTO WAIT**	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	μP/μC MODE	SCCR0
P011		—	—	**AUTOWAIT DISABLE**	—	**MEMORY DISABLE**	—	—	SCCR1
P012	**HALT/ STANDBY**	**PWRDWN/ IDLE**	—	**BUS STEST**	**CPU STEST**	—	**INT1 NMI**	**PRIVILEGE DISABLE**	SCCR2
P013 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTL
P01D to P01F	Reserved								
	DIGITAL PORT CONTROL REGISTERS								
P020	Reserved								APORT1
P021	Port A Control Register 2 (must be 0)								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	—	—	—	—	—	Port B Control Register 2 (must be 0)			BPORT2
P026	—	—	—	—	—	Port B Data			BDATA
P027	—	—	—	—	—	Port B Direction			BDIR
P028 to P02B	Reserved								
P02C	Port D Control Register 1 (must be 0)					—	—	—	DPORT1
P02D	Port D Control Register 2 (must be 0)†					—	—	—	DPORT2
P02E	Port D Data					—	—	—	DDATA
P02F	Port D Direction					—	—	—	DDIR
	TIMER 1 MODULE REGISTER								
	Modes: Dual-Compare and Capture/Compare								
P040	Bit 15	T1 Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	
P042	Bit 15	Compare-Register MSbyte						Bit 8	T1C
P043	Bit 7	Compare-Register LSbyte						Bit 0	

† To configure pin D3 as CLKOUT, set port D control register 2 = 08h.

Table 19. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	TIMER 1 MODULE REGISTER (CONTINUED)								
P044	Bit 15			Capture/Compare-Register MSbyte				Bit 8	T1CC
P045	Bit 7			Capture/Compare-Register LSbyte				Bit 0	
P046	Bit 15			Watchdog-Counter MSbyte				Bit 8	WDCNTR
P047	Bit 7			Watchdog-Counter LSbyte				Bit 0	
P048	Bit 7			Watchdog-Reset Key				Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
	Mode: Dual-Compare								
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
	Mode: Capture/Compare								
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
	Modes: Dual-Compare and Capture/Compare								
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	**T1 STEST**	**T1 PRIORITY**	—	—	—	—	—	—	T1PRI
	SCI1 MODULE CONTROL REGISTER								
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNC/ ISOSYNC	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RE-SET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	Reserved								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until after a full power-down cycle has been completed.

Table 19. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	SCI1 MODULE CONTROL REGISTER (CONTINUED)								
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	**SCI STEST**	**SCITX PRIORITY**	**SCIRX PRIORITY**	**SCI ESPEN**	**—**	**—**	**—**	**—**	SCIPRI
	T2A MODULE REGISTER								
	Modes: Dual-Capture and Dual-Compare								
P060	Bit 15	T2A Counter MSbyte						Bit 8	T2ACNTR
P061	Bit 7	T2A Counter LSbyte						Bit 0	
P062	Bit 15	Compare Register MSbyte						Bit 8	T2AC
P063	Bit 7	Compare Register LSbyte						Bit 0	
P064	Bit 15	Capture/Compare Register MSbyte						Bit 8	T2ACC
P065	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P066	Bit 15	Capture Register 2 MSbyte						Bit 8	T2AIC
P067	Bit 7	Capture Register 2 LSbyte						Bit 0	
P068 P069	Reserved								
P06A	—	—	—	T2A OVRFL-INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
	Mode: Dual-Compare								
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
	Mode: Dual-Capture								
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
	Modes: Dual-Capture and Dual-Compare								
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	**T2A STEST**	**T2A PRIORITY**	—	—	—	—	—	—	T2APRI

Table 19. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	ADC1 MODULE CONTROL REGISTER								
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	**AD STEST**	**AD PRIORITY**	**AD ESPEN**	—	—	—	—	—	ADPRI

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}, V_{CC3} (see Note 1) . . . . . –0.6 V to 7 V
Input voltage range, All pins except MC . . . . . –0.6 V to 7 V
MC . . . . . –0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±20 mA
Continuous output current per buffer, I_O (V_O = 0 to V_{CC})‡ . . . . . ±10 mA
Maximum I_{CC} current . . . . . 170 mA
Maximum I_{SS} current . . . . . – 170 mA
Continuous power dissipation . . . . . 1 W
Operating free-air temperature, T_A: L version . . . . . 0°C to 70°C
A version . . . . . –40°C to 85°C
T version . . . . . –40°C to 105°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Electrical characteristics are specified with all output buffers loaded with the specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.

NOTE 1: Unless otherwise noted, all voltage values are with respect to V_{SS}.

recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (see Note 1)		4.5	5	5.5	V
V_{CC}	RAM data retention supply voltage (see Note 2)		3		5.5	V
V_{CC3}	Analog supply voltage (see Note 1)		4.5	5	5.5	V
V_{SS3}	Analog supply ground		– 0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS}		0.8	V
		MC, normal operation	V_{SS}		0.3	
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC}	V
		XTAL2/CLKIN	0.8 V_{CC}		V_{CC}	
		$\overline{\text{RESET}}$	0.7 V_{CC}		V_{CC}	
V_{MC}	MC (mode control) voltage	EEPROM write protect override	11.7	12	13	V
		Microcomputer	V_{SS}		0.3	
		EPROM programming voltage (V_{PP})	13	13.2	13.5	
T_A	Operating free-air temperature	L version	0		70	°C
		A version	– 40		85	
		T version	– 40		105	

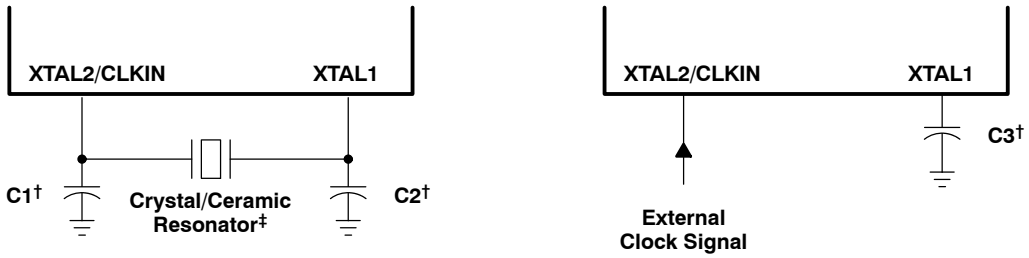
NOTES: 1. Unless otherwise noted, all voltage values are with respect to V_{SS}.
2. $\overline{\text{RESET}}$ must be externally activated when V_{CC} or SYSCLK is out of the recommended operating range.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level digital output voltage		I_{OL} = 1.4 mA			0.4	V
V_{OH}	High-level output voltage		I_{OH} = –50 μA	0.9 V_{CC}			V
			I_{OH} = –2 mA	2.4			
I_I	Input current	MC	0 V < V_I ≤ 0.3 V			10	μA
			0.3 V < V_I ≤ 13			650	
			12 V ≤ V_I ≤ 13 V (see Note 3)			50	mA
I_I	Input current	I/O pins	0 V ≤ V_I ≤ V_{CC}			±10	μA
I_{OL}	Low-level output current		V_{OL} = 0.4 V	1.4			mA
I_{OH}	High-level output current		V_{OH} = 0.9 V_{CC}	– 50			μA
			V_{OH} = 2.4 V	– 2			mA
I_{CC}	Supply current (Operating mode) OSC POWER bit = 0 (see Note 6)		SYSCLK = 5 MHz (see Notes 4 and 5)		30	45	mA
			SYSCLK = 3 MHz (see Notes 4 and 5)		20	30	
			SYSCLK = 0.5 MHz (see Notes 4 and 5)		7	11	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 7)		SYSCLK = 5 MHz (see Notes 4 and 5)		10	17	mA
			SYSCLK = 3 MHz (see Notes 4 and 5)		8	11	
			SYSCLK = 0.5 MHz (see Notes 4 and 5)		2	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 8)		SYSCLK = 3 MHz (see Notes 4 and 5)		6	8.6	mA
			SYSCLK = 0.5 MHz (see Notes 4 and 5)		2	3.0	
	Supply current (HALT mode)		XTALK2/CLKIN < 0.2 V (see Note 4)		2	30	μA

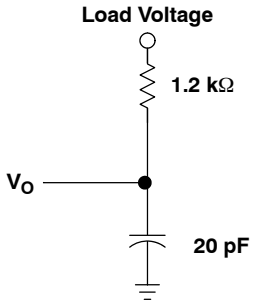
NOTES: 3. Microcontroller-single chip mode, ports configured as inputs, or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} –0.2 V.
4. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5-MHz SYSCLK this extra current = 0.01 mA × (total load capacitance + crystal capacitance in pF).
5. Maximum operating current = 7.6 (SYSCLK) + 7 mA.
6. Maximum standby current =3 (SYSCLK) + 2 mA. (Osc power bit = 0.)
7. Maximum standby current = 2.24 (SYSCLK) + 1.9 mA. (Osc power bit = 1 and valid up to 3-MHz SYSCLK.)
8. Input current I_{PP} is a maximum of 50 mA only when EPROM is being programmed.

RECOMMENDED CRYSTAL/CLOCK CONNECTIONS



† The values of C1 and C2 are typically 15 pF and C3 value is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.
‡ The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.

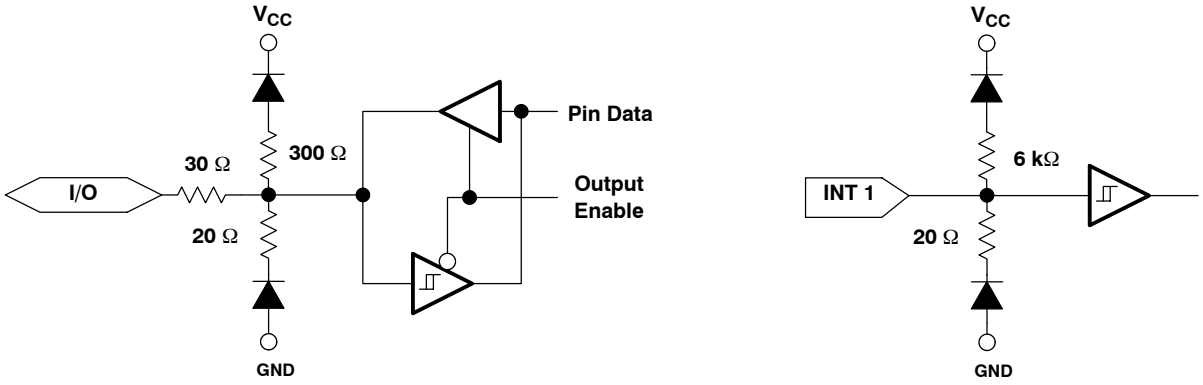
TYPICAL OUTPUT LOAD CIRCUIT§



Case 1: $V_O = V_{OH}$ = 2.4 V; Load Voltage = 0 V
Case 2: $V_O = V_{OL}$ = 0.4 V; Load Voltage = 2.1

§ All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

TYPICAL INPUT BUFFERS



PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	Address	R	Read
AR	Array	RXD	SCIRXD
B	Byte	SC	SYSCLK
CI	XTAL2/CLKIN	SCC	SCICLK
D	Data	TXD	SCITXD
PGM	Program	W	Write

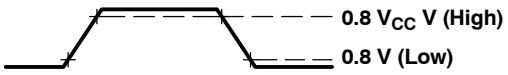
Lowercase subscripts and their meanings are:

c	cycle time (period)	r	rise time
d	delay time	su	setup time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

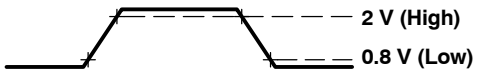
The following additional letters are used with these meanings:

H	High	V	Valid
L	Low	Z	High Impedance

All timings are measured between high and low measurement points as indicated in the figures below.



XTAL2/CLKIN Measurement Points



General Measurement Points

external clocking requirements for clock divided by 4†

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 9)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN	Crystal operating frequency	2	20	MHz
	SYSCLK	System clock‡	0.5	5	MHz

† For V_{IL} and V_{IH}, refer to recommended operating conditions.
‡ SYSCLK = CLKIN/4
NOTE 9: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

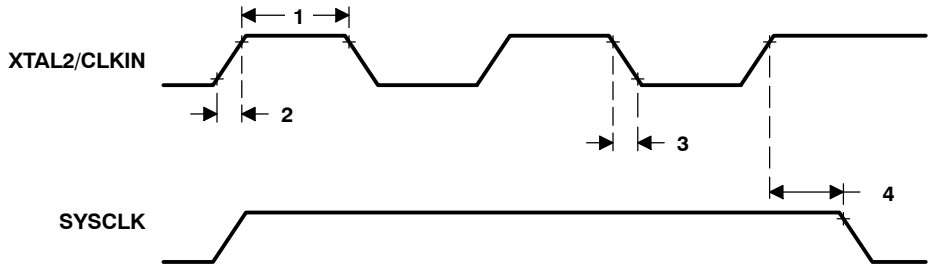


Figure 18. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL)†§

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 9)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN	Crystal operating frequency	2	5	MHz
	SYSCLK	System clock§	2	5	MHz

† For V_{IL} and V_{IH}, refer to recommended operating conditions.
§ SYSCLK = CLKIN/1
NOTE 9: This pulse can be either a high pulse, which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

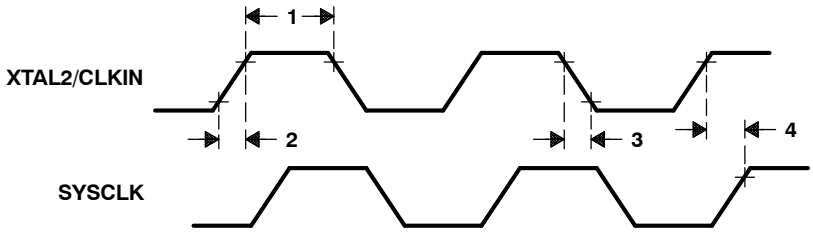


Figure 19. External Clock Timing for Divide-by-1

switching characteristics and timing requirements (see Note 10 and Figure 20)

NO.	PARAMETER			MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK (system clock)	Divide-by-4	200	2000	ns
			Divide-by-1	200	500	ns
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		0.5 t_c–20	0.5 t_c	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		0.5 t_c	0.5 t_c + 20	ns

NOTE 10: t_c = system-clock cycle time = 1/SYSCLK.

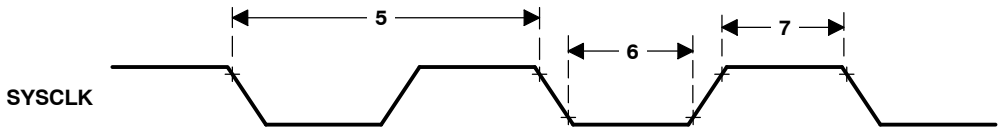
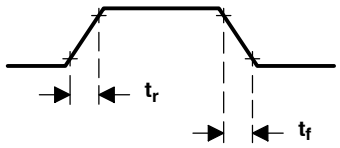


Figure 20. SYSCLK Timing

general-purpose output signal-switching time requirements

		MIN	TYP	MAX	UNIT
t_r	Rise time		30		ns
t_f	Fall time		30		ns



recommended EEPROM timing requirements for programming

		MIN	MAX	UNIT
$t_{w(PGM)B}$	Pulse duration, programming signal to be certain valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$	Pulse duration, programming signal to be certain valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.5	6	V
V_{PP}	Supply voltage at MC pin		13	13.2	13.5	V
I_{PP}	Supply current at MC pin during programming (V_{PP} = 13 V)			30	50	mA
SYSCLK	System clock	Divide-by-4	0.5		5	MHz
		Divide-by-1	2		5	

recommended EPROM timing requirements for programming

		MIN	TYP	MAX	UNIT
$t_{w(EPGM)}$	Pulse duration, programming signal (see Note 11)	0.40	0.50	3	ms

NOTE 11: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.

SERIAL COMMUNICATIONS INTERFACE 1 (SCI1) INTERNAL CLOCK ISOSYNCHRONOUS MODE I/O TIMING

SCI1 isosynchronous mode timing characteristics and requirements for internal clock (see Note 10 and Figure 21)

NO.	PARAMETER		MIN	MAX	UNIT
24	$t_{c(SCC)}$	Cycle time, SCICLK	$2t_c$	$131{,}072t_c$	ns
25	$t_{w(SCCL)}$	Pulse duration, SCICLK low	$t_c - 45$	$0.5t_{c(SCC)}+45$	ns
26	$t_{w(SCCH)}$	Pulse duration, SCICLK high	$t_c - 45$	$0.5t_{c(SCC)}+45$	ns
27	$t_{d(SCCL-TXDV)}$	Delay time, SCITXD valid after SCICLK low	– 50	60	ns
28	$t_{v(SCCH-TXD)}$	Valid time, SCITXD data after SCICLK high	$t_{w(SCCH)} - 50$		ns
29	$t_{su(RXD-SCCH)}$	Setup time, SCIRXD to SCICLK high	$0.25t_c + 145$		ns
30	$t_{v(SCCH-RXD)}$	Valid time, SCIRXD data after SCICLK high	0		ns

NOTE 10: t_c = system-clock cycle time = 1/SYSCLK.

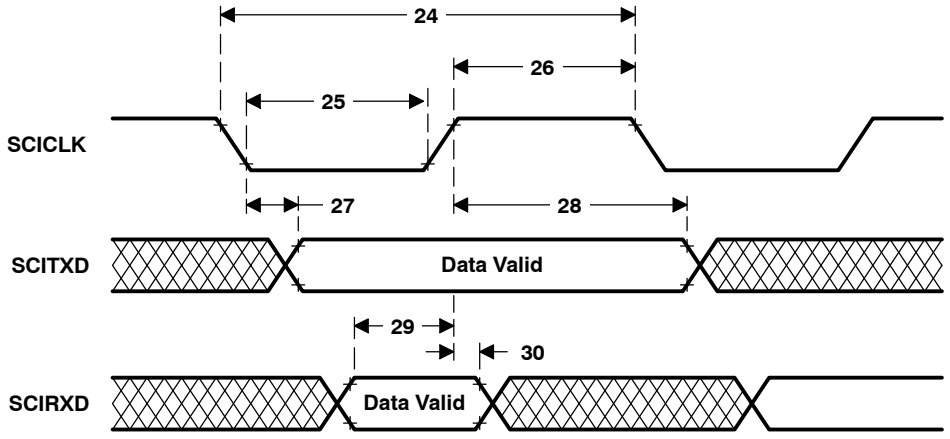


Figure 21. SCI1 Isosynchronous Mode Timing Diagram for Internal Clock

SERIAL COMMUNICATIONS INTERFACE 1 (SCI1) EXTERNAL CLOCK ISOSYNCHRONOUS MODE I/O TIMING

SCI1 isosynchronous mode timing characteristics and requirements for external clock (see Note 10 and Figure 22)

NO.	PARAMETER		MIN	MAX	UNIT
31	$t_{c(SCC)}$	Cycle time, SCICLK	$10t_c$		ns
32	$t_{w(SCCL)}$	Pulse duration, SCICLK low	$4.25t_c + 120$		ns
33	$t_{w(SCCH)}$	Pulse duration, SCICLK high	$t_c + 120$		ns
34	$t_{d(SCCL-TXDV)}$	Delay time, SCITXD valid after SCICLK low		$4.25t_c + 145$	ns
35	$t_{v(SCCH-TXD)}$	Valid time, SCITXD data after SCICLK high	$t_{w(SCCH)}$		ns
36	$t_{su(RXD-SCCH)}$	Setup time, SCIRXD to SCICLK high	40		ns
37	$t_{v(SCCH-RXD)}$	Valid time, SCIRXD data after SCICLK high	$2t_c$		ns

NOTE 10: t_c = system-clock cycle time = 1/SYSCLK.

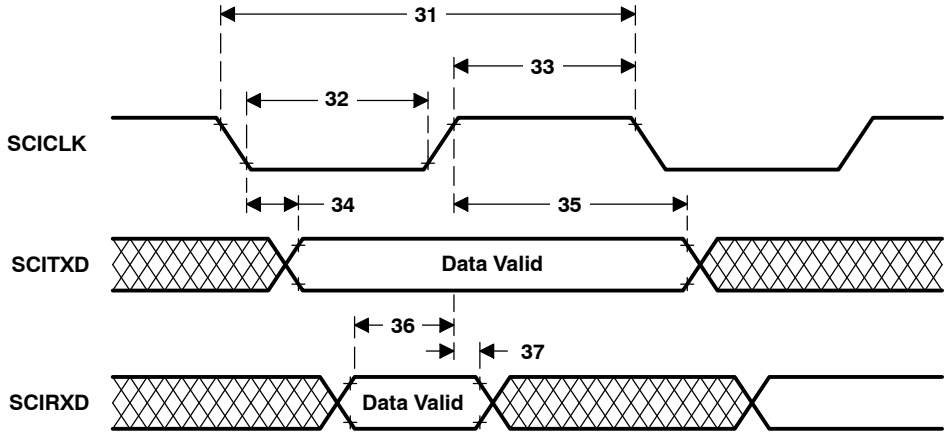


Figure 22. SCI1 Isosynchronous Mode Timing Diagram for External Clock

ADC1

The ADC1 has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3}. Their purpose is to enhance ADC1 performance by preventing digital switching noise on the logic circuitry that could be present on V_{SS} and V_{CC} from coupling into the ADC1 analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution . . . . . 8 bits (256 values)
Monotonic . . . . . Yes
Output conversion code . . . . . 00h to FFh (00h for $V_I \le V_{SS3}$; FFh for $V_I \ge V_{ref}$)
Conversion time (excluding sample time) . . . . . $164t_c$

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC3}	Analog supply voltage	4.5	5	5.5	V
		V_{CC} – 0.3		V_{CC} + 0.3	
V_{SS3}	Analog ground	V_{SS} – 0.3		V_{SS} + 0.3	V
V_{ref}	Non-V_{CC3} reference†	2.5	V_{CC3}	V_{CC3} + 0.1	V
	Analog input for conversion	V_{SS3}		V_{ref}	V

† V_{ref} must be stable, within ± 1/2 LSB of the required resolution, during the entire conversion time.

operating characteristics over ranges of recommended operating conditions

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
	Absolute accuracy (see Note 12)	V_{CC3} = 5.5 V, V_{ref} = 5.1 V		+1.5	LSB
	Differential/integral linearity error (see Notes 12 and 13)	V_{CC3} = 5.5 V, V_{ref} = 5.1 V		±0.9	LSB
I_{CC3}	Analog supply current	Converting		2	mA
		Nonconverting		5	μA
I_I	Input current, AN0-AN7	0 V ≤ V_I ≤ 5.5 V		2	μA
	V_{ref} input charge current			1	mA
Z_{ref}	Source impedance V_{ref}	SYSCLK ≤ 3 MHz		24	kΩ
		3 MHz < SYSCLK ≤ 5 MHz		10	kΩ

NOTES: 12. Absolute resolution = 20 mV. At V_{ref} = 5 V, this is 1 LSB. As V_{ref} decreases, LSB size decreases and thus absolute accuracy and differential / integral linearity errors in terms of LSBs increases.
13. Excluding quantization error of 1/2 LSB.

ADC1 (continued)

The ADC1 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined such that high-impedance sources can be accommodated without penalty to low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START) of the ADCTL is set to 1. After a hold time, the converter resets the SAMPLE START and CONVERT START bits, signaling that a conversion has started and the analog signal can be removed.

analog timing requirements

		MIN	MAX	UNIT
$t_{su(S)}$	Setup time, analog input to sample command	0		ns
$t_{h(AN)}$	Hold time, analog input from start of conversion	$18t_c$		ns
$t_{w(S)}$	Pulse duration, sample time per kilohm of source impedance (see Note 14)	1		μs/kΩ

NOTE 14: The value given is valid for a signal with a source impedance > 1 kΩ. If the source impedance is < 1 kΩ, use a minimum sampling time of 1 μs.

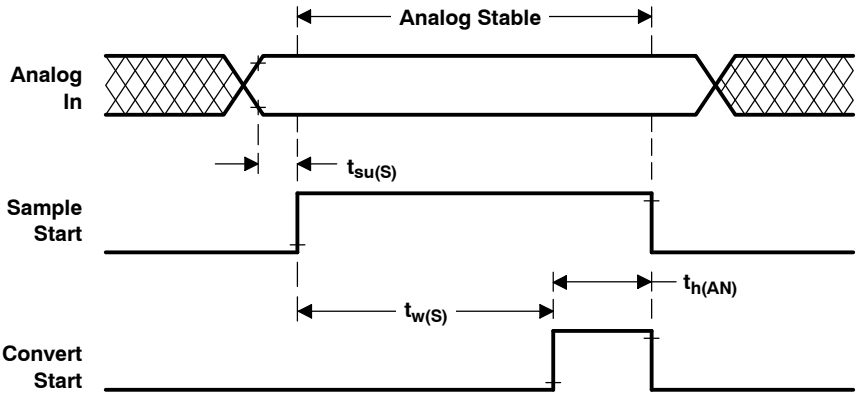


Figure 23. Analog Timing

Table 20 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 20. TMS370Cx4x Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 44 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C040AFNA TMS370C040AFNL TMS370C040AFNT TMS370C042AFNA TMS370C042AFNL TMS370C042AFNT TMS370C340AFNA TMS370C340AFNL TMS370C340AFNT TMS370C342AFNA TMS370C342AFNL TMS370C342AFNT TMS370C742AFNT
FZ – 44 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C742AFZT
JD – 40 pin (100-mil pin spacing)	CERAMIC DUAL-IN-LINE PACKAGE (CDIP)	JD(R-CDIP-T**) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370C742AJDT
N – 40 pin (100-mil pin spacing)	PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	N(R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE	TMS370C040ANA TMS370C040ANL TMS370C040ANT TMS370C042ANA TMS370C042ANL TMS370C042ANT TMS370C340ANA TMS370C340ANL TMS370C340ANT TMS370C342ANA TMS370C342ANL TMS370C342ANT TMS370C742ANT
JC – 40 pin (70-mil pin spacing)	CERAMIC SHRINK DUAL-IN-LINE PACKAGE (CSDIP)	JC(R-CDIP-T40) CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE	SE370C742AJCT
NJ – 40 pin (70-mil pin spacing)†	PLASTIC SHRINK DUAL-IN-LINE PACKAGE (PSDIP)	NJ(R-PDIP-T**) PLASTIC SHRINK DUAL-IN-LINE PACKAGE	TMS370C040ANJA TMS370C040ANJL TMS370C040ANJT TMS370C042ANJA TMS370C042ANJL TMS370C042ANJT TMS370C340ANJA TMS370C340ANJL TMS370C340ANJT TMS370C342ANJA TMS370C342ANJL TMS370C342ANJT TMS370C742ANJT

† NJ formerly known as N2; the mechanical drawing of the NJ is identical to the N2 package and did not need to be requalified.

MECHANICAL DATA

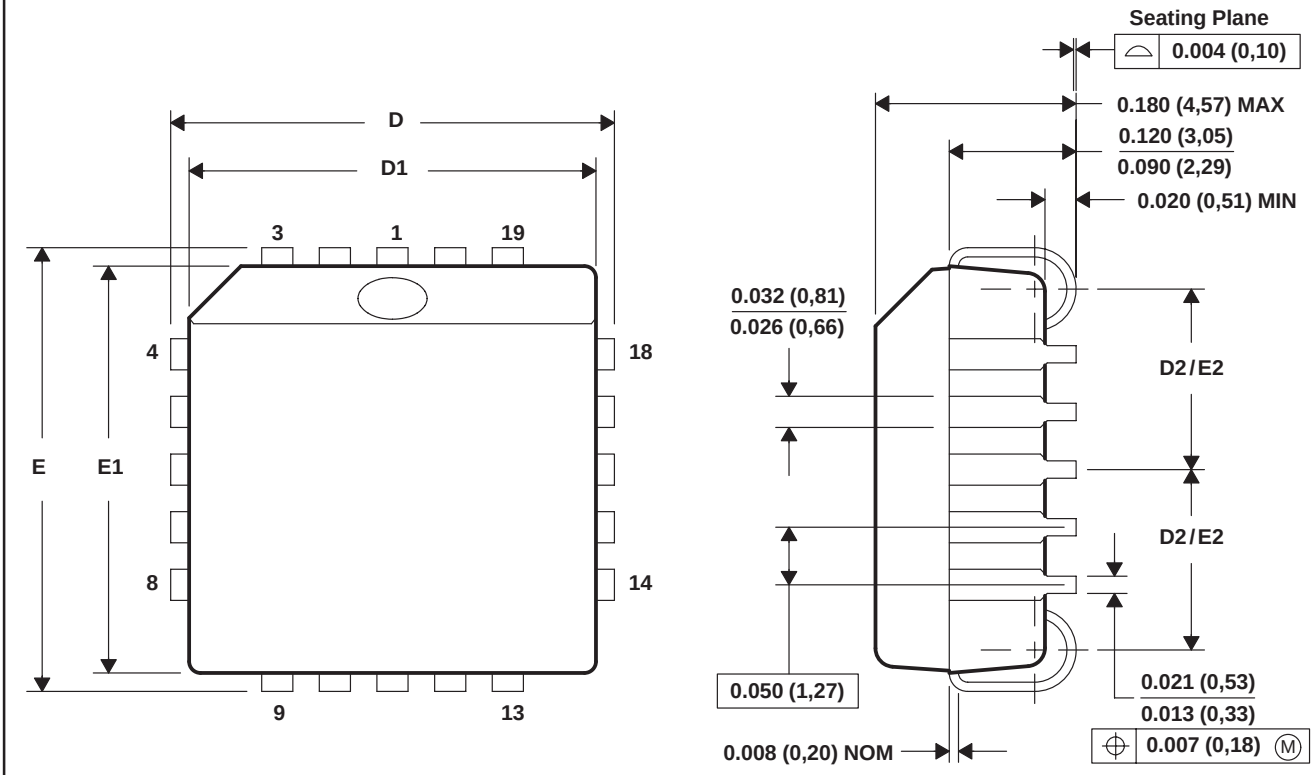
The following packaging information and addendum reflect the most current data available for the designated device(s). This data is subject to change without notice and without revision of this document.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

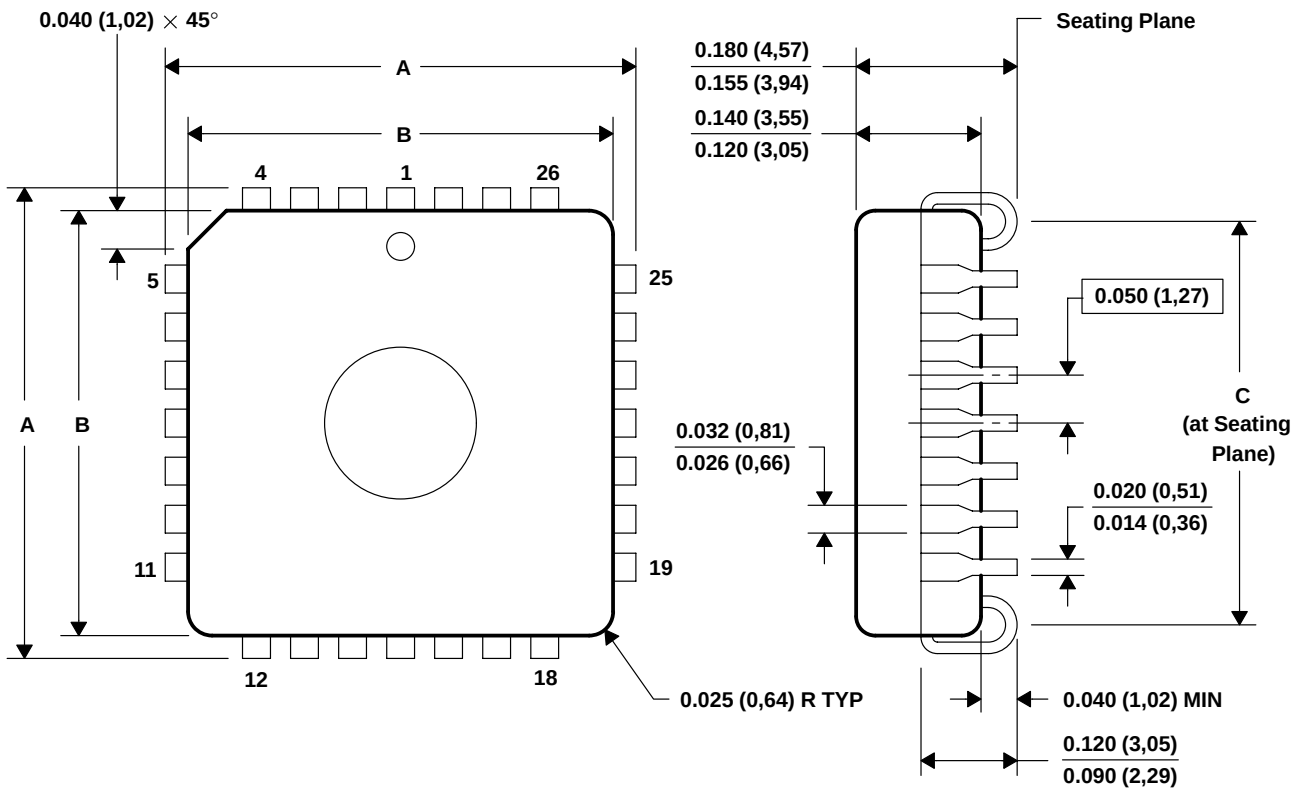
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

MJLC003A – FEBRUARY 1995

FZ (S-CQCC-J**)

J-LEADED CERAMIC CHIP CARRIER

28 LEAD SHOWN



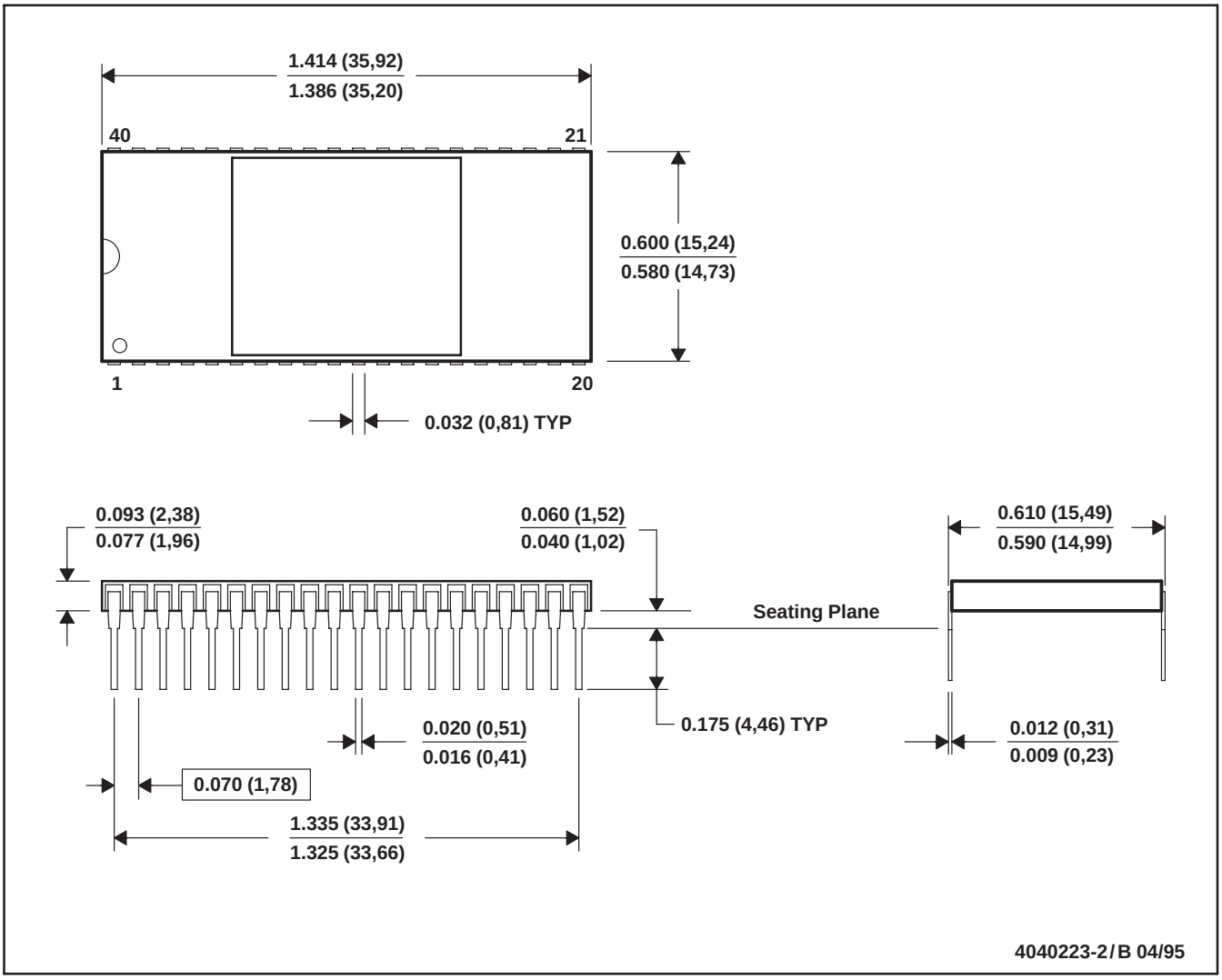
JEDEC OUTLINE	NO. OF PINS**	A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
MO-087AA	28	0.485 (12,32)	0.495 (12,57)	0.430 (10,92)	0.455 (11,56)	0.410 (10,41)	0.430 (10,92)
MO-087AB	44	0.685 (17,40)	0.695 (17,65)	0.630 (16,00)	0.655 (16,64)	0.610 (15,49)	0.630 (16,00)
MO-087AC	52	0.785 (19,94)	0.795 (20,19)	0.730 (18,54)	0.765 (19,43)	0.680 (17,28)	0.740 (18,79)
MO-087AD	68	0.985 (25,02)	0.995 (25,27)	0.930 (23,62)	0.955 (24,26)	0.910 (23,11)	0.930 (23,62)

4040219/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.

MCDI006 – OCTOBER 1994

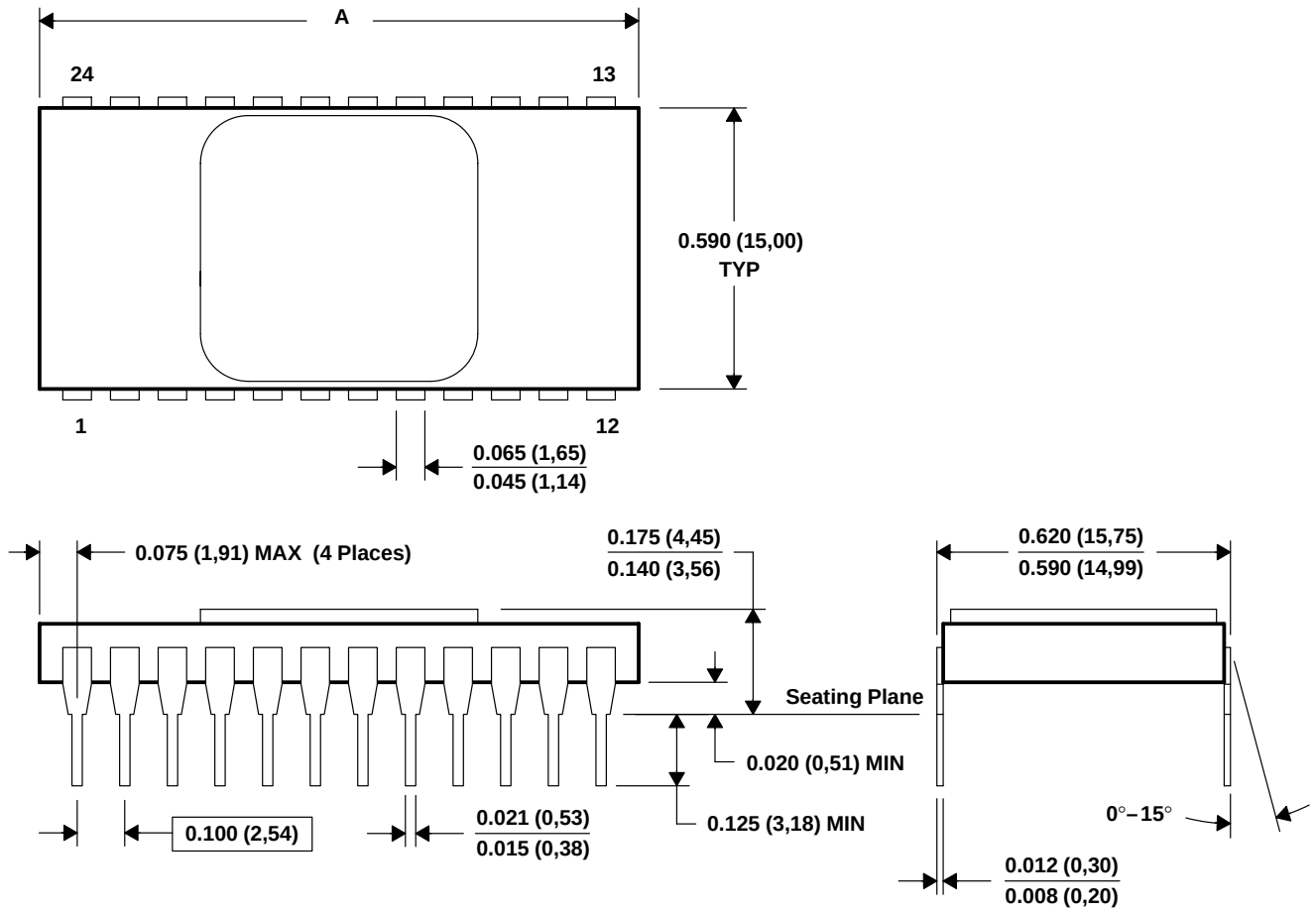
JC (R-CDIP-T40) **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.

JD (R-CDIP-T)** **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE**

24 PINS SHOWN



DIM \ PINS **	24	28	40	48	52
A MAX	1.250 (31,75)	1.450 (36,83)	2.050 (52,07)	2.435 (61,85)	2.650 (67,31)

4040087/B 04/95

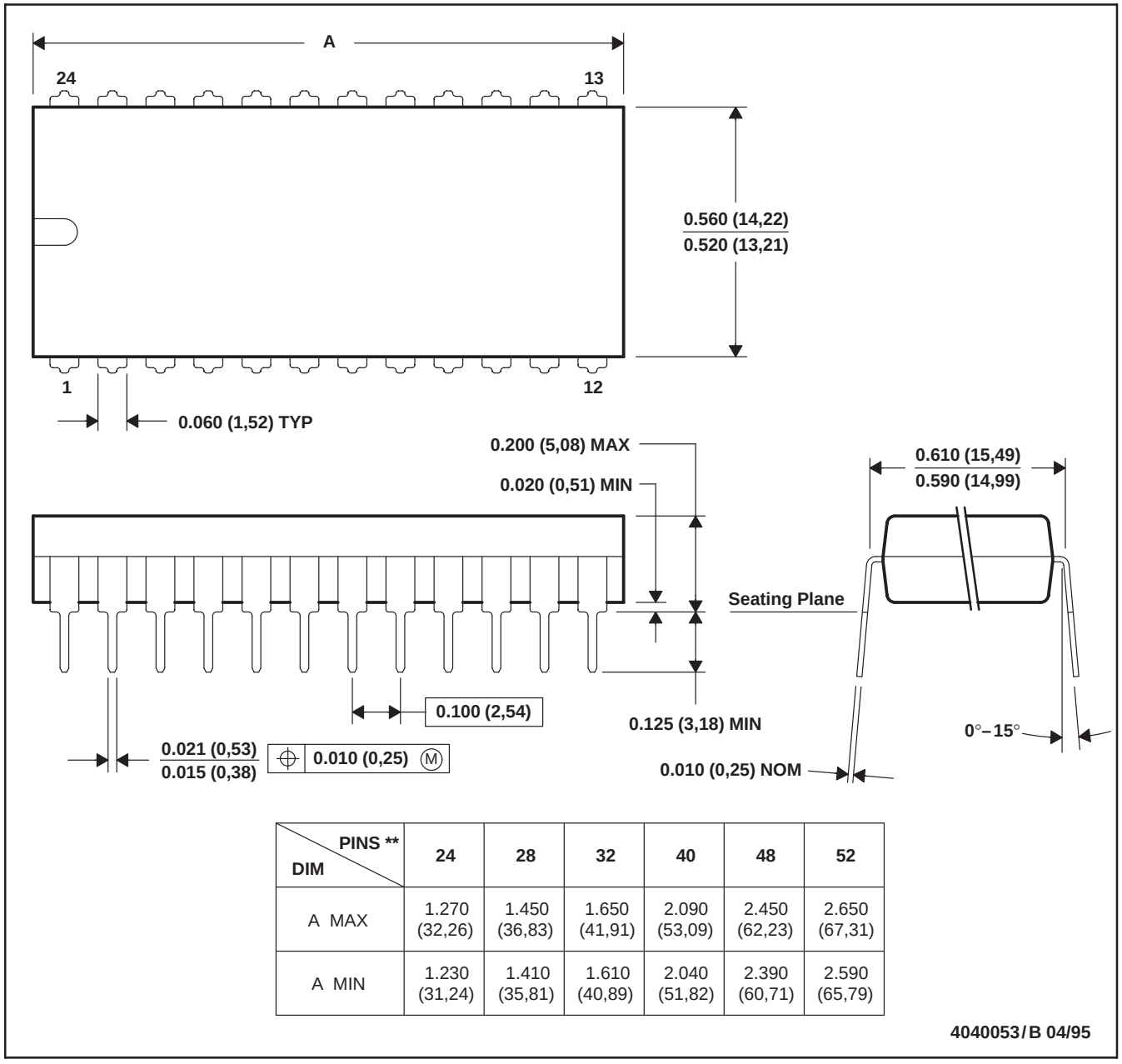
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold-plated.

MPDI008 – OCTOBER 1994

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

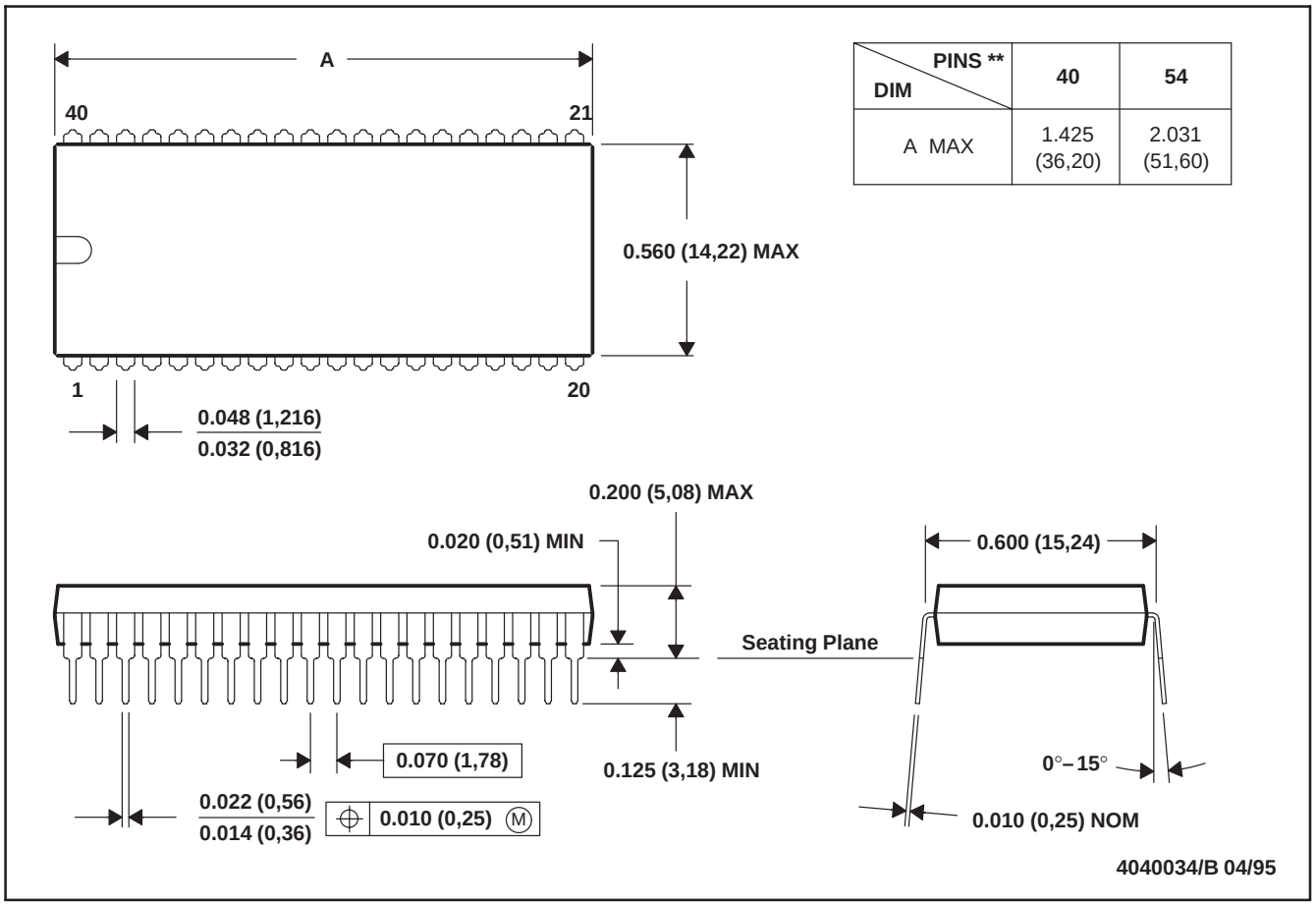
4040053/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

MSDI005 – OCTOBER 1994

NJ (R-PDIP-T**) PLASTIC SHRINK DUAL-IN-LINE PACKAGE

40 PIN SHOWN



DIM \ PINS **	40	54
A MAX	1.425 (36,20)	2.031 (51,60)

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TMS370C742AFNT	ACTIVE	PLCC	FN	44		TBD	Call TI	Call TI	
TMS370C742AFNTG4	ACTIVE	PLCC	FN	44	26	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
TMS370C742AN2T	OBSOLETE	XCEPT	N2	40		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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