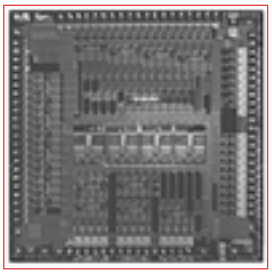
BCM3212
PRODUCT Brief



BCM3212 DOCSIS 1.1 ADVANCED CMTS MAC

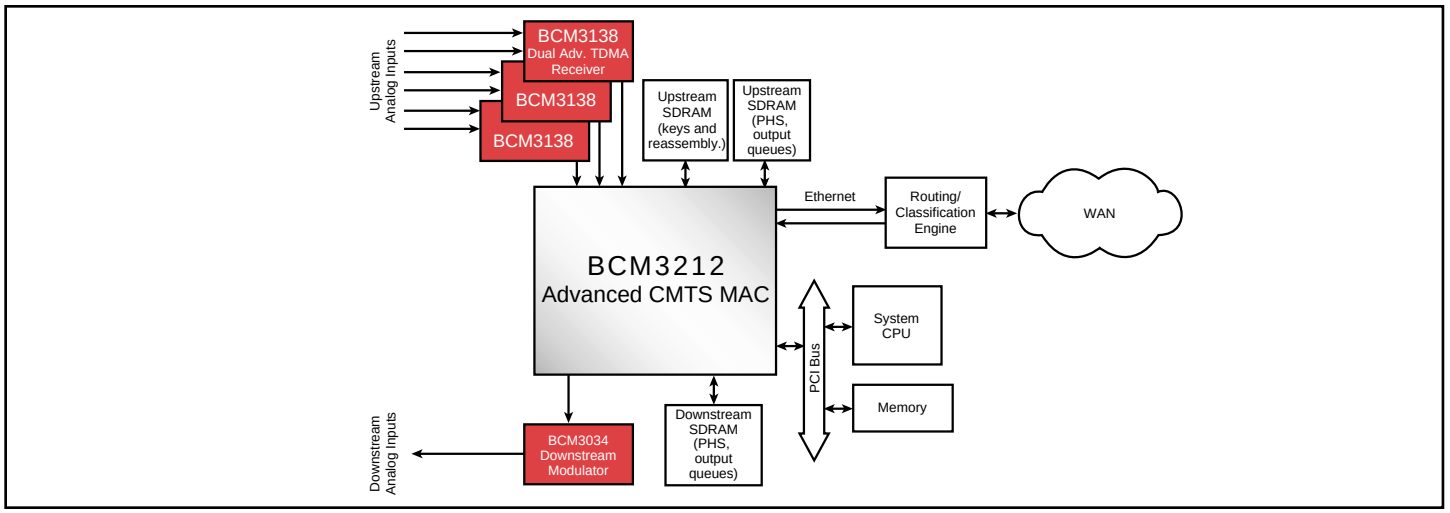
BCM3212 FEATURES

- **Performs DOCSIS 1.1 MAC layer functions, including:**
  - Fragment reassembly
  - Deconcatenation
  - Payload Header Suppression and Expansion
  - 56-bit DES encryption and decryption
  - Generation and checking of HCS and CRC
  - MPEG encapsulation of downstream traffic
  - Timestamp and SYNC message generation
- **Supports one downstream and up to six upstream channels simultaneously**
  - Many other downstream-to-upstream ratios can be achieved by connecting multiple BCM3212s via the seamless MAP master/slave interface
- **Processes up to 400,000 packets per second in the aggregate over all upstream and downstream channels**
- **Direct interface to:**
  - BCM3034 QAMLink® Advanced Universal QAM Modulator (providing downstream data rates up to 100 Mbps)
  - BCM3138 QAMLink® Dual-Channel Advanced PHY Burst Receiver (providing upstream data rates up to 30 Mbps per upstream channel)
- **Packet port provides a high-throughput data interface to other network equipment via the standard IEEE 802.3z GMII Ethernet interface**
- **PCI interface to external host CPU supports either 32-bit or 64-bit operation at either 33 MHz or 66 MHz**
- **PROPANE™ packet acceleration technology included for increased upstream performance**

SUMMARY OF BENEFITS

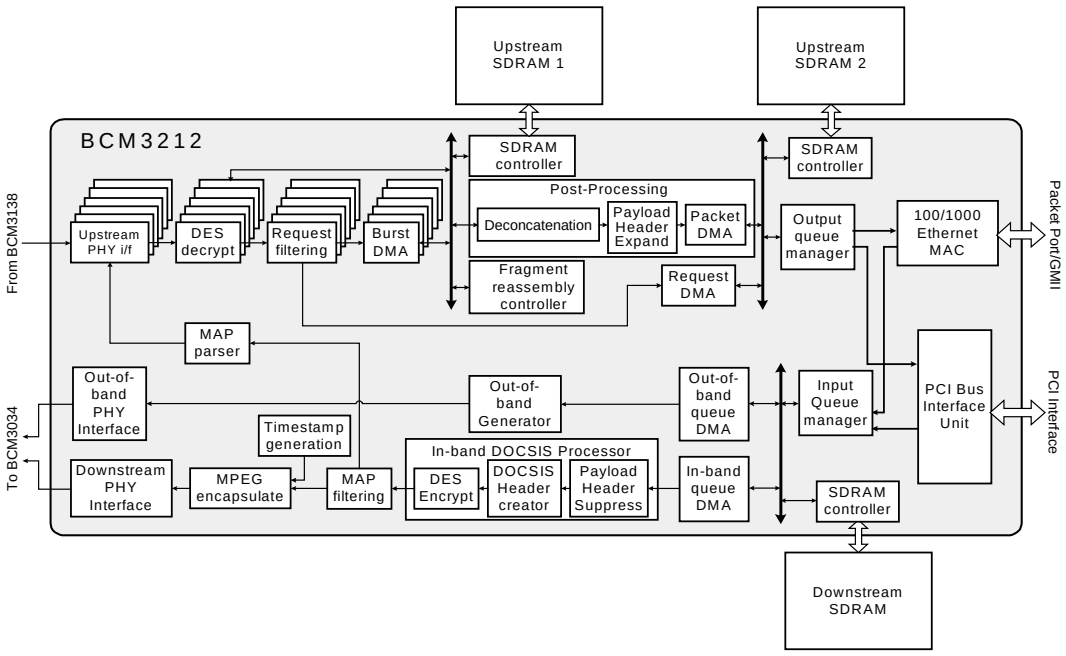
- **Hardware support for MAC-layer per-packet functions including fragmentation, concatenation, and payload header suppression offloads system CPU, giving higher overall system performance**
- **Extraction of bandwidth requests and DOCSIS MAC management messages allows software to access these messages without examining data packets**
- **Class-based queuing allows traffic prioritization:**
  - High, medium, and low priority downstream queues
  - High priority, low priority, request, and MAC management upstream queues
- **Support for carrier class redundancy via timestamp synchronization across multiple BCM3212s**
- **Supports high packet rates for maximum utilization of available cable plant bandwidth**
- **Out-of-Band (OOB) generator for messaging to BCM3352-based cable modems**
- **Can be remoted from external routing/classification engine for distributed CMTS (Mini Fiber Node) applications**
- **SPI master port controls register interface to BCM3034 and BCM3138 devices**
- **Packaged in an 841-pin, thermally enhanced plastic ball grid array**
- **Operates over industrial temperature range (-40 to +85 degrees C) PCI bus**

Typical Application Block Diagram



BCM3212 OVERVIEW

BCM3212 Simplified Block Diagram



The **BCM3212** is a highly integrated CMTS MAC IC for use in DOCSIS 1.1 and advanced TDMA PHY-layer CMTS products. With hardware support for concatenation parsing, fragment reassembly, payload header suppression, and advanced TDMA PHY-layer data rates, the **BCM3212** serves as the heart of a next-generation CMTS. The **BCM3212** provides a powerful yet cost-effective solution for a variety of CMTS architectures.

The **BCM3212** is based on sophisticated hardware processing engines for both the upstream and downstream paths. To achieve upstream throughput of 200,000 packets per second, the upstream processor design is segmented and uses two banks of SDRAM to minimize latency on the internal buses. The Upstream Processor performs DES decryption, fragment reassembly, deconcatenation, payload header expansion, PROPANE™ packet acceleration, upstream MIB statistic gathering, and priority queuing for the resultant packets. Each upstream queue can be independently configured to output packets to either the PCI or GMII interface. DOCSIS MAC management messages and bandwidth requests are extracted and queued separately from data packets so that they are readily available to the system controller.

The downstream processor accepts packets from priority queues and performs payload header suppression, DOCSIS header creation, DES encryption, CRC and HCS generation, MPEG encapsulation and multiplexing, and timestamp generation on the in-band data. The **BCM3212** also includes an out-of-band generator and TDMA PHY-layer interface so that the **BCM3212** can communicate with the BCM3352 cable modem devices' out-of-band receiver for control of power management functions.

All configuration and management of the **BCM3212** is done via the PCI interface. The PCI interface accommodates either 32-bit or 64-bit hosts operating at either 33 MHz or 66 MHz. The 100/1000 Ethernet MAC provides a standard interface (IEEE 802.3z GMII or MII) for transporting packets to and from the **BCM3212**.

A single **BCM3212** supports the association of one downstream channel with up to six upstream channels. By connecting multiple **BCM3212** chips via the seamless Master/Slave Interface, many other ratios may be achieved, including two downstreams to 12 upstreams (2 x 12) and one downstream to 24 upstreams (1 x 24). In multiple-downstream configurations, upstream channels can be remotely provisioned to be associated with one of two downstreams to enable load shifting.

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