L9177

Peripheral on chip for low end engine control

Datasheet - production data

PowerSO46

Features

- Supply voltage from 6 V to 18 V
  - Basic functionality guaranteed down to 3.9 V
- 5 V regulator up to 300 mA with thermal shutdown protection in current limitation condition
- 5 V tracking regulator up to 40 mA and short to battery protection
- 5 V standby regulator up to 2.5 mA
- 2 channels injectors drivers
  - Parallel and serial driving
  - Output internally clamped to 60 V
  - Minimum overcurrent at 2.8 A
  - Ron 0.6 Ω worst case (at T_j = 150 °C)
- 3 relay drivers
  - 2 with parallel and serial driving, 1 with serial driving
  - Output internally clamped to 45 V
  - Minimum guaranteed output current 1 A
  - Ron 1.5 Ω worst case (at T_j = 150 °C)
- Tachometer driver
  - Parallel and serial driving
  - Minimum guaranteed output current 25 mA
  - Ron 5 Ω worst case (at T_j = 150 °C)
- Lamp driver
  - Serial driving
  - Output internally clamped to 45 V
  - Minimum guaranteed output current 1 A (2 A during in-rush)
  - Ron 1.5 Ω worst case (at T_j = 150 °C)
- Stepper motor driver
  - Parallel driving
  - Minimum guaranteed output current 500 mA - full step
  - Ron 2.6 Ω worst case on the diagonal (at T_j = 150 °C)
- O2 sensor heater
  - Parallel and serial driving
  - Output internally clamped to 45 V
  - Minimum guaranteed output current 3 A
  - Ron 0.5 Ω worst case (at T_j = 150 °C)
- Protected high side driver
  - 100 mA min. current limitation threshold
- Full diagnosis by SPI
  - Injector driver: OL, STG, OC
  - Relay and Lamp drivers: OL, STG, OC
  - O2 sensor heater: OL, STG, OC
  - Tachometer: OL, STG, OC
  - Stepper motor driver: OL, STG, STB, OC
  - general diagnostic: over-temperature
- Protection for STB, STG (for stepper motor drivers and tracking regulator)
- Self configuring variable reluctance sensor interface
- K-line transceiver
- Microcontroller reset logic
- Packaged in PowerSO46

Table 1. Device summary

Order code	Package	Packing
L9177	PowerSO46	Tube
L9177TR		Tape and reel

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1 Description

L9177 is a device realized in ST BCD proprietary technology, able to provide the full set of power supplies and signal preprocessing peripherals needed to control a 2 Cylinder internal combustion Engine for Low End Application (e.g. small motorcycle, K-car, nautical engines, etc.).

L9177 integrates a 5 V main voltage regulator, a 5 V 40 mA tracking regulator for sensor supply and a 2.5 mA 5 V standby regulator.

The two channels injector drivers, the O2 sensor heater and two relay drivers can be controlled both with parallel input and with SPI interface. One additional relay driver and the lamp driver are controlled by SPI. The stepper motor driver is designed for a double winding coil motor, used for engine idle speed control.

Low side drivers implement SR control to minimize emission.

A protected 50 mA high side driver is provided.

A Variable Reluctance Sensor interface allows the connection to a commercial magnetic pick-up, allowing the indirect measurement of internal combustion engine crank angle. A K-line (standard ISO-9141 compatible) is provided as data communication interface.

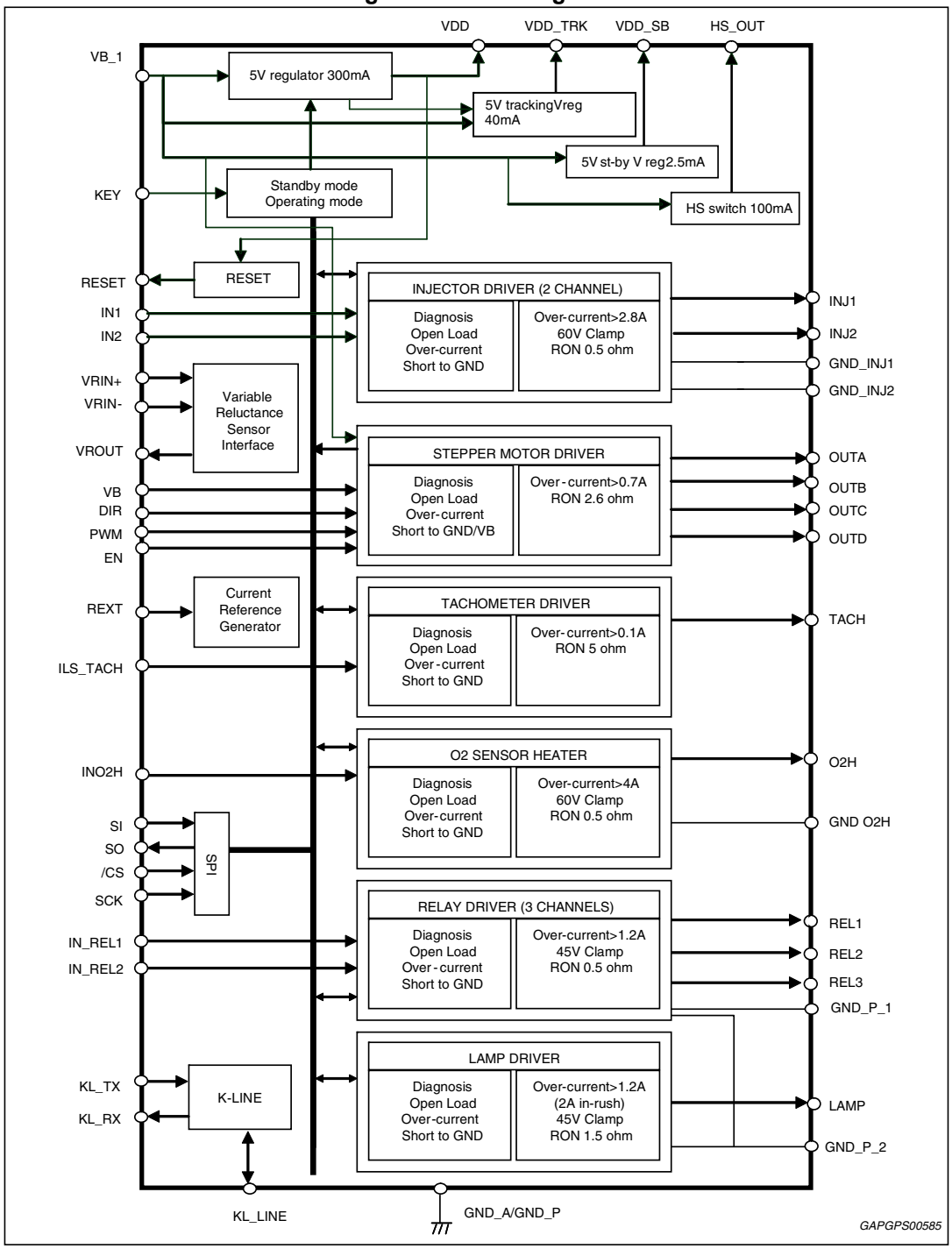
All functionalities are fully protected and provide complete diagnostics via a 24bit SPI interface. An overall protection against over temperature is provided as well.

The device is available in PowerSO46, ST proprietary package for high power application.

2 Block diagram and pin description

2.1 Block diagram

Figure 1. Block diagram



2.2 Pin description

Figure 2. Pin connection (top view)

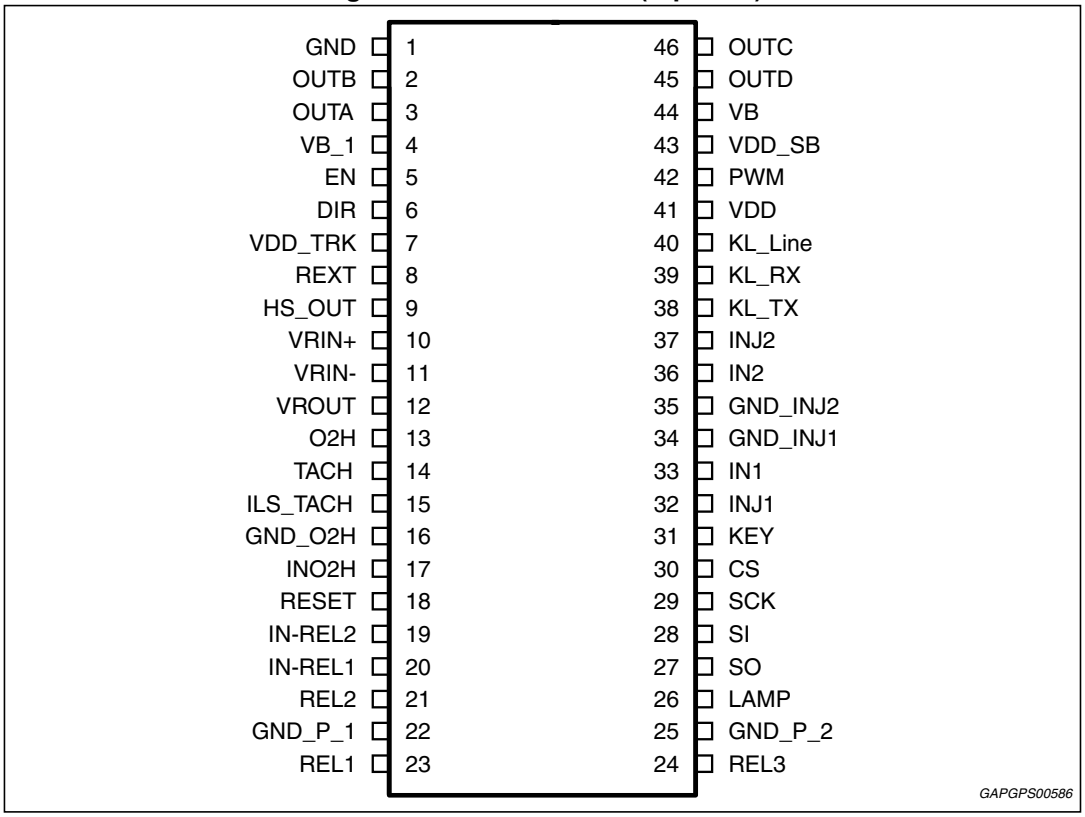


Table 2. Pin function

Pin #	Pin name	Description	I/O type	Class
1	GND	Analog and power ground	GND	PWR
2	OUTB	Output bridge 1	O	PWR
3	OUTA	Output bridge 1	O	PWR
4	VB_1	Battery line to bridge1	I	PWR
5	EN	Logic input to enable stepper motor	I	SIGNAL
6	DIR	Logic input to set stepper motor direction	I	SIGNAL
7	VDD_TRK	Tracking voltage regulator output	O	PWR
8	REXT	External resistor for precision current reference	I	SIGNAL
9	HS_OUT	High side switch output	O	PWR
10	VRIN+	VRS positive differential input	I	SIGNAL
11	VRIN-	VRS negative differential input	I	SIGNAL
12	VROUT	VRS output	O	SIGNAL
13	O2H	O2 sensor heater output	O	PWR

Table 2. Pin function (continued)

Pin #	Pin name	Description	I/O type	Class
14	TACH	Tachometer driver output	O	PWR
15	ILS_TACH	Tachometer driver input	I	SIGNAL
16	GND_O2H	O2 sensor heater ground	GND	PWR
17	INO2H	O2 sensor heater input	I	SIGNAL
18	RESET	Reset signal to the micro	O	SIGNAL
19	IN_REL2	Relay 2 parallel control input	I	SIGNAL
20	IN_REL1	Relay 1 parallel control input	I	SIGNAL
21	REL2	Relay 2 driver output	O	PWR
22	GND_P_1	Power ground relay 1-2	O	PWR
23	REL1	Relay 1 driver output	O	PWR
24	REL3	Relay 3 driver output	O	SIGNAL
25	GND_P_2	Power ground for lamp	GND	PWR
26	LAMP	Lamp driver output	O	PWR
27	SO	SPI data out	O	SIGNAL
28	SI	SPI data in	I	SIGNAL
29	SCK	SPI serial clock	I	SIGNAL
30	CS	SPI chip select	I	SIGNAL
31	KEY	Key signal	I	SIGNAL
32	INJ1	Injector 1driver power output	O	PWR
33	IN1	Injector 1 driver input command	I	SIGNAL
34	GND_INJ1	Injector 1 ground	GND	PWR
35	GND_INJ2	Injector 2 ground	GND	PWR
36	IN2	Injector 2 driver input command	I	SIGNAL
37	INJ2	Injector 2 driver power output	O	PWR
38	KL_TX	K-Line TX digital IN	I	SIGNAL
39	KL_RX	K-Line RX digital OUT	O	SIGNAL
40	KL_LINE	K-Line	I/O	PWR
41	VDD	5 V voltage regulator output	O	PWR
42	PWM	Logic Input to set Stepper Motor Speed	I	SIGNAL
43	VDD_SB	5 V standby voltage regulator output	O	PWR
44	VB	Battery line to bridge 2	I	PWR
45	OUTD	Output bridge 2	O	PWR
46	OUTC	Output bridge 2	O	PWR

3 Electrical specifications

3.1 Operating range

The device may not operate properly if maximum operating conditions are exceeded.

Table 3. Operating conditions

Symbol	Parameter	Value	Unit
VB	Supply voltage	6 to 18(1)	V
	I/O logic	0 to Vdd	V
	Stepper motor outputs	-0.3 to Vb+	V
	Low side	-0.3 to clamp voltage	V

1. Below 3.9 V the device is in a safety state (internal circuitries are on but all the outputs are off).

   From 3.9 V to 5.5 V (cranck functionality)
   Reset function; VDD > 3.3 V (rds-on state) IVDD=100mA; 3.3 V<VDD_TRK<VDD (rds-on state);
   Low-sides, K-Line, H-Bridge OFF if Reset = 0; SPI not available, internal registers resetted if Reset = 0;
   All Diagnosis disabled if Reset=0; VRS function limited (Vdiff max =1000mV).

   From 5.5 V to 6 V (low battery)
   All the functions are granted with the following degraded parameters; VDD5>4.510V; VDD Reset function guaranteed, but no Reset asserted; Tracking error < 100 mV (Iload = 40 mA, rds-on state).

   From 18 V to V_{B_off} (load dump transient)
   All the functions are granted with increased power dissipation and no reset is asserted during transient.

   From V_{B_off} to 40 V (internal circuitries are on but all the outputs are off)
   The device is on in a safety state.

3.2 Absolute maximum ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause permanent damage to the integrated circuit.

Table 4. Absolute maximum ratings

Parameter	Condition	Min	Max	Unit
DC supply voltage	pin VB/VB_1	-0.3	40	V
I/O low voltage pins(1)	-	-0.3	7	V
I/O low voltage digital pins(2)	-	-0.3	Vdd+0.3	V
I/O power pins(3) voltage range	-	-0.3	Clamp voltage	V
TACH pin	-	-0.3	40	V
OUTA-D	-	-0.3	VB +0.3	V

Table 4. Absolute maximum ratings (continued)

Parameter	Condition	Min	Max	Unit
KEY pin	To be protected with Rkey_ext to limit sourced/sinked current to ± 5 mA in dc conditions and ±20 mA during transients (ISO-pulses on battery line)	-0.3	10	V
VRIN- / VRIN+	Max current |20 mA| to be limited with external resistors	-0.3	Vdd + 0.3	V
VDD_TRK pin	-	-2	40	V
KL_LINE pin	-	-16	40	V
Maximum voltage shift between GND pins	PIN GND, GND_O2H, GND_P_1,2, GND_INJ1,2, GNDA, GNDP	-0.3	0.3	V
I/O power pins(3) maximum energy (single pulse, max. current)	Injector drivers	-	50	mJ
	O2 sensor heater	-	60	mJ
	Relay/lamp drivers	-	25	mJ
I/O power pins(3) maximum energy (continuous pulse, max. current, 36 million pulses with T = 100 ms)	Injector drivers	-	18	mJ
	O2 sensor heater	-	22	mJ
	Relay/lamp drivers	-	8	mJ
Reverse current through O2H output without supply voltage(4)	Static (room temperature, max reverse diode voltage 1.5 V)	-	2.5	A
	Dynamic (guarantee by iso-pulse test immunity on application board)	-	-	
Reverse current through INJx outputs without supply voltage(4)	Static (room temperature, max reverse diode voltage 1.5 V)	-	2.2	A
	Dynamic (guarantee by iso-pulse test immunity on application board)	-	-	
Reverse current through LAMP output without supply voltage(4)	Static (room temperature, max reverse diode voltage 1.5v)	-	1.2	A
	Dynamic (guarantee by iso-pulse test immunity on application board)	-	-	
Reverse current through RLYx outputs without supply voltage(4)	Static (room temperature, max reverse diode voltage 1.5 V)	-	1.5	A
	Dynamic (guarantee by iso-pulse test immunity on application board)	-	-	
Reverse current through TACH output without supply voltage(4)	Static (room temperature, max reverse diode voltage 1.5 V)	-	0.5	A
	Dynamic (guarantee by iso-pulse test immunity on application board)	-	-	

1. Pins are VDD, VDD_SB, REXT, DIR
2. Pins are CS, SCK, SI, SO, VROUT, RESET, PWM, EN, INO2H, ILS_TACH, IN, KL_TX, KL_RX
3. Pins are O2H, LAMP, INJ1-2, REL1-2-3
4. Reverse battery connection, parameter not tested for info only

Table 5. ESD protection

Item	Condition	Min	Max	Unit
All pins (1)	HBM	-2	2	kV
All pins	MM	-200	200	V
All pins	CDM (values for corner pins in brackets)	-500 / (-750)	500 / (750)	V
Pins to connector (2)	HBM	-4	4	kV

1. Except:
OUTA-D, TACH, O2H, LAMP, INJ1-2, REL1-2-3 vs. GNDP1:-1 / 1 kV
OUTA-D, TACH, O2H, LAMP, INJ1-2, REL1-2-3 vs. GNDP2, GNDO2:-1.5 / 1.5 kV

2. Pins are OUTA-D, TACH, O2H, LAMP, INJ1-2, KEY, REL1-2-3,VB,KL_LINE, VDD_TRK all GND connected together. The device is AEC-Q100 compliant.

3.3 Latch-up test

According to JEDEC 78 class 2 level A.

3.4 Temperature ranges and thermal data

Table 6. Temperature ranges and thermal data

Symbol	Parameter	Min	Max	Unit
T_{amb}	Operating temperature (ECU environment)	-40	125	°C
T_j	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	-40	150	°C
T_{ot}	Thermal shut-down temperature	155	200	°C
O_{Thys}	Thermal shut-down temperature hysteresis	10		°C
$R_{Th\ j\text{-}amb}$	Thermal resistance junction-to-ambient(1)		16	°C/W
$R_{Th\ j\text{-}case}$	Thermal resistance junction-to-case		2	°C/W

1. with 2s2p PCB thermally enhanced.

3.5 Electrical characteristics

V_B = 6 V to 18 V, T_{amb} = -40 °C to 125 °C.

3.5.1 Supply

Table 7. Supply electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_B	Operating supply voltage range	-	6	-	18	V
V_{B_off}	Vbat switch off threshold voltage	-	30	32	34	V
$V_{B\ OVh}$	Overvoltage threshold hysteresis	-	0.5	-	-	V

Table 7. Supply electrical characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{B\ UVL}$	Undervoltage disable LOW threshold	-	3.5	3.7	3.9	V
$V_{B\ UVh}$	Undervoltage threshold hysteresis	-	0.3	-	1	V
$I_{VB(dis)}$	Standby current	VB= 13 V, device disabled, KEY<0.7 V	-	-	120	µA
I_{VB}	Quiescent current	VB= 13 V, outputs floating	-	-	20	mA
V_{rext}	ASIC Bias reference	Application note	-	1.22	-	V
fint_clk	Internal clock reference	Application note	-	5.6	-	MHz

3.5.2 Key

Table 8. Key electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_Key_L	Input low threshold	-	1.5	-	-	V
V_Key_H	Input high threshold	-	-	-	3.3	V
V_Key_Hyst	Input voltage hysteresis	-	0.5	-	1.8	V
R_Key	Internal pull down	-	50	150	300	kΩ
T_key_deglitch	Key input filter time	Guaranteed by scan	26	-	40	µs
T_key_delay	Maximum delay time from Key to regulator enable	Time from key rising edge to 20% VDD rising edge	-	-	200	µs

Figure 3. Input threshold

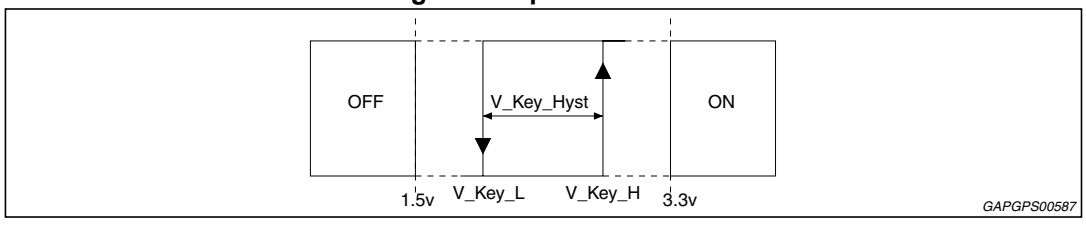
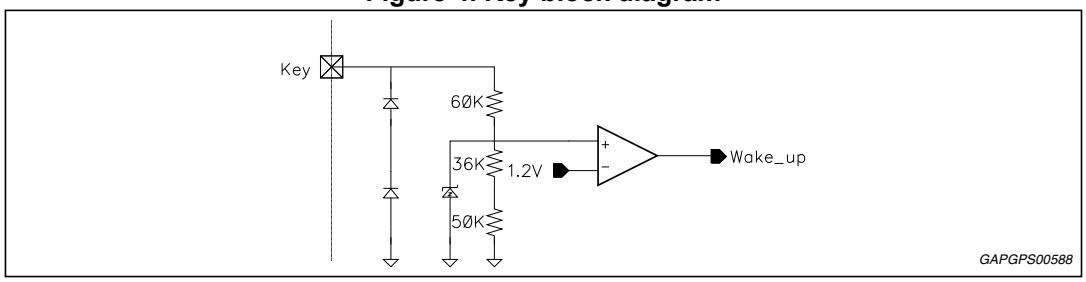


Figure 4. Key block diagram



3.5.3 Digital pins

Table 9. Digital pins characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{in_L}	Input level threshold low	-	0.3*Vdd	-	-	V
V_{in_H}	Input level threshold high	-	-	-	0.7*Vdd	V
V_{hin}	Input voltage hysteresis	-	0.1	-	-	V
R_pull	Internal pull-down/pull-up(1)	-	50	150	250	kΩ
I_pull_down	Active pull-down	-	10	-	100	µA

1. Pins with pull-up: SI, SCK, CS, KL-TX;
Pins with pull-down: EN, PWM, ISL-TACH, INO2H, IN_REL1-2, IN1-2;
Pins with active pull-down: DIR.

3.5.4 Digital output pins

Table 10. Digital output pins characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
	Output level low	I_{sink} = 2mA	-	-	0.4	V
	Output level high	I_{source} = 2mA(1)	Vdd-0.5	-	-	V

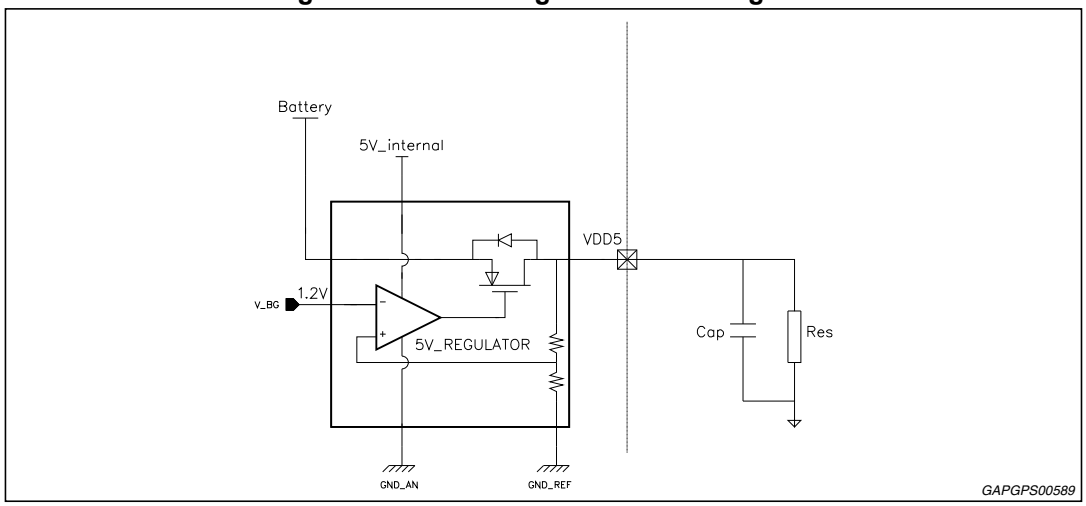
1. Pins with open drain output: RESET, VROUT;
Pins with push-pull stage and tri-state condition: SDO

3.5.5 5 V voltage regulator

Table 11. VDD output electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{dd}	Output voltage	-	4.9	5	5.1	V
Ln_vdd	Line regulation	V_B = 6 V to 18 V I_{load} = 150 mA	-25	-	25	mV
Ld_vdd	Load regulation	V_B = 13 V I_{load} = 5 mA to 300 mA	-25	-	25	mV
V_{dd_OS}	Max overshoot	Recovery from ISO pulse stimuli on battery line (guaranteed by design)	-	-	5.5	V
V_{dd_SR}	Voltage slew-rate at power-on	C_{load} = 4.7 µF	2	-	25	V/ms
I_{dd}	Load current	-	5	-	300	mA
I_{dd_max}	Current limitation	Output short to 4 V	350	-	600	mA
I_{dd_STG}	Short to ground current limitation	Output shorted to GND	350	-	700	mA
PSRR	Power supply rejection ratio	Sin wave @ 1 kHz 1V pp V_B = 13 V I_{load} = 5 mA to 300 mA	40	-	-	dB
V_{dr5}	V_B - V_{dd} - V_{dd} dropout voltage	V_B = 5 V I_{load} = 300 mA	0.30	-	0.75	V

Figure 5. 5 V main regulator block diagram

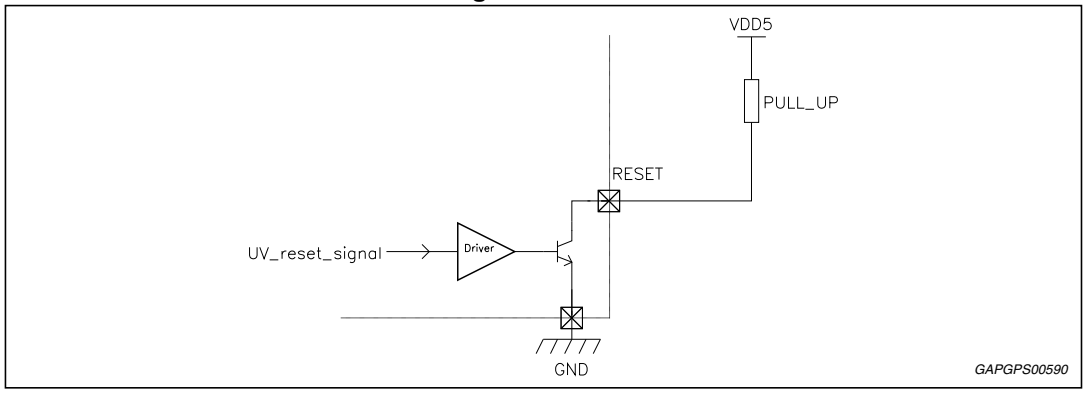


3.5.6 Reset

Table 12. Reset function electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VUV_LO	Output low voltage	1 < Vdd< Vth_UV, I_{reset} = 2 mA	-	-	0.6	V
IUV_LO	Reset current capability	1 < Vdd < Vth_UV, V_{reset} = 0.6 V	2	-	-	mA
I_{lk}	Leakage current	VUV_reset = 4.5 V	-	-	1	µA
Vth_UV	Vdd under voltage low threshold	V_B = 13.5 V	4.5	-	Vdd - 150 mV	V
Vth_UV Tht	Vdd under voltage high threshold	-	4.5	-	Vdd - 50 mV	V
Vth_UV HYS	Vdd under voltage hysteresis	-	50	-	-	mV
Td_UV_ rst	Power on UV reset delay	-	17	22	30	ms
T_{fUV_reset}	UV reset filter	Vdd< Vth_UV	25	50	75	µs

Figure 6. Reset

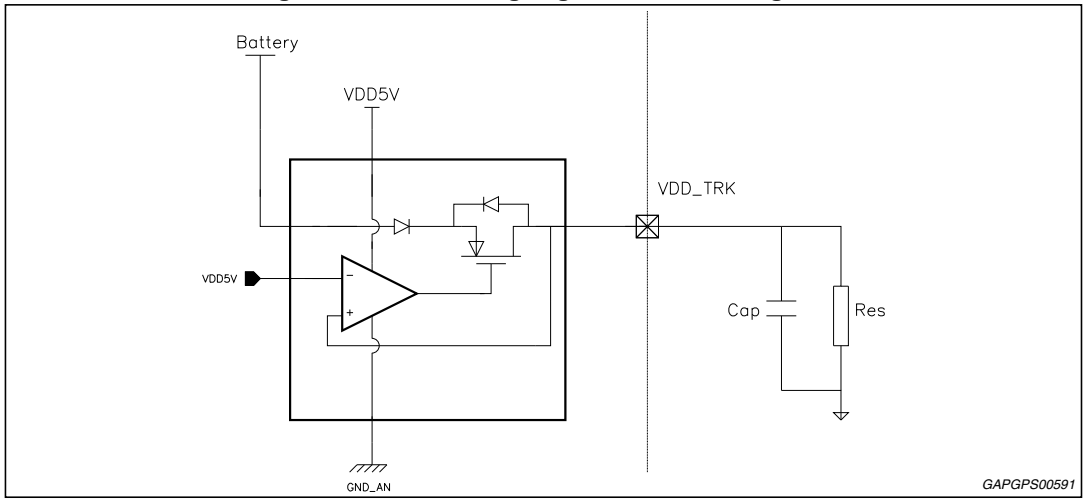


3.5.7 5 V tracking voltage regulator

Table 13. VDD_TRK output electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
DV_{ddtrk}	Output voltage tracking error	V_B = 6 V, I_{trk} = 1 to 40 mA	-15	-	15	mV
V_{short}	Tracking output short circuit voltage range	-	-2	-	V_B	V
I_{trk_max}	Output current limitation	Output short to 4 V	50	-	100	mA
I_{trk_sb}	Tracking output reverse current (limited by the regulator)	Output shorted to V_B = 16 V	-	-	10	mA
I_{dd}	Load current	-	1	-	40	mA
Ln_vdd_trk	Line regulation	V_B = 6 V to 18 V - I_{load} = 40 mA	-15	-	15	mV
Ld_vdd_trk	Load regulation	V_B = 13 V I_{load} = 1 to 40 mA	-15	-	15	mV
PSRR	Power supply rejection ratio	Sin wave @ 1 kHz 1V pp V_B = 13 V I_{load} = 1 to 40 mA	40	-	-	dB

Figure 7. 5 V tracking regulator block diagram

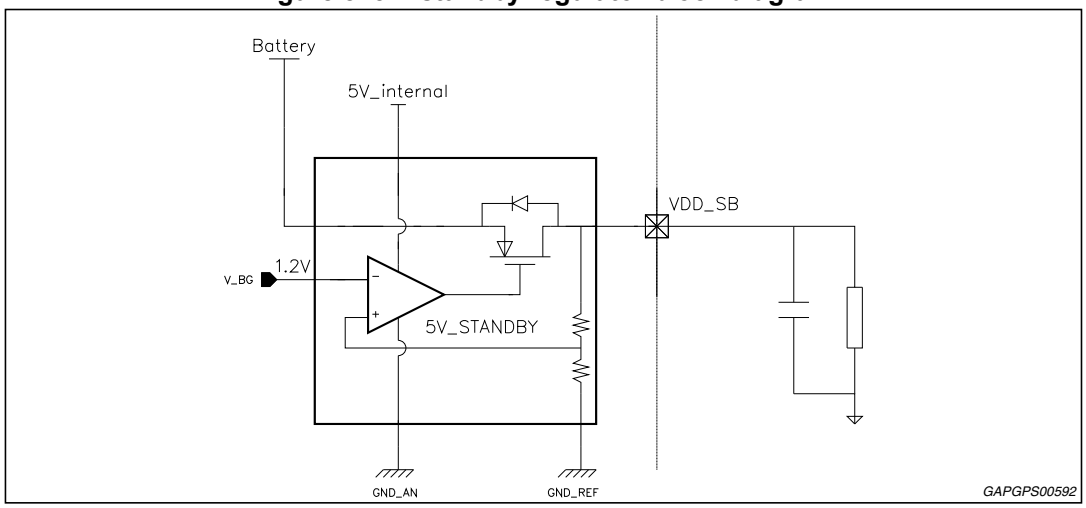


3.5.8 Standby regulator

Table 14. VDD_SB output electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{ddsb}	Output voltage	-	4.75	5	5.25	V
Ln_vsb	Line regulation	V_B =6 V to 18 V I_{load} = 1 mA	-25	-	25	mV
Ld_vsb	Load regulation	V_B =13 V I_{load} = 0.1 mA to 2.5 mA	-25	-	25	mV
V_{dd_OS}	Max overshoot	-	-	-	5.5	V
I_{dd}	Load current	-	0.1	-	2.5	mA
I_{sb_max}	Current limitation	Output short to 4 V	5	-	50	mA
V_{sb_SR}	Voltage slew-rate at power on	Cload = 1 µF	2	-	30	V/ms
PSRR	Power supply rejection ratio	Sin wave @ 1 kHz 1V pp V_B = 13 V I_{load} = 0.1 to 1 mA	40	-	-	dB

Figure 8. 5 V standby regulator block diagram

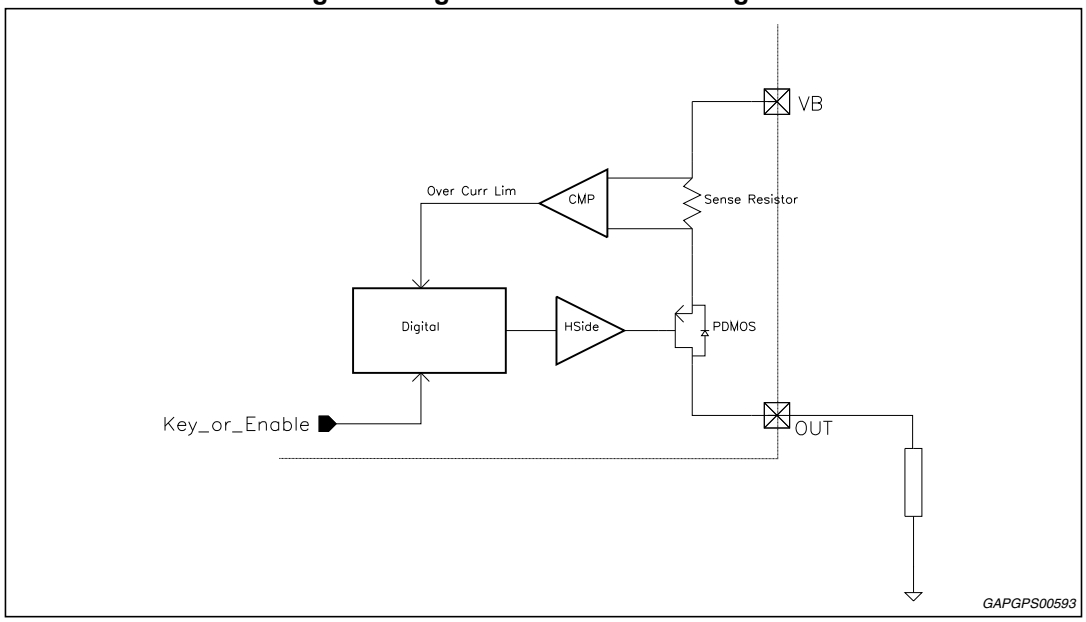


3.5.9 High side switch

Table 15. HS_OUT output electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{on_hs}	Ron	I_{hs} = 50 mA	-	-	14	Ω
I_{hs_max}	Current limitation	V_B =13.5 V	100	-	400	mA

Figure 9. High-side driver block diagram



3.5.10 Injector driver

Table 16. Injector driver electrical characteristic

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{max}	Output current	-	-	-	2.2	A
I_oc	Overcurrent threshold	-	2.8	-	5	A
V_{DS}	Output clamping voltage	I = 2.2 A	55	-	65	V
R_{on}	On resistance	I = 2.2 A	-	-	0.6	Ω
I_{lk_off}	Leakage current	V_{out} = 18 V, diagnosis OFF	-	-	10	µA
I_{lk_on}	Leakage current	V_{out} = 18 V, diagnosis ON	-	-	100	µA
t_{on-off}	Turn on-off delay	from CMD edge to 50% output variation	-	-	6	µs
V_{OL}	Open load output voltage	Driver in OFF condition	0.46*VDD	0.5*VDD	0.54*VDD	V
V_{diagth_H}(1)	Diagnostic high threshold	Driver in OFF condition	0.54*VDD	0.6*VDD	0.66*VDD	V
V_{diagth_L}(1)	Diagnostic low threshold	Driver in OFF condition	0.36*VDD	0.4*VDD	0.44*VDD	V

1. $V_{diagth\_L} < V_{out} < V_{diagth\_H}$ → Open Load; $V_{out} < V_{diagth\_L}$ → Short to GND

Figure 10. Low-side driver block diagram

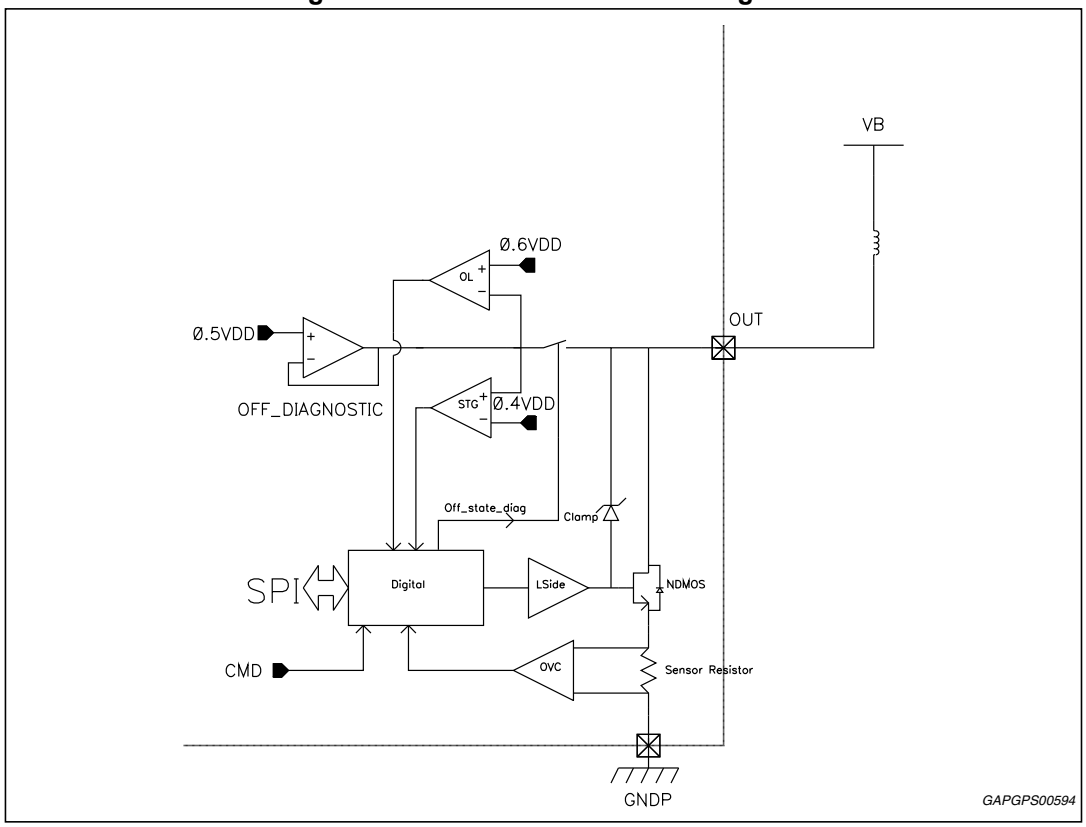
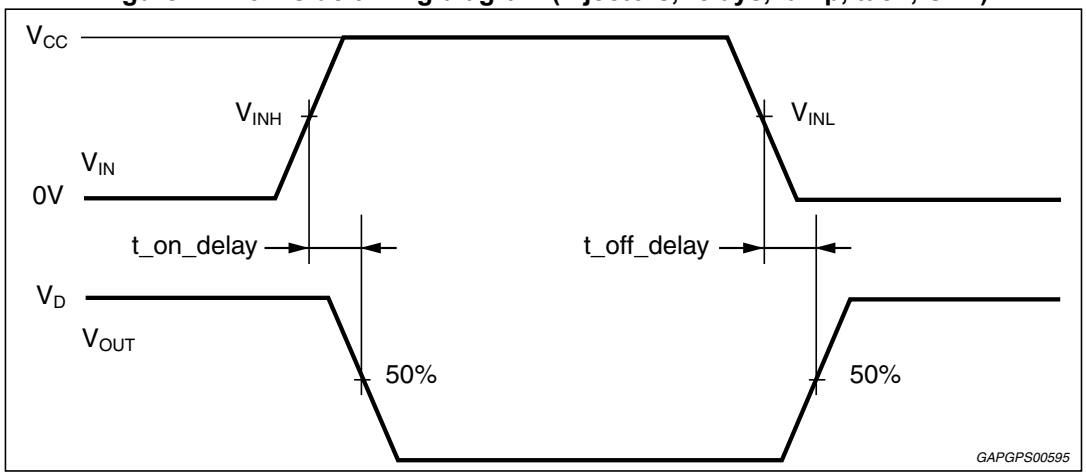


Figure 11. Low-side timing diagram (injectors, relays, lamp, tach, O2H)



3.5.11 Relay drivers

Table 17. Relay driver characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{max}	Output current	-	-	-	1	A
I_oc	Overcurrent threshold	-	1.2	-	2.5	A
V_{DS}	Output clamping voltage	I = 1 A	40	-	50	V
R_{on}	On resistance	I = 1 A	-	-	1.5	Ω
I_{lk_off}	Leakage current	V_{out} = 18 V, diagnosis OFF	-	-	10	µA
I_{lk_on}	Leakage current	V_{out} = 18 V, diagnosis ON	-	-	100	µA
t_{on_off}	Turn on-off delay	From CMD (serial or parallel) rising edge	-	-	6	µs
V_{OL}	Open load output voltage	Driver in OFF condition	0.46*VDD	0.5*VDD	0.54*VDD	V
V_{diagth_H}(1)	Diagnostic high threshold	Driver in OFF condition	0.54*VDD	0.6*VDD	0.66*VDD	V
V_{diagth_L}(1)	Diagnostic low threshold	Driver in OFF condition	0.36*VDD	0.4*VDD	0.44*VDD	V

1. $V_{diagth\_L} < V_{out} < V_{diagth\_H}$ → Open Load; $V_{out} < V_{diagth\_L}$ → Short to GND

3.5.12 Lamp driver

Table 18. Lamp driver characteristics

Symbol	Parameter	Condition	Min	Typ	Max	unit
I_{LI}	Linear current limitation	-	2	-	4	A
I_{oc}	Overcurrent threshold	Masked for lamp driver during in-rush	1.2	-	2.4	A
t_{dgmsk}	Diagnosis masking time	Guaranteed by scan	2	-	5	ms
V_{DS}	Output clamping voltage	I = 200 mA	40	-	50	V
R_{on}	On resistance	I = 200 mA	-	-	1.5	Ω
I_{lk_off}	Leakage current	V_{out} = 18 V, diagnosis OFF	-	-	10	µA
I_{lk_on}	Leakage current	V_{out} = 18 V, diagnosis ON	-	-	100	µA
t_{on_off}	Turn on-off delay	From SPI CS rising edge	-	-	6	µs
V_{OL}	Open load output voltage	Driver in OFF condition	0.46*VDD	0.5*VDD	0.54*VDD	V
V_{diagth_H}(1)	Diagnostic high threshold	Driver in OFF condition	0.54*VDD	0.6*VDD	0.66*VDD	V
V_{diagth_L}(1)	Diagnostic low threshold	Driver in OFF condition	0.36*VDD	0.4*VDD	0.44*VDD	V

1. $V_{diagth\_L} < V_{out} < V_{diagth\_H}$ → Open Load; $V_{out} < V_{diagth\_L}$ → Short to GND

3.5.13 Tachometer driver

Table 19. Tachometer driver electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{oc}	Overcurrent threshold	-	100	-	500	mA
R_{on}	On resistance	I = 25 mA	-	-	5	Ω
I_{lk_off}	Leakage current	V_{out} = 18 V, diagnosis OFF	-	-	10	µA
I_{lk_on}	Leakage current	V_{out} = 18 V, diagnosis ON	-	-	100	µA
t_{on_off}	Turn on-off delay	From CMD (serial or parallel) rising edge	-	-	6	µs
V_{OL}	Open load output voltage	driver in OFF condition	0.46*VDD	0.5*VDD	0.54*VDD	V
V_{diagth_H}(1)	Diagnostic high threshold	Driver in OFF condition	0.54*VDD	0.6*VDD	0.66*VDD	V
V_{diagth_L}(1)	Diagnostic low threshold	Driver in OFF condition	0.36*VDD	0.4*VDD	0.44*VDD	V

1. $V_{diagth\_L}<V_{out}<V_{diagth\_H}$ → Open Load; $V_{out}<V_{diagth\_L}$ → Short to GND

3.5.14 Stepper motor driver

Table 20. Stepper motor driver electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{oc}	Overcurrent threshold	ON condition	0.85	-	2	A
R_{dsON}	On resistance HS+LS	I_{out} = 0.5 A, T_j = 150 °C, V_B = 14 V	-	-	2.6	Ω
$f_{stepper}$	Working frequency	Application note	-	-	20	kHz
V_{out_off}(1)	OUTA_B_C_D output voltage	OUTA short to OUTB; OUTC short to OUTD; Stepper driver disable	0.44*VDD	0.5*VDD	0.54*VDD	V
V_{diagth_H}	Diagnostic high threshold	Driver in OFF condition	0.54*VDD	0.6*VDD	0.66*VDD	V
V_{diagth_L}	Diagnostic low threshold	Driver in OFF condition	0.36*VDD	0.4*VDD	0.44*VDD	V
I_{DSS_OUT}	Output leakage current	Driver in OFF condition	-	-	10	µA
t_{scvb}	Over current switch_off time	Guaranteed by scan	-	-	25	µs
t_{rb}	Rise output time	V_B = 12 V, R_l = 39 Ω	-	-	15	µs
t_{fb}	Fall output time	V_B = 12 V, R_l = 39 Ω	-	-	15	µs
$t_{rb\text{-}a}$	Rise output time	T_{amb} = 25 °C, V_B = 12 V, R_l = 39 Ω	-	-	10	µs
$t_{fb\text{-}a}$	Fall output time		-	-	10	µs
t_{pHLb}	Turn-off in/out delay time	V_B = 12 V, R_l = 39 Ω	-	-	15	µs
t_{pLHb}	Turn-off in/out delay time		-	-	15	µs
$V_{reverse\_HS}$	Reverse HS diode drop	Driver in OFF condition $I_{injected}$ = 0.5 A	-	-	1.5	V

Table 20. Stepper motor driver electrical characteristics (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{reverse\_LS}$	Reverse LS diode drop	Driver in OFF condition $I_{Sourced}$ = 0.5 A	-	-	-1.5	V

1. VoutA >Vdiagth_H and VoutB<Vdiagth_L or VoutC>Vdiagth_H and VoutD<Vdiagth_L → Open load
   VoutA_B_C_D>Vdiagth_H → Short to Battery
   VoutA_B_C_D<Vdiagth_L → Short to GND
   VoutA <Vdiagth_H and VoutB>Vdiagth_Lor VoutC<Vdiagth_H and VoutD>Vdiagth_L → No Fault

Figure 12. Stepper motor driver block diagram

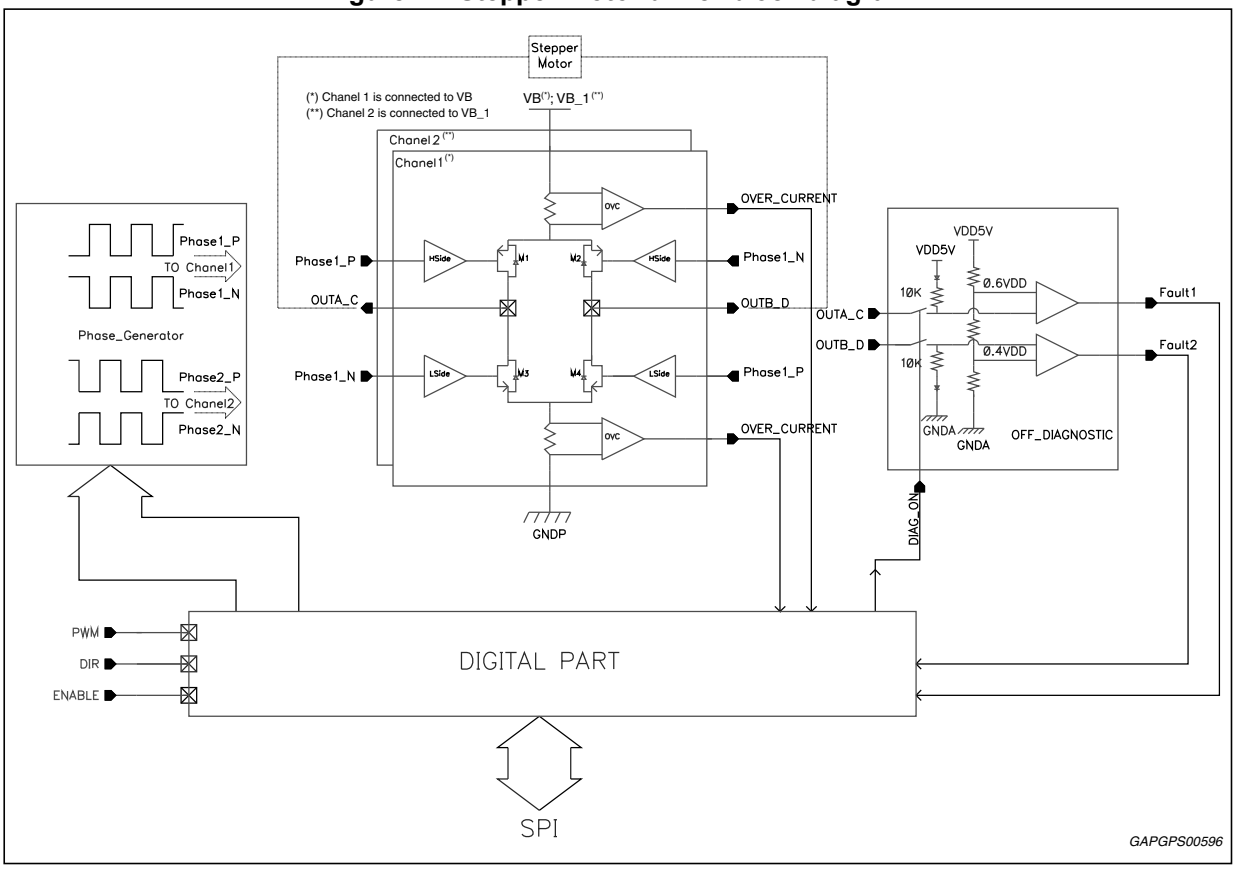
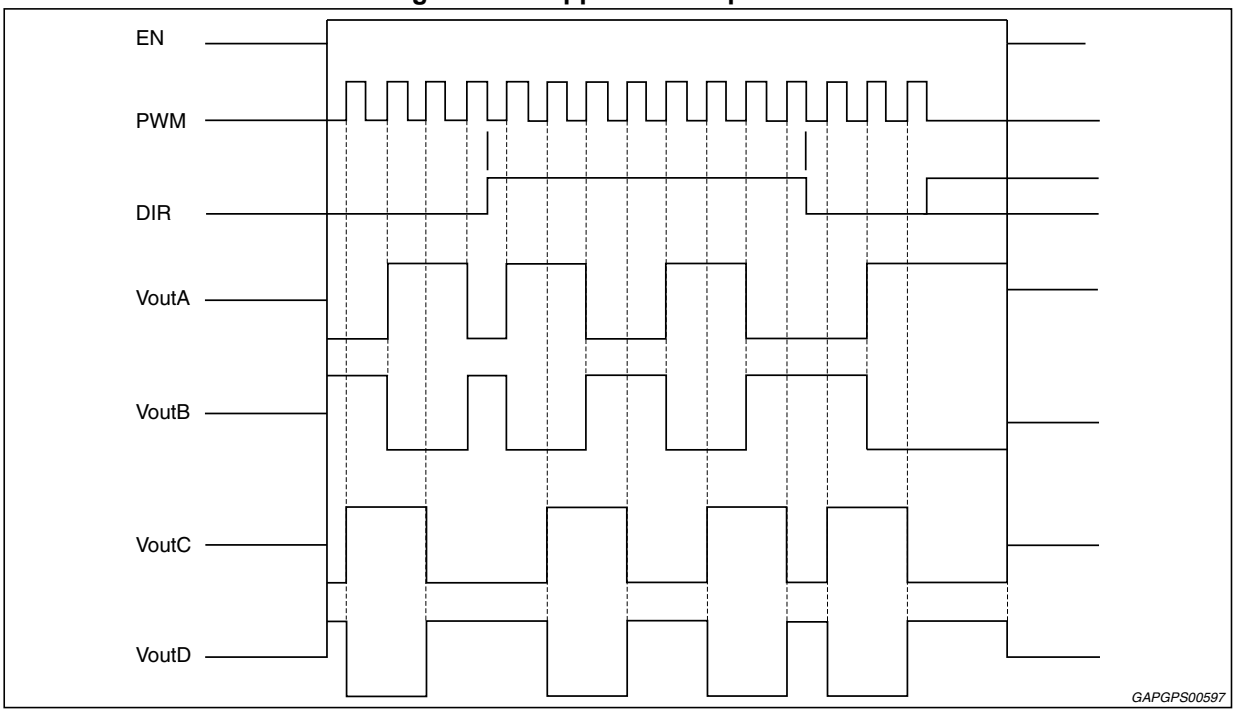


Figure 13. Stepper motor operations



3.5.15 O2 sensor heater driver

Table 21. O2 sensor heater driver characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{dsON}	On resistance	I_{out} = 3 A	-	-	0.5	Ω
V_C	Output clamping voltage	I_{out} = 3 A	40	-	50	V
I_{lk_off}	Leakage current	V_{out} = 18 V, diagnosis OFF	-	-	10	µA
I_{lk_on}	Leakage current	V_{out} = 18 V, diagnosis ON	-	-	100	µA
t_{on_off}	Turn on-off delay	From CMD (serial or parallel) rising edge	-	-	6	µs
V_{OL}	Open load output voltage	Driver in OFF condition	0.46*VDD	0.5*VDD	0.54*VDD	V
I_{OC}	Overcurrent threshold		3.8	-	5	A
V_{diagth_H}(1)	Diagnostic high threshold	Driver in OFF condition	0.54*VDD	0.6*VDD	0.66*VDD	V
V_{diagth_L}(1)	Diagnostic low threshold	Driver in OFF condition	0.36*VDD	0.4*VDD	0.44*VDD	V

1. $V_{diagth\_L} < V_{out} < V_{diagth\_H} \rightarrow$ Open Load; $V_{out} < V_{diagth\_L} \rightarrow$ Short to GND

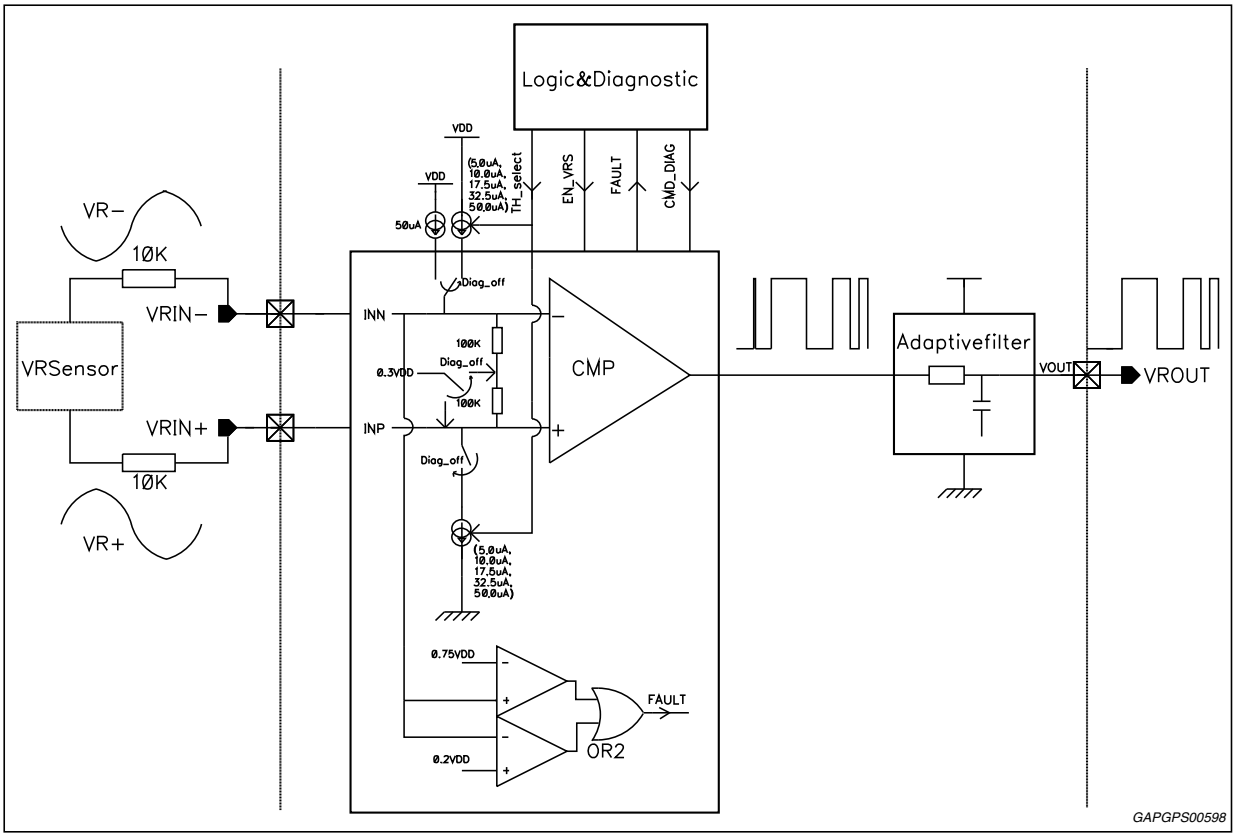
3.5.16 Variable reluctance sensor interface

Table 22. Variable reluctance sensor interface electrical characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{HTH}	Input high to low differential threshold voltage at VRIN+ and VRIN- nodes	-	-50	-	50	mV
V_{CM}	Common mode operating range at VRIN+ and VRIN-	-	0	1.5	3	V
$V_{cm\_internal}$	Internal common mode voltage	Switch off hysteresis current	0.27*VDD	0.3*VDD	0.33*VDD	V
V_{diagth_H}(1)	Diagnostic high threshold	Diagnostic voltage referred to VRIN- (see *Figure 14*)	0.67*VDD	0.75*VDD	0.82*VDD	V
V_{diagth_L}(1)	Diagnostic low threshold		0.18*VDD	0.2*VDD	0.22*VDD	V
I_{diag}	Diagnostic current	Current from VRIN- when diagnostic on	35	50	65	µA
$R_{internal\_common}$	Internal common mode resistor	Switch off hysteresis current	50	200	350	kΩ
I_{IB}	Input bias current	VRIN+ = VRIN- = 1.5 V	-	-	2	µA
I_{leak}	Output leakage	VROUT = 5 V	-	-	1	µA
V_{CLPH}	Input high clamping voltage	VRIN+ = |VRIN-| = 20 mA	-	5	-	V
V_{CLPL}	Input low clamping voltage	VRIN+ = |VRIN-| = |20 mA|	-1.5	-	-0.3	V
t_{of}	Output fall time	C_{LOAD} = 20 pF, R_{LOAD} = 5 kΩ	-	-	300	ns
t_{of_1nf}	Output fall time	C_{LOAD} = 1nF	-	-	1.5	µs
V_{OUTL}	Output buffer low voltage	I_{sink} = 2 mA	-	-	0.6	V
I_{OUTL}	Output current capability	V_{out} = 0.6 V	2	-	-	mA
t_{prop}	Propagation delay	VRS INM = 0.5 V, INP applied to 1 V to make VRS OUT commuted	0.1	0.45	0.8	µs

1. if (VRIN- > Vdiagth_H) or (VRIN- < Vdiagth_L) then Fault is detected.

Figure 14. VRS block diagram



3.5.17 K-line

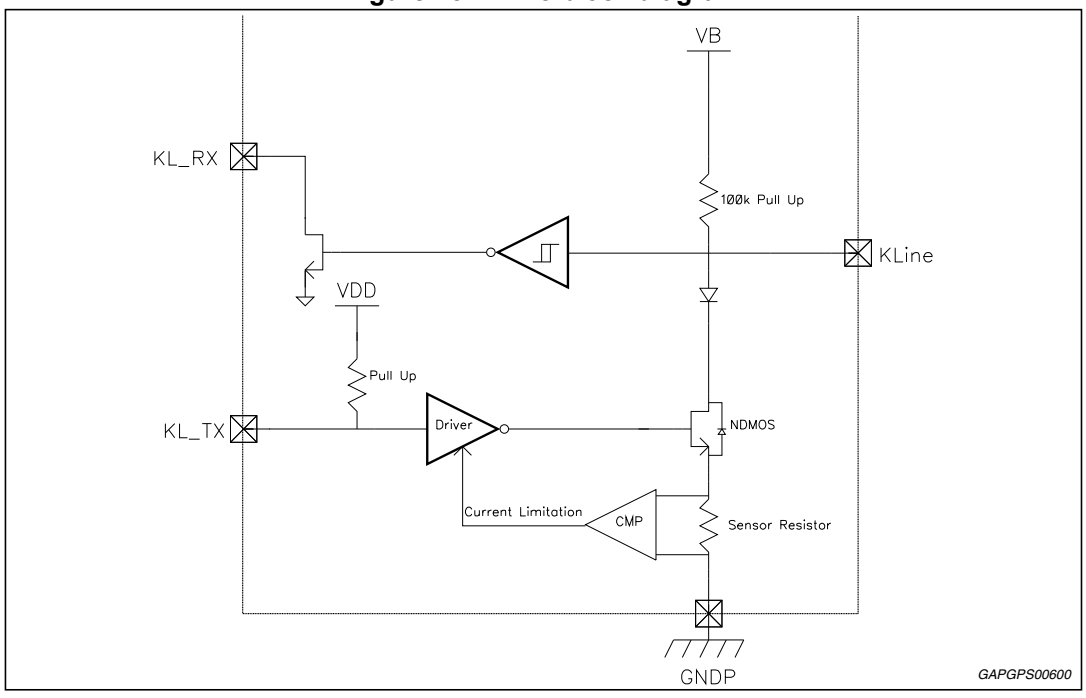
Table 23. K-Line interface electrical characteristics

Pin	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
KL_TX	ITXsource	Transmitter input source current	-	10	-	100	µA
	ITXsink	Transmitter input sink current	KL_TX = VDD	-	-	2.1	µA
K_LINE	VKoutL	Transmitter output low voltage	IsinkK_LINE = 35 mA, KL_TX = Low	-1	-	1.5	V
	VKinH	Receiver input high voltage	-	0.7xVB	-	VB	V
	VKinL	Receiver input low voltage	-	-1	-	0.35xVB	V
	VKH	Receiver input hysteresis	-	0.05xVB	-	0.3xVB	V
	IKleak	Receiver leakage current	KL_LINE = VB,KL_TX = High	-	-	1	µA

Table 23. K-Line interface electrical characteristics (continued)

Pin	Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_LINE	IKshort	Transmitter short circuit current	KL_LINE = VB, KL_TX = Low	60	-	-	mA
	IKrev	Reverse battery or GND loss current	ENABLE = KEY = VB = 0 V, KL_LINE = -13.5	-	-	10	mA
	IKpull-up	KLINE internal pull-up	KL_TX = High	60	-	140	kΩ
	IKuv	Under voltage current	KEY = High, KL_TX = Low, VB = 13.5 V, KL_LINE = -1 V	-	-	1	mA
KL_RX	VRXoutL	KL_RX output low voltage	I_{sink} = 0.4 mA	-	-	0.4	V
KL_TX to K_LINE	Tp_HLT	Transmitter turn-on delay time	CKline = 10 nF, RKline = 510 Ω	-	-	5	µs
K_LINE	T_fT	Transmitter fall time	CKline = 10 nF, RKline = 510 Ω	-	-	10	µs
KL_LINE to KL_RX	TpR	Receiver turn-on delay time	C_{load} = 20 pF, RPKL_Rx = 2 kΩ	-	-	4	µs
KL_RX	T_fR	Receiver fall time	C_{load} = 20 pF, RPKL_Rx = 2 kΩ	-	-	2	µs
	T_rR	Receiver rise time	C_{load} = 20 pF, RPKL_Rx = 2 kΩ	-	-	2	µs
K_LINE	fMax	Max transmission Operating frequency	Application note	-	-	60	kHz

Figure 15. K-line block diagram



3.5.18 SPI interface

Table 24. SPI characteristics and timings

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
SICin	Input capacitance	-	-	-	20	pF
SCKCin		-	-	-	20	pF
t_{SCKCS}	Clock inactive time before frame	-	100	-	-	ns
t_{CSSO}	Access time	See *Figure 17*	-	-	500	ns
t_{SOdis}	Output data (SO) disable time	No Capacitor on SO, See *Figure 16*	-	-	500	ns
t_{lead}	Channels elect (CS) lead time	See *Figure 17*	500	-	-	ns
t_{SCKFSO}	Output valid time	See *Figure 17*, @ f_{CLK} = 5.4 MHz	60	-	-	ns
t_{SOCS}	Output data (SO) disable time	No capacitor on SO, see *Figure 17*		-	500	ns
$t_{SIsetup}$	Input data (SI) set-up time	See *Figure 17*, @ f_{CLK} = 5.4 MHz	20	-	-	ns
t_{SIhold}	Input data (SI) hold time	See *Figure 17*, @ f_{CLK} = 5.4 MHz	20	-	-	ns
t_{SCK}	CLK period	-	185	-	-	ns
t_{CSCK}	Clock inactive time after frame	-	600	-	-	ns
t_{CSN}	CS de asserted time	-	600	-	-	ns

Figure 16. -SO loading for disable time measurement

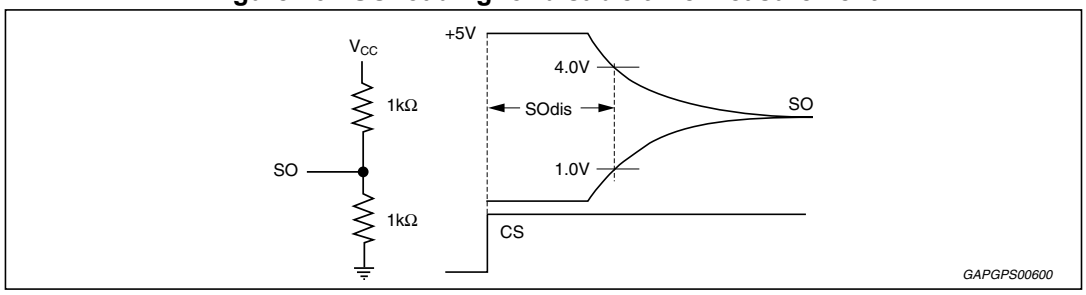
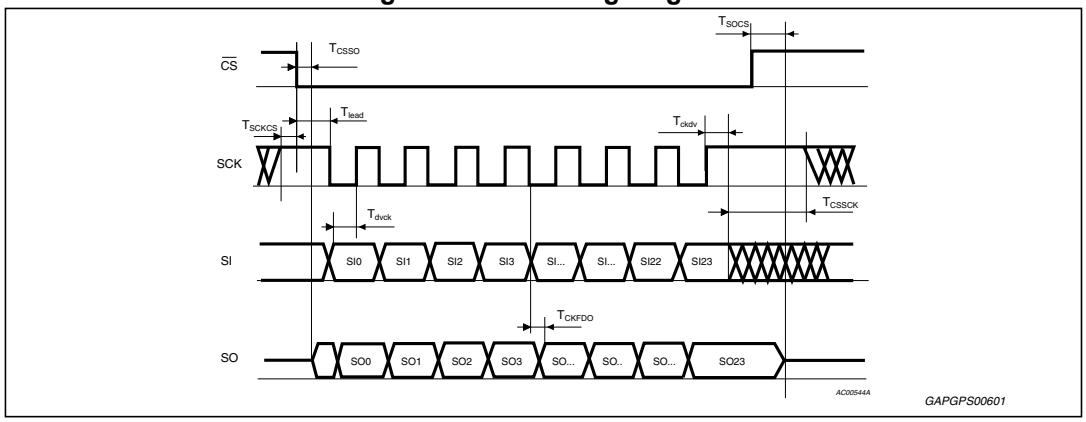


Figure 17. SPI timing diagram



4 Functional description

4.1 Chip working conditions

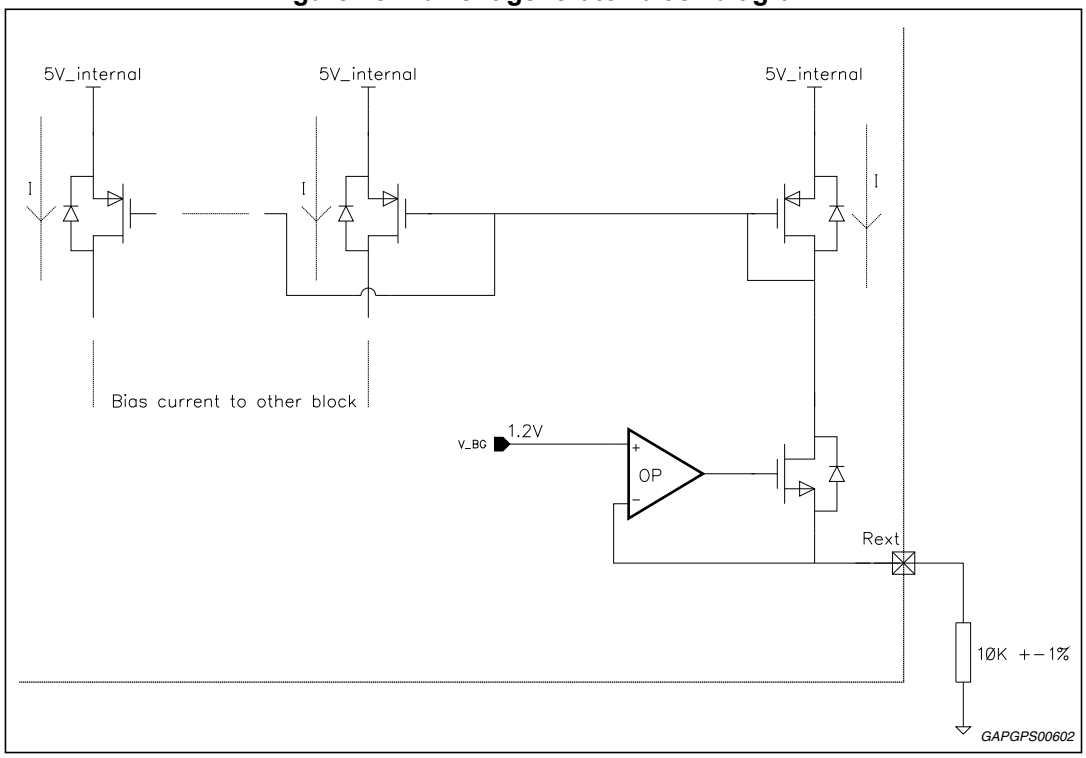
Table 25. L9177 outputs working conditions

-	Standby	Run mode	VB_OV	VB_UV	Reset	Over current	Thermal warning
VDD_SB regulator	ON	ON	ON	ON	ON	Current limitation	ON
VDD regulator	OFF	ON	OFF	OFF	ON	Current limitation	OFF if linked with VDD current limitation
VDD_TRK regulator	OFF	ON	OFF	OFF	ON	Current limitation	OFF if linked with VDD_TRK current limitation
All LS drivers	OFF	ON	OFF	OFF	OFF	Over current switch off	ON
Diagnostics of all LS drivers	OFF	ON	OFF	OFF	ON	-	ON
HS Driver	OFF	ON	OFF	OFF	OFF	Current limitation	ON
Stepper Motor Driver	OFF	ON	OFF	OFF	OFF	Over current switch off	ON
K-line Transceiver	OFF	ON	OFF	OFF	OFF	Current limitation	ON
VRS	OFF	ON	OFF	OFF	OFF	-	ON
SPI	Default	Default	Default	Default	Default	ON	ON

4.2 Chip bias current generation

The Internal current generator circuit is buffering internal band-gap voltage (1.2 V typ.) on a high precision external resistor (10 kΩ ±1 %) and generates an accurate current reference used to create all the chip bias currents.

Figure 18. Current generator block diagram



4.3 Power up/down sequences

Below figures show the power-on, power-off and time diagram behaviour of L9177.

VDD_SB (standby voltage) rises together with battery input, and in standby it is always present if battery is present, no matter the KEY_IN status.

When the KEY_IN signal rises up and remains stable for at least T_key_deglitch (see *Table 8*), the device goes in ON state, meaning that all voltage regulators and functions are active.

Wake-up is an intermediate status between standby and on mode, with current consumption higher than the standby one.

When Key_IN goes low, device goes in OFF mode but standby regulator remains ON.

Figure 19. Power-up sequence

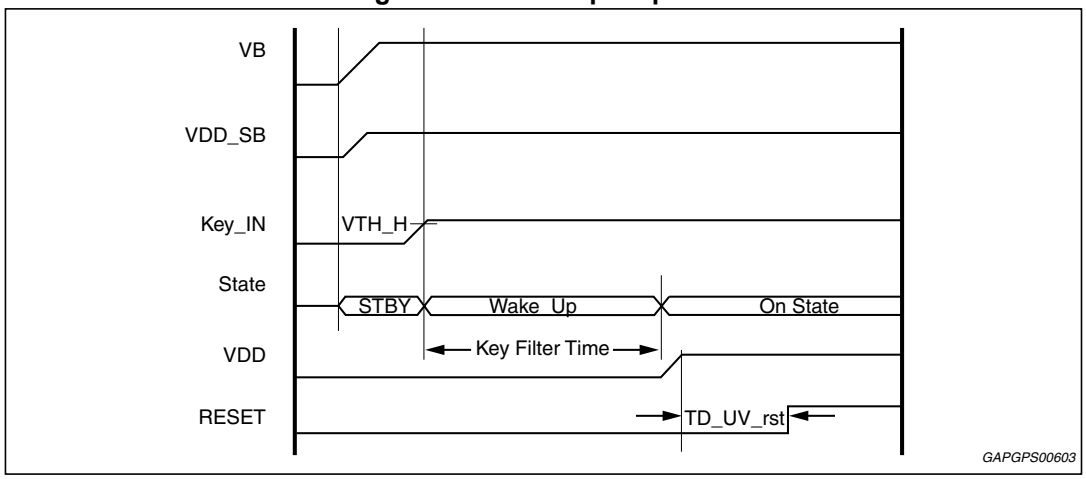
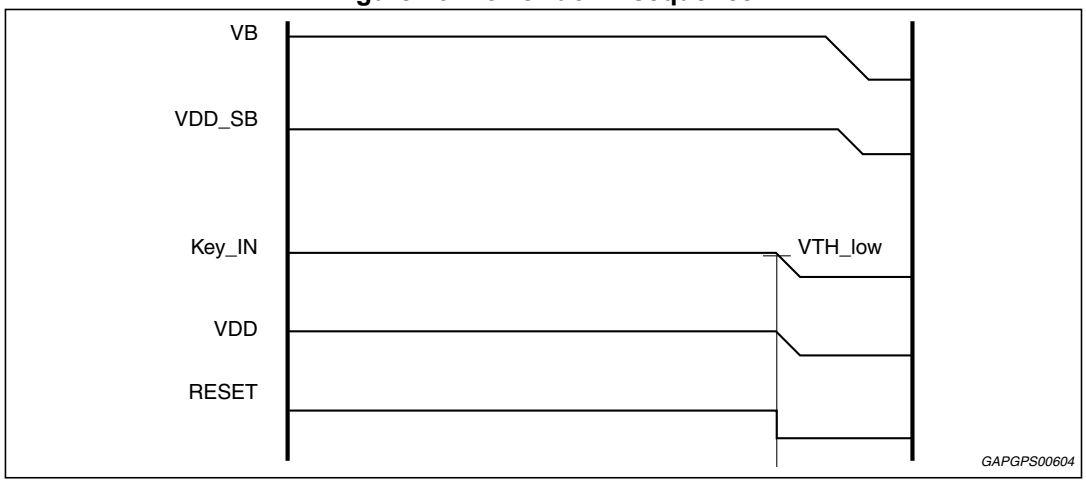


Figure 20. Power-down sequence



Reset signal detects a VDD undervoltage longer than UV_Reset_Filter_time by going to low level. When VDD recovers to normal level Reset signal returns to high level after Power_On_UV_Reset_Delay time (td_UV_rst). The Reset signal resets all the internal SPI registers.

4.4 SPI

SPI is a standard four wires interface, that communicates with a data word of 24 bits. By means of SPI all the channels can be driven in serial way and diagnosis is sent out.Timing of SPI's operations are reported in *Figure 17*. The input data (DIN) is read on the rising edge of the SPI's clock (SCLK), in the same way the output data (DOUT) must be read by the Microcontroller on the SCLK's rising edge.

4.4.1 Data in (DIN)

DIN command is used to turn On/Off internal channels which do not have Parallel Input command, and to clear diagnostic latches.

DIN is decoded at the end of the frame if the integrity checks are passed.

Table 26. Data in (DIN) words content

DIN0	DIN1	DIN2	DIN3	DIN4	DIN5	DIN6	DIN7
Mask	LAMP_0	LAMP_1	VRS Diag	VRS Hys0	VRS Hys1	VRS Hys2	0
DIN8	**DIN9**	**DIN10**	**DIN11**	**DIN12**	**DIN13**	**DIN14**	**DIN15**
INJ1_0	INJ1_1	INJ2_0	INJ2_1	O2H_0	O2H_1	RLY1_0	RLY1_1
DIN16	**DIN17**	**DIN18**	**DIN19**	**DIN20**	**DIN21**	**DIN22**	**DIN23**
RLY2_0	RLY2_1	RLY3_0	RLY3_1	TACH_0	TACH_1	Clear diag	Parity

Data in structure (LSB first)

- **Mask** bit is used to mask serial command for diagnosis only readings on DOUT:

  0 - Read Diag. All DIN bits are ignored.

  1 - Write. All DIN are transferred into the internal registers.
- **Command** bits are used to control the output drivers: (INJ1-2, O2H, RLY1-2-3, LAMP and TACH) as described in following table:

Table 27. Data in command bits structure

xxx_1	xxx_0	Description
1	0	Turn-off driver / parallel polarity 0
1	1	Turn-on driver / parallel polarity 1
0	X	No change (the driver will maintain the previous condition)

- VRS Diag bit is used active high to enable diagnostic phase of VRS block.
- Programmable VRS Hysteresis: VRS hysteresis is programmable in 5 steps according to *Table 28: Data in VRS hysteresis*.
- Clear Diag, when set to 1 generates a request to clear those diagnostic flags which are latched.
- In addition odd parity bit (that is the last bit of the frame and includes in its calculation the "Don't care" bits) is used for DIN word check together with falling clock edges count.

Table 28. Data in VRS hysteresis

Hys 2	Hys 1	Hys 0	Description
0	0	0	Default hysteresis value
0	0	1	Hys VRS = 100 mV
0	1	0	Hys VRS = 200 mV
0	1	1	Hys VRS = 350 mV
1	0	0	Hys VRS = 650 mV
1	0	1	Hys VRS = 1000 mV
1	1	1	Not Valid (Hys doesn't change)

4.4.2 Data out

Status flag are sampled and sent out through DOUT pin at each R/W SPI operation. The structure of the 24 bit word is described in *Table 29*. A three bits diagnosis is provided for stepper motor driver, a two bit diagnosis for others drivers. VRS diagnosis is coded as '0' means No Fault, while '1' means Fault. Over temperature warning is coded as '0' means No Fault, while '1' means Fault.

The SPI default value is: all bits set to zero.

Table 29. Data out (DOUT) words content

DOUT0	DOUT1	DOUT2	DOUT3	DOUT4	DOUT5	DOUT6	DOUT7
INJ1 Diag0	INJ1 Diag1	INJ2 Diag0	INJ2 Diag1	O2H Diag0	O2H Diag1	RLY1 Diag0	RLY1 Diag1
DOUT8	**DOUT9**	**DOUT10**	**DOUT11**	**DOUT12**	**DOUT13**	**DOUT14**	**DOUT15**
RLY2 Diag0	RLY2 Diag1	RLY3 Diag0	RLY3 Diag1	LAMP Diag0	LAMP Diag1	TACH Diag0	TACH Diag1
DOUT16	**DOUT17**	**DOUT18**	**DOUT19**	**DOUT20**	**DOUT21**	**DOUT22**	**DOUT23**
VRS Diag	Thermal Warning	Brdg1 Diag0	Brdg1 Diag1	Brdg1 Diag2	Brdg2 Diag0	Brdg2 Diag1	Brdg2 Diag2

Data out structure

Table 30. Two bits diagnosis (normal drivers)

Bit 1	Bit 0	Fault
0	0	No Fault
0	1	Short to Ground (OFF)
1	0	Open Load (OFF)
1	1	Overcurrent (ON)

Table 31. Three bits diagnosis (bridge stage)

Bit 2	Bit 1	Bit 0	Fault
0	0	0	No Fault
0	0	1	Short to Ground (OFF)
1	0	1	Short to VBAT (OFF)
0	1	0	Open Load (OFF)
0	1	1	Overcurrent (ON)

4.5 Diagnosis

L9177 provides a full set of diagnosis; deglitch timings listed below are digital, generated from internal clock and their accuracy is guaranteed by scan patterns and clock measurement.

4.5.1 Voltage regulators thermal warning and shutdown

The 5V linear voltage regulator/tracking regulator is shut down when the thermal shutdown temperature is reached and also the regulator is in current limitation. The shutdown is filtered with Tdcg filter of 30 µs ±25 %. As soon as the over temperature disappear the regulator is switched on again. Over temperature flag without any latch is present via SPI.

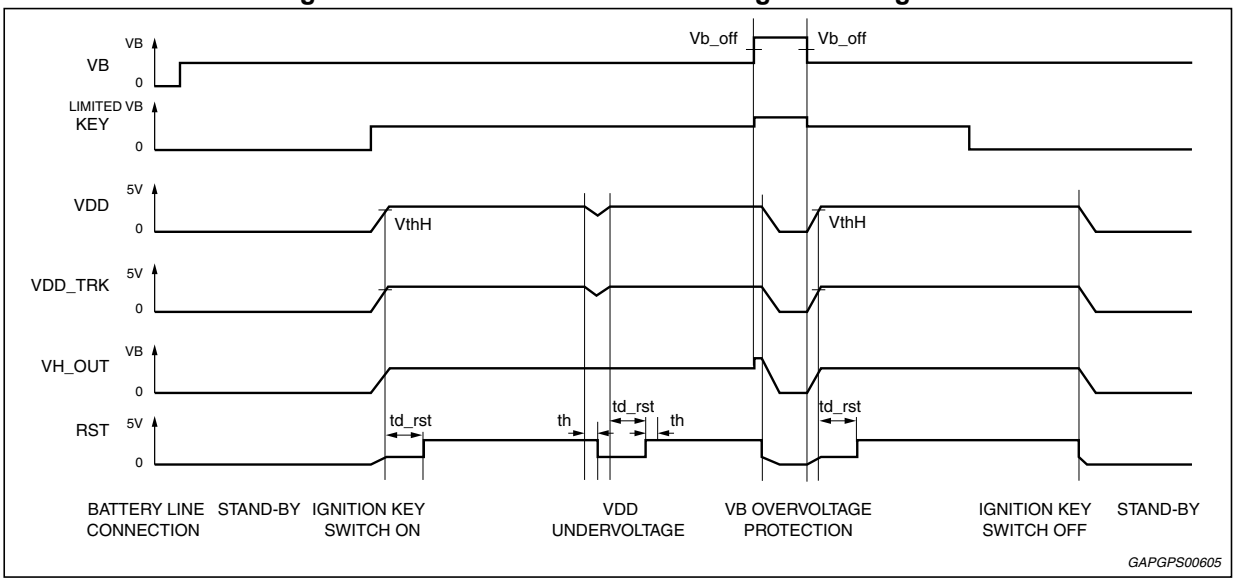
4.5.2 Overvoltage shut down

If the VB_off voltage is reached after Tdgc filtering time of 30 µs ±25 % the L9177 enters a safety state where main outputs are switched-off. Voltage regulators, all low side channels, stepper motor driver and KLINE are switched off and reset is asserted. As soon as the battery comes below VB_off minus VB_off_h the L9177 recover standard operation.

4.5.3 Undervoltage shut down

If the VB_UV voltage is reached after analog Tdgc 1 µs ±20 % filtering time the L9177 enters a safety state where main outputs are switched-off. Voltage regulators, all low side channels, stepper motor driver and KLINE are switched off. As soon as the battery rises above VB_UV plus the hysteresis the L9177 recovers normal operation.

Figure 21. L9177 under and over voltage time diagram



4.5.4 Low side on/off diagnosis (INJ, RLY's, TACH, O2H)

About low side channels OFF diagnosis, L9177 issues a masking filter Tmask after channel turning off (falling edge of driving command) to avoid false fault detecting due to output transition from low to high. Tmask is of 1 ms ±25 % for all channels except for the relays, for which Tmask is 3.5 ms ±25 %. Once masking time expires a deglitch filter Tdgc_noise of 3.6 µs ±40 % for noise immunity is activated. A fault longer than deglitch time is latched. Off state diagnostic fault can be overwritten by on state fault. Off state fault does not prevent the driver to switch on. The latched fault is cleared on request.

During on-phase if an over current fault occurs the drivers enters in current limitation condition for a digital filtering time Tdgc of 20 µs ±25 %,then it is switched OFF and the fault is latched. The channel is turned ON again by input command transition. The latched fault is cleared on request via SPI.

Over current fault has higher priority respect to OFF condition faults.

Figure 22. Low side driver diagnosis time diagram

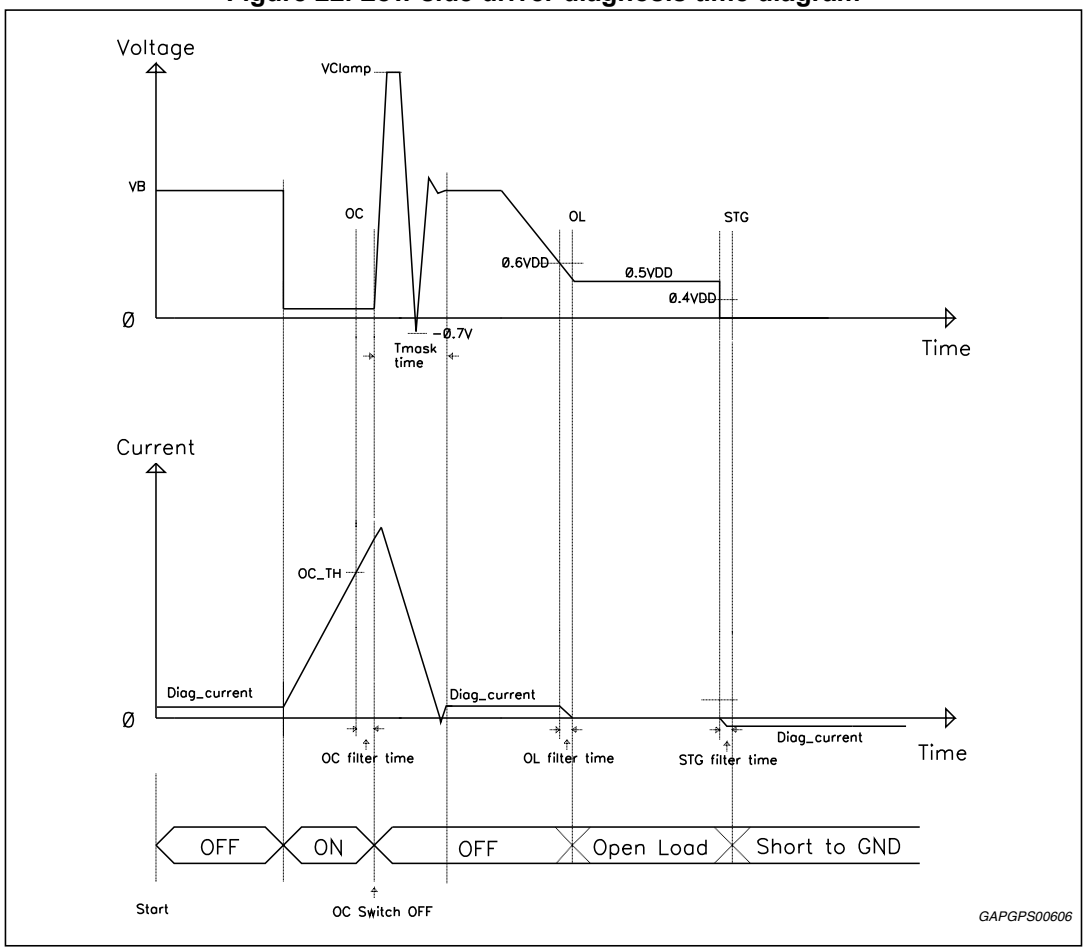
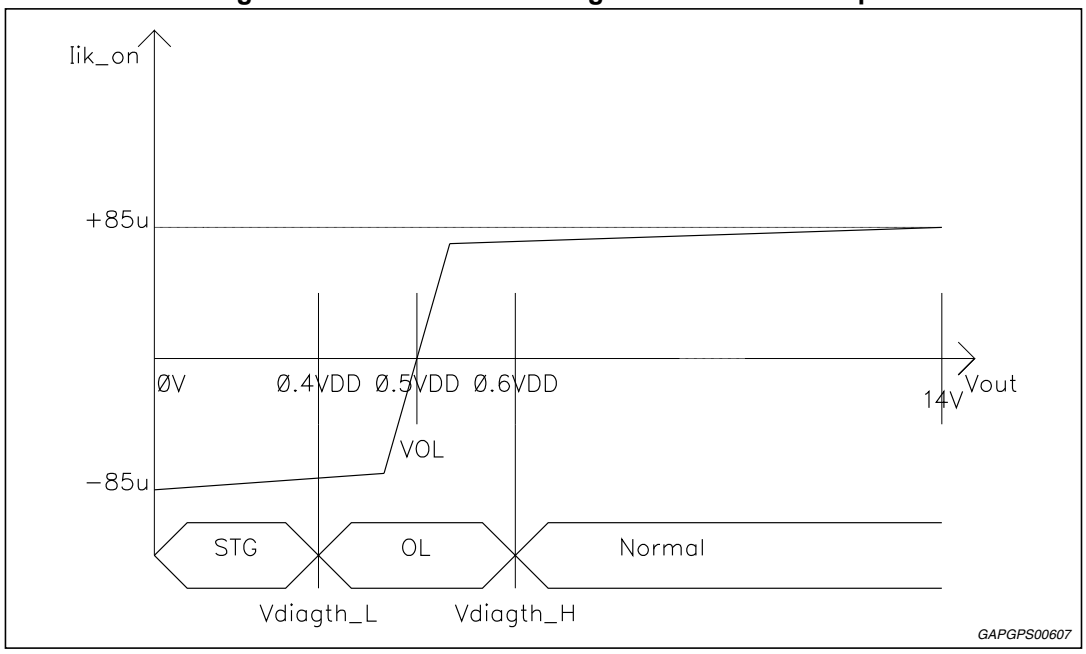


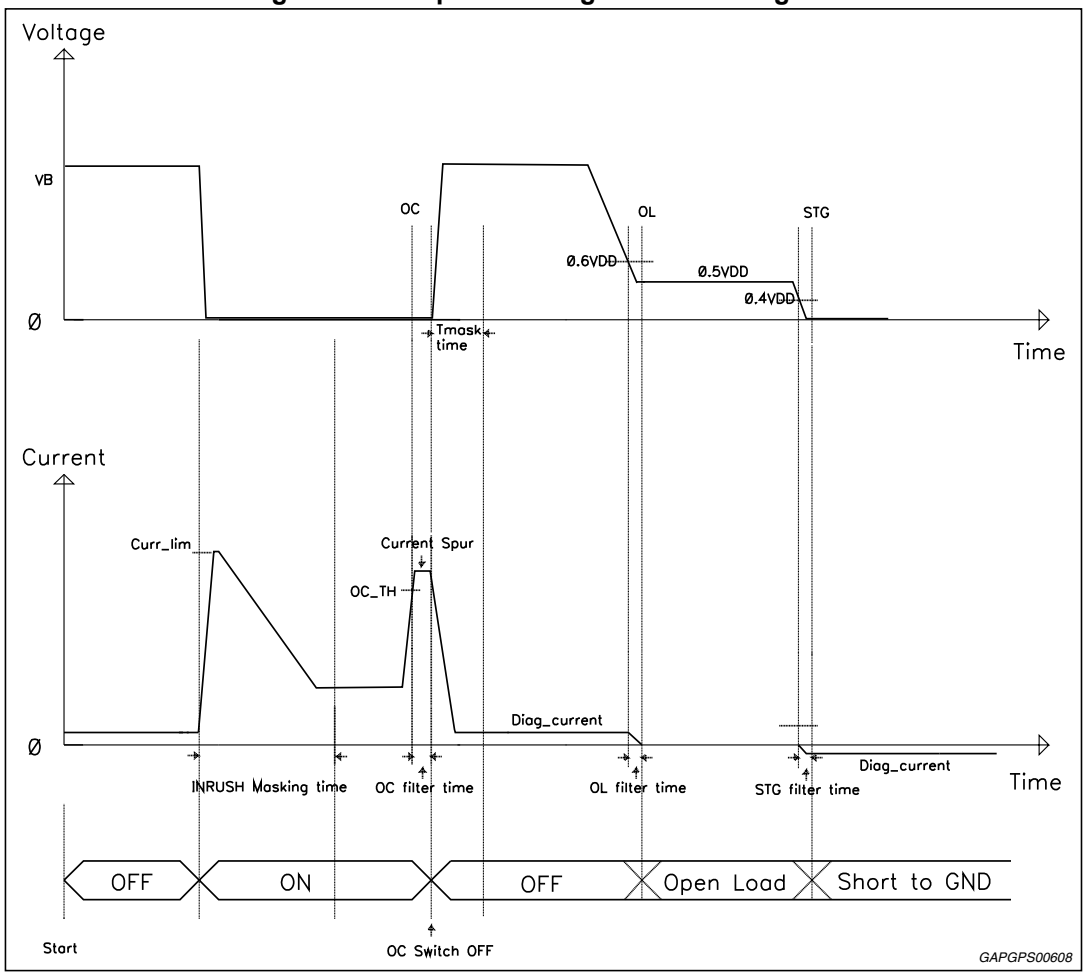
Figure 23. Low side driver diagnosis I-V relationship



4.5.5 Lamp driver on/off diagnosis

In OFF condition diagnosis is the same as Low side, with Tmask 3.5 ms ±25 % and Tdgc_noise 3.6 µs ± 40 %, while in ON condition initial Inrush current is masked for Tmask_rush of 45 ms ±25 % then, if an over current fault occurs the drivers enters in current limitation condition for a digital filtering time Tdgc of 20 µs ±25 %, then it is switched OFF and the fault is latched. The channel is turned ON again by input command transition. The latched fault is cleared on request via SPI. Over current fault has higher priority with respect to OFF condition faults.

Figure 24. Lamp driver diagnosis time diagram



4.5.6 Stepper motor driver off diagnosis (EN signal high and output in high impedance state)

In OFF condition Short to GND/Short to Vb or Open Load condition is continuously detected through a deglitch filter of 125 µs ±25 %, after Tmask masking time of 1 ms ±25 % to filter ON/ OFF transition. To avoid false diagnostic due to motor residual movement, the stepper has to be disabled at least 40 ms after the PWL signal has been disabled. A fault longer than deglitch time is latched. Off state diagnostic fault can be overwritten by on state fault. Off state fault does not prevent the stepper to switch on. The latched fault is cleared on request.

4.5.7 Stepper motor driver on diagnosis (EN signal Low and output driven by input commands)

In ON condition when over current fault is detected and validated after digital filtering time Tdgc of 20 µs ±25 %, the bridge is turned OFF and the fault is latched. The bridge is turned ON again by input command EN transition. The latched fault is cleared on request. Over current fault has higher priority with respect to OFF condition faults. Each Bridge has dedicated fault diagnosis detection coded by three bits.

Figure 25. Stepper motor driver diagnosis time diagram

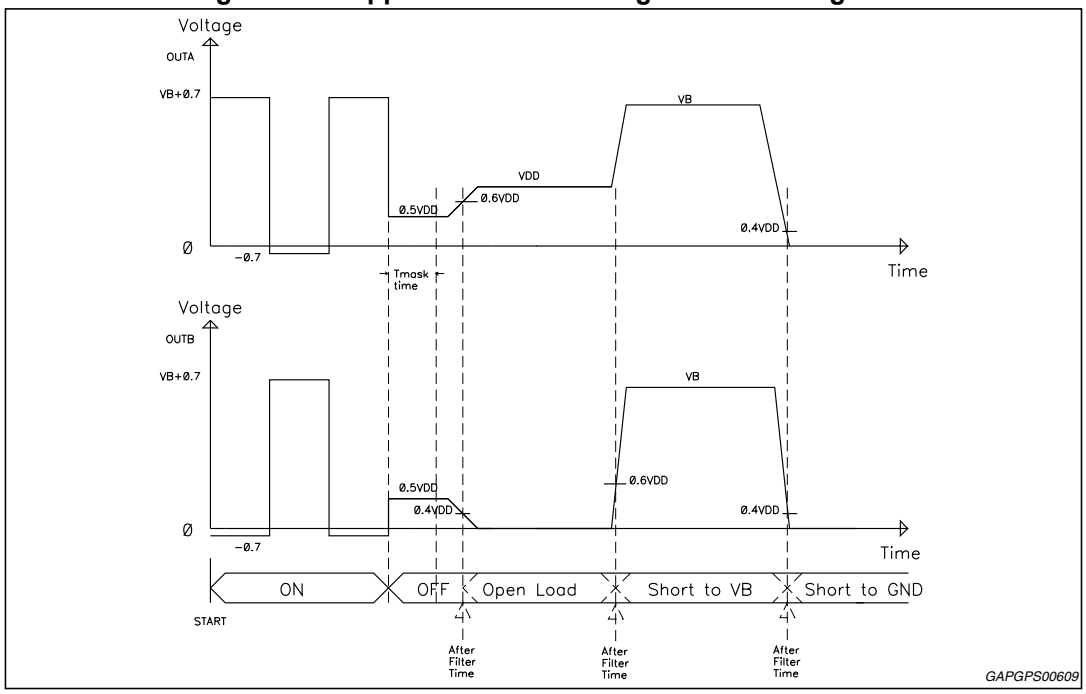
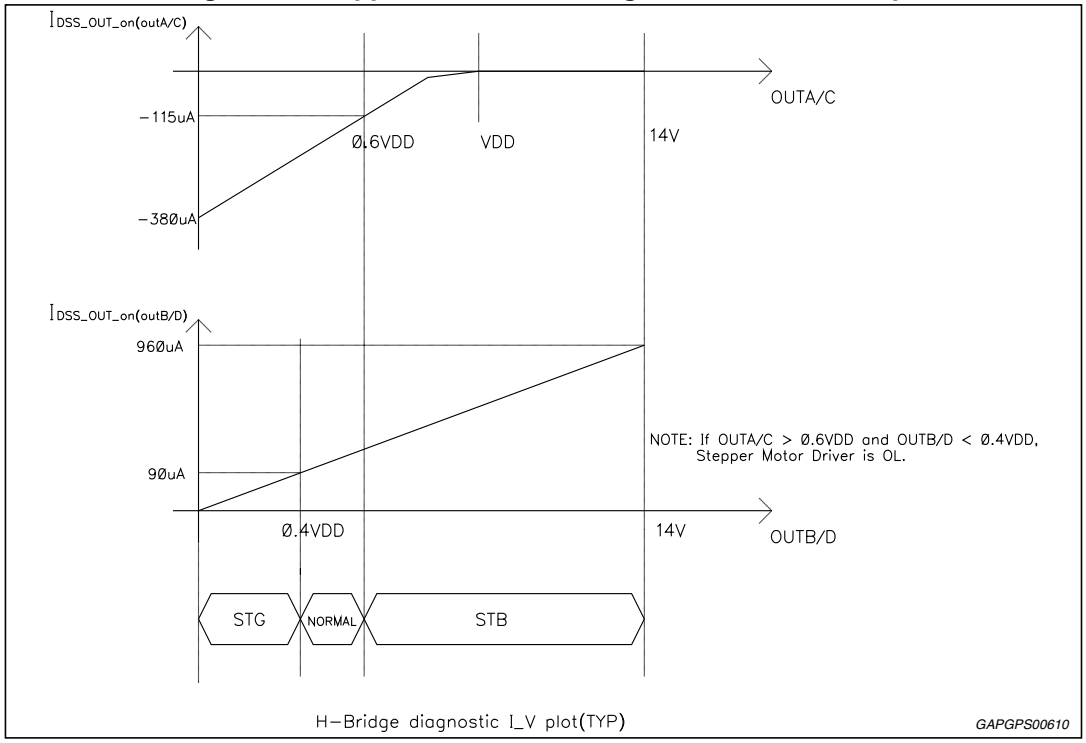


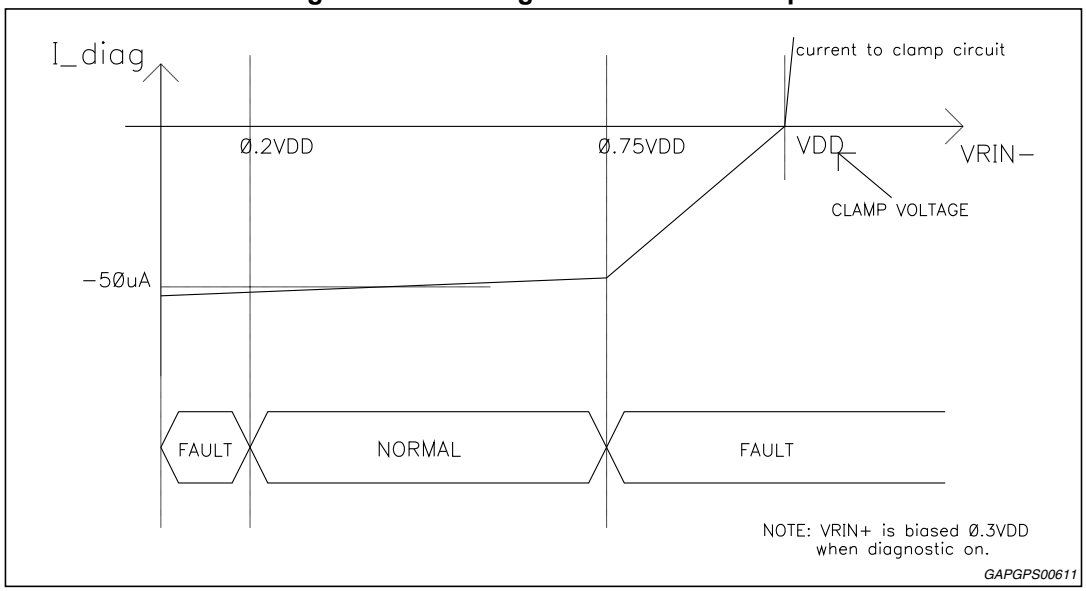
Figure 26. Stepper motor driver diagnosis I-V relationship



4.5.8 VRS diagnosis

VRS block enters diagnosis phase on request via SPI and then generates a Fault bit. If the fault exceeds the Tdgc filter time of 30 µs ±20 %, it is latched. The latched fault is cleared on request via SPI.

Figure 27. VRS diagnosis I-V relationship



4.6 VRS interface

4.6.1 Function characteristic

The flying wheel interface is an interface between the µP and the flying wheel sensor: it conditions signal coming from magnetic pick-up sensor or hall effect sensor and feeds the digital signal to microcontroller that extracts flying wheel rotational position, angular speed and acceleration.

Figure 28. VRS typical characteristics

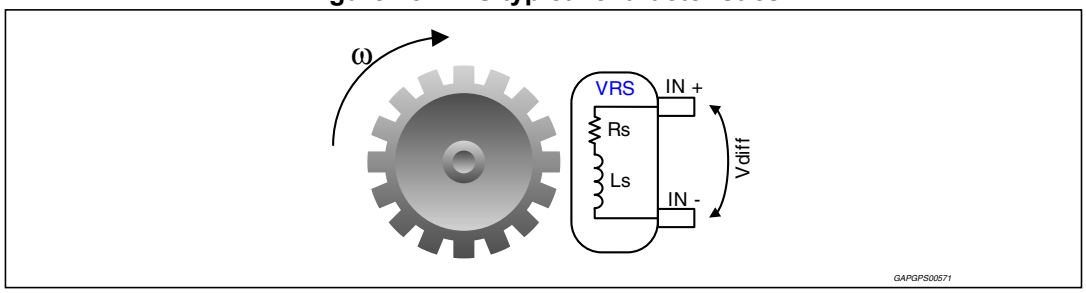
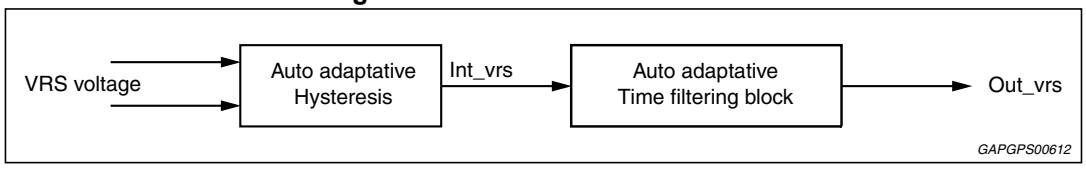


Figure 29. VRS interface structure



4.6.2 Auto-adaptative hysteresis

Input signals difference is obtained trough a full differential amplifier; its output, DV signal, is fed to peak detection circuit and then to A/D converter implemented with 4 voltage comparator (5 levels Pvi).Output of A/D is sent to Logic block (hysteresis selection *Table 33*) that implements correlation function between Peak voltage and hysteresis value; hysteresis value is used by square filtering circuit which conditions DV signal.

Figure 30. Auto-adaptive hysteresis block diagram

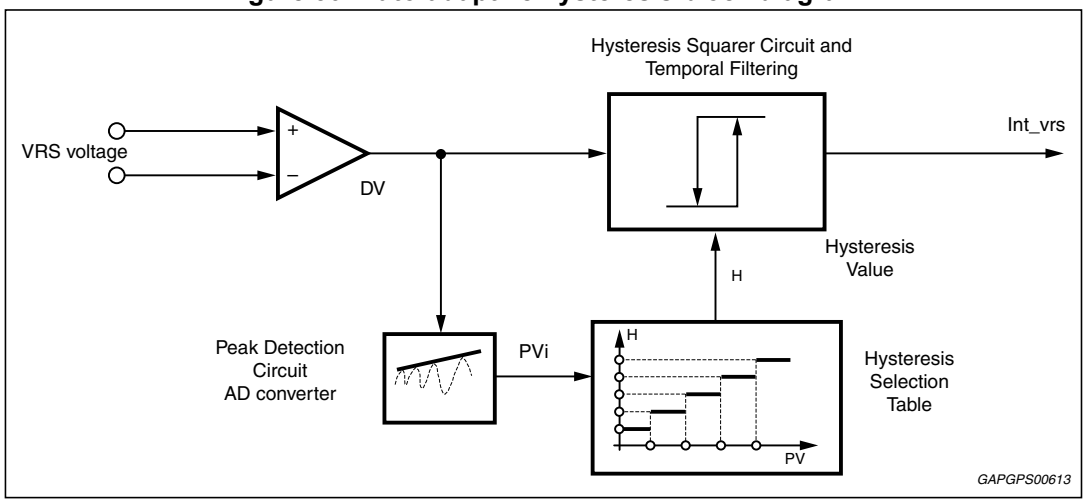
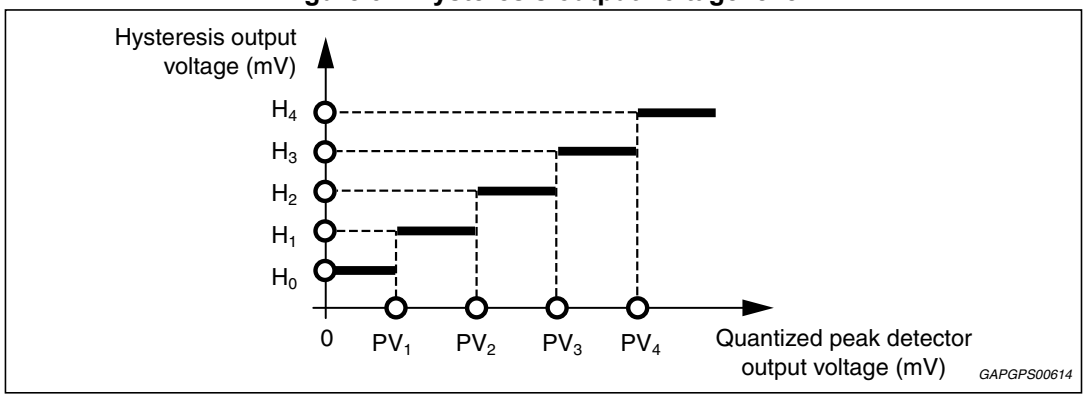


Figure 31. Hysteresis output voltage level



To the previous 5 levels PV = [0 PV1 PV2 PV3 PV4] correspond a set of 5 thresholds:

- H = [HO HIH2 H3 H4]

The advised values for the previous defined vectors are:

- PV = [0 PV1 PV2 PV3 PV4] = [0, 900, 1560, 2230, 2900] mV
- H = [H0 H1 H2 H3 H4] = [100, 200, 350, 650, 1000] mV

Table 32. Peak voltage detector precision

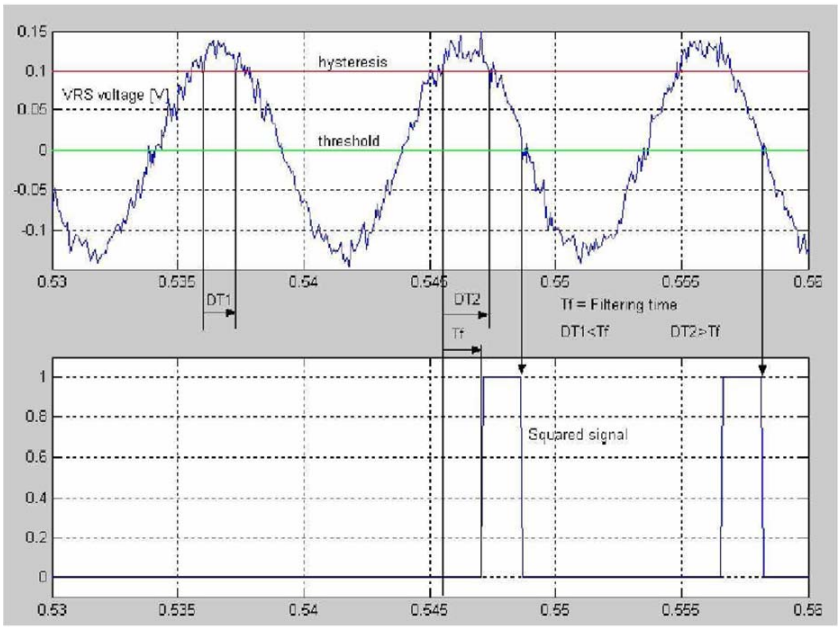
Pick voltage [PV]	Value			Unit
	Min.	Typ.	Max.	
PV1	850	900	950	mV
PV2	1452	1560	1638	mV
PV3	2118	2230	2341	mV
PV4	2755	2900	3045	mV

Table 33. Hysteresis threshold precision

Pick voltage [PV]	Value			Unit
	Min.	Typ.	Max.	
H0	70	100	130	mV
HV1	140	200	220	mV
HV2	250	347	390	mV
HV3	490	644	720	mV
HV4	730	1000	1120	mV

*Note: Hysteresis voltages are achieved injecting an hysteresis bias current on V_{RIN} ± external resistors (typ. 10 kΩ each, see Figure 38 application circuit). Resulting HV voltage is HV = I_hys*Rtyp. Changing the value of R would change in a linear mode the hysteresis value.*

Figure 32. Input-output behaviour of VRS interface



4.6.3 Auto-adaptative time filter

This characteristic is useful to set the best internal filter time in function of the input signal frequency.

Tfilter time is function of the duration of the previous period Tn according to following formula:

$$Tfilter(n+1) = 1/32*Tn \quad \text{if } Tn > Tfilter(n)$$

The filtering time purpose is filtering very short spikes.

The digital filtering time is applied to internal squared signal (int_vrs), obtained by voltage comparators.

The output of time filtering block is out_vrs signal.

The filtering time Tfilter is applied to int_vrs signal in two different way:

- Rising edge: if int_vrs high level lasts less than Tfilter out_vrs is not set to high level. In absence of any spikes during input signal rising edge out_vrs signal is expected with a delay of Tfilter time.
- Falling edge: the falling edge of int_vrs is not delayed through time filtering block: after falling edge for a time Tfilter any other transition on int_vrs signal is ignored

The initial value (Default) and maximum for Tfilter must be considered at RPM_min = 20 e.g. Tmax filter = 180 µs. The minimum available value is Tmin filter = 2.8 µs.

Figure 33. Auto-adaptative time filter behaviour 1

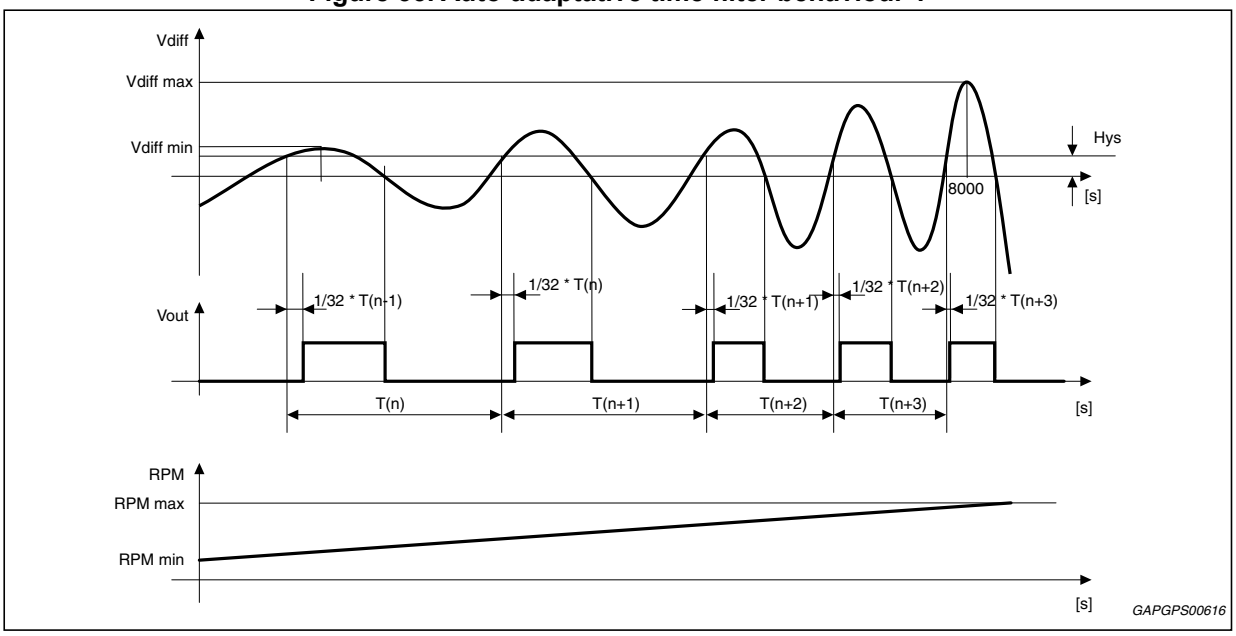
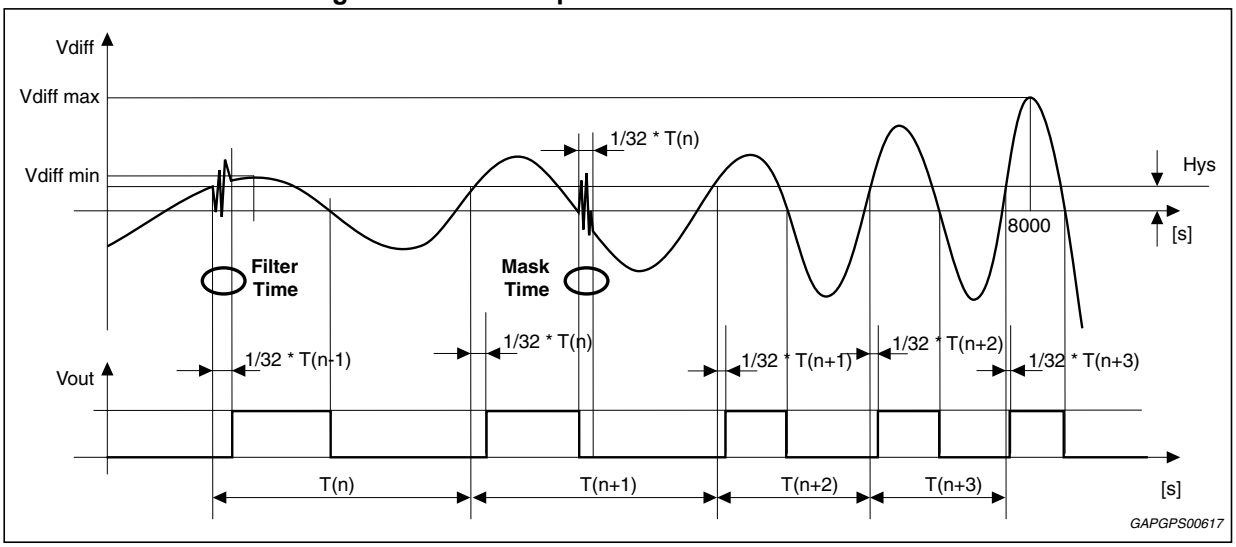


Figure 34. Auto-adaptative time filter behaviour 2



5 Low side drivers

Low side drivers have a voltage slew rate control during switch-on/off phase to reduce emissions.

The slew-rate control is achieved controlling the gate charging current and the behavior is described in *Figure 35* and *Figure 36*.

Figure 35. Low side drivers slew rate implementation

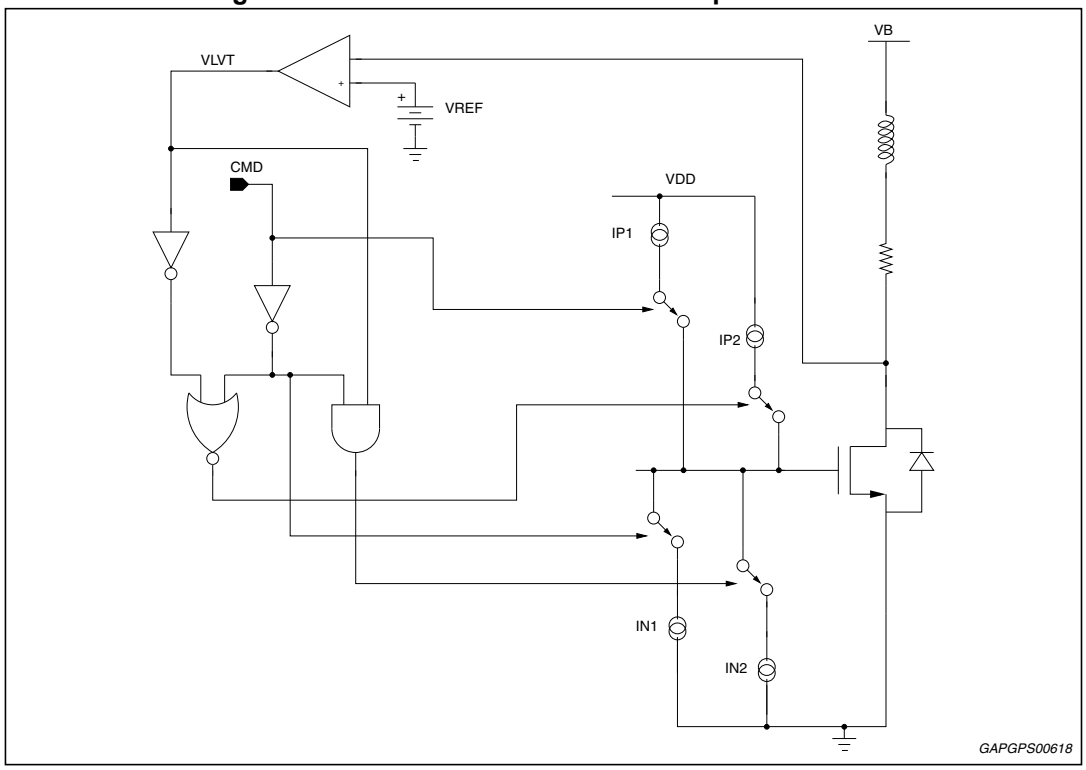
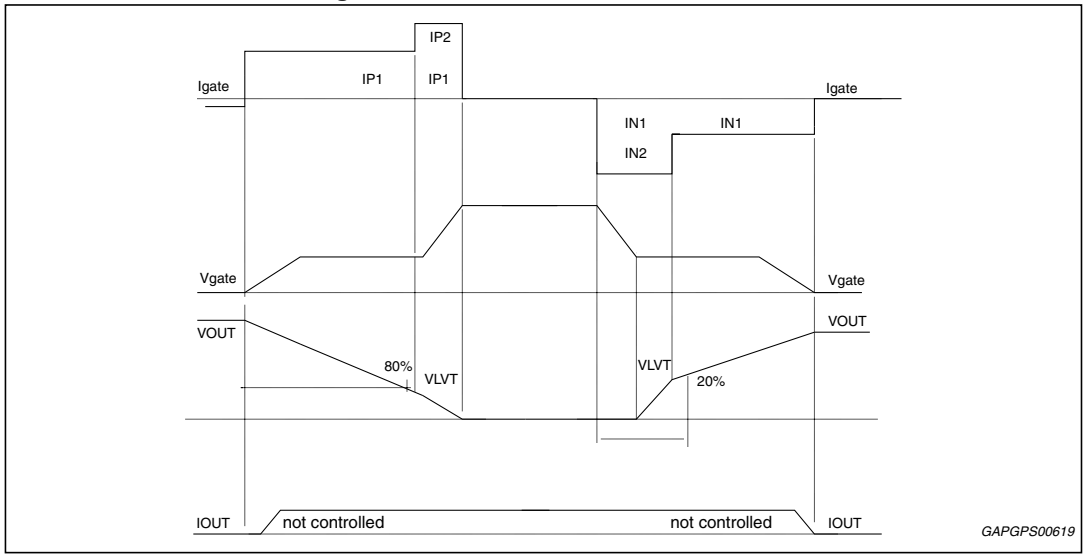


Figure 36. Low side drivers slew rate



At switch-on command the charging current is provided by current generator IP1 and is kept constant until the output voltage is decreased of roughly 80% of typical battery level. At this point the low side transistor is on and VLVT signal is set to logic 1 to connect IP2 current generator in parallel with IP1, completing the gate charge curve and providing maximum gate drive.

When the power transistor is switched-off the gate is discharged quickly using both IN1 and IN2 currents; as soon as the output voltage reaches roughly 20 % of the nominal battery voltage only IN1 is kept connected to complete the gate discharging.

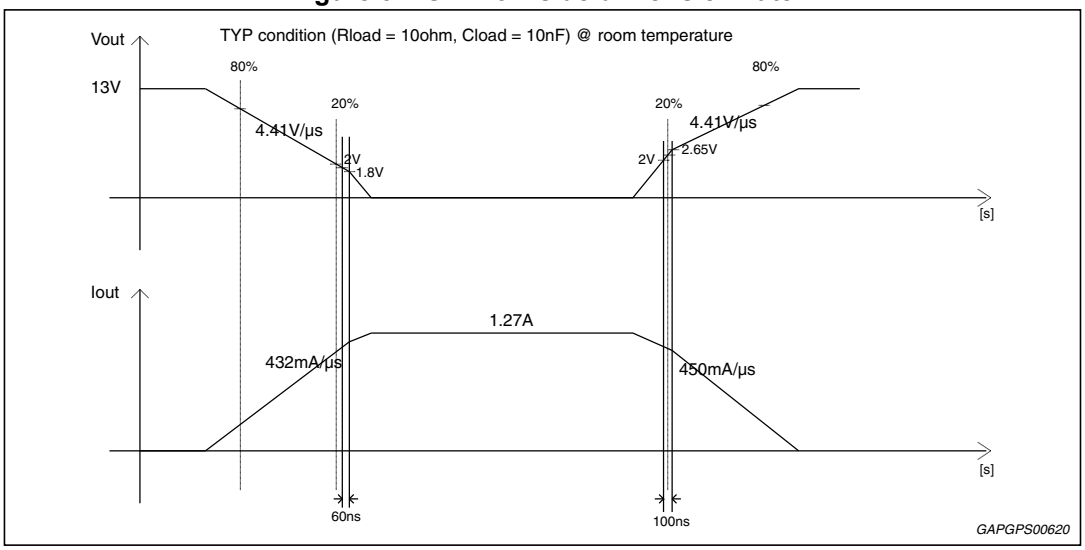
In *Table 34* the values for IPx and INx current generators are reported for each low side.

As an example *Figure 37* shows the resulting slew rate, in typical conditions, of O2H low side driver.

Table 34. Values for IPx and INx current generators for each low side

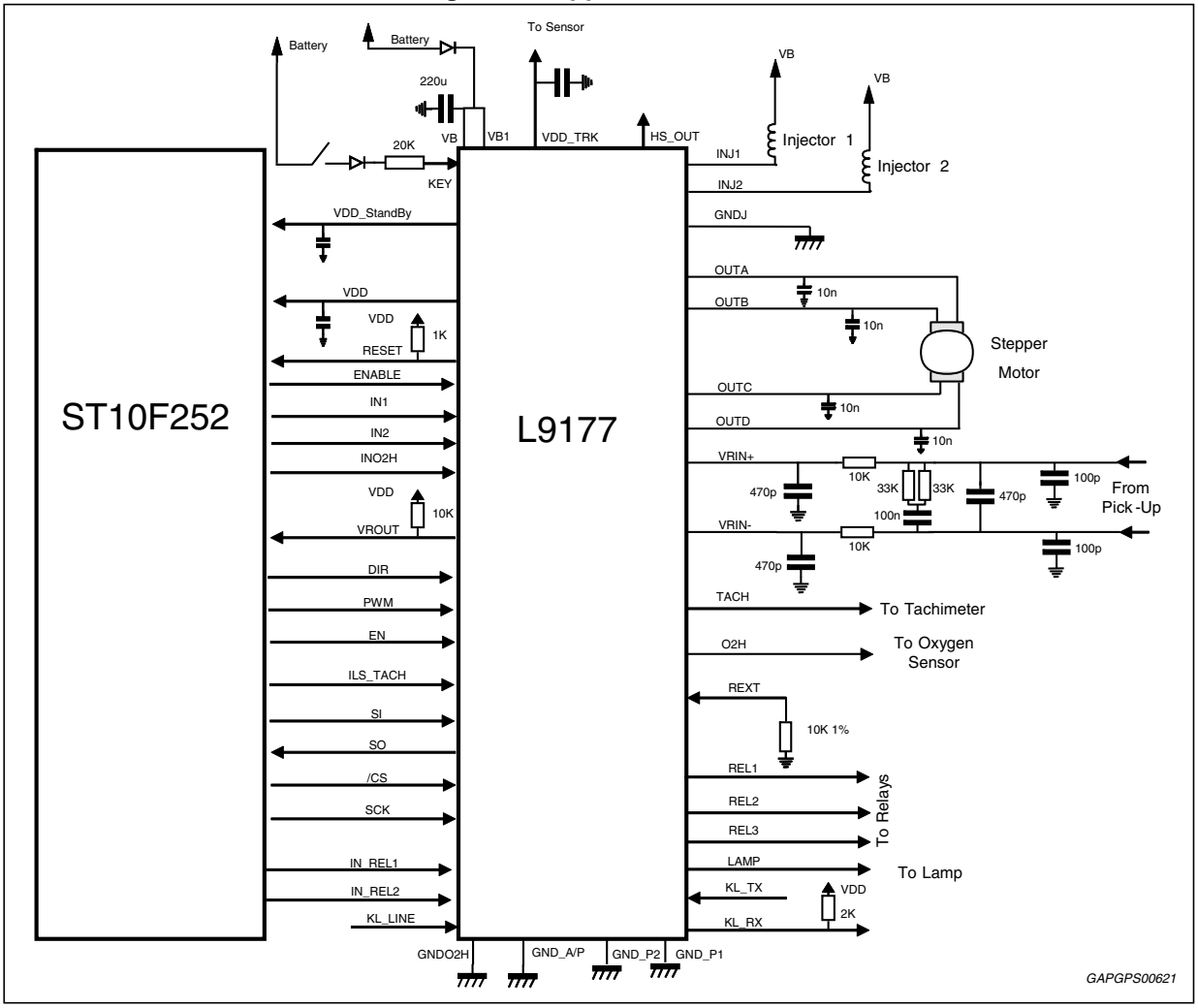
Low side	IP1	IP2	IN1	IN2	Unit
O2H	243	81	253	337	µA
INJ	174	23	180	124	µA
RLY's	78	0	80	120	µA
LAMP	78	0	62	119	µA
TACH	22	0	21	25	µA

Figure 37. O2H low side driver slew rate



6 Application circuit

Figure 38. Application circuit



6.1 Bill of material

Table 35. Bill of material

Block	Component	Name	Usage	Min	Typ	Max	Unit
Supply	Capacitor	C1VB_MAIN	Bulk capacitor		220		µF
	Diode	D1	Reverse polarization protection diode				
Key	Resistor	R_Key	Current limiting resistor		20		kΩ
Rext	Resistor	R_ext	Pull-up resistor		10 1%		kΩ
Reset	Resistor	R_reset	Pull-up resistor		1		kΩ
Vdd	Capacitor	C_Vdd value	Output capacitor (Ceramic or Tantalum)	4.7		60	µF
		C_Vdd ESR				1.5	Ω
Vdd_trk	Capacitor	C_Vtrk value	Output capacitor	2.2		100	µF
		C_Vtrk ESR		10		100	mΩ
Vdd_sby	Capacitor	C_Vdd_stby value	Output capacitor	1		10	µF
		C_Vdd_stby ESR				200	mΩ
VRS	Capacitor	C_VRS+_in	Filter Capacitor			100	pF
VRS	Capacitor	C_VRS-_in	Filter Capacitor			100	pF
VRS	Capacitor	C_VRS+_out	Filter Capacitor			470	pF
VRS	Capacitor	C_VRS-_out	Filter Capacitor			470	pF
VRS	Resistor	R_VRS+	Current limiting resistor			10	kΩ
VRS	Resistor	R_VRS-	Current limiting resistor			10	kΩ
VRS	Capacitor	CF_1	Filter Capacitor			470	pF
VRS	Capacitor	CF_2	Filter Capacitor			100	nF
VRS	Resistor	RF_1	Filter resistor			33	kΩ
VRS	Resistor	RF_2	Filter resistor			33	kΩ
VRS	Resistor	R_VROUT	Pull-up resistor		10		kΩ
K-Line	Resistor	RX pull-up	Pull-up resistor			2	kΩ
Stepper	Capacitor	OUTA	EMI filter capacitor			10	nF
Stepper	Capacitor	OUTB	EMI filter capacitor			10	nF
Stepper	Capacitor	OUTC	EMI filter capacitor			10	nF
Stepper	Capacitor	OUTD	EMI filter capacitor			10	nF

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

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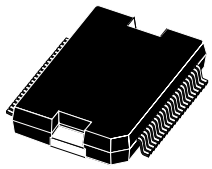
Figure 39. PowerSO46 mechanical data and package dimensions

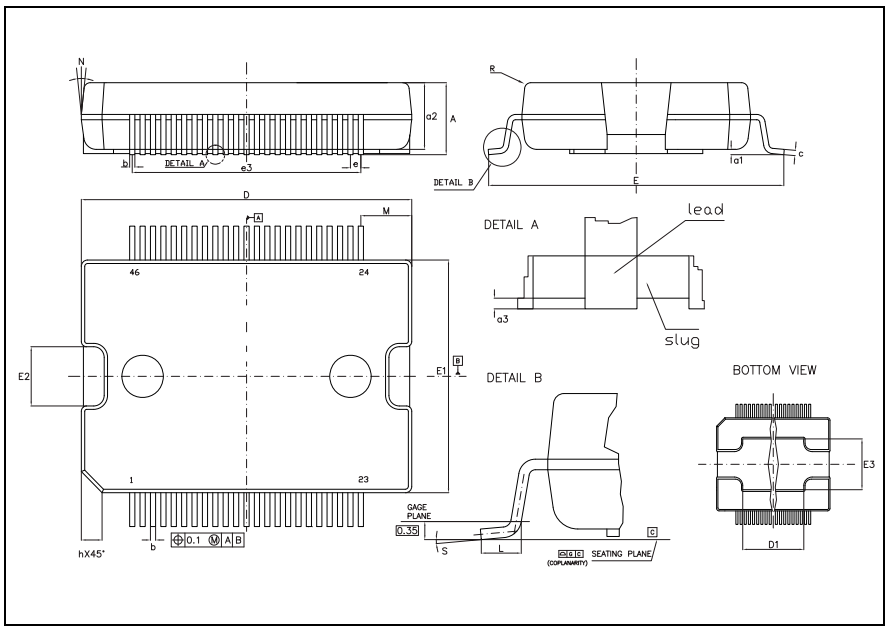
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.600			0.1417
a1	0.100		0.300	0.0039		0.0118
a2			3.300			0.1299
a3			0.100			0.0039
b	0.180		0.360	0.0071		0.0142
c	0.230		0.320	0.0091		0.0126
D	15.800		16.000	0.6220		0.6299
D1	9.400		9.800	0.3701		0.3858
E	13.900		14.500	0.5472		0.5709
E1	10.900		11.100	0.4291		0.4370
E2			2.900			0.1142
E3	5.800		6.200	0.2283		0.2441
e		0.500			0.0197	
e3		11.000			0.4331	
G			0.100			0.0039
H	15.500		15.900	0.6102		0.6260
h			1.100			0.0433
L	0.800		1.100	0.0315		0.0433
N			10°			10°
s			8°			8°

Note: “D and E1” do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006”)
- Critical dimensions are "a3", "E" and "G".

OUTLINE AND MECHANICAL DATA



PowerSO46



GAPGPS00622

8 Revision history

Table 36. Document revision history

Date	Revision	Changes
06-Nov-2013	1	Initial release.

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