

SN54ABT863, SN74ABT863 9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS201E – FEBRUARY 1991 – REVISED JULY 1998

- State-of-the-Art *EPIC-IIB™* BiCMOS Design Significantly Reduces Power Dissipation
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB) Packages, and Thin Shrink Small-Outline (PW), Ceramic Chip Carriers (FK), Plastic (NT), and Ceramic (JT) DIPs

description

The 'ABT863 devices are 9-bit transceivers designed for asynchronous communication between data buses. The control-function implementation allows for maximum flexibility in timing.

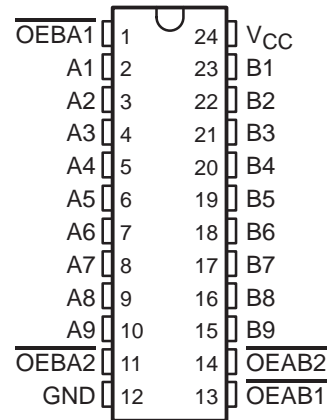
These devices allow noninverted data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic levels at the output-enable (\overline{OEAB} and \overline{OEBA}) inputs.

The outputs are in the high-impedance state during power up and power down. The outputs remain in the high-impedance state while the device is powered down.

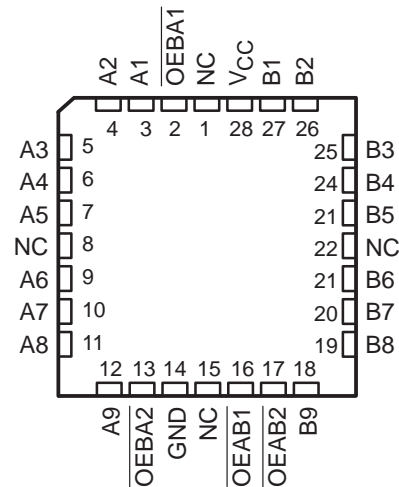
When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT863 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT863 is characterized for operation from -40°C to 85°C .

SN54ABT863 . . . JT PACKAGE
SN74ABT863 . . . DB, DW, NT, OR PW PACKAGE
(TOP VIEW)



SN54ABT863 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



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 **TEXAS
INSTRUMENTS**

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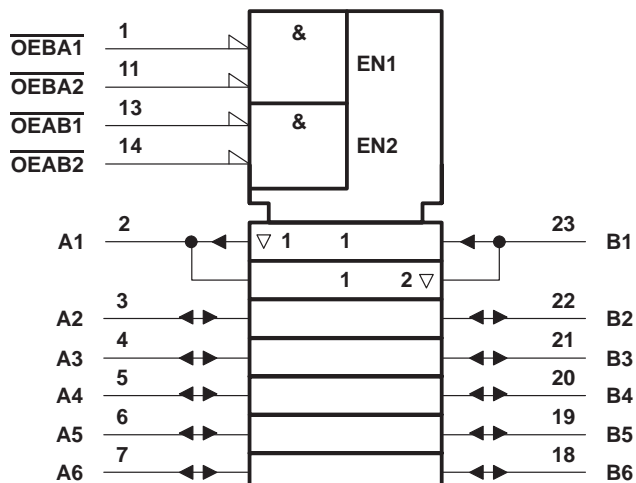
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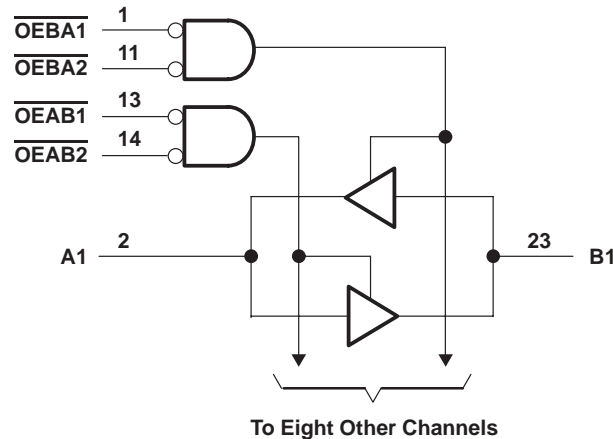
FUNCTION TABLE

| INPUTS | | | | OPERATION |
|--------|-------|-------|-------|---------------|
| OEAB1 | OEAB2 | OEBA1 | OEBA2 | |
| L | L | L | L | Latch A and B |
| L | L | H | X | A to B |
| L | L | X | H | |
| H | X | L | L | B to A |
| X | H | L | L | |
| H | X | H | X | Isolation |
| H | X | X | H | |
| X | H | X | H | |
| X | H | H | X | |

logic symbol†



logic diagram (positive logic)



Pin numbers shown are for the DB, DW, JT, NT, and PW packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|-----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (except I/O ports) (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high or power-off state, V_O | -0.5 V to 5.5 V |
| Current into any output in the low state, I_O : SN54ABT863 | 96 mA |
| SN74ABT863 | 128 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DB package | 104°C/W |
| DW package | 81°C/W |
| NT package | 67°C/W |
| PW package | 120°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

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recommended operating conditions (see Note 3)

| | | SN54ABT863 | | SN74ABT863 | | UNIT |
|---------------------|------------------------------------|-----------------|-----------------|------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V _{IH} | High-level input voltage | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V _I | Input voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | | -24 | | -32 | mA |
| I _{OL} | Low-level output current | | 48 | | 64 | mA |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | | | 5 | ns/V |
| Δt/ΔV _{CC} | Power-up ramp rate | 200 | | 200 | | μs/V |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | T _A = 25°C | | | SN54ABT863 | | SN74ABT863 | | UNIT |
|--------------------------|--|--|-------------------------|------|------|------------|------|------------|------|------|
| | | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| V _{IK} | V _{CC} = 4.5 V, I _I = -18 mA | | -1.2 | | | -1.2 | | -1.2 | | V |
| V _{OH} | V _{CC} = 4.5 V, I _{OH} = -3 mA | | 2.5 | | | 2.5 | | 2.5 | | V |
| | V _{CC} = 5 V, I _{OH} = -3 mA | | 3 | | | 3 | | 3 | | |
| | V _{CC} = 4.5 V | I _{OH} = -24 mA | 2 | | | 2 | | | | |
| I _{OH} = -32 mA | | 2* | | | | | 2 | | | |
| V _{OL} | V _{CC} = 4.5 V | | I _{OL} = 48 mA | | | 0.55 | | | | V |
| | | | I _{OL} = 64 mA | | | 0.55* | | 0.55 | | |
| V _{hys} | | | 100 | | | | | | | mV |
| I _I | Control inputs | V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND | ±1 | | | ±1 | | ±1 | | µA |
| | A or B ports | V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND | ±20 | | | ±20 | | ±20 | | |
| I _{OZPU} | V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, OE = * don't care | | ±50 | | | ±50** | | ±50 | | µA |
| I _{OZPD} | V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, OE = * don't care | | ±50 | | | ±50** | | ±50 | | µA |
| I _{OZH} ‡ | V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, OE ≥ 2 V | | 10 | | | 10 | | 10 | | µA |
| I _{OZL} ‡ | V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, OE ≥ 2 V | | -10 | | | -10 | | -10 | | µA |
| I _{off} | V _{CC} = 0, V _I or V _O ≤ 4.5 V | | ±100* | | | | | ±100 | | µA |
| I _{CEX} | V _{CC} = 5.5 V, V _O = 5.5 V | Outputs high | 50 | | | 50 | | 50 | | µA |
| I _O § | V _{CC} = 5.5 V, V _O = 2.5 V | | -50 | -100 | -225 | -50 | -225 | -50 | -225 | mA |
| I _{CC} | A or B ports | V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND | Outputs high | | 1 | 250 | 250 | 250 | 250 | µA |
| | | | Outputs low | | 24 | 30 | 38 | 38 | 38 | mA |
| | | | Outputs disabled | | 0.5 | 250 | 250 | 250 | 250 | µA |
| ΔI _{CC} ¶ | Data inputs | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | Outputs enabled | | 1.5 | | 1.5 | | mA | |
| | | | Outputs disabled | | 0.05 | | 0.05 | | | |
| | Control inputs | V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND | 1.5 | | 1.5 | | 1.5 | | | |
| C _i | Control inputs | V _I = 2.5 V or 0.5 V | 4 | | | | | | | pF |
| C _{io} | A or B ports | V _O = 2.5 V or 0.5 V | 7 | | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.

** On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V_{CC} = 5 V.

‡ The parameters I_{OZH} and I_{OZL} include the input leakage current.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

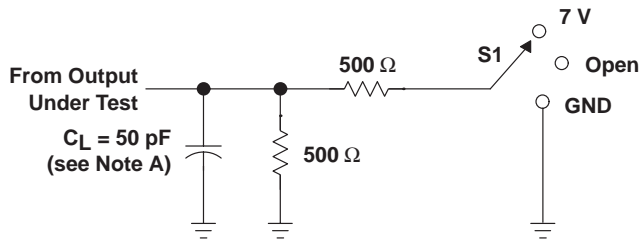
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 5$ V, $T_A = 25^\circ$ C | | | SN54ABT863 | | SN74ABT863 | | UNIT |
|-----------|--|-------------|---------------------------------------|-----|-----|------------|-----|------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A or B | B or A | 1 | 2.6 | 4.1 | 1 | 7 | 1 | 5.7 | ns |
| t_{PHL} | | | 1 | 2.3 | 3.3 | 1 | 3.9 | 1 | 3.9 | |
| t_{PZH} | \overline{OEAB} or \overline{OEBA} | B or A | 1 | 3.2 | 4.3 | 1 | 5.4 | 1 | 5.5 | ns |
| t_{PZL} | | | 1 | 3.3 | 4.4 | 1 | 5.5 | 1 | 5.4 | |
| t_{PHZ} | \overline{OEAB} or \overline{OEBA} | B or A | 2.5 | 4.8 | 6 | 2.5 | 6.8 | 2.5 | 6.7 | ns |
| t_{PLZ} | | | 1.5 | 4.4 | 5.9 | 1.5 | 7.8 | 1.5 | 6.9 | |

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PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |

LOAD CIRCUIT

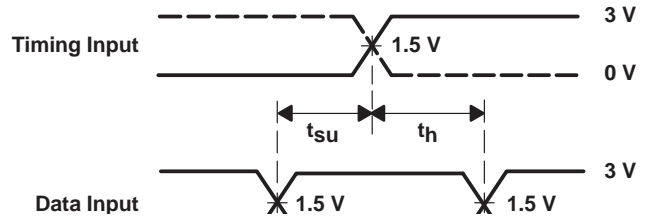
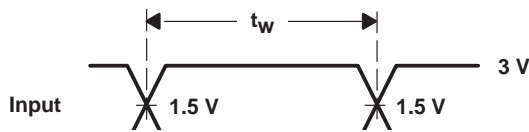


Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| SN74ABT863DBLE | OBSOLETE | SSOP | DB | 24 | | TBD | Call TI | Call TI |
| SN74ABT863DBR | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT863DBRE4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT863DBRG4 | ACTIVE | SSOP | DB | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT863DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT863DWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT863DWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT863DWR | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT863DWRE4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT863DWRG4 | ACTIVE | SOIC | DW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT863DBR | SSOP | DB | 24 | 2000 | 330.0 | 16.4 | 8.2 | 8.8 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74ABT863DWR | SOIC | DW | 24 | 2000 | 330.0 | 24.4 | 10.75 | 15.7 | 2.7 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74ABT863DBR | SSOP | DB | 24 | 2000 | 346.0 | 346.0 | 33.0 |
| SN74ABT863DWR | SOIC | DW | 24 | 2000 | 346.0 | 346.0 | 41.0 |

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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