200-mA PSM Step Down Converter with Bypass Capability

FEATURES

- 2.7-V to 6-V Input Voltage Range
- 1.2-V to 5-V Output
- Efficiency of 95% for V_{OUT} of 3.3 V @ 200-mA Load
- Selectable Pulse Skipping Modulation (PSM) or Bypass Mode (BP) Operation
- 150-mΩ Bypass Switch for 800-mA Loads
- Integrated MOSFET with Low External Part Count
- Shutdown Current <1 μA
- Integrated UVLO and Power on Reset
- Integrated Soft-Start
- Over Temperature Protection
- MLP33-10 or MSOP-10 Packages

APPLICATIONS

- Cellular Phones, Cordless Phones
- Computer Point of Use, Notebook
- PDAs
- Battery Powered Devices
- MP3 Players

DESCRIPTION

The Si9177 is a dual-mode power adjustable output converter. When it is set to PSM mode, the Si9177 operates as a pulse-skipping-modulation controlled step-down (buck) converter with an output voltage range of 1.2 V to 5 V. It has an integrated MOSFET, capable of supplying 200-mA load current with a 1.5-μH inductor. The output voltage is adjusted by a resistive divider on the F_B pin. The typical conversion efficiency is above 90%. A logic HIGH at the BP/$\overline{PSM}$ pin puts Si9177 in bypass mode. The main PMOS buck switch is forced

to turn on at 100% duty cycle, overriding the F_B signal. The voltage differential between input and output is the resistive voltage drop on the internal 150-mΩ PMOS and the inductor. The Si9177 delivers 800-mA load in bypass mode.

The Si9177 is available in the space saving MLP33-10 and MSOP-10 packages. In order to satisfy the stringent ambient temperature requirements, the Si9177 is rated to handle the industrial temperature range of -25°C to 85°C.

TYPICAL APPLICATION CIRCUIT

Si9177

Vishay Siliconix

New Product

VISHAY
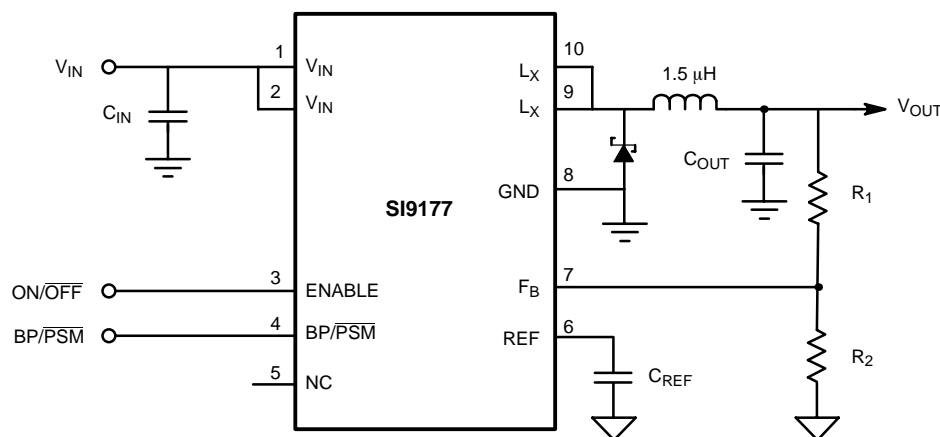
ABSOLUTE MAXIMUM RATINGS (T$_A$ = 25°C)

V_{IN} . . . . 6.5 V
BP/$\overline{PSM}$, ENABLE, F$_B$, L$_X$ . . . . -0.3 V to V$_{IN}$ + 0.3 V
Storage Temperature . . . . -55 to 150°C
Operating Junction Temperature . . . . 150°C
Power Dissipation (Package)[a.]
MLP33-10[b.] . . . . 481 mW
MSOP-10[c] . . . . 915 mW

Thermal Impedance (Θ_{JA})
MLP33-10 . . . . 135°C/W
MSOP-10 . . . . 71°C/W

Notes
a. Device mounted with all leads soldered or welded to PC board.
b. Derate 7.4 mW/ °C above 25°C.
c. Derate 14 mW/ °C above 25°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

V_{IN} . . . . 2.7 V to 6 V
C_{IN} . . . . 10 µF
C_{OUT} . . . . 10 µF

Inductor . . . . 1.5 µH
C_{REF} . . . . Open
Operating Temperature Range . . . . -25 to 85   °C
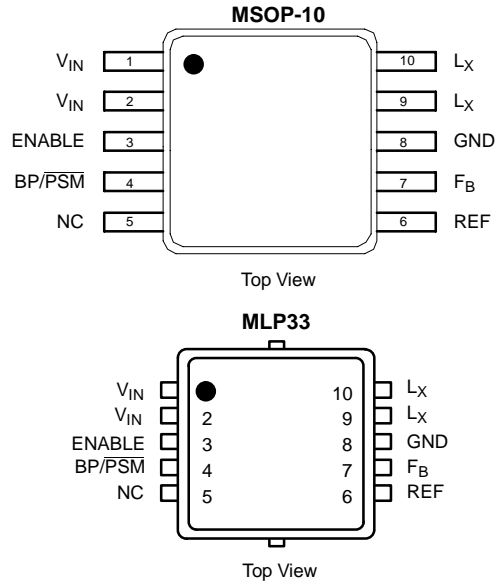
SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Specified -40°C to 85°C, V$_{IN}$ = V$_{DD}$, C$_{IN}$ = 10 µF C$_{OUT}$ = 4.7 µF, L = 2.2 µH, 2.6 V $\leq$ V$_{IN}$ $\leq$ 5.5 V R$_1$ = 11.3 kΩ, R$_2$ = 20 kΩ	Limits			Unit
			Min[a]	Typ[b]	Max[a]	
Converter Operation						
Input Voltage	V$_{IN}$		2.7		6	V
Maximum Bypass Mode Current	I$_{OUT}$		800			mA
Maximum PSM Mode Current			200			
MOSFET On-resistance	r$_{DS(on)}$	V$_{IN}$ $\geq$ 3.3 V		150	300	mΩ
Power Supply Rejection	PSRR			60		dB
Feedback Voltage	V$_{FB}$	I$_{REF}$ = 0	1.175	1.215	1.255	V
		I$_{REF}$ = 0, T$_A$ = 25°C	1.195	1.215	1.235	
Start-Up						
Start-Up Delay Time	t$_{DELAY}$	C$_{REF}$ = 0.1 µF, See Figure 1		5		ms
Soft Start Time	t$_{ss}$	See Figure 1		100		µs
ENABLE, BP/$\overline{PSM}$						
Logic High	V$_{IH}$		1.5			V
Logic Low	V$_{IL}$				0.4	
Input Current	I$_{IH}$	ENABLE, BP/$\overline{PSM}$ = V$_{IN}$		1		µA
	I$_{IL}$	ENABLE, BP/$\overline{PSM}$ = GND		1		
Protection						
Under Voltage Lockout	V$_{UVLO}$		2.2	2.35	2.5	V
Under Voltage Lockout Hysteresis	V$_{HUVLO}$			0.1		
Thermal Shutdown	T$_{SD}$	Temperature rising		165		°C
Thermal Shutdown Hysteresis	T$_{HSD}$	V$_{IN}$ = 3.3 V		25		
Supply Current						
BP Mode	I$_{IN}$	V$_{IN}$ = 3.3 V		75	110	µA
PSM Mode				190	250	
Shutdown		V$_{IN}$ = 3.3 V, ENABLE = 0 V			1	

Notes
a. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
b. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
c. Guaranteed by design and characterization, not subject to production testing.

PIN CONFIGURATION

MSOP-10

V_{IN}	1	10 L_X
V_{IN}	2	9 L_X
ENABLE	3	8 GND
BP/$\overline{PSM}$	4	7 F_B
NC	5	6 REF

Top View

MLP33

V_{IN}		10 L_X
V_{IN}	2	9 L_X
ENABLE	3	8 GND
BP/$\overline{PSM}$	4	7 F_B
NC	5	6 REF

Top View

ORDERING INFORMATION

Part Number	Temperature Range	Package
Si9177BM-TI	-25°C to 85°C	Tape and Reel
Si9177BH-TI		

Eval Kit	Temperature Range	Board Type
Si9177DB	-25°C to 85°C	Surface Mount

PIN DESCRIPTION

Pin No.	Name	Function
1, 2	V_{IN}	Input voltage source for buck converter, MOSFET driver, and IC control circuits.
3	ENABLE	Logic high enables the converter. Logic low shuts down the IC and decreases current consumed to <1 μA.
4	BP/$\overline{PSM}$	Logic high = Bypass mode, logic low = PSM mode.
5	NC	No Connection
6	REF	1.215-V reference.
7	F_B	Direct output voltage sense feedback
8	GND	IC ground
9, 10	L_X	Inductor connection node

TIMING WAVEFORMS

90%

V_{OUT}

10%

V_{IN}

t_{DELAY} = Start-Up Delay Time
t_{SS} = Soft-Start Time

t_{DELAY} t_{SS}
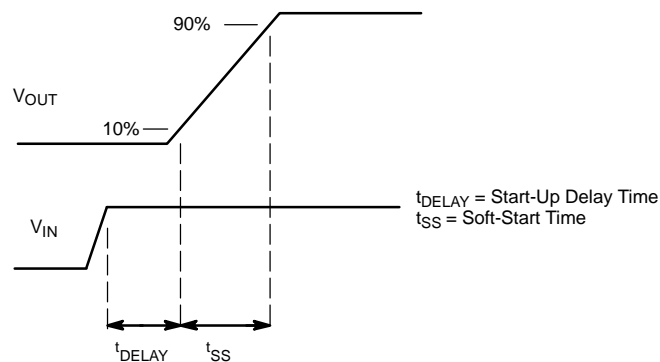
FIGURE 1. Soft-Start Timing

Vishay Siliconix　　　　　*New Product*

VISHAY

FUNCTIONAL BLOCK DIAGRAM
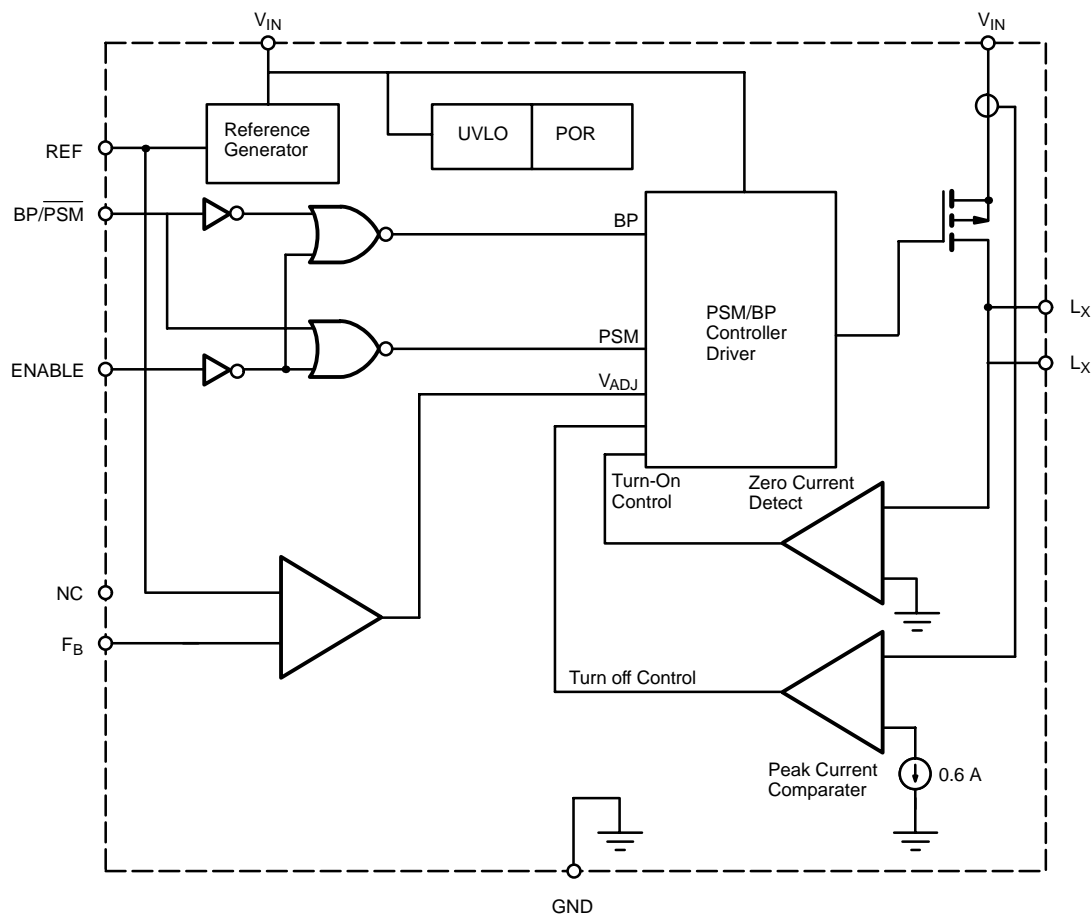
APPLICATION CIRCUIT
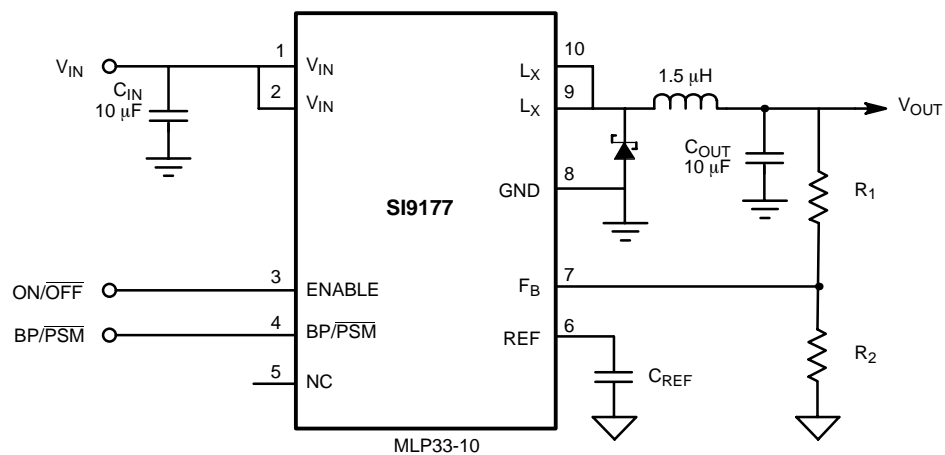
DETAIL OPERATIONAL DESCRIPTION

Start-Up

When voltage is first applied to the V_{IN} pin, the UVLO circuitry prevents the internal p-channel MOSFET from turning on. Once the V_{IN} voltage exceeds the UVLO threshold of 2.4 V, and with no other shutdown condition detected, an internal power-on-reset timer is activated to delay the start of switching if the BP/$\overline{PSM}$ pin is held a logic LOW level. The amount of delay is set by the capacitor C_{REF} on the REF pin and the peak current in the inductor is limited to 600 mA. If the BP/$\overline{PSM}$ pin has a logic HIGH applied, then Bypass Mode soft-start is achieved by gradually turning on the p-channel MOSFET in 40 µs insuring that the output voltage rises smoothly.

Pulse Skipping Mode

Si9177 is designed to operate with light loads. When the BP/$\overline{PSM}$ pin is connected to logic LOW level, the Si9177 operates in pulse-skipping mode. PSM enhances efficiency in light load conditions when compared to fixed frequency PWM mode because switch conduction losses, gate charge and switching losses are reduced. By delivering energy to the load only when needed, the p-channel MOSFET gate capacitance is charged and discharged less frequently and MOSFET conduction loss is minimized thereby reducing total losses and increasing converter efficiency. In PSM, the switching frequency, f_{SW}, increases as and decreases as the load current increases and decreases. The typical conversion efficiency in PSM mode is 90%.

By operating as a constant on-time converter, the Si9177 achieves PSM operation. The p-channel MOSFET switching transistor is turned on to deliver energy to the load. The switch remains on for the minimum on-time or until the inductor current reaches 600 mA. If the applied on-time is sufficient to increase the output voltage above the in-regulation set point (F_B pin voltage is greater than V_{FB}), the p-channel MOSFET turns off for a minimum off-time and continues to apply constant on-time pulses to insure regulation is maintained. If the on-time of the p-channel switch causes the output voltage to rise above the set point, the converter turns off and remains off until the voltage on F_B decreases below V_{FB}.

The on-time and minimum off-time are set internally to minimize ripple voltage at the maximum load current. The Si9177 has internal compensation reducing the number of required components and is designed for an inductor value of 1.5 µH and an output capacitor value of 10 µF.

BYPASS Mode

Si9177 can also operate in BYPASS mode to handle heavy load currents or to provide the maximum output voltage to the load. This mode is enabled by setting the BP/PSM pin to a logic HIGH. In this mode the IC ignores the feedback signal at the F_B pin, forcing the internal p-channel MOSFET to turn on continuously. The input-to-output voltage differential is reduced to the voltage drop across the 150-mΩ MOSFET and the inductor. Si9177 can bypass 800 mA at 95% typical efficiency or provide nearly the entire input voltage to the load. Whenever the converter enters BYPASS mode, the p-channel MOSFET turns on gradually within 40 µs to reduce surge current to the input capacitor.

Shutdown

Si9177 is designed to conserve as much battery life as possible by decreasing current consumption during normal operation, as well as the shutdown mode. With logic LOW level on the ENABLE pin, the current consumption of the IC is decreases to less than 1 µA by shutting off all circuits. A logic HIGH enables the controller, allowing start up as described in the "Start-Up" section above.

Reference and Power-On-Reset Timer

The reference voltage of Si9177 is set to 1.215 V. It is internally connected to the non-inverting input of the error amplifier. The power on reset delay time is set by the capacitance on the REF pin and can be determined from the following relationship:

$$t_{PORDELAY} = 4 \times 10^4 \times C_{REF}$$

Output Voltage

The Si9177 is designed with an adjustable output voltage, V_{OUT}, which is set by resistors R_1 and R_2, and the feedback voltage, V_{FB}. V_{OUT} is defined according to the following relationship:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB}$$

where V_{FB} is 1.215 V.

The values of R_1 and R_2 should be kept between 5 kΩ and 100 kΩ.

Power Switches

The p-channel MOSFET switch is integrated in Si9177 for optimum performance and minimum overall converter size. This MOSFET is designed to minimize the gate charge loss as well as the conduction loss. The typical on-resistance is 150 mΩ with a minimum input voltage of 3.3 V.

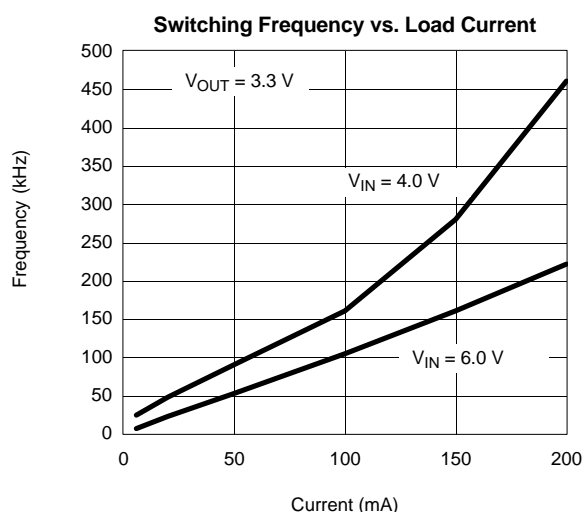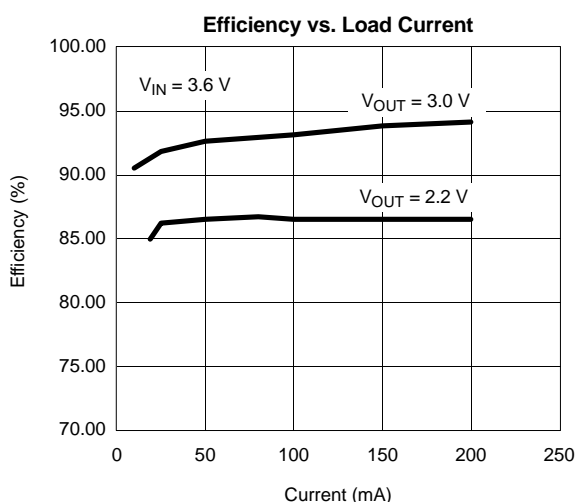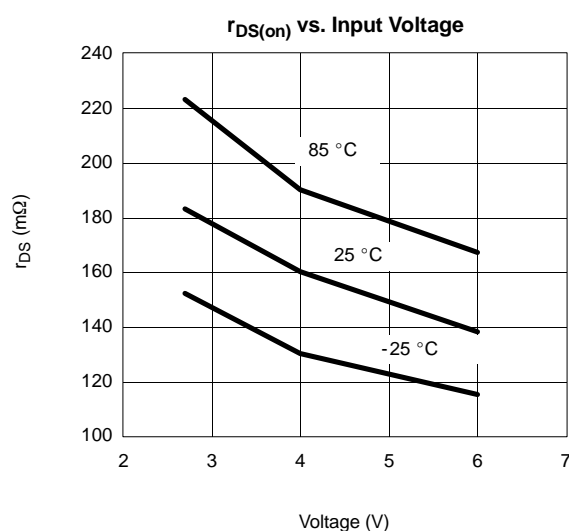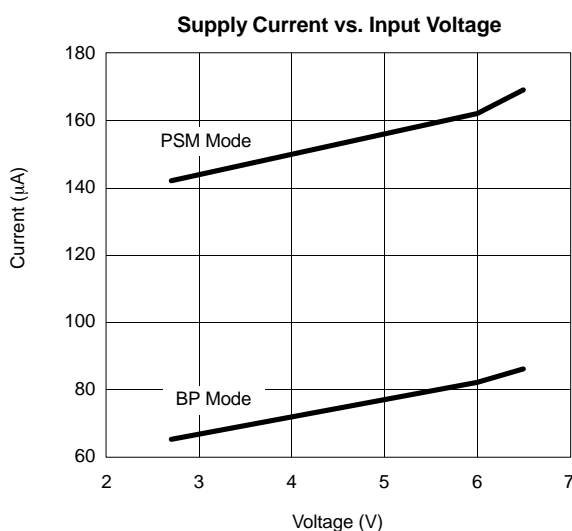## DETAIL OPERATIONAL DESCRIPTION (CONT'D)

An external Schottky diode is required for PSM mode operation. The Schottky diode handles the freewheeling inductor current after the p-channel MOSFET is turned off.

The current rating of the Schottky is based on the maximum load current in PSM mode with the conduction time being the greatest at maximum input voltage. Combined with the maximum load current of 200 mA, the Schottky must be able to conduct 200 mA continuously. Since the forward voltage drop of the diode, V_F, determines the conduction losses, select the diode with the lowest V_F to maximize the converter's efficiency. The diode should also be selected for fast switching

speed to improve efficiency. The diode must be connected from the L_X pin to GND.
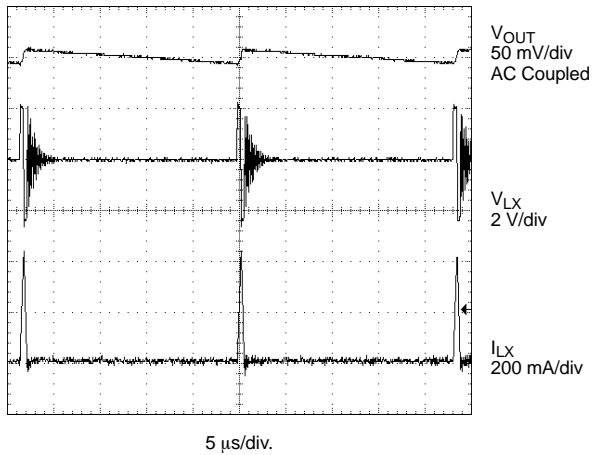
Over Temperature Protection

Si9177 includes an over temperature protection circuit to prevent thermal runaway in the MOSFET switch. If the junction temperature reaches 165°C, an internal soft-start capacitor is discharged, shutting down the output stage. The converter remains disabled until the junction temperature falls below 140°C, allowing the converter to resume operation.
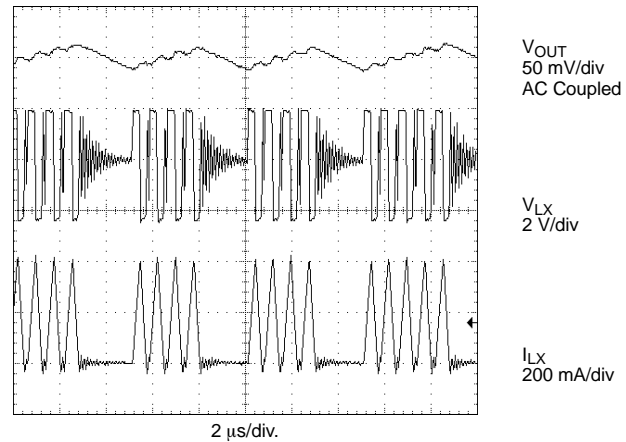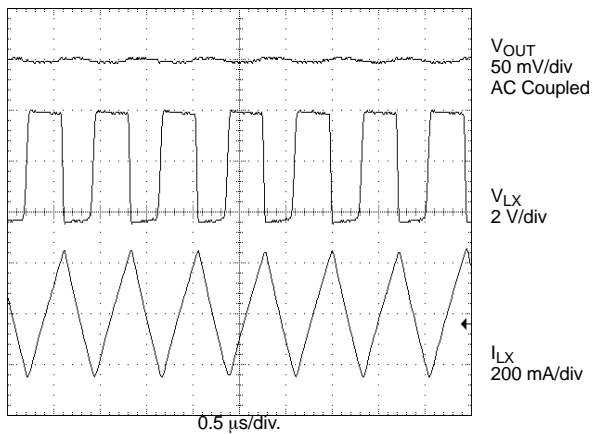
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Supply Current vs. Input Voltage

$r_{DS(on)}$ vs. Input Voltage

Efficiency vs. Load Current

Switching Frequency vs. Load Current

TYPICAL WAVEFORMS

Typical Switching Waveforms
V_{IN} = 4 V, V_{OUT} = 2.0 V, I_{OUT} = 6 mA

V_{OUT}
50 mV/div
AC Coupled

V_{LX}
2 V/div

I_{LX}
200 mA/div

5 μs/div.

Typical Switching Waveforms
V_{IN} = 4 V, V_{OUT} = 2.0 V, I_{OUT} = 100 mA

V_{OUT}
50 mV/div
AC Coupled

V_{LX}
2 V/div

I_{LX}
200 mA/div

2 μs/div.

Typical Switching Waveforms
V_{IN} = 4 V, V_{OUT} = 2.0 V, I_{OUT} = 200 mA

V_{OUT}
50 mV/div
AC Coupled

V_{LX}
2 V/div

I_{LX}
200 mA/div

0.5 μs/div.

Load Transient
V_{IN} = 4 V, V_{OUT} = 2.0 V

V_{OUT}
100 mV/div
AC Coupled

I_{OUT}
100 mA/div

100 μs/div.
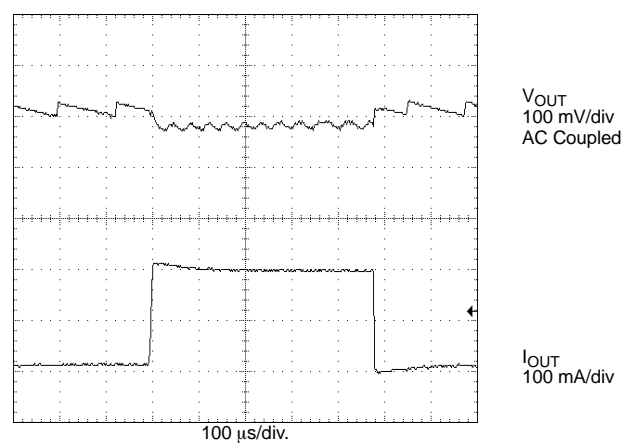
Start-Up
V_{IN} = 4 V, V_{OUT} = 2.0 V, I_{OUT} = 100 mA
V_{ENABLE} = V_{IN}

V_{IN}
2 V/div

V_{OUT}
1 V/div

50 μs/div.
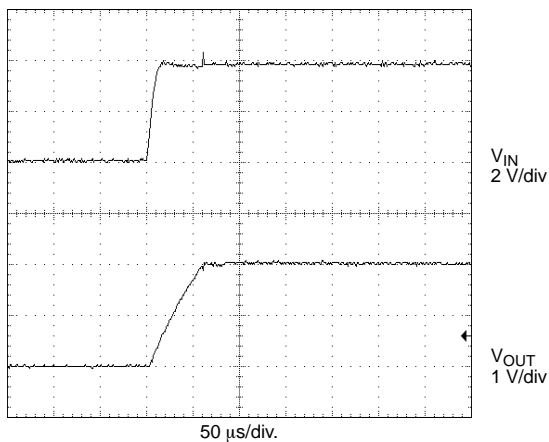
Start-Up from Disable
V_{IN} = 4 V, V_{OUT} = 2.0 V, I_{OUT} = 100 mA

V_{ENABLE}
2 V/div

V_{OUT}
1 V/div

50 μs/div.
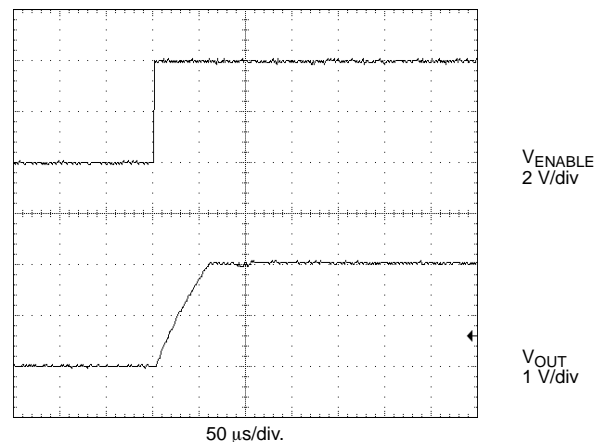
TYPICAL WAVEFORMS

Start-Up in Bypass Mode
V_{IN} = 4 V, I_{OUT} = 100 mA
V_{ENABLE}, BP = V_{IN}

V_{IN}
2 V/div

V_{OUT}
2 V/div

50 µs/div.
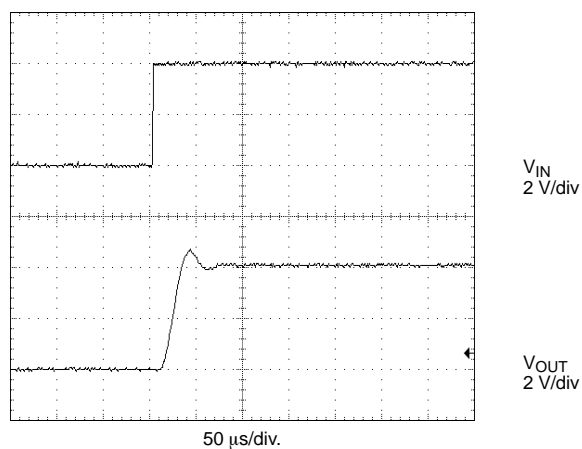
Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Vishay](#):
  [SI9177BH-T1-E3](#) [SI9177BH-T1](#) [SI9177BM-T1](#) [SI9177BM-T1-E3](#)