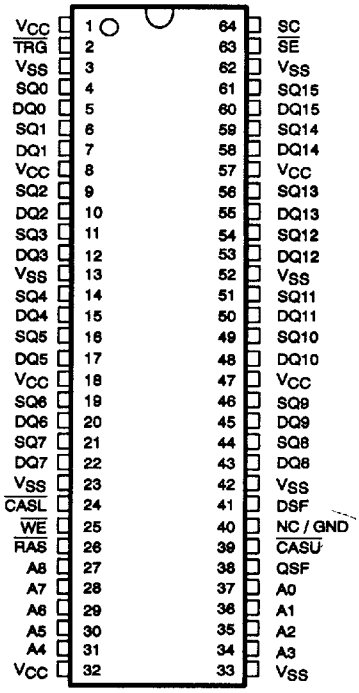
- **Organization:**
  - **DRAM: 262144 Words × 16 Bits**
  - **SAM: 256 Words × 16 Bits**
- **Dual-Port Accessibility – Simultaneous and Asynchronous Access From the DRAM and SAM Ports**
- **Data Transfer Function From the DRAM to the Serial Data Register**
- **(4 × 4) × 4 Block-Write Feature for Fast Area Fill Operations. As Many as Four Memory Address Locations Written Per Cycle From the 16-Bit On-Chip Color Register**
- **Write-Per-Bit Feature for Selective Write to Each RAM I/O. Two Write-Per-Bit Modes to Simplify System Design**
- **Byte Write Control ($\overline{CASL}$, $\overline{CASU}$) Provides Flexibility**
- **Extended Data Output for Faster System Cycle Time**
- **Enhanced Page-Mode Operation for Faster Access**
- **$\overline{CAS}$-Before-$\overline{RAS}$ and Hidden Refresh Modes**
- **Long Refresh Period . . . Every 8 ms (Max)**
- **Up to 55-MHz Uninterrupted Serial Data Streams**
- **256 Selectable Serial-Register Starting Locations**
- **$\overline{SE}$-Controlled Register-Status QSF**
- **Split-Register Transfer Read for Simplified Real-Time Register Load**
- **Programmable Split-Register Stop Point**
- **3-State Serial Outputs Allow Easy Multiplexing of Video Data Streams**
- **All Inputs/Outputs and Clocks TTL Compatible**
- **Compatible With JEDEC Standards**
- **Texas Instruments EPIC™ CMOS Process**
- **Designed to Work With the Industry-Leading Texas Instruments Graphics Family**
- **Performance Ranges:**

DGH PACKAGE
(TOP VIEW)



PIN NOMENCLATURE

A0–A8	Address Inputs
$\overline{CASL}$, $\overline{CASU}$	Column-Address Strobe/Byte Selects
DQ0–DQ15	DRAM Data I/O, Write Mask Data
$\overline{SE}$	Serial Enable
$\overline{RAS}$	Row-Address Strobe
SC	Serial Clock
SQ0–SQ15	Serial Data Output
$\overline{TRG}$	Output Enable, Transfer Select
$\overline{WE}$	DRAM Write Enable Select
DSF	Special Function Select
QSF	Special Function Output
V_{CC}	5-V Supply (TYP)
V_{SS}	Ground
NC/GND	No Connect/Ground (Important: not connected internally to V_{SS})

	ACCESS TIME ROW ENABLE $t_{a(R)}$ (MAX)	ACCESS TIME SERIAL DATA $t_{a(SQ)}$ (MAX)	DRAM CYCLE TIME $t_{c(W)}$ (MIN)	DRAM PAGE MODE $t_{c(P)}$ (MIN)	SERIAL CYCLE TIME $t_{c(SC)}$ (MIN)	OPERATING CURRENT SERIAL PORT STANDBY I_{CC1} (MAX)	OPERATING CURRENT SERIAL PORT ACTIVE I_{CC1A} (MAX)
TMS55161-60	60 ns	15 ns	110 ns	30 ns	18 ns	180 mA	225 mA
TMS55161-70	70 ns	20 ns	130 ns	30 ns	22 ns	165 mA	205 mA
TMS55161-80	80 ns	25 ns	150 ns	35 ns	30 ns	150 mA	185 mA

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description

The TMS55161 multiport video RAM is a high-speed dual-ported memory device. It consists of a dynamic random-access memory (DRAM) organized as 262144 words of 16 bits each interfaced to a serial data register [serial-access memory (SAM)] organized as 256 words of 16 bits each. The TMS55161 supports three basic types of operation: random access to and from the DRAM, serial access from the serial register, and transfer of data from any row in the DRAM to the serial register. Except during transfer operations, the TMS55161 can be accessed simultaneously and asynchronously from the DRAM and SAM ports.

The TMS55161 is equipped with several features designed to provide higher system-level bandwidth and to simplify design integration on both the DRAM and SAM ports. On the DRAM port, greater pixel draw rates can be achieved by the device's (4 × 4) × 4 block-write feature. The block-write mode allows 16 bits of data (present in an on-chip color data register) to be written to any combination of four adjacent column-address locations. As many as 64 bits of data can be written to memory during each $\overline{CAS}$ cycle time. Also on the DRAM port, a write mask or a write-per-bit feature allows masking of any combination of the 16 inputs/outputs on any write cycle. The persistent write-per-bit feature uses a mask register which, once loaded, can be used on subsequent write cycles without reloading. The TMS55161 also offers byte control. Byte control can be applied in read cycles, write cycles, block-write cycles, load-write-mask-register cycles, and load-color-register cycles. The TMS55161 also offers extended output mode. The extended output mode is effective in both the page-mode cycles and standard cycles.

The TMS55161 offers a split-register transfer read (DRAM to SAM) feature for the serial register (SAM port). This feature enables real-time register load implementation for truly continuous serial data streams without critical timing requirements. The register is divided into a high half and a low half. While one half is being read out of the SAM port, the other half can be loaded from the memory array. For applications not requiring real-time register load (for example, loads done during CRT retrace periods), the full-register mode of operation is retained to simplify system design.

The SAM port is designed for maximum performance. Data can be accessed from the SAM at serial rates up to 55 MHz. During the split-register transfer read operations, internal circuitry detects when the last bit position is accessed from the active half of the register and immediately transfers control to the opposite half. A separate output, QSF, is included to indicate which half of the serial register is active.

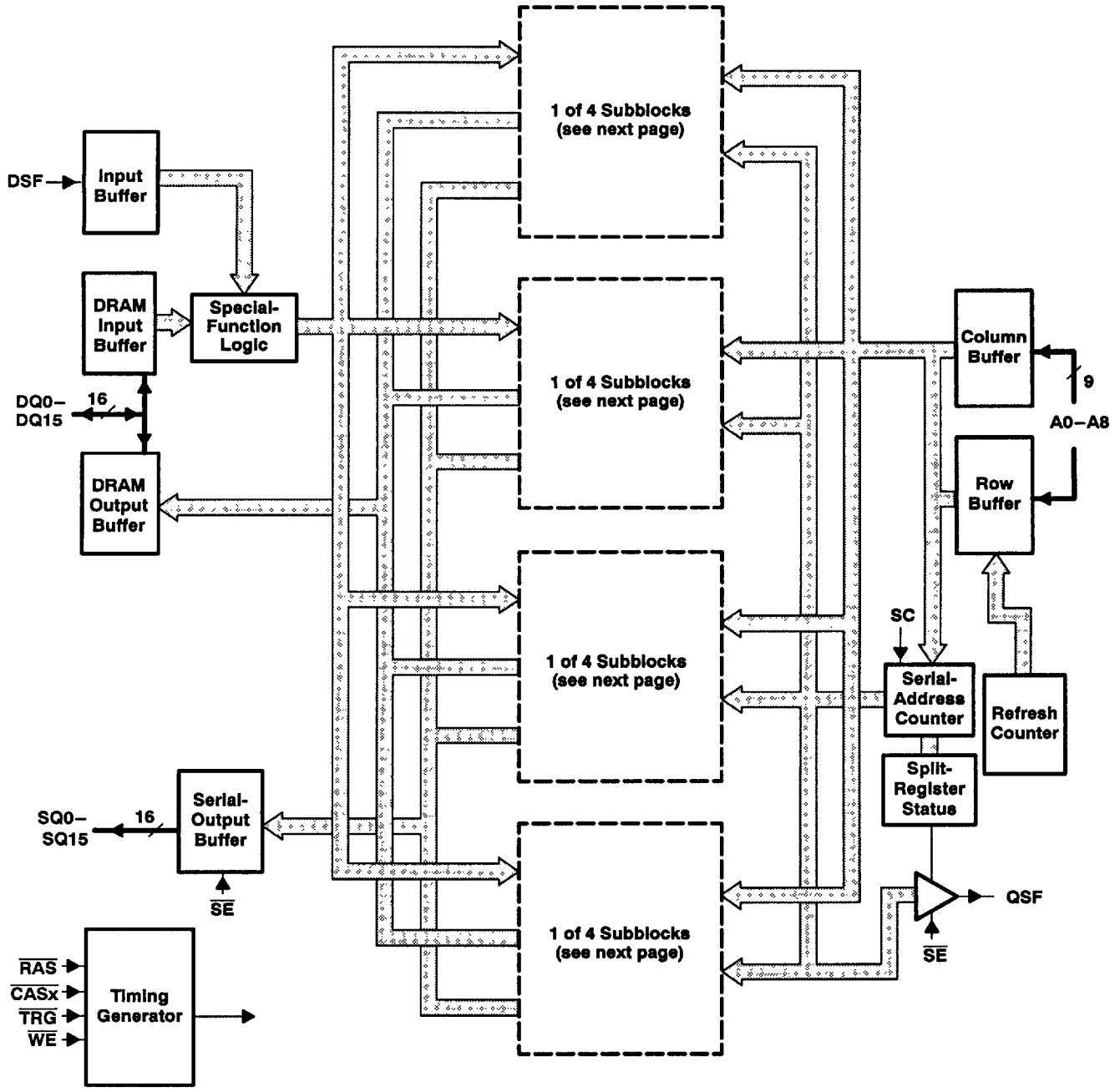
All inputs, outputs, and clock signals on the TMS55161 are compatible with Series 74 TTL. All address lines and data-in lines are latched on chip to simplify system design. All data outs are unlatched to allow greater system flexibility.

The TMS55161 employs state-of-the-art Texas Instruments EPIC™ scaled-CMOS, double-level polysilicon/polycide gate technology for very high performance combined with low cost and improved reliability.

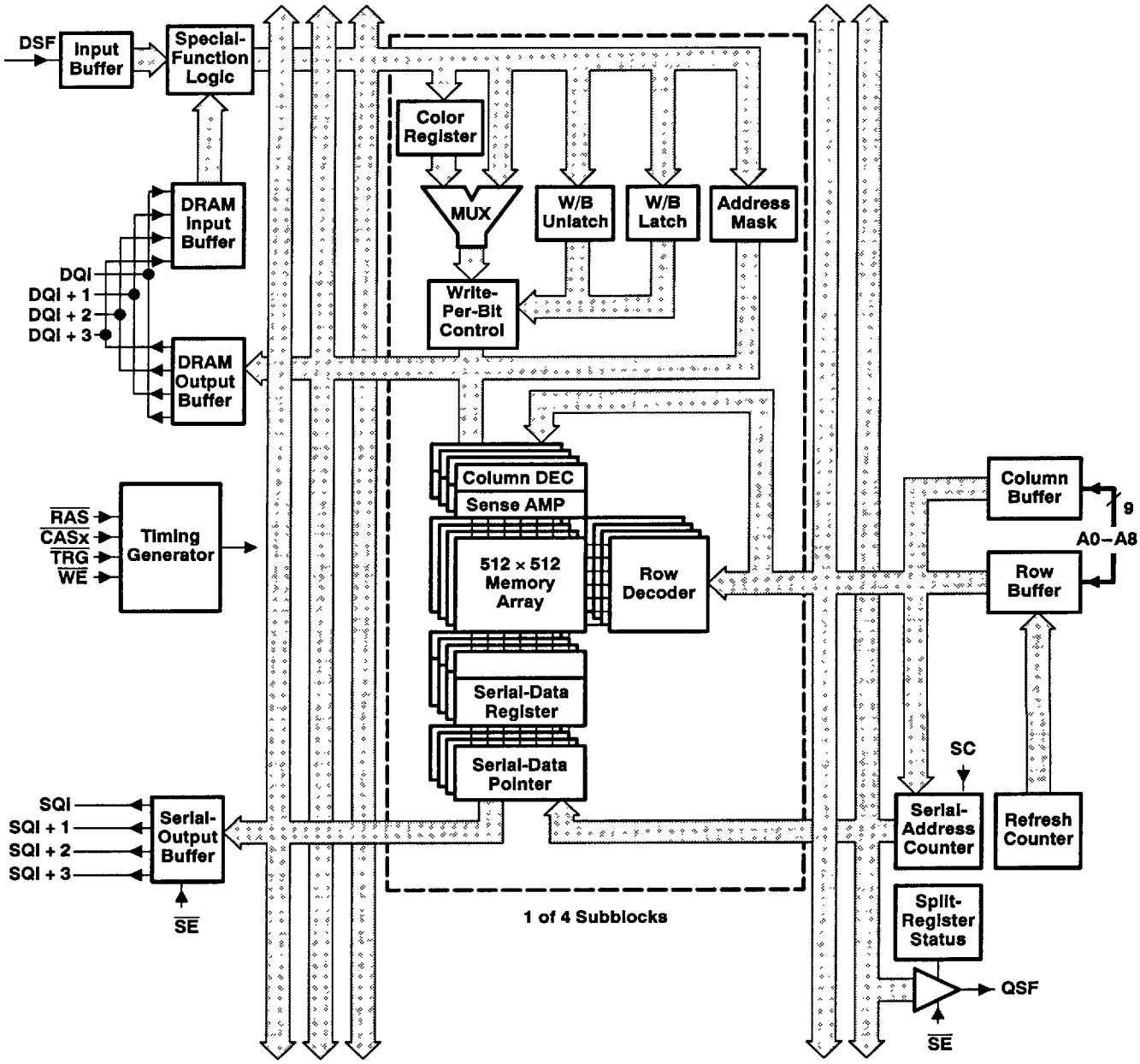
The TMS55161 is offered in a 64-pin small-outline gull-wing-leaded package (DGH suffix) for direct surface mounting.

The TMS55161 and other TI multiport video RAMs are supported by a broad line of graphics processors and control devices from Texas Instruments.

functional block diagram



functional block diagram (continued)



TEXAS INSTRUMENTS
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Table 1. Function Table

FUNCTION	RAS FALL				CASx FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CASx‡	TRG	WE	DSF	DSF	RAS	CASx§	RAS	CASL CASU WE	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CAS-before-RAS refresh (no reset) and stop point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CAS-before-RAS refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CAS-before-RAS refresh (no reset)★	L	X	H	H	X	X	X	X	X	CBRN
Full-register transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
Load write mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
X = Don't care
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled

† DQ0–DQ15 are latched on either the first falling edge of CASx or the falling edge of WE, whichever occurs later.
‡ Logic L is selected when either or both CASL and CASU are low.
§ The column address and block address are latched on the first falling edge of CASx.
¶ CBRS cycle should be performed immediately after the power-up initialization cycle.
# A0–A3, A8: don't care; A4–A7 : stop-point code
‖ CAS-before-RAS refresh (option reset) mode will end persistent write-per-bit mode and stop-point mode.
★ CAS-before-RAS refresh (no reset) mode will not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CAS-before-RAS (option reset) cycle.

Table 2. Pin Description Versus Operational Mode

PIN	DRAM	TRANSFER	SAM
A0 – A8	Row, column address	Row address, tap point	
$\overline{CASL}$ $\overline{CASU}$	Column-address strobe, DQ output enable	Tap-address strobe	
DQ	DRAM data I/O, Write mask		
DSF	Block-write enable Write-mask-register-load enable Color-register-load enable $\overline{CAS}$-before-$\overline{RAS}$ (option reset)	Split-register transfer enable	
$\overline{RAS}$	Row-address strobe	Row-address strobe	
$\overline{SE}$			SQ output enable, QSF output enable
SC			Serial clock
SQ			Serial data output
$\overline{TRG}$	DQ output enable	Transfer enable	
$\overline{WE}$	Write enable		
QSF			Serial-register status
NC/GND	Make no external connection or tie to system GND		
V_{CC}†	5-V supply		
V_{SS}†	Ground		

† For proper device operation, all V_{CC} pins must be connected to a 5-V supply and all V_{SS} pins must be tied to ground.

pin definitions

address (A0–A8)

Eighteen address bits are required to decode one of 262144 storage cell locations. Nine row-address bits are set up on pins A0–A8 and latched onto the chip on the falling edge of $\overline{RAS}$. Nine column-address bits are set up on pins A0–A8 and latched onto the chip on the first falling edge of $\overline{CASx}$. All addresses must be stable on or before the falling edge of $\overline{RAS}$ and the first falling edge of $\overline{CASx}$.

During the full-register transfer read operation, the states of A0–A8 are latched on the falling edge of $\overline{RAS}$ to select one of the 512 rows where the transfer will occur. At the first falling edge of $\overline{CASx}$, the column-address bits A0–A8 are latched. The most significant column-address bit (A8) selects which half of the row will be transferred to the SAM. The appropriate 8-bit column address (A0–A7) selects one of 256 tap points (starting positions) for the serial data output.

During the split-register transfer read operation, address bit A7 is ignored at the falling edge of $\overline{CASx}$. An internal counter selects which half of the register will be used. If the high half of the SAM is currently in use, the low half of the SAM is loaded with the low half of the DRAM half row, and vice versa. Column address (A8) selects the DRAM half row. The remaining seven address bits (A0–A6) are used to select 1 of 127 possible starting locations within the SAM. Locations 127 and 255 are not valid tap points.

row-address strobe ($\overline{RAS}$)

$\overline{RAS}$ is similar to a chip enable, so that all DRAM cycles and transfer cycles are initiated by the falling edge of $\overline{RAS}$. $\overline{RAS}$ is a control input that latches the states of the row address, $\overline{WE}$, $\overline{TRG}$, $\overline{CASL}$, $\overline{CASU}$, and DSF onto the chip to invoke DRAM and transfer read functions of the TMS55161.

column-address strobe ($\overline{CASL}$, $\overline{CASU}$)

$\overline{CASL}$ and $\overline{CASU}$ are control inputs that latch the states of the column address and DSF to control DRAM and transfer functions of the TMS55161. $\overline{CASx}$ also act as output enables for the DRAM output pins, DQ0–DQ15.

In DRAM operation, $\overline{CASL}$ enables data to be written to or read from the lower byte (DQ0–DQ7), and $\overline{CASU}$ enables data to be written to or from the upper byte (DQ8–DQ15).

In transfer operations, address bits A0–A8 are latched at the first falling edge of $\overline{CASx}$ as the start position (tap) for the serial data output (SQ0–SQ15).

output enable/transfer select ($\overline{TRG}$)

The $\overline{TRG}$ pin selects either DRAM or transfer operation as $\overline{RAS}$ falls. For DRAM operation, $\overline{TRG}$ must be held high as $\overline{RAS}$ falls. During DRAM operation, $\overline{TRG}$ functions as an output enable for the DRAM output pins, DQ0–DQ15. For transfer operation, $\overline{TRG}$ must be brought low before $\overline{RAS}$ falls.

write mask select, write enable ($\overline{WE}$)

In DRAM operation, $\overline{WE}$ enables data to be written to the DRAM. $\overline{WE}$ is also used to select the DRAM write-per-bit mode of operation. Holding $\overline{WE}$ low on the falling edge of $\overline{RAS}$ invokes the write-per-bit operation. The TMS55161 supports both the nonpersistent write-per-bit mode and the persistent write-per-bit mode.

special function select (DSF)

The DSF input is latched on the falling edge of $\overline{RAS}$ or the first falling edge of $\overline{CASx}$ similar to an address. DSF determines which of the following functions are invoked on a particular cycle:

- CBR refresh with no reset (CBRN)
- CBR refresh with no reset and stop-point set (CBRS)
- Block write (BW, BWM)
- Loading write-mask register for the persistent write-per-bit mode (LMR)
- Loading color register for the block-write mode (LCR)
- Split-register transfer read (SRT)

DRAM data I/O, write mask data (DQ0–DQ15)

DRAM data is written or read through the common I/O DQ pins. The 3-state DQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. Data out is the same polarity as data in. The outputs are in the high-impedance (floating) state as long as either $\overline{TRG}$ or $\overline{CASx}$ is held high. Data does not appear at the outputs until after both $\overline{CASx}$ and $\overline{TRG}$ have been brought low. The write mask is latched into the device via the random DQ pins by the falling edge of $\overline{RAS}$ and is used on all write-per-bit cycles. In a transfer operation, the DQ outputs remain in the high-impedance state for the entire cycle.

serial data outputs (SQ0–SQ15)

Serial data is read from the SQ pins. The SQ output buffers provide direct TTL compatibility (no pullup resistors) with a fanout of one Series 74 TTL load. The serial outputs are in the high-impedance (floating) state as long as the serial enable pin, $\overline{SE}$, is high. The serial outputs are enabled when $\overline{SE}$ is brought low.

serial clock (SC)

Serial data is accessed out of the data register from the rising edge of SC. The TMS55161 is designed to work with a wide range of clock duty cycles to simplify system design. There is no refresh requirement because the data registers that comprise the SAM are static. There is also no minimum SC operating frequency.

serial enable ($\overline{SE}$)

During serial-access operations, $\overline{SE}$ is used as an enable/disable for the SQ outputs. $\overline{SE}$ low enables the serial data output. $\overline{SE}$ high disables the serial data output. $\overline{SE}$ is also used as an enable/disable for output pin QSF.

IMPORTANT: While $\overline{SE}$ is held high, the serial clock is not disabled. External SC pulses increment the internal serial-address counter regardless of the state of $\overline{SE}$. This ungated serial clock scheme minimizes access time of serial output from $\overline{SE}$ low because the serial clock input buffer and the serial-address counter are not disabled by $\overline{SE}$.

special function output (QSF)

QSF is an output pin that indicates which half of the SAM is being accessed. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the serial register (SAM). When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM.

During full-register transfer operations, QSF can change state upon completing the cycle. This state is determined by the tap point loaded during the transfer cycle. The QSF output is enabled by $\overline{SE}$. If $\overline{SE}$ is high, the QSF output will be in the high-impedance state.

no connect/ground (NC/GND)

The NC/GND pin should be tied to system ground or left floating for proper device operation.

functional operation description

random access operation

Table 3. DRAM Function Table

FUNCTION	RAS FALL				CASx FALL	ADDRESS		DQ0–DQ15†		MNE CODE
	CASx‡	TRG	WE	DSF	DSF	RAS	CASx§	RAS	CASL CASU WE	
Reserved (do not use)	L	L	L	L	X	X	X	X	X	—
CAS-before-RAS refresh (no reset) and stop-point set¶	L	X	L	H	X	Stop Point#	X	X	X	CBRS
CAS-before-RAS refresh (option reset)‖	L	X	H	L	X	X	X	X	X	CBR
CAS-before-RAS refresh (no reset)★	L	X	H	H	X	X	X	X	X	CBRN
DRAM write (nonmasked)	H	H	H	L	L	Row Addr	Col Addr	X	Valid Data	RW
DRAM write (nonpersistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	Write Mask	Valid Data	RWM
DRAM write (persistent write-per-bit)	H	H	L	L	L	Row Addr	Col Addr	X	Valid Data	RWM
DRAM block write (nonmasked)	H	H	H	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BW
DRAM block write (nonpersistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	Write Mask	Col Mask	BWM
DRAM block write (persistent write-per-bit)	H	H	L	L	H	Row Addr	Block Addr A2–A8	X	Col Mask	BWM
Load write-mask register □	H	H	H	H	L	Refresh Addr	X	X	Write Mask	LMR
Load color register	H	H	H	H	H	Refresh Addr	X	X	Color Data	LCR

Legend:
X = Don't care
Col Mask = H: Write to address/column enabled
Write Mask = H: Write to I/O enabled

† DQ0–DQ15 are latched on either the first falling edge of CASx or the falling edge of WE, whichever occurs later.
‡ Logic L is selected when either or both CASL and CASU are low.
§ The column address and block address are latched on the first falling edge of CASx.
¶ CBRS cycle should be performed immediately after the power-up initialization cycle.
# A0–A3, A8: don't care; A4–A7: stop-point code
‖ CAS-before-RAS refresh (option reset) mode will end persistent write-per-bit mode and stop-point mode.
★ CAS-before-RAS refresh (no reset) mode will not end persistent write-per-bit mode or stop-point mode.
□ Load-write-mask-register cycle sets the persistent write-per-bit mode. The persistent write-per-bit mode is reset only by the CAS-before-RAS (option reset) cycle.

enhanced page mode

Enhanced-page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. This mode eliminates the time required for row-address setup, row-address hold, and address multiplex. The maximum $\overline{RAS}$ low time and the minimum $\overline{CAS}$ page cycle time are used to determine the number of columns that can be accessed.

Unlike conventional page-mode operations, the enhanced page mode allows the TMS55161 to operate at a higher data bandwidth. Data retrieval begins as soon as the column address is valid rather than when $\overline{CASx}$ transitions low. A valid column address can be presented immediately after the row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CASx}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CASx}$ low) if $t_{a(CA)}$ max (access time from column address) has been satisfied.

refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refreshes are accomplished by bringing either or both $\overline{CASL}$ and $\overline{CASU}$ low earlier than $\overline{RAS}$. The external row address is ignored, and the refresh row address is generated internally. Three types of CBR refresh cycles are available. The CBR refresh (option reset) ends the persistent write-per-bit mode and the stop-point mode. The CBRN and CBRS refreshes (no reset) do not end the persistent write-per-bit mode or the stop-point mode. The 512 rows of the DRAM do not necessarily need to be refreshed consecutively as long as the entire refresh is completed within the required time period, $t_{rf(MA)}$. The output buffers remain in the high-impedance state during the $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles regardless of the state of $\overline{TRG}$.

hidden refresh

A hidden refresh is accomplished by holding both $\overline{CASL}$ and $\overline{CASU}$ low in the DRAM read cycle and cycling $\overline{RAS}$. The output data of the DRAM read cycle remains valid while the refresh is being carried out. Like the $\overline{CAS}$-before-$\overline{RAS}$ refresh, the refreshed row addresses are generated internally during the hidden refresh.

$\overline{RAS}$-only refresh

A $\overline{RAS}$-only refresh is accomplished by cycling $\overline{RAS}$ at every row address. Unless $\overline{CASx}$ and $\overline{TRG}$ are low, the output buffers remain in the high-impedance state to conserve power. Externally generated addresses must be supplied during $\overline{RAS}$-only refresh. Strobing each of the 512 row addresses with $\overline{RAS}$ causes all bits in each row to be refreshed.

extended data output

The TMS55161 features extended data output during DRAM accesses. While $\overline{RAS}$ and $\overline{TRG}$ are low, the DRAM output remains valid even when $\overline{CASx}$ returns high. The output remains valid until $\overline{WE}$ is low, $\overline{TRG}$ is high, or both $\overline{CASx}$ and $\overline{RAS}$ are high. The extended-data-output mode functions in all read cycles including DRAM-read, page-mode-read, and read-modify-write cycles.

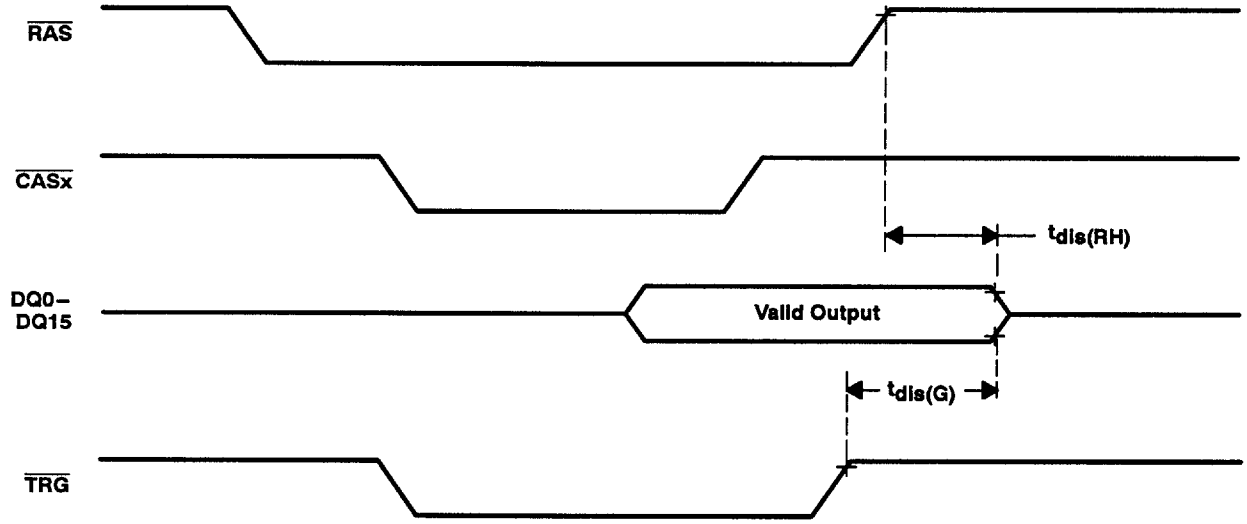


Figure 1. DRAM-Read Cycle With $\overline{RAS}$-Controlled Output

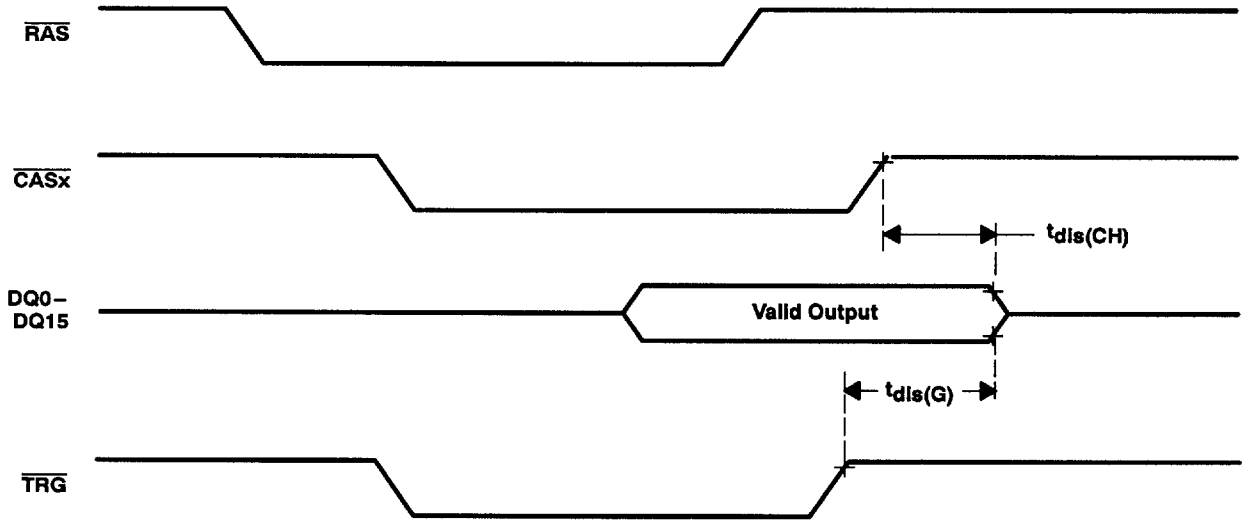


Figure 2. DRAM-Read Cycle With $\overline{CASx}$-Controlled Output

extended data output (continued)

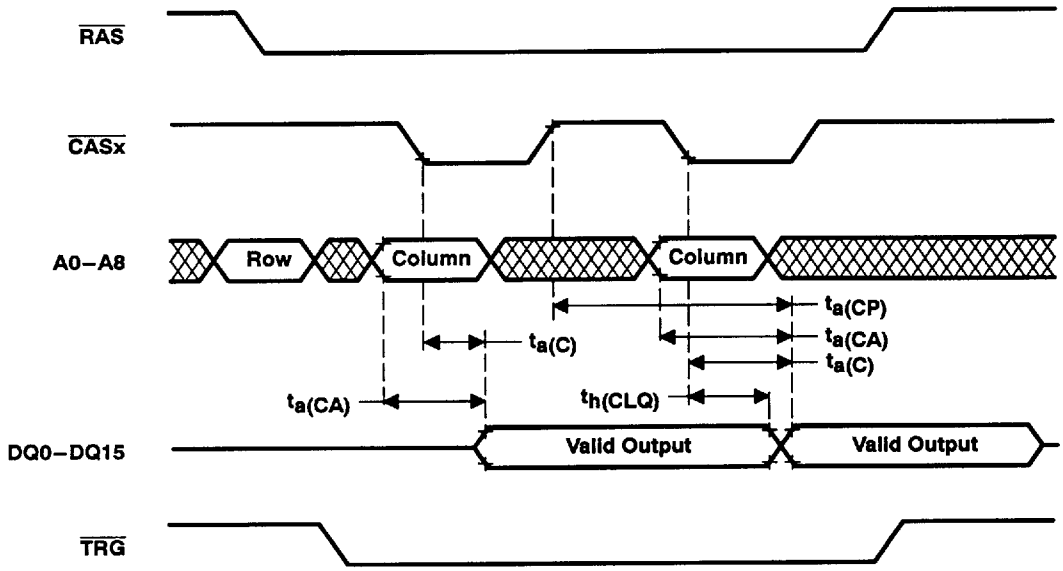


Figure 3. DRAM-Page-Read Cycle With Extended Output

byte operation

Byte operation can be applied in DRAM read cycles, write cycles, block-write cycles, load-write-mask-register cycles and load-color-register cycles. In byte operation, the column address (A0–A8) is latched at the first falling edge of $\overline{CAS}x$. In read cycles, $\overline{CASL}$ enables the lower byte (DQ0–DQ7) and $\overline{CASU}$ enables the upper byte (DQ8–DQ15) (see Figure 4).

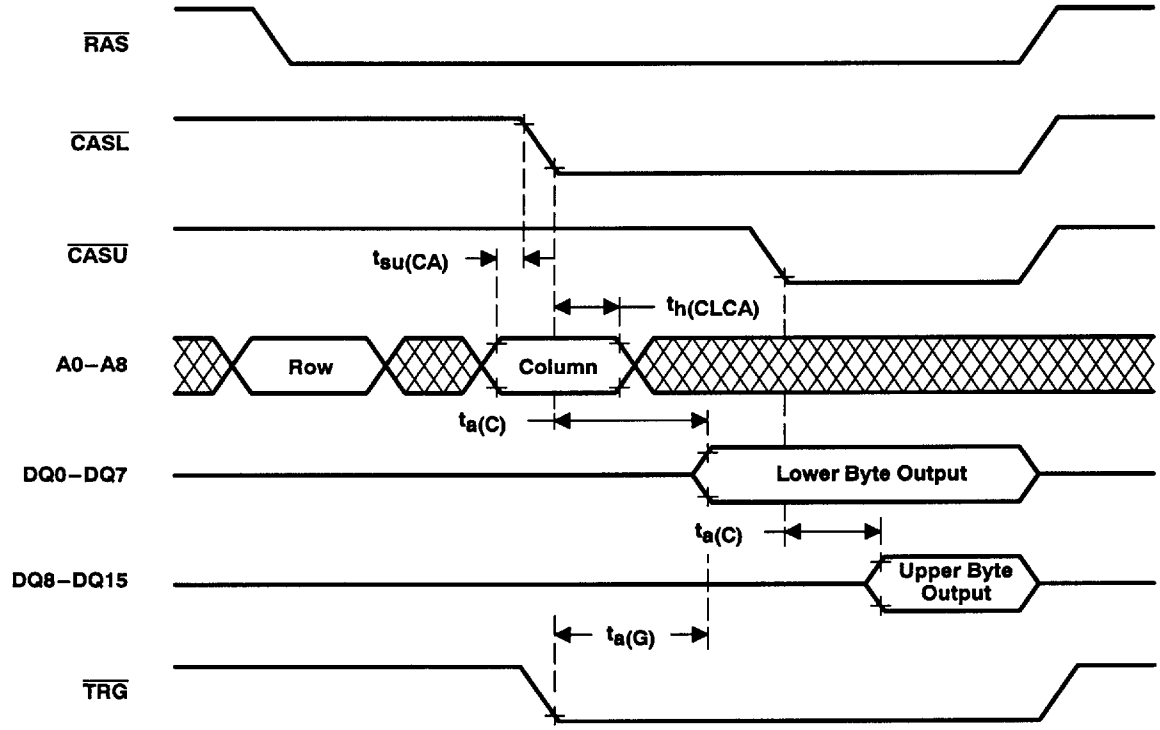


Figure 4. Example of a Byte-Read Cycle

byte operation (continued)

In byte-write operation, $\overline{CASL}$ enables data to be written to the lower byte (DQ0–DQ7) and $\overline{CASU}$ enables data to be written to the upper byte (DQ8–DQ15). In an early-write cycle, $\overline{WE}$ is brought low prior to both $\overline{CASx}$ signals. Data setup and hold times for DQ0–DQ15 are referenced to the first falling edge of $\overline{CASx}$ (see Figure 5).

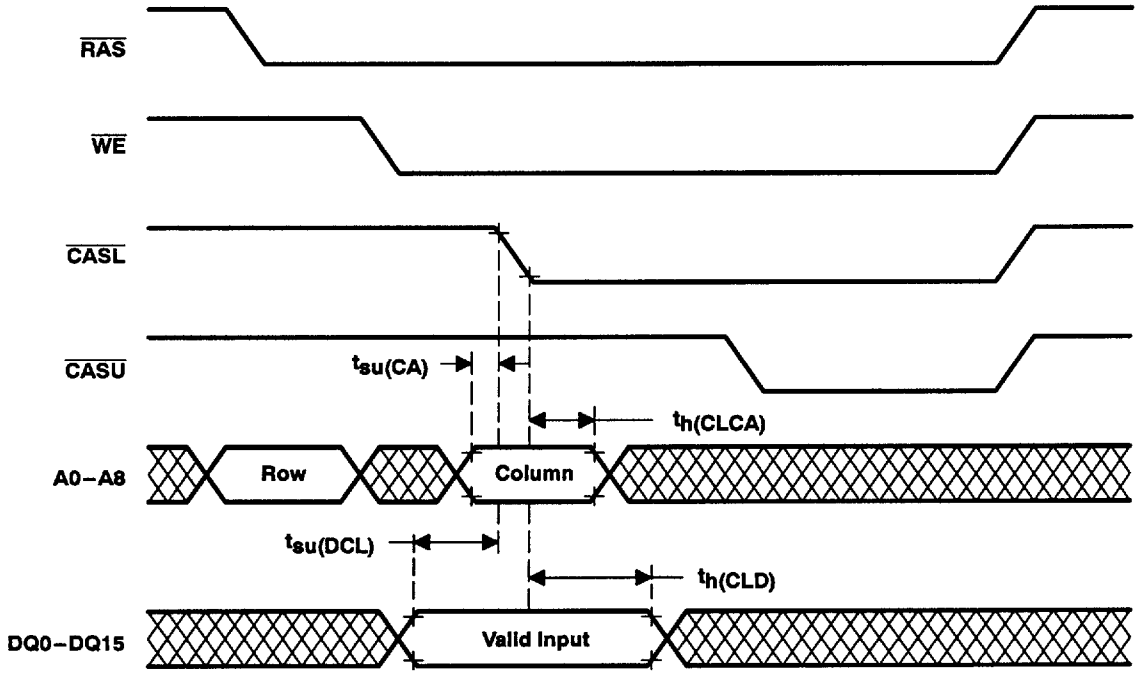


Figure 5. Example of an Early-Write Cycle

byte operation (continued)

For late-write or read-modify-write cycles, $\overline{WE}$ is brought low after either or both $\overline{CASL}$ and $\overline{CASU}$ fall. The data is strobed in with data setup and hold times for DQ0–DQ15 referenced to $\overline{WE}$ (see Figure 6).

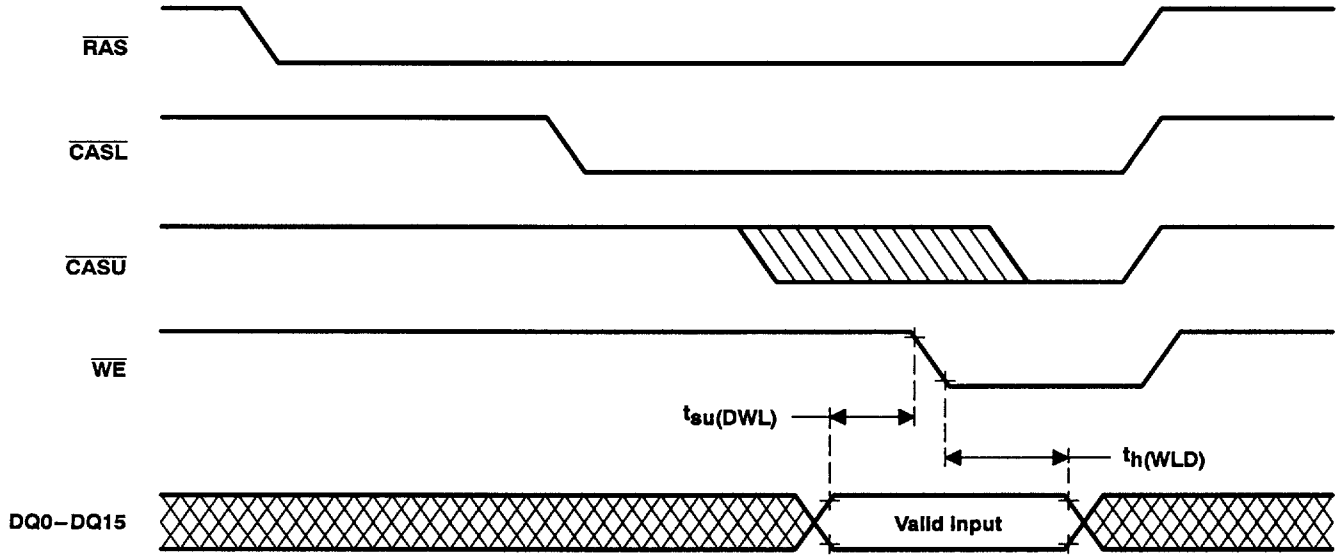


Figure 6. Example of a Late-Write Cycle

write-per-bit

The write-per-bit feature allows masking any combination of the 16 DQs on any write cycle. The write-per-bit operation is invoked when $\overline{WE}$ is held low on the falling edge of $\overline{RAS}$. If $\overline{WE}$ is held high on the falling edge of $\overline{RAS}$, the write operation is performed without any masking. The TMS55161 offers two write-per-bit modes: the nonpersistent write-per-bit and the persistent write-per-bit.

nonpersistent write-per-bit

When $\overline{WE}$ is low on the falling edge of $\overline{RAS}$, the write mask is reloaded. A 16-bit binary code (the write-per-bit mask) is input to the device via the DQ pins and latched on the falling edge of $\overline{RAS}$. The write-per-bit mask selects which of the 16 I/Os are to be written and which are not. After $\overline{RAS}$ has latched the on-chip write-per-bit mask, input data is driven onto the DQ pins and is latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. $\overline{CASL}$ enables the lower byte (DQ0–DQ7) to be written through the mask and $\overline{CASU}$ enables the upper byte (DQ8–DQ15) to be written through the mask. If a data low (write mask = 0) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is not written to that I/O. If a data high (write mask = 1) is strobed into a particular I/O pin on the falling edge of $\overline{RAS}$, data is written to that I/O (see Figure 7).

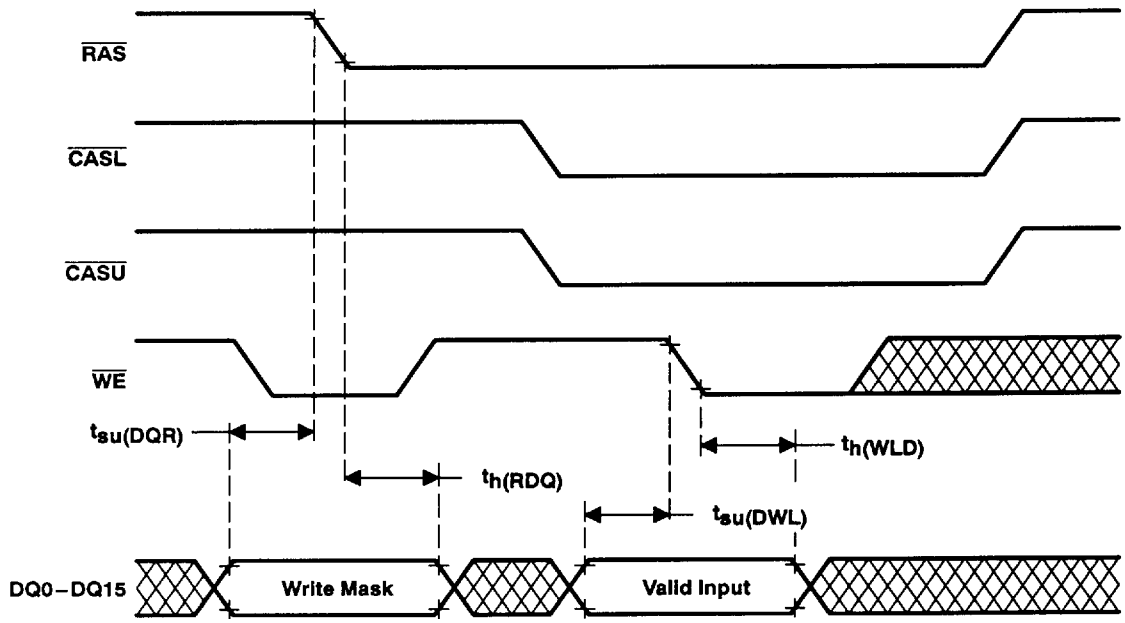


Figure 7. Example of a Nonpersistent Write-Per-Bit (Late-Write) Operation

persistent write-per-bit

The persistent write-per-bit mode is initiated only by performing a load-write-mask-register cycle first. In the persistent write-per-bit mode, the write-per-bit mask is not overwritten but remains valid over an arbitrary number of write cycles until another LMR cycle is performed or power is removed.

The load-write-mask-register cycle is performed using DRAM write-cycle timing except DSF is held high on the falling edge of $\overline{RAS}$ and held low on the first falling edge of $\overline{CASx}$. A binary code is input to the write-mask register via the random I/O pins and latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. Byte-write control can be applied to the write mask during the load-write-mask-register cycle. The persistent write-per-bit mode can then be used in exactly the same way as the nonpersistent write-per-bit mode except that the input data on the falling edge of $\overline{RAS}$ is ignored. When the device is set to the persistent write-per-bit mode, it remains in this mode and is reset only by a $\overline{CAS}$-before-$\overline{RAS}$ refresh with option reset cycle (see Figure 8).

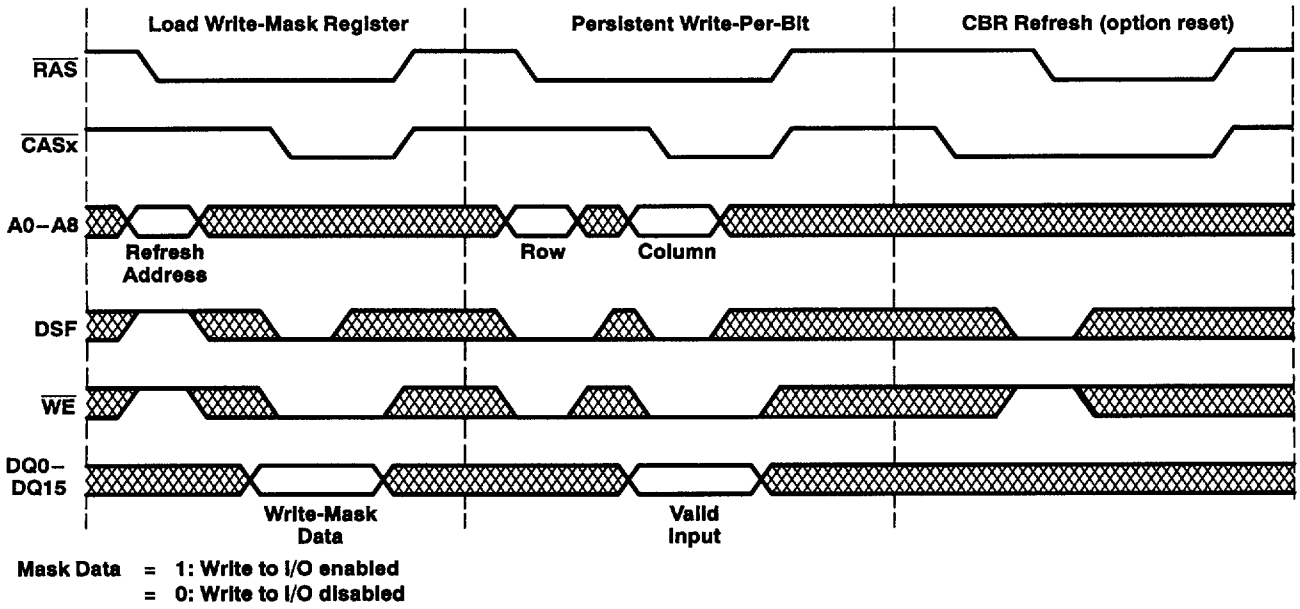


Figure 8. Example of a Persistent Write-Per-Bit Operation

block write

The block-write feature allows up to 64 bits of data to be written simultaneously to one row of the memory array. This function is implemented as (4 columns × 4 DQs) repeated in four quadrants. In this manner, each of the four one-megabit quadrants can have up to four consecutive columns written at a time with up to four DQs per column (see Figure 9).

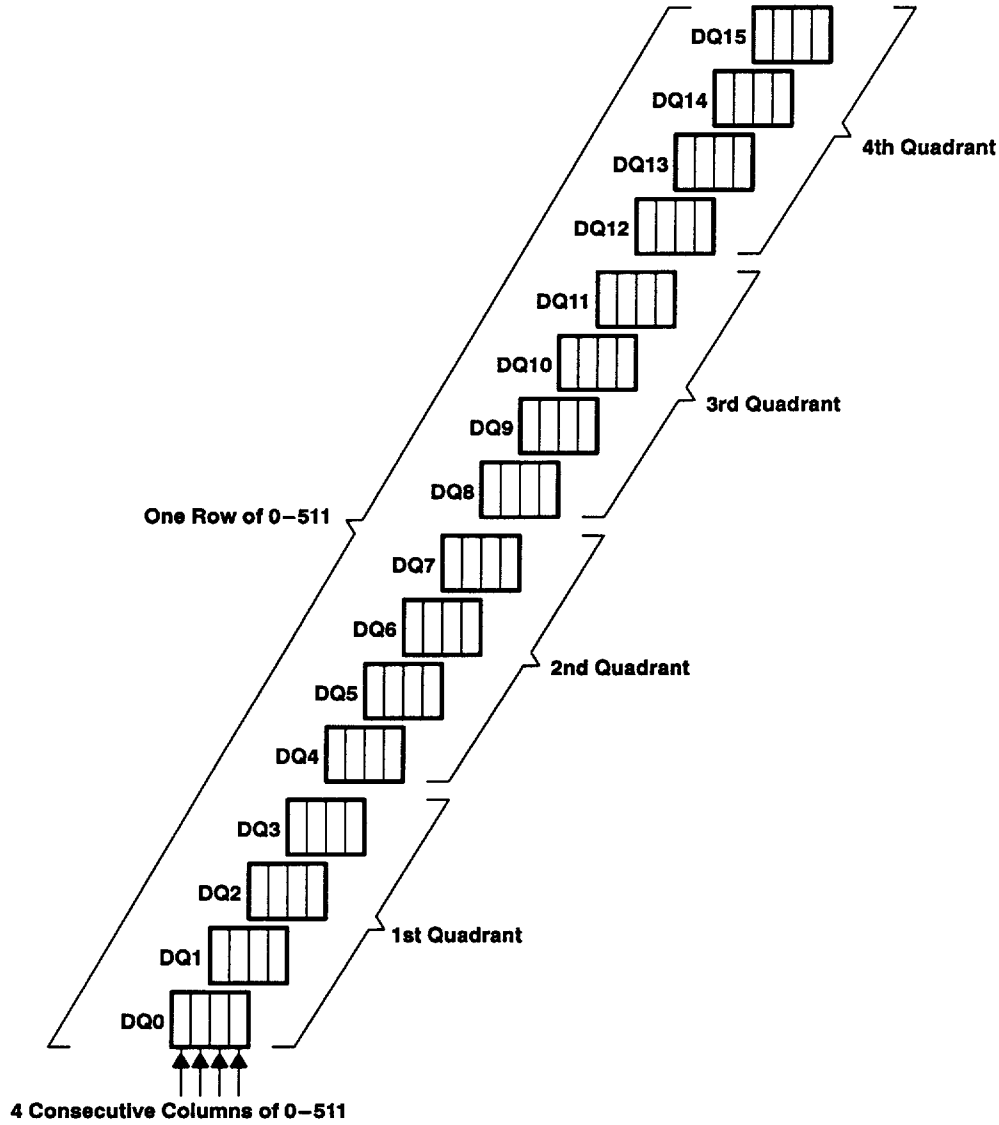


Figure 9. Block-Write Operation

Each one-megabit quadrant has a 4-bit column mask to mask off any or all of the four columns from being written with data. Nonpersistent write-per-bit or persistent write-per-bit functions can be applied to the block-write operation to provide write masking options. The DQ data is provided by four bits from the on-chip color register. Bits 0–3 from the 16-bit write-mask register, bits 0–3 from the 16-bit column-mask register, and bits 0–3 from the 16-bit color-data register configure the block write for the first quadrant, while bits 4–7, 8–11, and 12–15 of the corresponding registers control the other quadrants in a similar fashion (see Figure 10).

block write (continued)

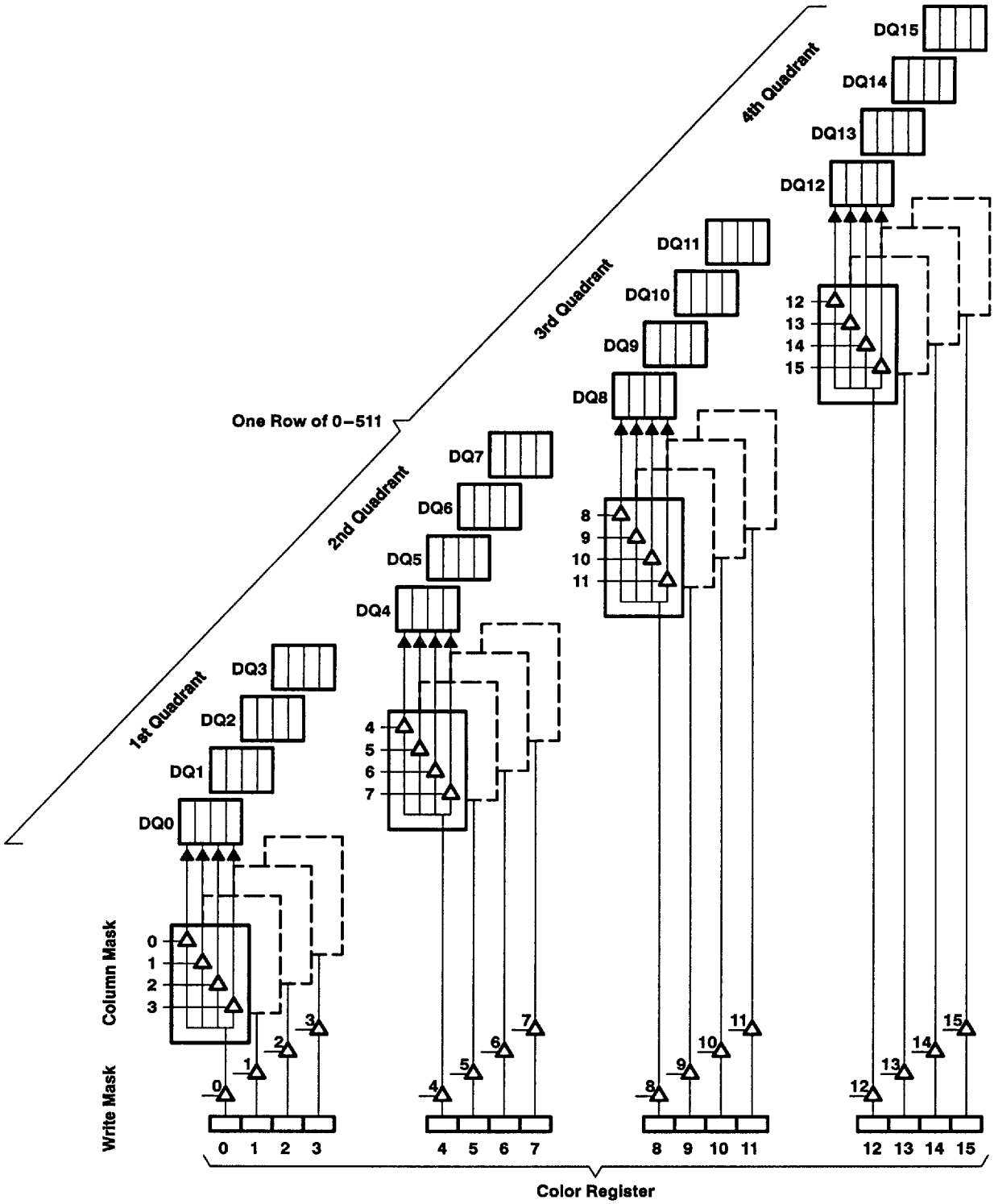


Figure 10. Block Write With Masks

block write (continued)

Every four columns make a block, which makes 128 blocks along one row. Block 0 comprises columns 0–3, block 1 comprises columns 4–7, block 2 comprises columns 8–11, etc., as shown in Figure 11.

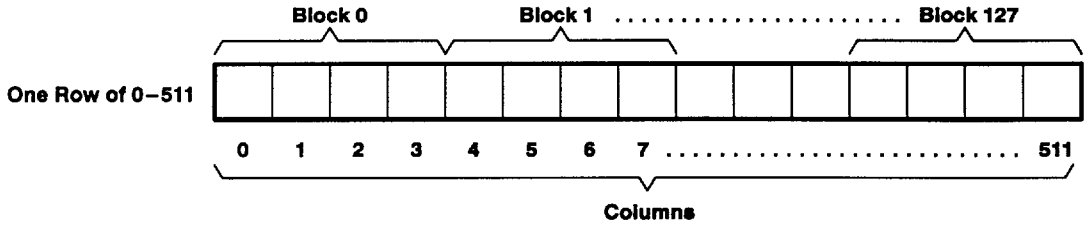


Figure 11. Block Columns Organization

During block-write cycles, only the seven most significant column addresses (A2–A8) are latched on the first falling edge of $\overline{CAS}$x to decode one of the 128 blocks. Address bits A0–A1 are ignored. Each one-megabit quadrant has the same block selected.

A block-write cycle is entered in a manner similar to a DRAM write cycle except DSF is held high on the first falling edge of $\overline{CAS}$x. As in a DRAM write operation, $\overline{CASL}$ and $\overline{CASU}$ enable the corresponding lower and upper DRAM DQ bytes to be written, respectively. The column-mask data is input via the DQs and is latched on either the first falling edge of $\overline{CAS}$x or the falling edge of $\overline{WE}$, whichever occurs later. The 16-bit color-data register must be loaded prior to performing a block write as described below. Refer to the write-per-bit section for details on use of the write-mask capability allowing additional performance options.

Example of block write:

block-write column address = 110000000 (A0–A8 from left to right)

	bit 0			bit 15
color-data register =	1011	1011	1100	0111
write-mask register =	1110	1111	1111	1011
column-mask register =	1111	0000	0111	1010
	1st Quad	2nd Quad	3rd Quad	4th Quad

Column-address bits A0 and A1 are ignored. Block 0 (columns 0–3) is selected for each one-megabit quadrant. The first quadrant has DQ0–DQ2 written with bits 0–2 from the color-data register (101) to all four columns of block 0. DQ3 is not written and retains its previous data due to the write-mask-register bit 3 being a 0.

The second quadrant (DQ4–DQ7) has all four columns masked off due to the column mask bits 4–7 being 0, so that no data is written.

The third quadrant (DQ8–DQ11) has its four DQs written with bits 8–11 from the color-data register (1100) to columns 1–3 of its block 0. Column 0 is not written and retains its previous data on all four DQs due to the column mask-register bit 8 being 0.

The fourth quadrant (DQ12–DQ15) has DQ12, DQ14, and DQ15 written with bits 12, 14, and 15 from the color-data register to column 0 and column 2 of its block 0. DQ13 retains its previous data on all columns due to the write mask. Columns 1 and 3 retain their previous data on all DQs due to the column mask. If the previous data for the quadrant was all 0s, the fourth quadrant would contain the data pattern shown in Figure 12 after the block-write operation shown in the previous example.

block write (continued)

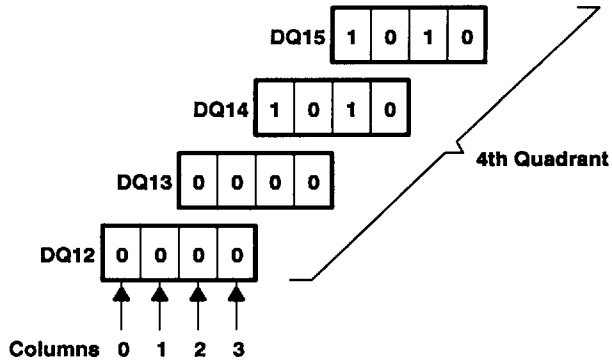
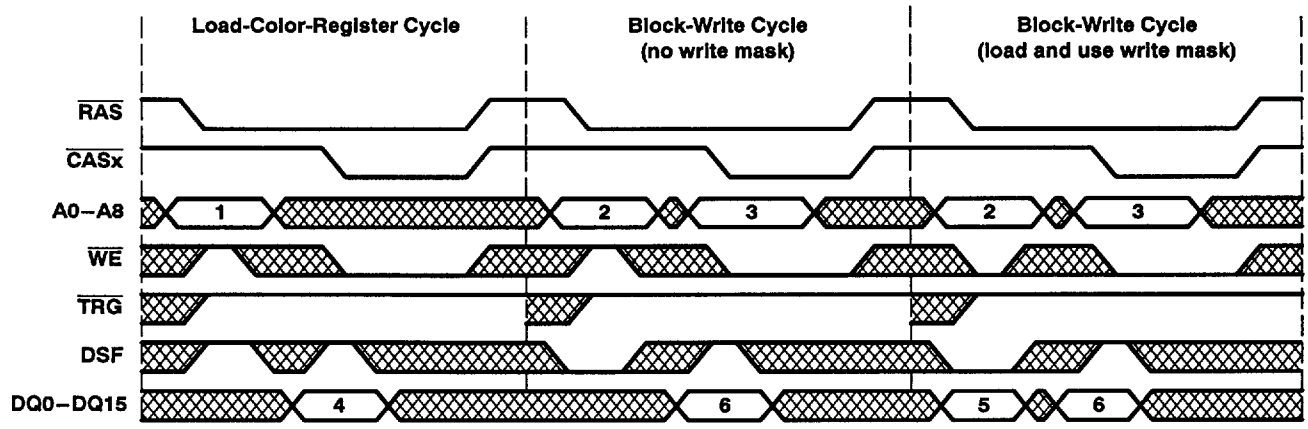


Figure 12. Example of Fourth Quadrant After a Block-Write Operation

load color register

The load-color-register cycle is performed using normal DRAM write-cycle timing except that DSF is held high on the falling edges of $\overline{RAS}$, $\overline{CASL}$, and $\overline{CASU}$. The color register is loaded from pins DQ0–DQ15, which are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later. If only one $\overline{CASx}$ is low, only the corresponding byte of the color register is loaded. When the color register is loaded, it retains data until power is lost or until another load-color-register cycle is performed (see Figure 13 and Figure 14).



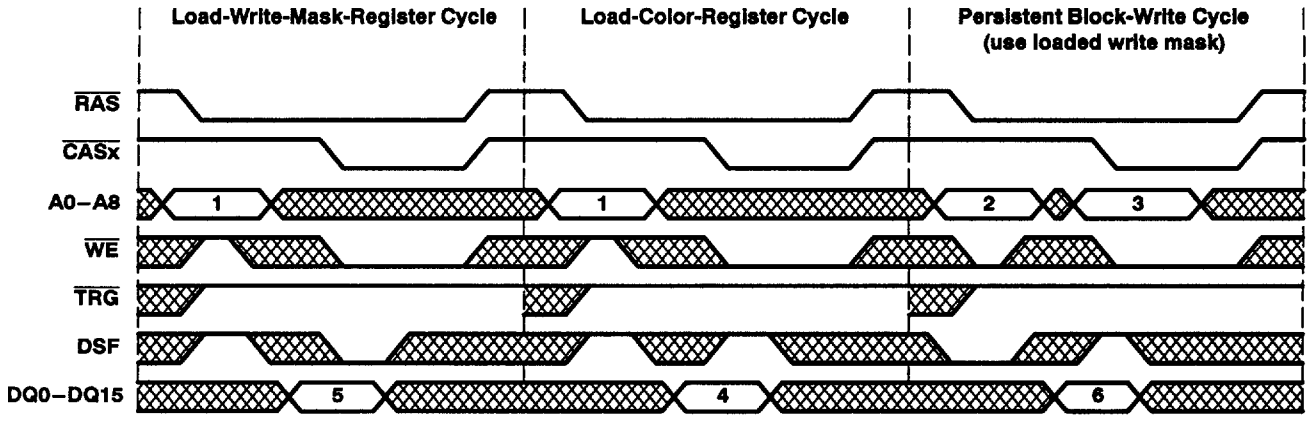
Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the first falling edge of $\overline{CASx}$.
4. Color-register data
5. Write-mask data: DQ0–DQ15 are latched on the falling edge of $\overline{RAS}$.
6. Column-mask data: DQi–DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.

= don't care

Figure 13. Example of Block Writes

load color register (continued)



Legend:

1. Refresh address
2. Row address
3. Block address (A2–A8) is latched on the first falling edge of $\overline{CASx}$.
4. Color-register data
5. Write-mask data: DQ0 – DQ15 are latched on the falling edge of $\overline{CASx}$.
6. Column-mask data: DQi – DQi+3 (i = 0, 4, 8, 12) are latched on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.

= don't care

Figure 14. Example of a Persistent Block Write

DRAM-to-SAM transfer operation

During the DRAM-to-SAM transfer operation, one half of a row (256 columns) in the DRAM array is selected to be transferred to the 256-bit serial-data register. The transfer operation is invoked by bringing $\overline{TRG}$ low and holding $\overline{WE}$ high on the falling edge of $\overline{RAS}$. The state of DSF, which is latched on the falling edge of $\overline{RAS}$, determines whether the full-register transfer read operation or the split-register transfer read operation will be performed.

Table 4. SAM Function Table

FUNCTION	$\overline{RAS}$ FALL				$\overline{CASx}$ FALL	ADDRESS		DQ0–DQ15		MNE CODE
	$\overline{CASx}$†	$\overline{TRG}$	$\overline{WE}$	DSF	DSF	$\overline{RAS}$	$\overline{CASx}$	$\overline{RAS}$	$\overline{CASx}$ $\overline{WE}$	
Full-register transfer read	H	L	H	L	X	Row Addr	Tap Point	X	X	RT
Split-register transfer read	H	L	H	H	X	Row Addr	Tap Point	X	X	SRT

† Logic L is selected when either or both $\overline{CASL}$ and $\overline{CASU}$ are low.
X = don't care

full-register transfer read

A full-register transfer read operation loads data from a selected half of a row in the DRAM into the SAM. $\overline{TRG}$ is brought low and latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. The nine column-address bits (A0–A8) are latched at the first falling edge of $\overline{CASx}$, where address bit A8 selects which half of the row is transferred. Address bits A0–A7 select one of the SAM's 256 available tap points from which the serial data is read out (see Figure 15).

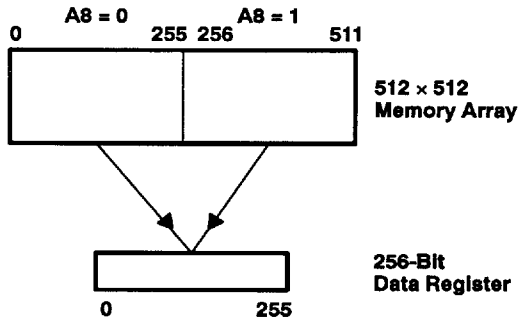


Figure 15. Full-Register Transfer Read

A full-register transfer read can be performed in three ways: early load, real-time load (or midline load), or late load. Each of these offers the flexibility of controlling the $\overline{TRG}$ trailing edge in the full-register transfer read cycle (see Figure 16).

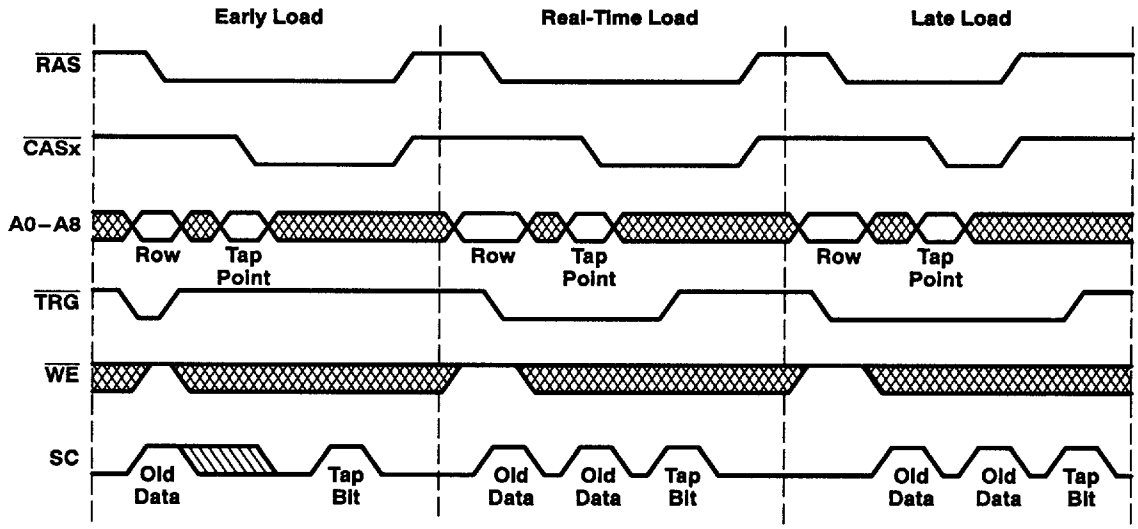


Figure 16. Example of Full-Register Transfer Read Operations

split-register transfer read

In the split-register transfer read operation, the serial-data register is split into halves. The low half contains bits 0–127, and the high half contains bits 128–255. While one half is being read out of the SAM port, the other half can be loaded from the memory array.

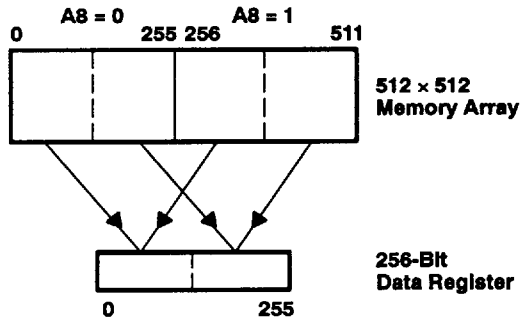
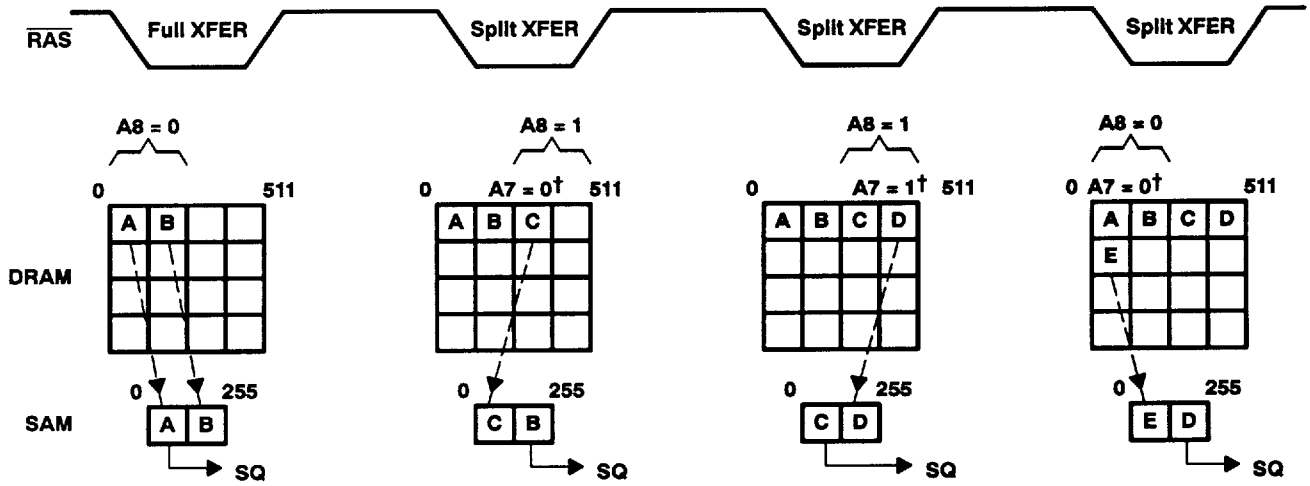


Figure 17. Split-Register Transfer Read

To invoke a split-register transfer read cycle, DSF is brought high, $\overline{TRG}$ is brought low, and both are latched at the falling edge of $\overline{RAS}$. Nine row-address bits (A0–A8) are also latched at the falling edge of $\overline{RAS}$ to select one of the 512 rows available for the transfer. Eight of the nine column-address bits (A0–A6 and A8) are latched at the first falling edge of $\overline{CAS}$x. Column-address bit A8 selects which half of the row is to be transferred. Column-address bits A0–A6 select one of the 127 tap points in the specified half of the SAM. Column-address bit A7 is ignored, and the split-register transfer is internally controlled to select the inactive register half.



† A7 shown is internally controlled.

Figure 18. Example of a Split-Register Transfer Read Operation

A full-register transfer read must precede the first split-register transfer read to ensure proper operation. After the full-register transfer read cycle, the first split-register transfer read can follow immediately without any minimum SC clock requirement.

split-register transfer read (continued)

QSF indicates which half of the register is being accessed during serial-access operation. When QSF is low, the serial-address pointer is accessing the lower (least significant) 128 bits of the SAM. When QSF is high, the pointer is accessing the higher (most significant) 128 bits of the SAM. QSF changes state upon completing a full-register transfer read cycle. The tap point loaded during the current transfer cycle determines the state of QSF. QSF also changes state when a boundary between two register halves is reached.

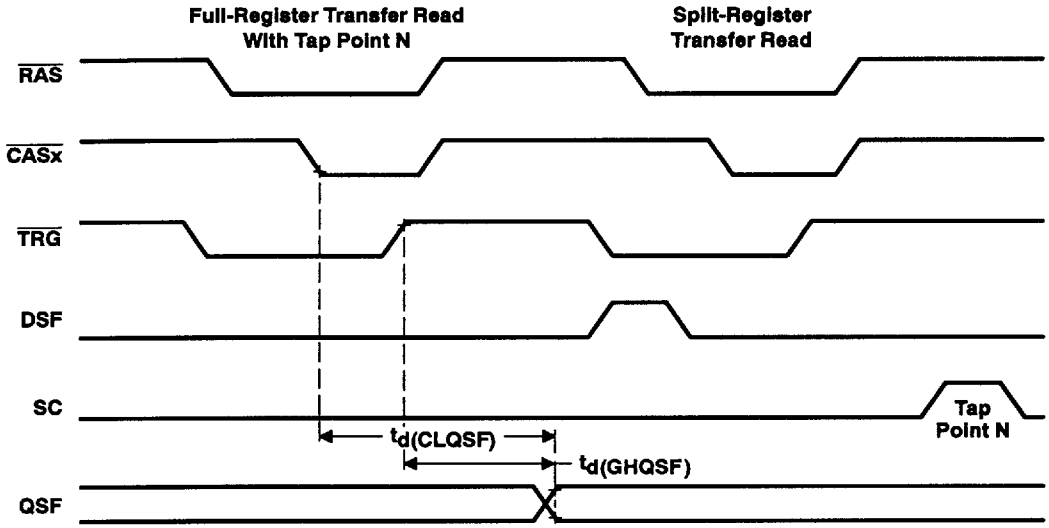


Figure 19. Example of a Split-Register Transfer Read After a Full-Register Transfer Read

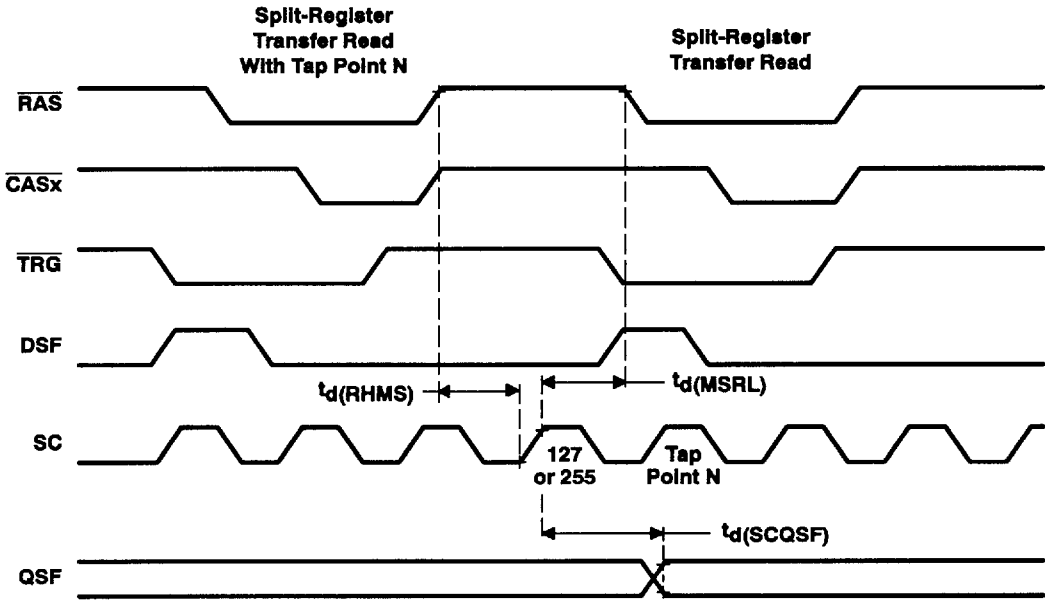


Figure 20. Example of Successive Split-Register Transfer Read Operations

serial-read operation

The serial-read operation can be performed through the SAM port simultaneously and asynchronously with DRAM operations except during transfer operations. Serial data can be read from the SAM by clocking SC starting at the tap point loaded by the preceding transfer cycle, proceeding sequentially to the most significant bit (bit 255), and then wrapping around to the least significant bit (bit 0), as shown in Figure 21.

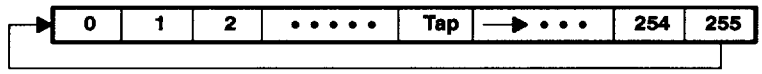


Figure 21. Serial Pointer Direction for Serial Read

For split-register transfer read operation, serial data can be read out from the active half of the SAM by clocking SC starting at the tap point loaded by the preceding split-register transfer cycle. The serial pointer then proceeds sequentially to the most-significant bit of the half, bit 127 or bit 255. If there is a split-register transfer read to the inactive half during this period, the serial pointer points next to the tap point location loaded by that split-register transfer (see Figure 22).

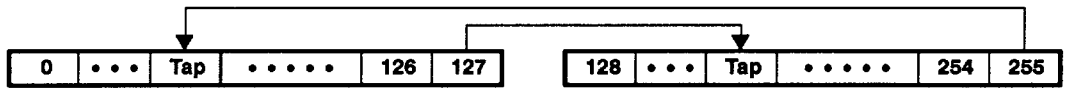


Figure 22. Serial Pointer for Split-Register Read – Case I

If there is no split-register transfer read to the inactive half during this period, the serial pointer points next to the least significant bit of the inactive half (bit 128 or bit 0) (see Figure 23).

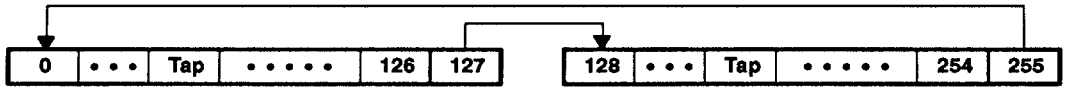


Figure 23. Serial Pointer for Split-Register Read – Case II

split-register programmable stop point

The TMS55161 offers programmable stop-point mode for split-register transfer read operation. This mode can be used to improve 2-D drawing performance in a nonscanline data format.

In split-register transfer read operation, the stop point is defined as a register location at which the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM. While in stop-point mode, the SAM is divided into partitions whose length is programmed via row addresses A4–A7 in a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ set (CBRS) cycle. The last serial-address location of each partition is the stop point (see Figure 24).

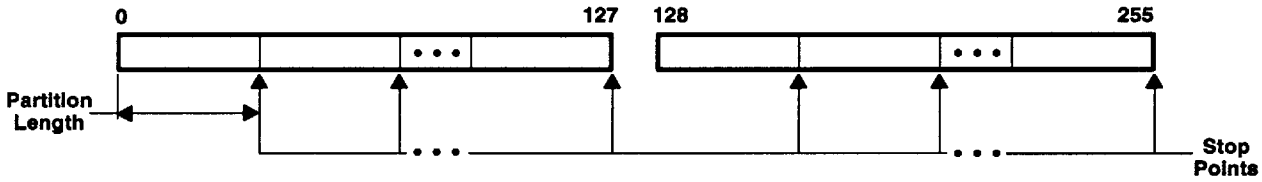


Figure 24. Example of the SAM With Partitions

split-register programmable stop point (continued)

Stop-point mode is not active until the CBRS cycle is initiated. The CBRS operation is performed by holding $\overline{CAS}$x and $\overline{WE}$ low and DSF high on the falling edge of $\overline{RAS}$. The falling edge of $\overline{RAS}$ also latches row addresses A4–A7, which are used to define the SAM's partition length. The other row-address inputs are don't care. Stop-point mode should be initiated after the initialization cycles have been performed (see Table 5).

Table 5. Programming Code for Stop-Point Mode

MAXIMUM PARTITION LENGTH	ADDRESS AT $\overline{RAS}$ IN CBRS CYCLE						NUMBER OF PARTITIONS	STOP-POINT LOCATIONS
	A8	A7	A6	A5	A4	A0–A3		
16	X	L	L	L	L	X	16	15, 31, 47, 63, 79, 95, 111, 127, 143, 159, 175, 191, 207, 223, 239, 255
32	X	L	L	L	H	X	8	31, 63, 95, 127, 159, 191, 223, 255
64	X	L	L	H	H	X	4	63, 127, 191, 255
128 (default)	X	L	H	H	H	X	2	127, 255

In stop-point mode, the tap point loaded during the split-register transfer read cycle determines in which SAM partition the serial output begins and at which stop point the serial output stops coming from one half of the SAM and switches to the opposite half of the SAM (see Figure 25).

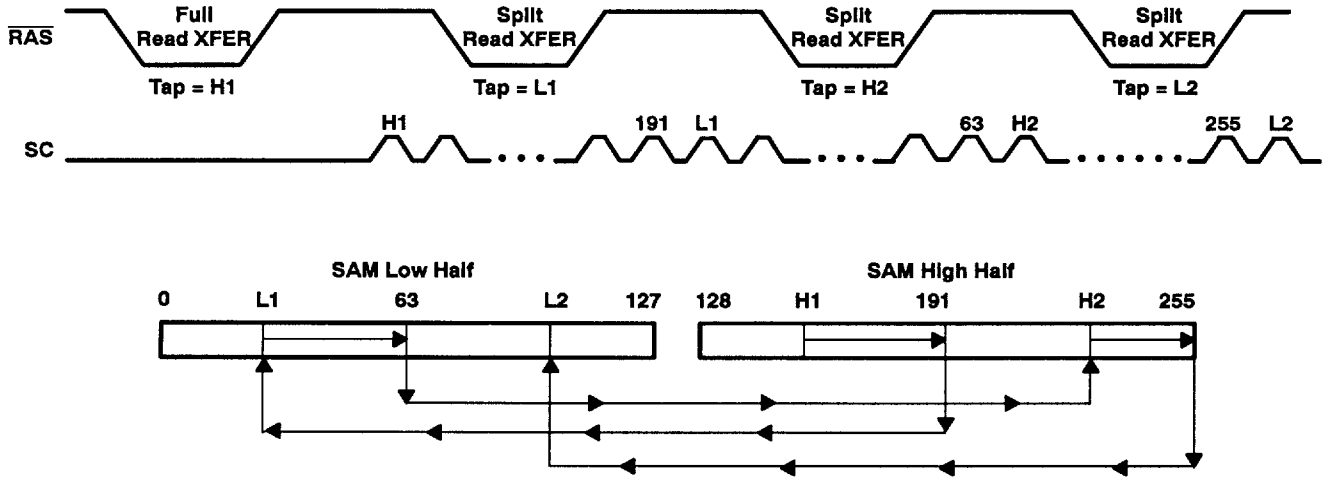


Figure 25. Example of Split-Register Operation With Programmable Stop Points

256-/512-bit compatibility of split-register programmable stop point

The stop-point mode is designed to be compatible both for 256-bit SAM and 512-bit SAM devices. After the CBRS cycle is initiated, the stop-point mode becomes active. In the stop-point mode, and only in the stop-point mode, the column-address bits AY7 and AY8 are internally swapped to assure the compatibility (see Figure 26). This address-bit swap applies to the column address, and it is effective for all DRAM and transfer cycles. For example, during the split-register transfer cycle with stop point, column-address bit AY8 is a don't care and AY7 decodes the DRAM row half for the split-register transfer. During stop-point mode, a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ option reset (CBR) cycle is not recommended because it ends the stop-point mode and restores address bits AY7 and AY8 to their normal function. Consistent use of CBR cycles ensures that the TMS55161 remains in normal mode.

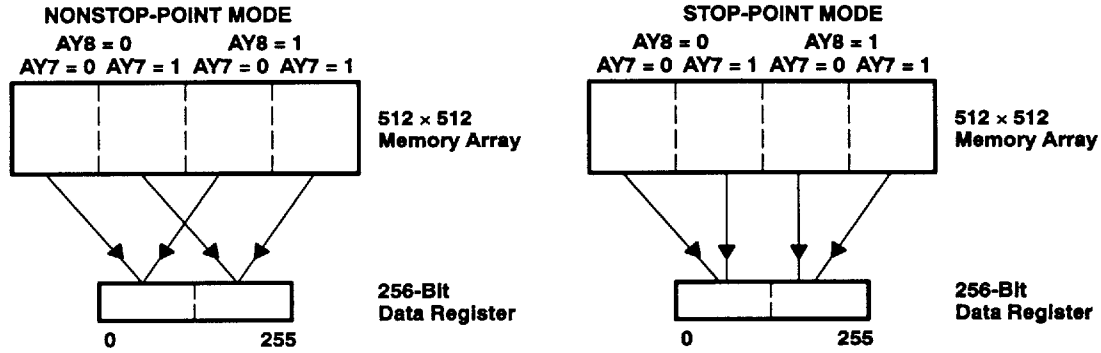


Figure 26. DRAM-to-SAM Mapping, Nonstop Point Versus Stop Point

IMPORTANT: For proper device operation in a split-register stop-point mode, a CBRS cycle should be initiated right after the power-up initialization cycles have been performed.

power up

To achieve proper device operation, an initial pause of 200 µs is required after power up followed by a minimum of eight $\overline{\text{RAS}}$ cycles or eight $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ cycles to initialize the DRAM port. A full-register transfer read cycle and two SC cycles are needed to initialize the SAM port.

After initialization, the internal state of the TMS55161 is as follows:

	STATE AFTER INITIALIZATION
QSF	Defined by the transfer cycle during initialization
Write mode	Nonpersistent mode
Write mask register	Undefined
Color register	Undefined
Serial-register tap point	Defined by the transfer cycle during initialization
SAM port	Output mode

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) ..... −1 V to 7 V
Input voltage range ..... −1 V to 7 V
Short-circuit output current ..... 50 mA
Power dissipation ..... 1.1 W
Operating free-air temperature range, T_A ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SAM PORT	'55161-60		'55161-70		'55161-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −1 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 5.8 V, All other pins at 0 V to V_{CC}			±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 V to V_{CC} See Note 3			±10		±10		±10	µA
I_{CC1}	Operating current‡	See Note 4	Standby		180		165		150	mA
I_{CC1A}	Operating current‡	$t_{c(SC)}$ = MIN	Active		225		205		185	mA
I_{CC2}	Standby current	All clocks = V_{CC}	Standby		5		5		5	mA
I_{CC2A}	Standby current	$t_{c(SC)}$ = MIN	Active		70		65		60	mA
I_{CC3}	$\overline{RAS}$-only refresh current	See Note 4	Standby		180		165		150	mA
I_{CC3A}	$\overline{RAS}$-only refresh current	$t_{c(SC)}$ = MIN, See Note 4	Active		225		205		185	mA
I_{CC4}	Page-mode current‡	$t_{c(P)}$ = MIN, See Note 5	Standby		140		140		120	mA
I_{CC4A}	Page-mode current‡	$t_{c(SC)}$ = MIN, See Note 5	Active		185		185		165	mA
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ current	See Note 4	Standby		180		165		150	mA
I_{CC5A}	$\overline{CAS}$-before-$\overline{RAS}$ current	$t_{c(SC)}$ = MIN, See Note 4	Active		225		205		185	mA
I_{CC6}	Data-transfer current	See Note 4	Standby		200		180		160	mA
I_{CC6A}	Data-transfer current	$t_{c(SC)}$ = MIN	Active		250		225		200	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open

NOTES: 3. $\overline{SE}$ is disabled for SQ output leakage tests.
4. Measured with one address change while $\overline{RAS}$ = V_{IL}, $t_{c(rd)}$, $t_{c(W)}$, $t_{c(TRD)}$ = MIN.
5. Measured with one address change while $\overline{CASx}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 6)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, address strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write enable input		7	pF
$C_{i(SC)}$	Input capacitance, serial clock		7	pF
$C_{i(SE)}$	Input capacitance, serial enable		7	pF
$C_{i(DSF)}$	Input capacitance, special function		7	pF
$C_{i(TRG)}$	Input capacitance, transfer register input		7	pF
$C_{o(O)}$	Output capacitance, SQ and DQ		7	pF
$C_{o(QSF)}$	Output capacitance, QSF		9	pF

NOTE 6: V_{CC} = 5 V ± 0.5 V, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 7)

PARAMETER		TEST CONDITIONS†	ALT. SYMBOL	'55161-60		'55161-70		'55161-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CASx}$	$t_{d(RLCL)}$ = MAX	t_{CAC}		17		20		20	ns
$t_{a(CA)}$	Access time from column address	$t_{d(RLCL)}$ = MAX	t_{AA}		30		35		40	ns
$t_{a(CP)}$	Access time from $\overline{CASx}$ high	$t_{d(RLCL)}$ = MAX	t_{CPA}		35		40		45	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	$t_{d(RLCL)}$ = MAX	t_{RAC}		60		70		80	ns
$t_{a(G)}$	Access time of DQ from $\overline{TRG}$ low		t_{OEA}		15		20		20	ns
$t_{a(SQ)}$	Access time of SQ from SC high	C_L = 30 pF	t_{SCA}		15		20		25	ns
$t_{a(SE)}$	Access time of SQ from $\overline{SE}$ low	C_L = 30 pF	t_{SEA}		12		15		20	ns
$t_{dis(CH)}$	Disable time, random output from $\overline{CASx}$ high (see Note 8)	C_L = 50 pF	t_{OFF}	0	15	0	20	0	20	ns
$t_{dis(RH)}$	Disable time, random output from $\overline{RAS}$ high (see Note 8)	C_L = 50 pF		0	15	0	20	0	20	ns
$t_{dis(G)}$	Disable time, random output from $\overline{TRG}$ high (see Note 8)	C_L = 50 pF	t_{OEZ}	0	15	0	20	0	20	ns
$t_{dis(WL)}$	Disable time, random output from $\overline{WE}$ low (see Note 8)	C_L = 30 pF	t_{WEZ}	0	15	0	20	0	20	ns
$t_{dis(SE)}$	Disable time, serial output from $\overline{SE}$ high (see Note 8)	C_L = 30 pF	t_{SEZ}	0	10	0	15	0	20	ns

† Measured with outputs open. For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.

NOTES: 7. Switching times for RAM port output are measured with a load equivalent to 1 TTL load and 50 pF. Data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V. Switching times for SAM port output are measured with a load equivalent to 1 TTL load and 30 pF. Serial data out reference level: V_{OH} / V_{OL} = 2 V/0.8 V.

8. $t_{dis(CH)}$, $t_{dis(RH)}$, $t_{dis(G)}$, $t_{dis(WL)}$, and $t_{dis(SE)}$ are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature†

		ALT. SYMBOL	'55161-60		'55161-70		'55161-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Cycle time, read	t_{RC}	110		130		150		ns
$t_{c(W)}$	Cycle time, write	t_{WC}	110		130		150		ns
$t_{c(rdW)}$	Cycle time, read-modify-write	t_{RMW}	150		175		200		ns
$t_{c(P)}$	Cycle time, page-mode read, write	t_{PC}	30		30		35		ns
$t_{c(RDWP)}$	Cycle time, page-mode read-modify-write	t_{PRMW}	80		90		100		ns
$t_{c(TRD)}$	Cycle time, transfer read	t_{RC}	110		130		150		ns
$t_{c(SC)}$	Cycle time, serial clock (see Note 9)	t_{SCC}	18		22		30		ns
$t_{w(CH)}$	Pulse duration, $\overline{CASx}$ high	t_{CPN}	10		10		10		ns
$t_{w(CL)}$	Pulse duration, $\overline{CASx}$ low (see Note 10)	t_{CAS}	10	10 000	10	10 000	20	10 000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high	t_{RP}	40		50		60		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low (see Note 11)	t_{RAS}	60	10 000	70	10 000	80	10 000	ns
$t_{w(WL)}$	Pulse duration, $\overline{WE}$ low	t_{WP}	10		10		15		ns
$t_{w(TRG)}$	Pulse duration, $\overline{TRG}$ low		15		20		20		ns
$t_{w(SCH)}$	Pulse duration, SC high (see Note 9)	t_{SC}	5		8		10		ns
$t_{w(SCL)}$	Pulse duration, SC low (see Note 9)	t_{SCP}	5		8		10		ns
$t_{w(GH)}$	Pulse duration, $\overline{TRG}$ high	t_{TP}	20		20		20		ns
$t_{w(RL)P}$	Pulse duration, $\overline{RAS}$ low (page mode)	t_{RASP}	60	100 000	70	100 000	80	100 000	ns
$t_{su(CA)}$	Setup time, column address before $\overline{CASx}$ low	t_{ASC}	0		0		0		ns
$t_{su(SFC)}$	Setup time, DSF before $\overline{CASx}$ low	t_{FSC}	0		0		0		ns
$t_{su(RA)}$	Setup time, row address before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(WMR)}$	Setup time, $\overline{WE}$ before $\overline{RAS}$ low	t_{WSR}	0		0		0		ns
$t_{su(DQR)}$	Setup time, DQ before $\overline{RAS}$ low	t_{MS}	0		0		0		ns
$t_{su(TRG)}$	Setup time, $\overline{TRG}$ high before $\overline{RAS}$ low	t_{THS}	0		0		0		ns
$t_{su(SFR)}$	Setup time, DSF low before $\overline{RAS}$ low	t_{FSR}	0		0		0		ns
$t_{su(DCL)}$	Setup time, data valid before $\overline{CASx}$ low	t_{DSC}	0		0		0		ns
$t_{su(DWL)}$	Setup time, data valid before $\overline{WE}$ low	t_{DSW}	0		0		0		ns
$t_{su(rd)}$	Setup time, read command, $\overline{WE}$ high before $\overline{CASx}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	Setup time, early write command, $\overline{WE}$ low before $\overline{CASx}$ low	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	Setup time, $\overline{WE}$ low before $\overline{CASx}$ high, write	t_{CWL}	15		15		20		ns
$t_{su(WRH)}$	Setup time, $\overline{WE}$ low before $\overline{RAS}$ high, write	t_{RWL}	15		15		20		ns
$t_{h(CLCA)}$	Hold time, column address after $\overline{CASx}$ low	t_{CAH}	10		10		15		ns
$t_{h(SFC)}$	Hold time, DSF after $\overline{CASx}$ low	t_{CFH}	10		10		15		ns
$t_{h(RA)}$	Hold time, row address after $\overline{RAS}$ low	t_{RAH}	10		10		10		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 9. Cycle time assumes t_t = 3 ns.

10. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CASx}$ low time [$t_{w(CL)}$].

11. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)†

			ALT. SYMBOL	'55161-60		'55161-70		'55161-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(TRG)}$	Hold time, $\overline{TRG}$ after $\overline{RAS}$ low		t_{THH}	10		10		10		ns
$t_{h(RWM)}$	Hold time, write mask after $\overline{RAS}$ low		t_{RWH}	10		10		10		ns
$t_{h(RDQ)}$	Hold time, DQ after $\overline{RAS}$ low (write-mask operation)		t_{MH}	10		10		10		ns
$t_{h(SFR)}$	Hold time, DSF after $\overline{RAS}$ low		t_{RFH}	10		10		10		ns
$t_{h(RLCA)}$	Hold time, column address valid after $\overline{RAS}$ low (see Note 12)		t_{AR}	30		30		35		ns
$t_{h(CLD)}$	Hold time, data valid after $\overline{CASx}$ low		t_{DH}	15		15		15		ns
$t_{h(RLD)}$	Hold time, data valid after $\overline{RAS}$ low (see Note 12)		t_{DHR}	35		35		35		ns
$t_{h(WLD)}$	Hold time, data valid after $\overline{WE}$ low		t_{DH}	15		15		15		ns
$t_{h(CHrd)}$	Hold time, read, $\overline{WE}$ high after $\overline{CASx}$ high (see Note 13)		t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Hold time, read, $\overline{WE}$ high after $\overline{RAS}$ high (see Note 13)		t_{RRH}	0		0		0		ns
$t_{h(CLW)}$	Hold time, write, $\overline{WE}$ low after $\overline{CASx}$ low		t_{WCH}	10		15		15		ns
$t_{h(RLW)}$	Hold time, write, $\overline{WE}$ low after $\overline{RAS}$ low (see Note 12)		t_{WCR}	30		35		35		ns
$t_{h(WLG)}$	Hold time, $\overline{TRG}$ high after $\overline{WE}$ low (see Note 14)		t_{OEH}	10		10		10		ns
$t_{h(SHSQ)}$	Hold time, SQ valid after SC high		t_{SOH}	4		5		5		ns
$t_{h(RSF)}$	Hold time, DSF after $\overline{RAS}$ low		t_{FHR}	30		30		35		ns
$t_{h(CLQ)}$	Hold time, output valid after $\overline{CASx}$ low		t_{DHC}	4		5		5		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ high		t_{CSH}	53		60		80		ns
		See Note 15	t_{CHR}	10		10		15		
$t_{d(CHRL)}$	Delay time, $\overline{CASx}$ high to $\overline{RAS}$ low		t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ high		t_{RSH}	17		20		20		ns
$t_{d(CLWL)}$	Delay time, $\overline{CASx}$ low to $\overline{WE}$ low (see Notes 16 and 17)		t_{CWD}	37		45		45		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CASx}$ low (see Note 18)		t_{RCD}	20	43	20	50	20	60	ns
$t_{d(CARH)}$	Delay time, column address valid to $\overline{RAS}$ high		t_{RAL}	30		35		40		ns
$t_{d(CACH)}$	Delay time, column address valid to $\overline{CASx}$ high		t_{CAL}	30		35		40		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{WE}$ low (see Note 16)		t_{RWD}	80		95		105		ns
$t_{d(CAWL)}$	Delay time, column address valid to $\overline{WE}$ low (see Note 16)		t_{AWD}	50		60		65		ns
$t_{d(CLRL)}$	Delay time, $\overline{CASx}$ low to $\overline{RAS}$ low (see Note 15)		t_{CSR}	0		0		0		ns
$t_{d(RHCL)}$	Delay time, $\overline{RAS}$ high to $\overline{CASx}$ low (see Note 15)		t_{RPC}	0		0		0		ns
$t_{d(CLGH)}$	Delay time, $\overline{CASx}$ low to $\overline{TRG}$ high for DRAM read cycles			17		20		20		ns
$t_{d(GHD)}$	Delay time, $\overline{TRG}$ high before data applied at DQ		t_{OED}	10		15		15		ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 12. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
13. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
14. Output-enable-controlled write. Output remains in the high-impedance state for the entire cycle.
15. $\overline{CAS}$-before-$\overline{RAS}$ refresh operation only
16. Read-modify-write operation only
17. $\overline{TRG}$ must disable the output buffers prior to applying data to the DQ pins.
18. The maximum value is specified only to assure $\overline{RAS}$ access time.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)†

		ALT. SYMBOL	'55161-60		'55161-70		'55161-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(RLTH)}$	Delay time, $\overline{RAS}$ low to $\overline{TRG}$ high (see Note 19)	t_{RTH}	50		55		60		ns
$t_{d(RLSH)}$	Delay time, $\overline{RAS}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t_{RSD}	65		70		80		ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address valid	t_{RAD}	15	30	15	35	15	40	ns
$t_{d(GLRH)}$	Delay time, $\overline{TRG}$ low to $\overline{RAS}$ high	t_{ROH}	10		15		15		ns
$t_{d(CLSH)}$	Delay time, $\overline{CASx}$ low to first SC high after $\overline{TRG}$ high (see Note 20)	t_{CSD}	20		20		25		ns
$t_{d(SCTR)}$	Delay time, SC high to $\overline{TRG}$ high (see Notes 19 and 20)	t_{TSL}	5		5		5		ns
$t_{d(THRH)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ high (see Note 19)	t_{TRD}	−10		−10		−10		ns
$t_{d(THRL)}$	Delay time, $\overline{TRG}$ high to $\overline{RAS}$ low (see Note 21)	t_{TRP}	40		50		60		ns
$t_{d(THSC)}$	Delay time, $\overline{TRG}$ high to SC high (see Note 19)	t_{TSD}	10		10		15		ns
$t_{d(RHMS)}$	Delay time, $\overline{RAS}$ high to last (most significant) rising edge of SC before boundary switch during split-register transfer read cycles		15		20		20		ns
$t_{d(CLTH)}$	Delay time, $\overline{CASx}$ low to $\overline{TRG}$ high in real-time transfer read cycles	t_{CTH}	15		15		15		ns
$t_{d(CASH)}$	Delay time, column address to first SC in early-load transfer read cycles	t_{ASD}	25		25		30		ns
$t_{d(CAGH)}$	Delay time, column address to $\overline{TRG}$ high in real-time transfer read cycles	t_{ATH}	20		20		20		ns
$t_{d(DCL)}$	Delay time, data to $\overline{CASx}$ low	t_{DZC}	0		0		0		ns
$t_{d(DGL)}$	Delay time, data to $\overline{TRG}$ low	t_{DZO}	0		0		0		ns
$t_{d(MSRL)}$	Delay time, last (most significant) rising edge of SC to $\overline{RAS}$ low before boundary switch during split-register transfer read cycles		15		20		20		ns
$t_{d(SCQSF)}$	Delay time, last (127 or 255) rising edge of SC to QSF switching at the boundary during split-register transfer read cycles (see Note 22)	t_{SQD}		20		25		30	ns
$t_{d(CLQSF)}$	Delay time, $\overline{CASx}$ low to QSF switching in transfer read cycles (see Note 22)	t_{CQD}		25		30		35	ns
$t_{d(GHQSF)}$	Delay time, $\overline{TRG}$ high to QSF switching in transfer read cycles (see Note 22)	t_{TQD}		20		25		30	ns
$t_{d(RLQSF)}$	Delay time, $\overline{RAS}$ low to QSF switching in transfer read cycles (see Note 22)	t_{RQD}		65		70		75	ns
$t_{rf(MA)}$	Refresh time interval, memory	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

† Timing measurements are referenced to V_{IL} max and V_{IH} min.

NOTES: 19. Real-time load transfer read or late-load transfer read cycle only
20. Early-load transfer read cycle only
21. Full-register (read) transfer cycles only
22. Switching times for QSF output are measured with a load equivalent to 1 TTL load and 30 pF and output reference level is V_{OH} / V_{OL} = 2 V/0.8 V.

PARAMETER MEASUREMENT INFORMATION

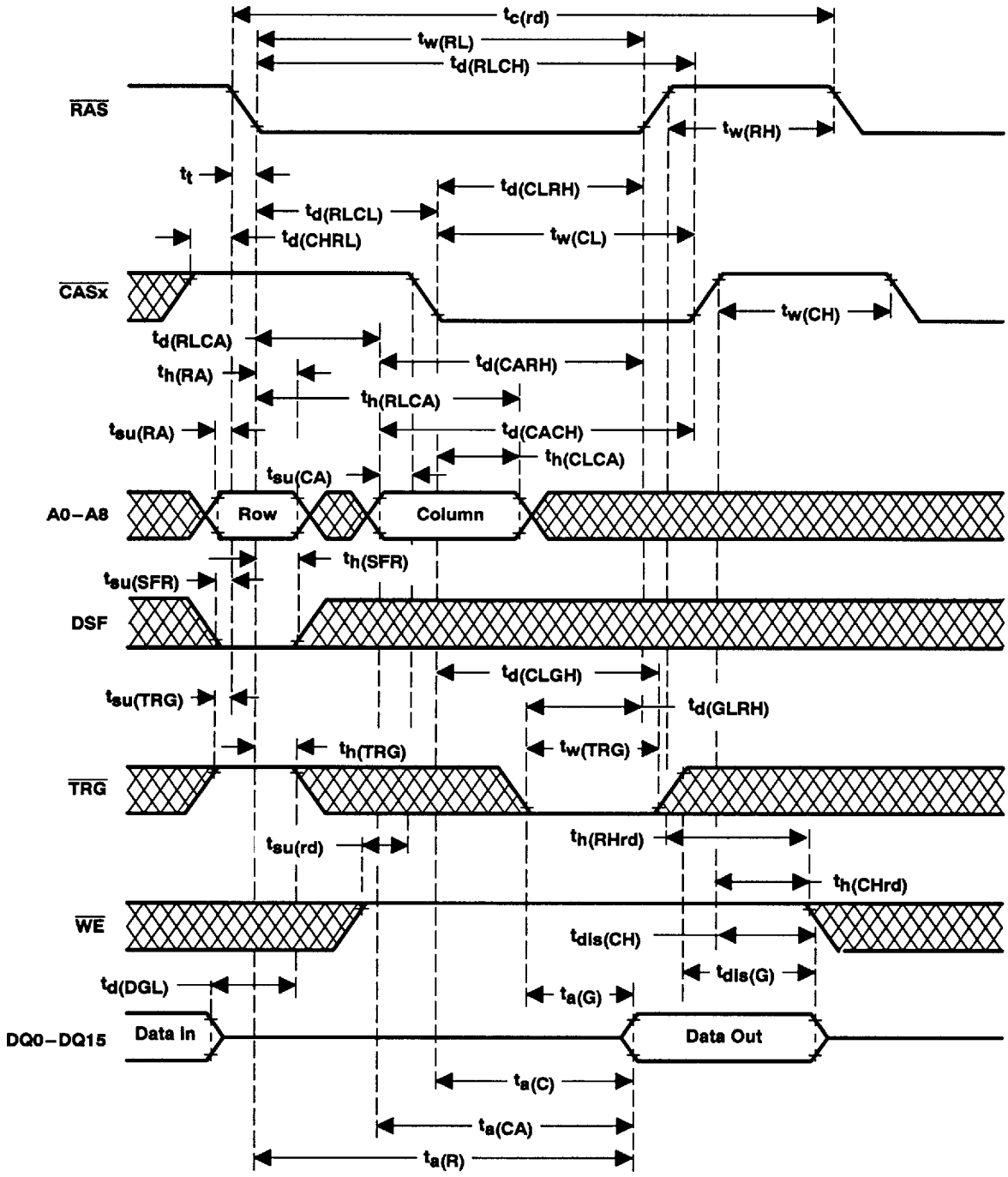


Figure 27. Read-Cycle Timing With $\overline{\text{CASx}}$-Controlled Output

PARAMETER MEASUREMENT INFORMATION

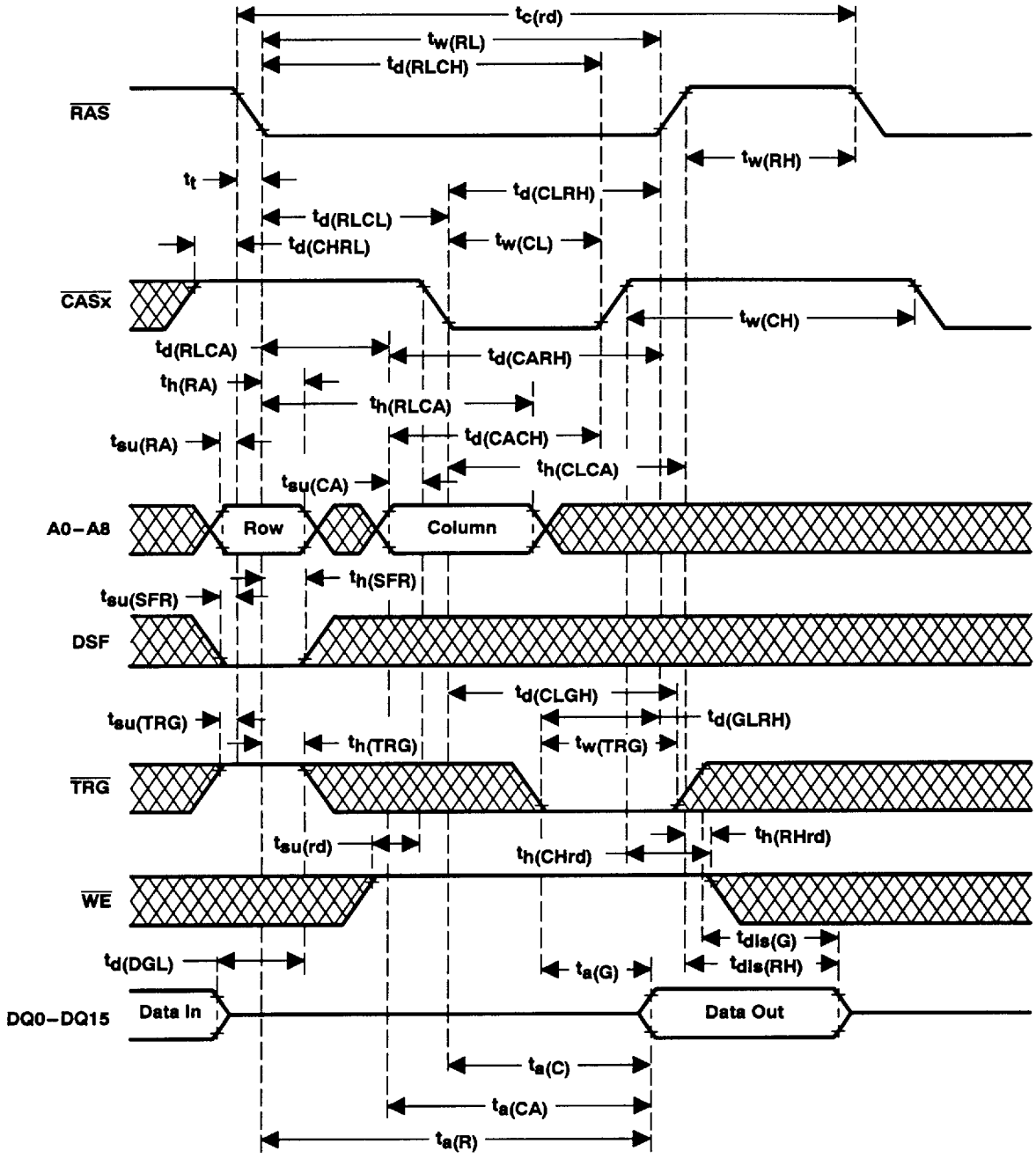


Figure 28. Read-Cycle Timing With $\overline{RAS}$-Controlled Output

PARAMETER MEASUREMENT INFORMATION

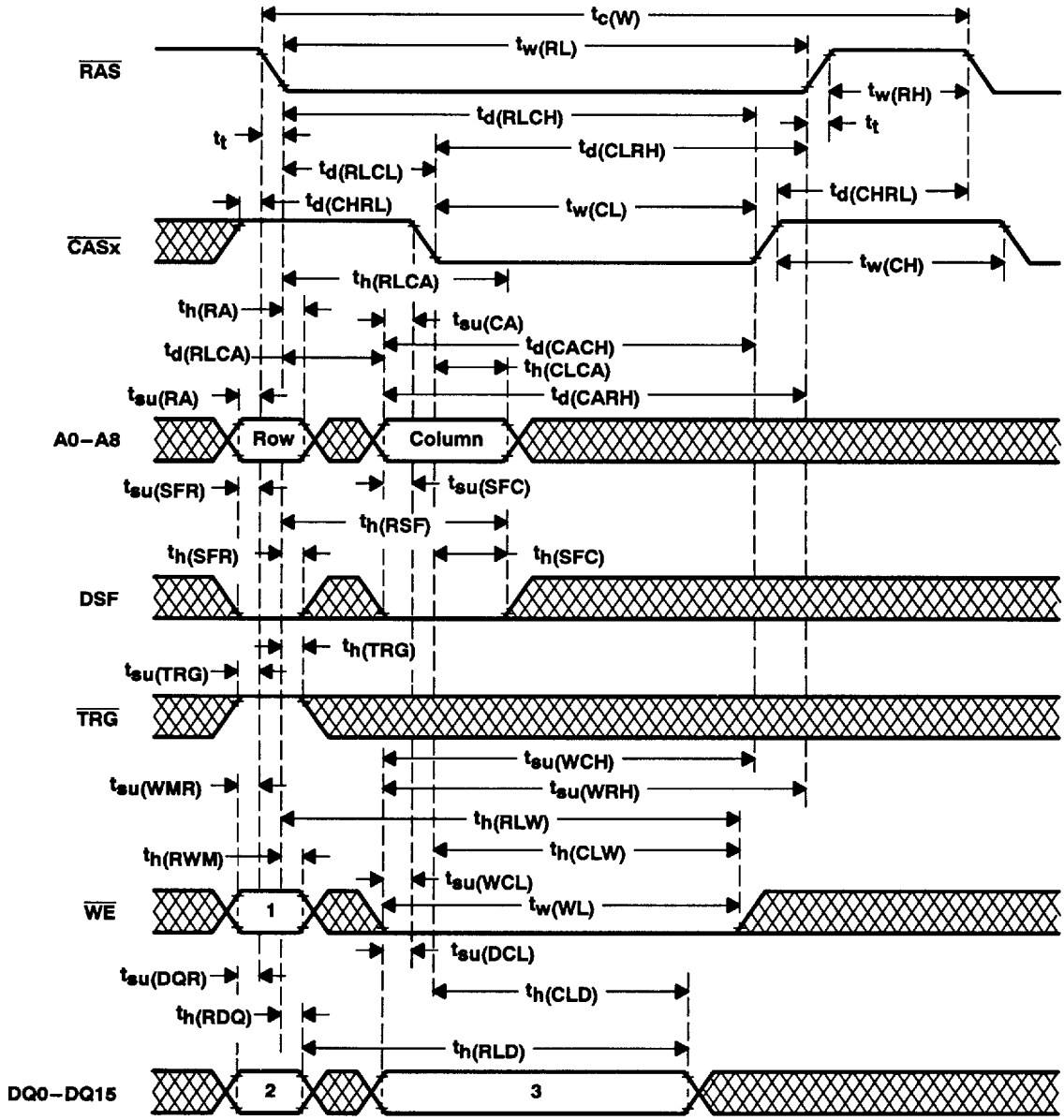


Figure 29. Early-Write-Cycle Timing

Table 6. Early-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

PARAMETER MEASUREMENT INFORMATION

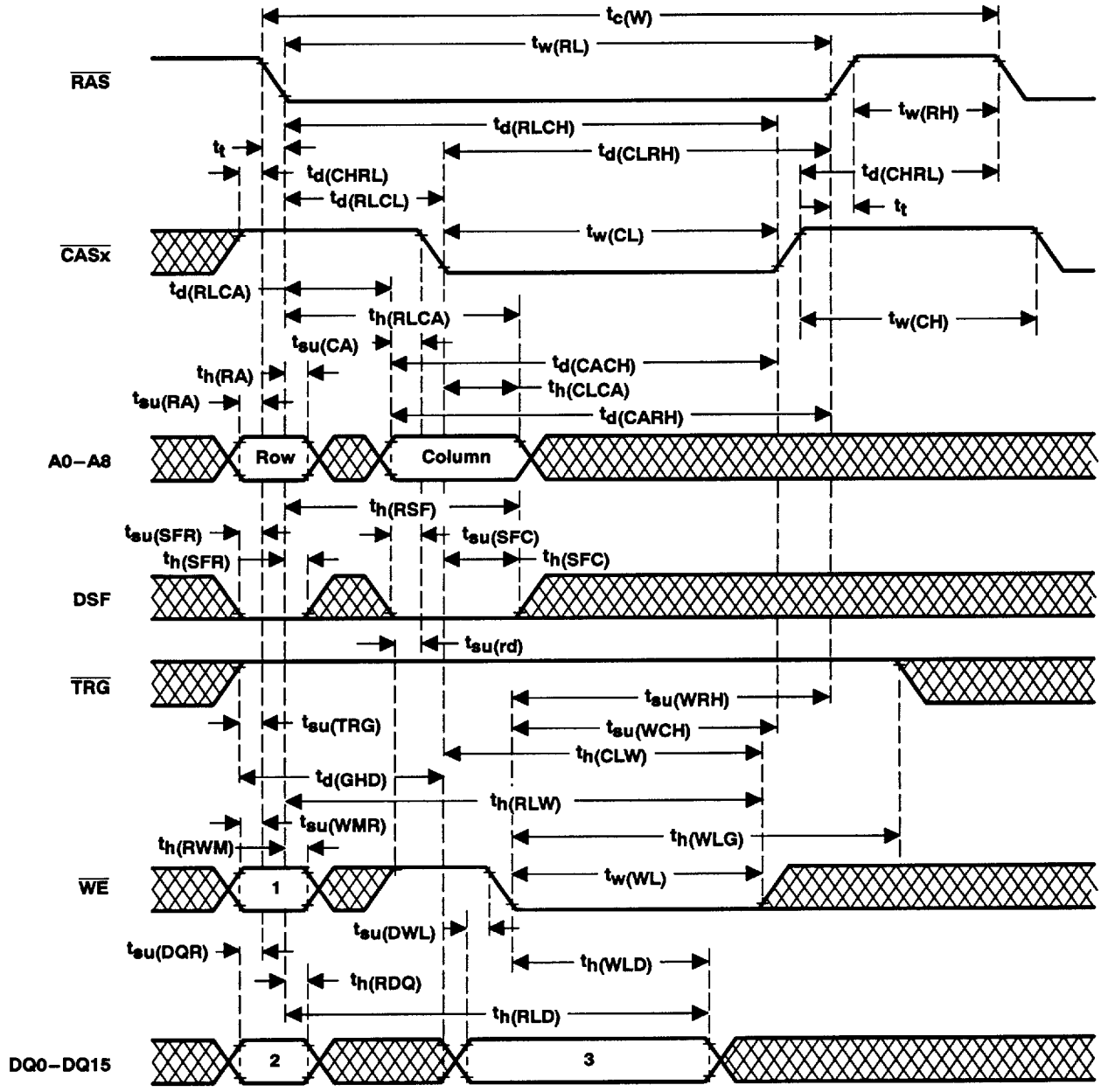
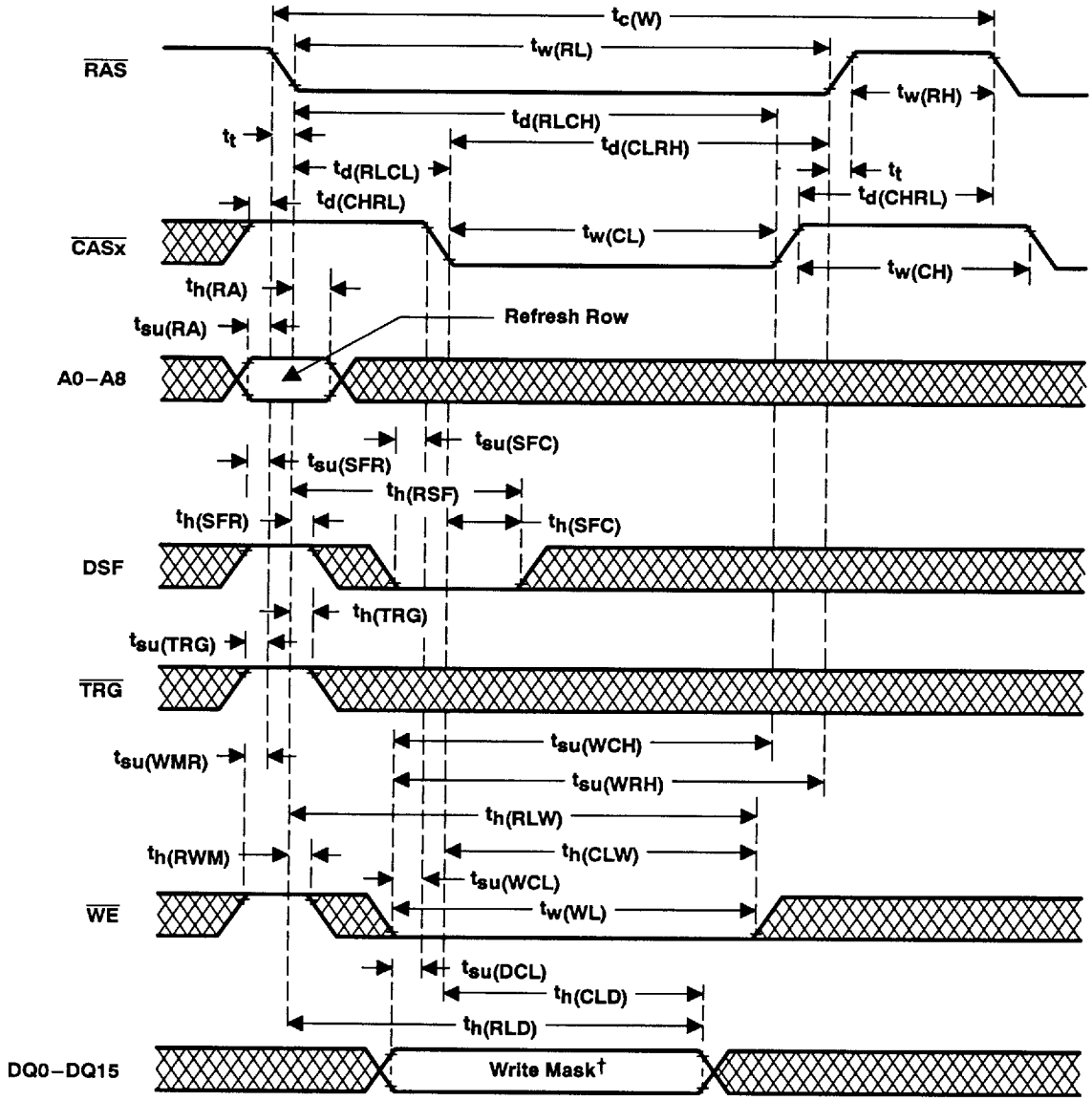


Figure 30. Late-Write-Cycle Timing (Output-Enable-Controlled Write)

Table 7. Late-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

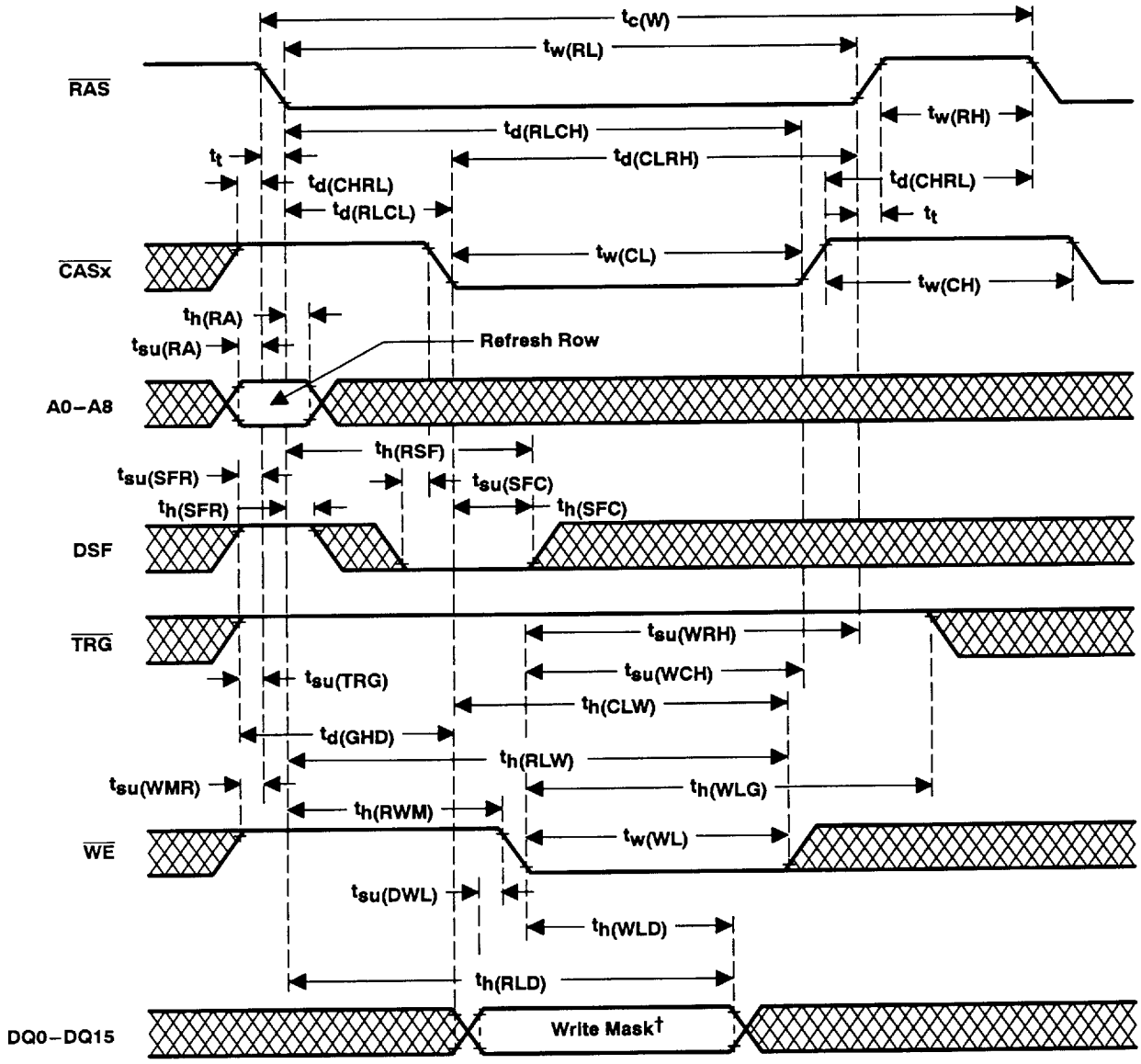
PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle will put the device into the persistent write-per-bit mode.

Figure 31. Load-Write-Mask-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION



† Load-write-mask-register cycle will put the device into the persistent write-per-bit mode.

Figure 32. Load-Write-Mask-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

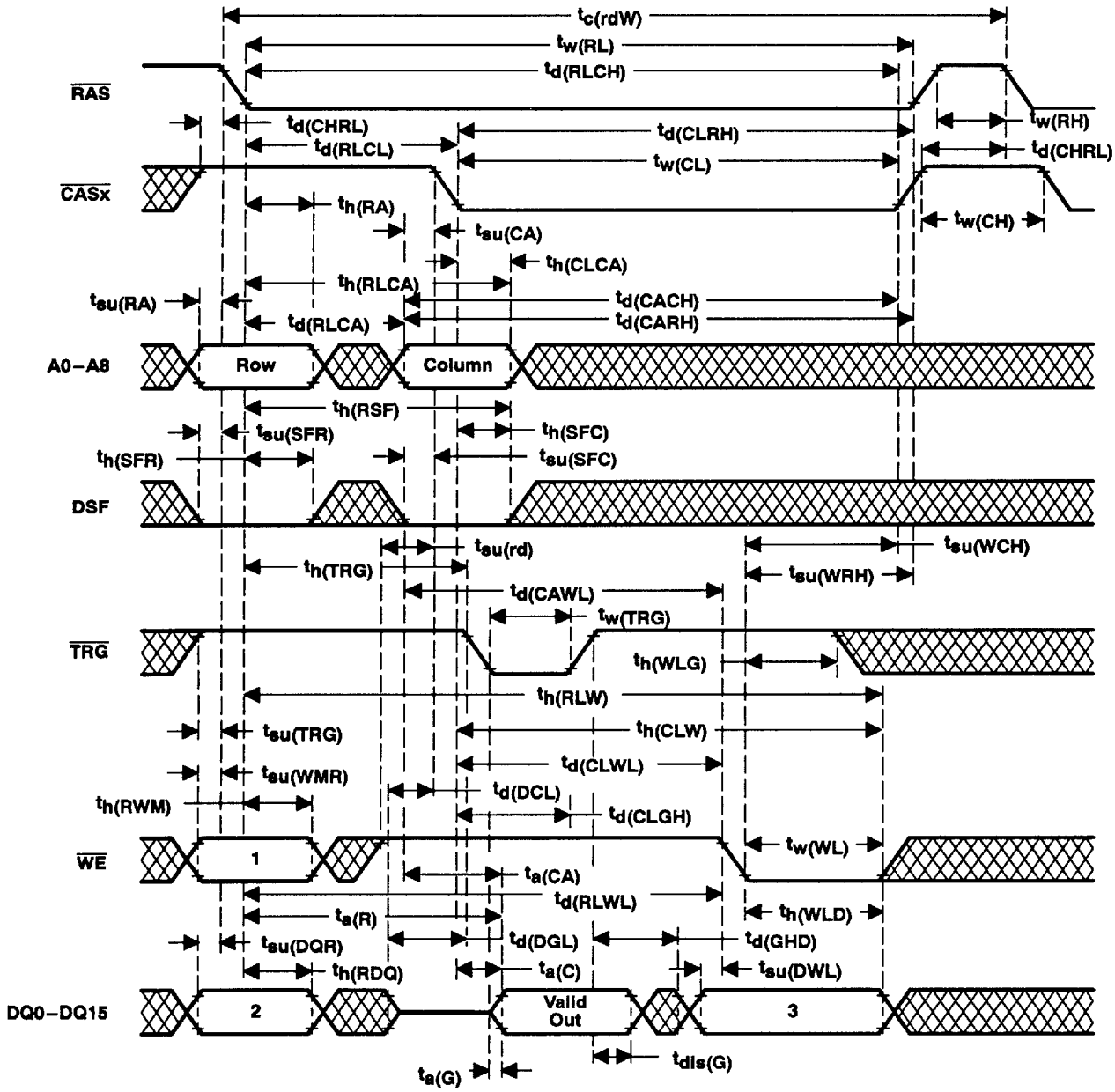
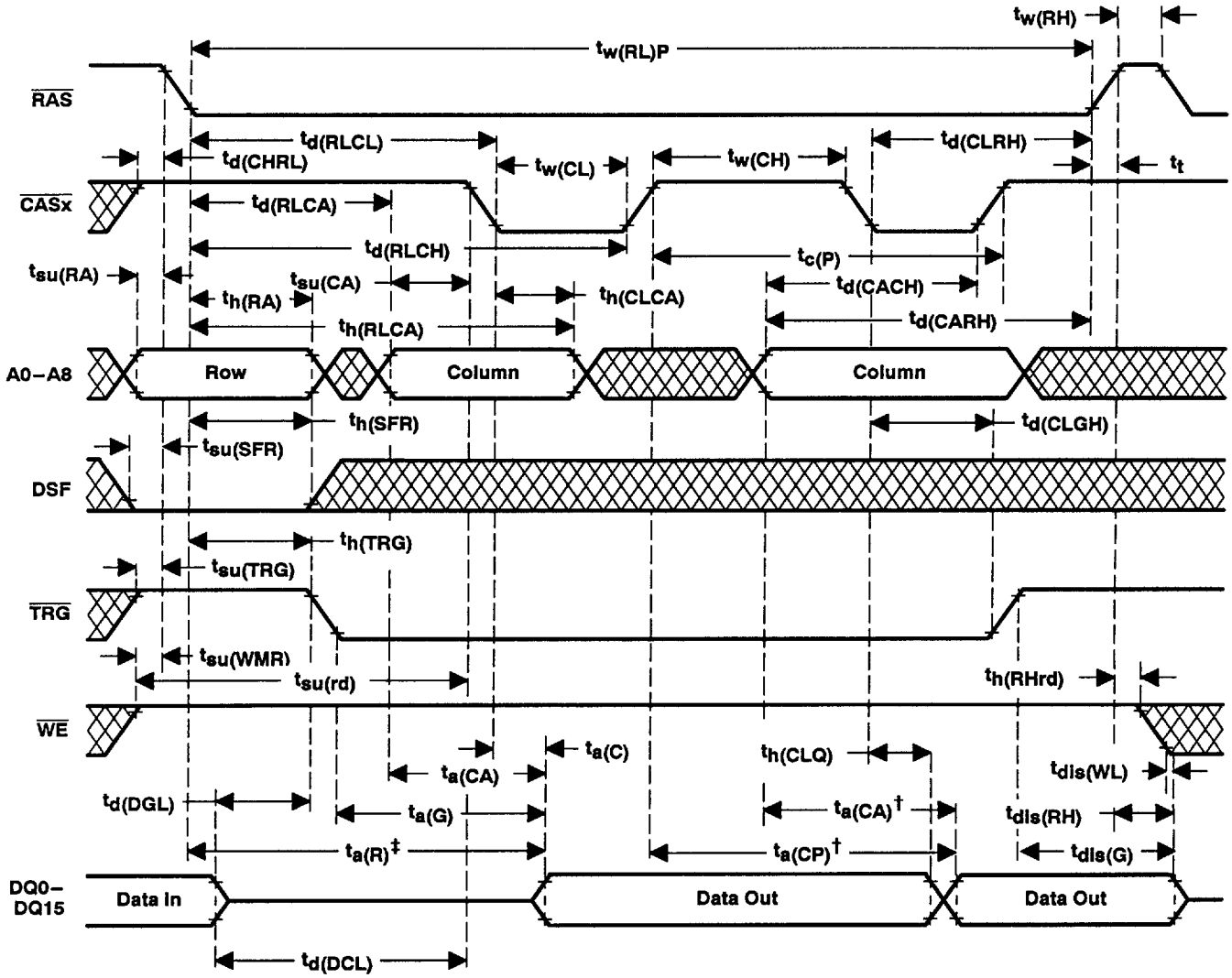


Figure 33. Read-Write/Read-Modify-Write-Cycle Timing

Table 8. Read-Write/Read-Modify-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Write operation (nonmasked)	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	Don't care	Valid data

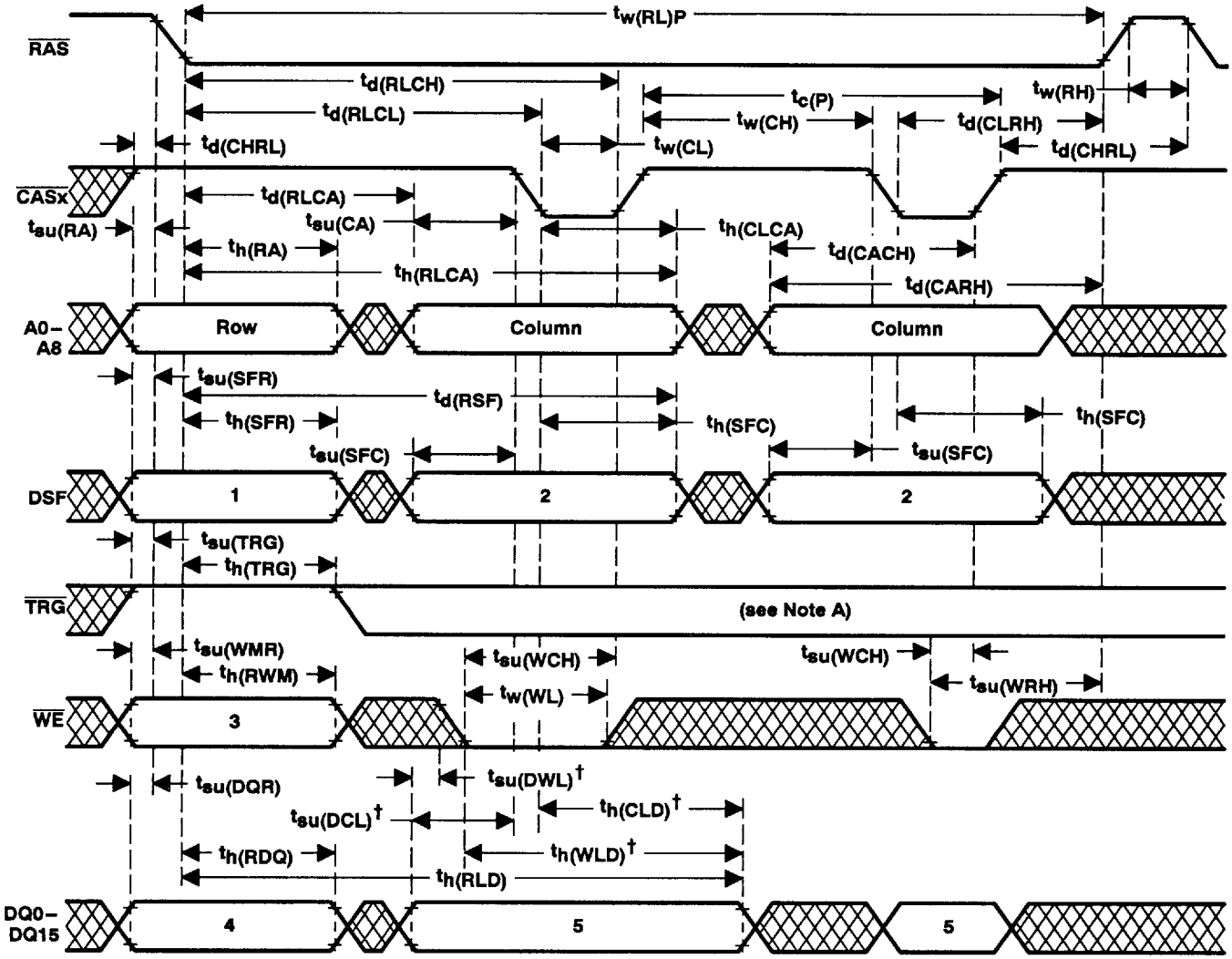
PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.
‡ Output can go from the high-impedance state to an invalid data state prior to the specified access time.
NOTE A: A write cycle or a read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated and the proper polarity of DSF is selected on the falling edge of $\overline{RAS}$ and $\overline{CASx}$ to select the desired write mode (normal, block write, etc.).

Figure 34. Enhanced-Page-Mode Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later

NOTE A: A read cycle or a read-modify-write cycle can be intermixed with write cycles, observing read and read-modify-write timing specifications. To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late write feature is used. If the early write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

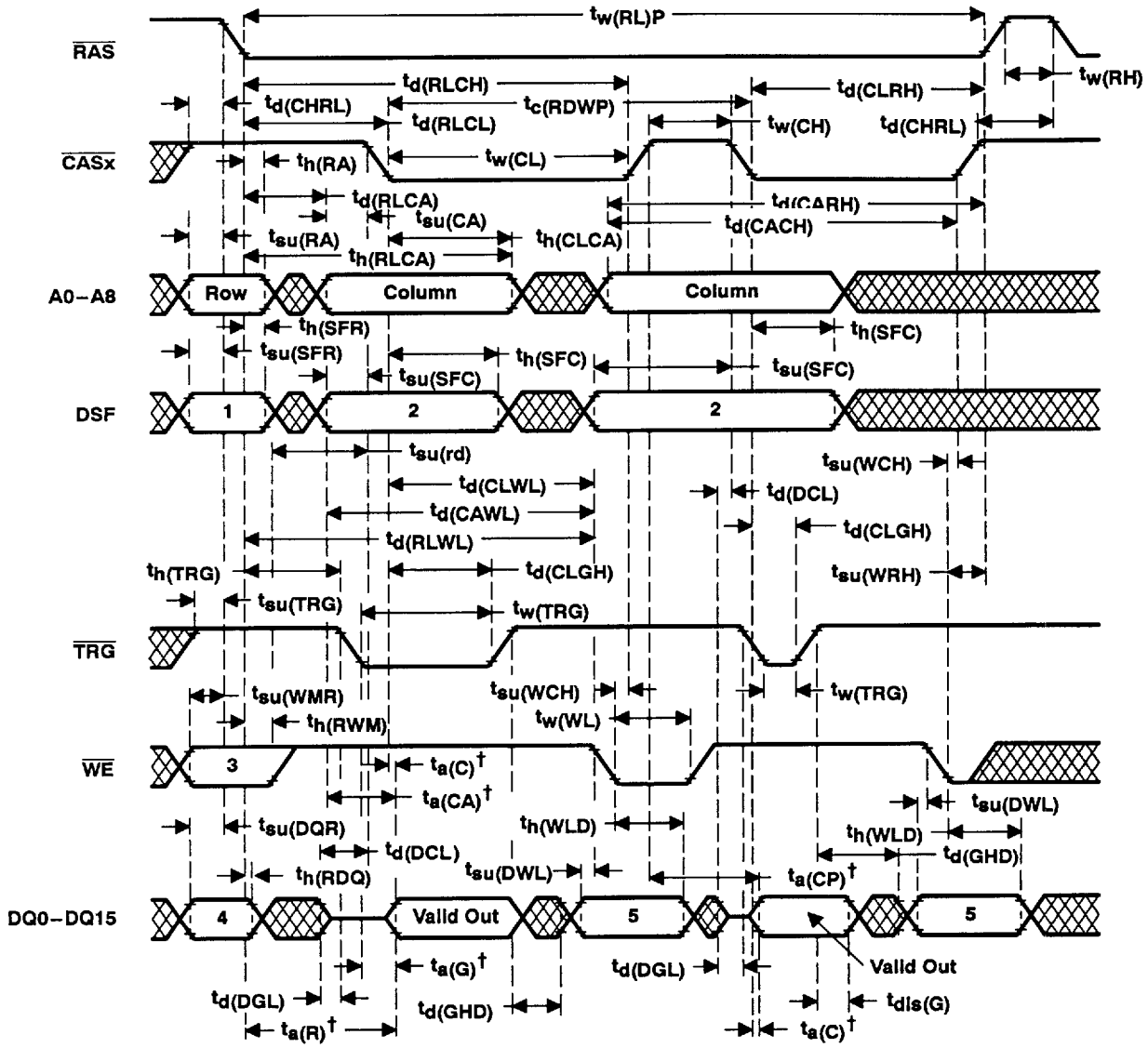
Figure 35. Enhanced-Page-Mode Write-Cycle Timing

Table 9. Enhanced-Page-Mode Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load-write mask on either the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurrs later.‡	H	L	H	Don't care	Write mask

‡ Load-write-mask-register cycle will set the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CASx}$ is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Output can go from the high-impedance to an invalid data state prior to the specified access time.
NOTE A: A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

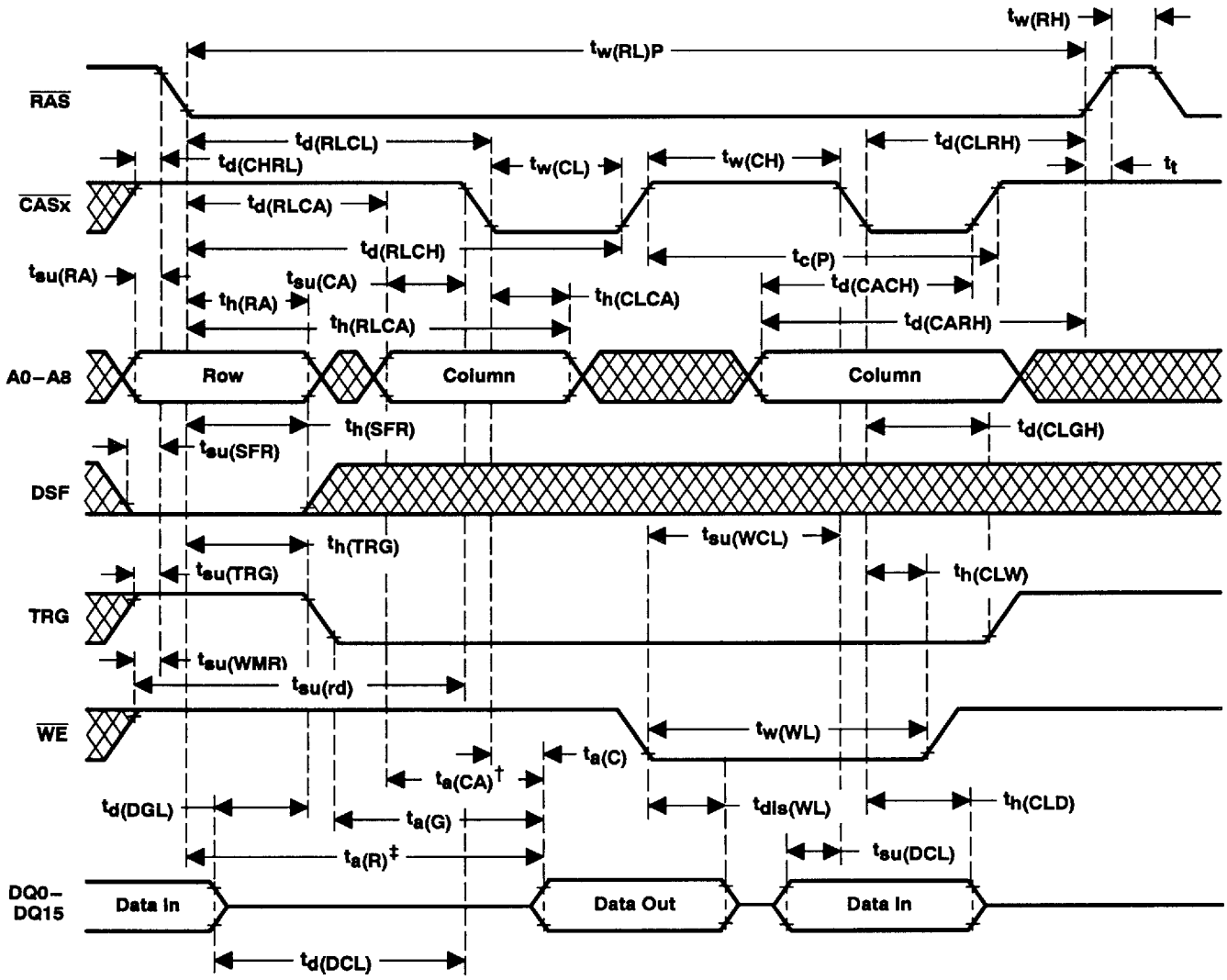
Figure 36. Enhanced-Page-Mode Read-Modify-Write-Cycle Timing

Table 10. Enhanced-Page-Mode Read-Modify-Write-Cycle State Table

CYCLE	STATE				
	1	2	3	4	5
Write operation (nonmasked)	L	L	H	Don't care	Valid data
Write operation with nonpersistent write-per-bit	L	L	L	Write mask	Valid data
Write operation with persistent write-per-bit	L	L	L	Don't care	Valid data
Load write mask on either the first falling edge of $\overline{CAS}$x or the falling edge of $\overline{WE}$, whichever occurs later.‡	H	L	H	Don't care	Write mask

‡ Load-write-mask cycle will set the device to the persistent write-per-bit mode. Column address at the falling edge of $\overline{CAS}$x is a don't care during this cycle.

PARAMETER MEASUREMENT INFORMATION



† Access time is $t_{a(CA)}$ dependent.
‡ Output can go from the high-impedance state to an invalid data state prior to the specified access time.

Figure 37. Enhanced-Page-Mode Read/Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

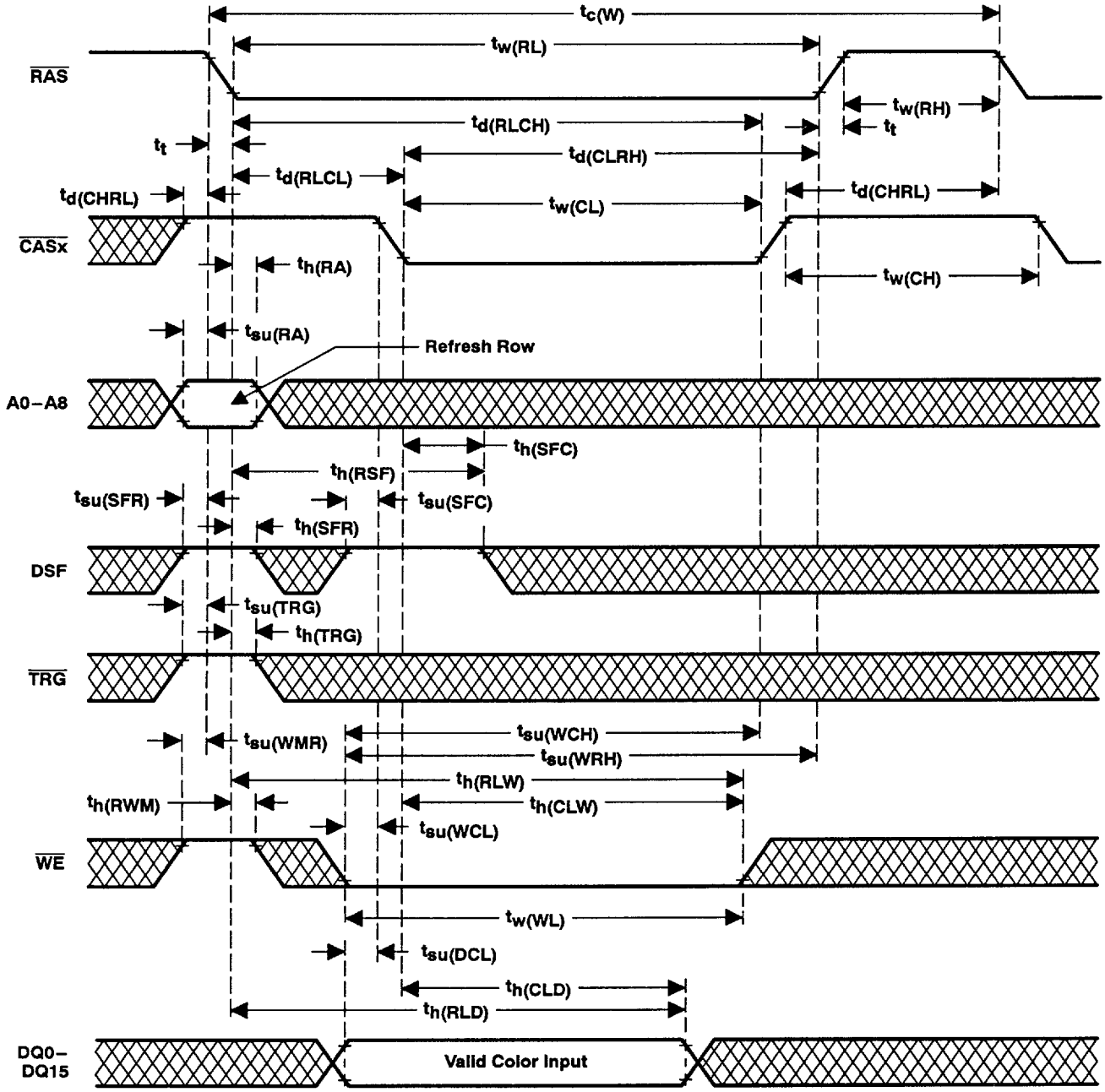


Figure 38. Load-Color-Register-Cycle Timing (Early-Write Load)

PARAMETER MEASUREMENT INFORMATION

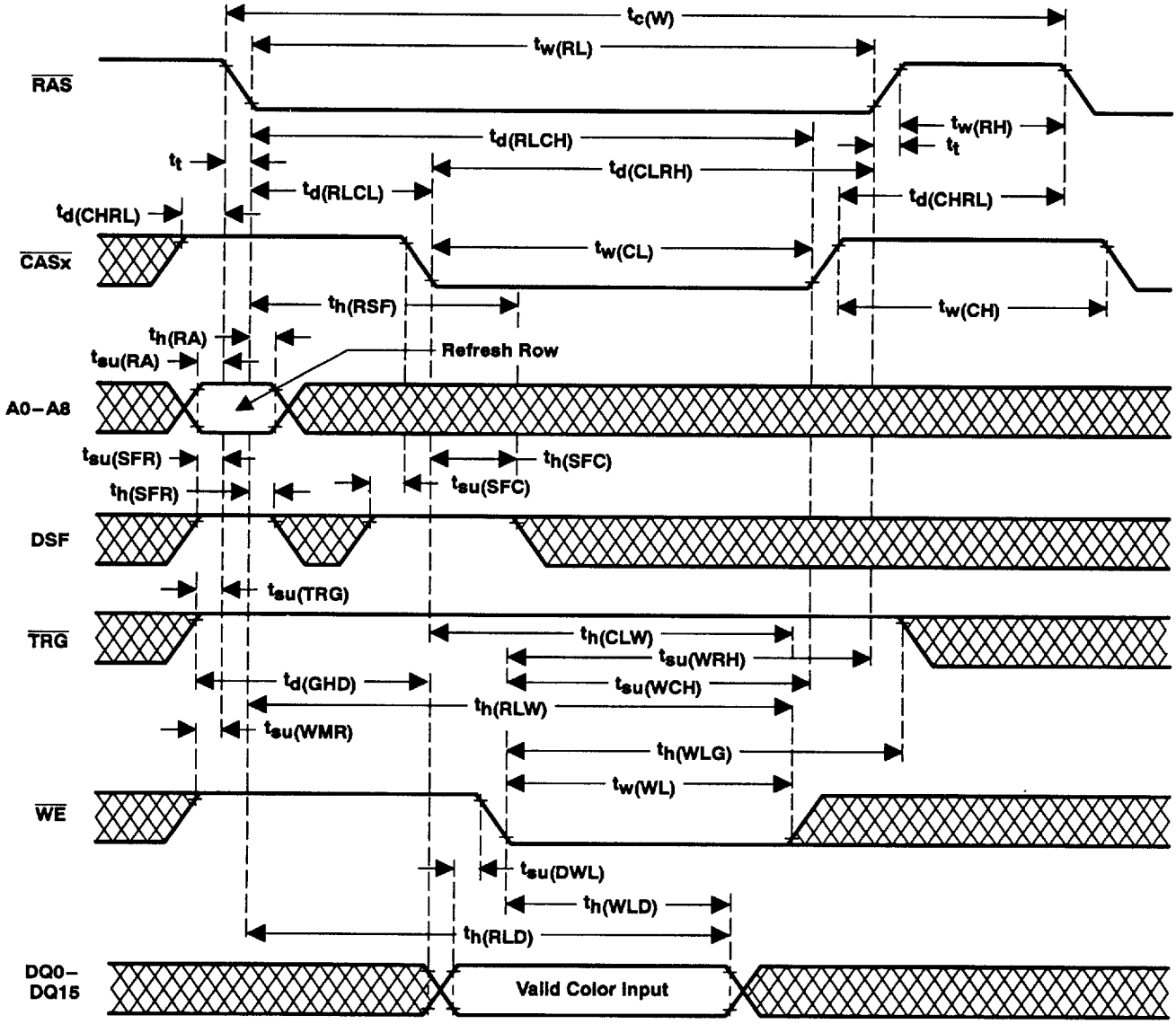


Figure 39. Load-Color-Register-Cycle Timing (Late-Write Load)

PARAMETER MEASUREMENT INFORMATION

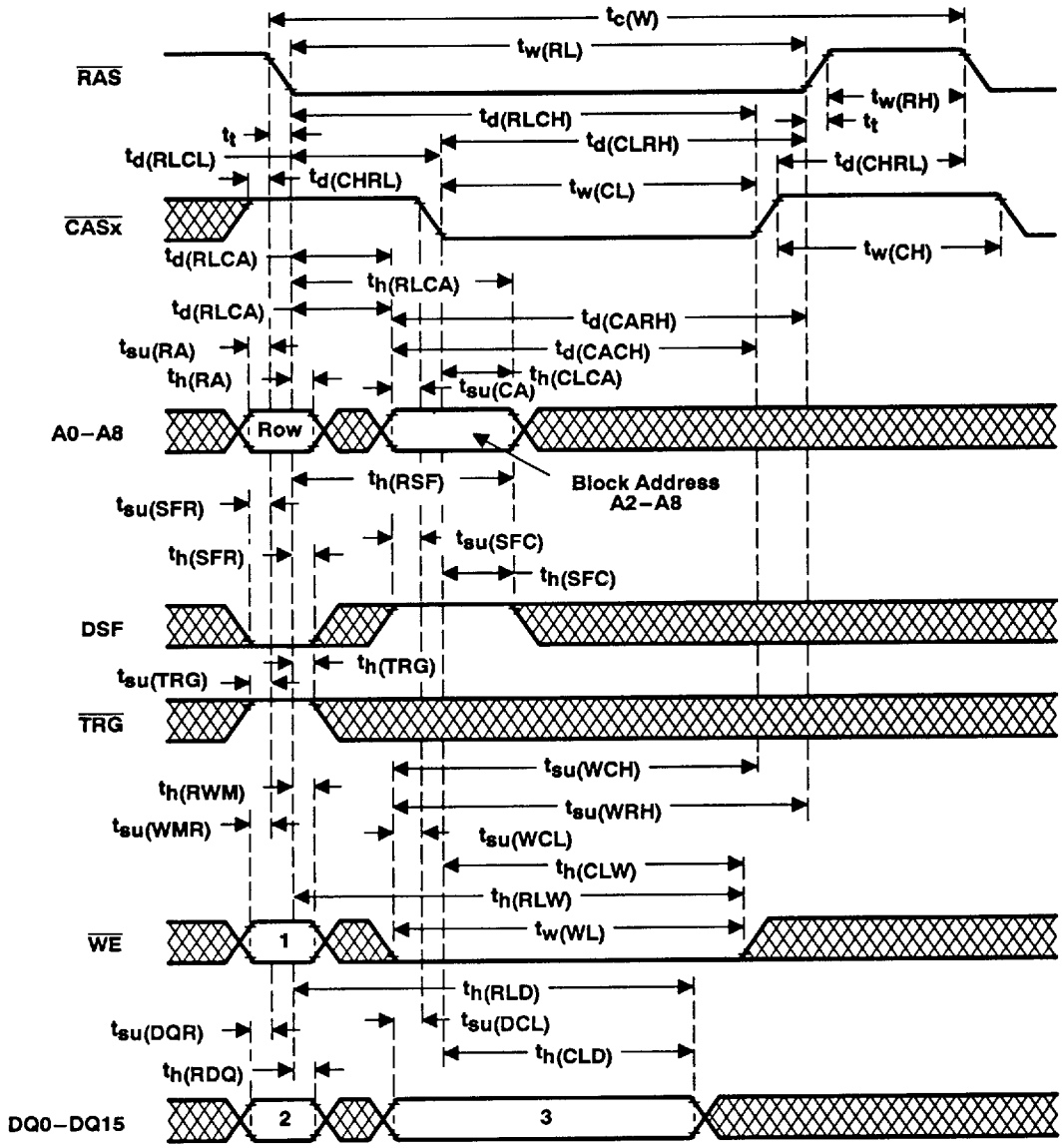


Figure 40. Block-Write-Cycle Timing (Early Write)

Table 11. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi+3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

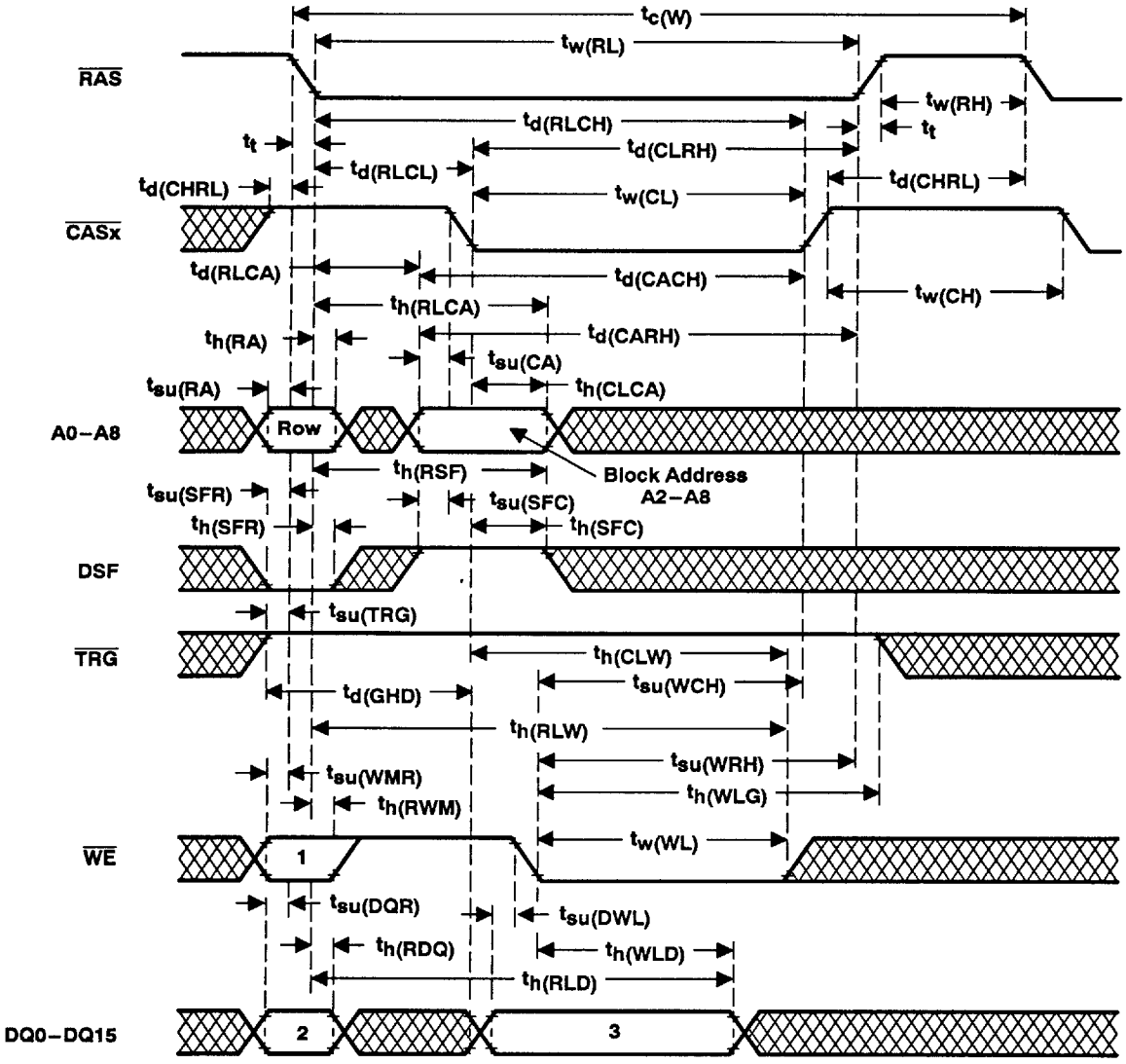


Figure 41. Block-Write-Cycle Timing (Late Write)

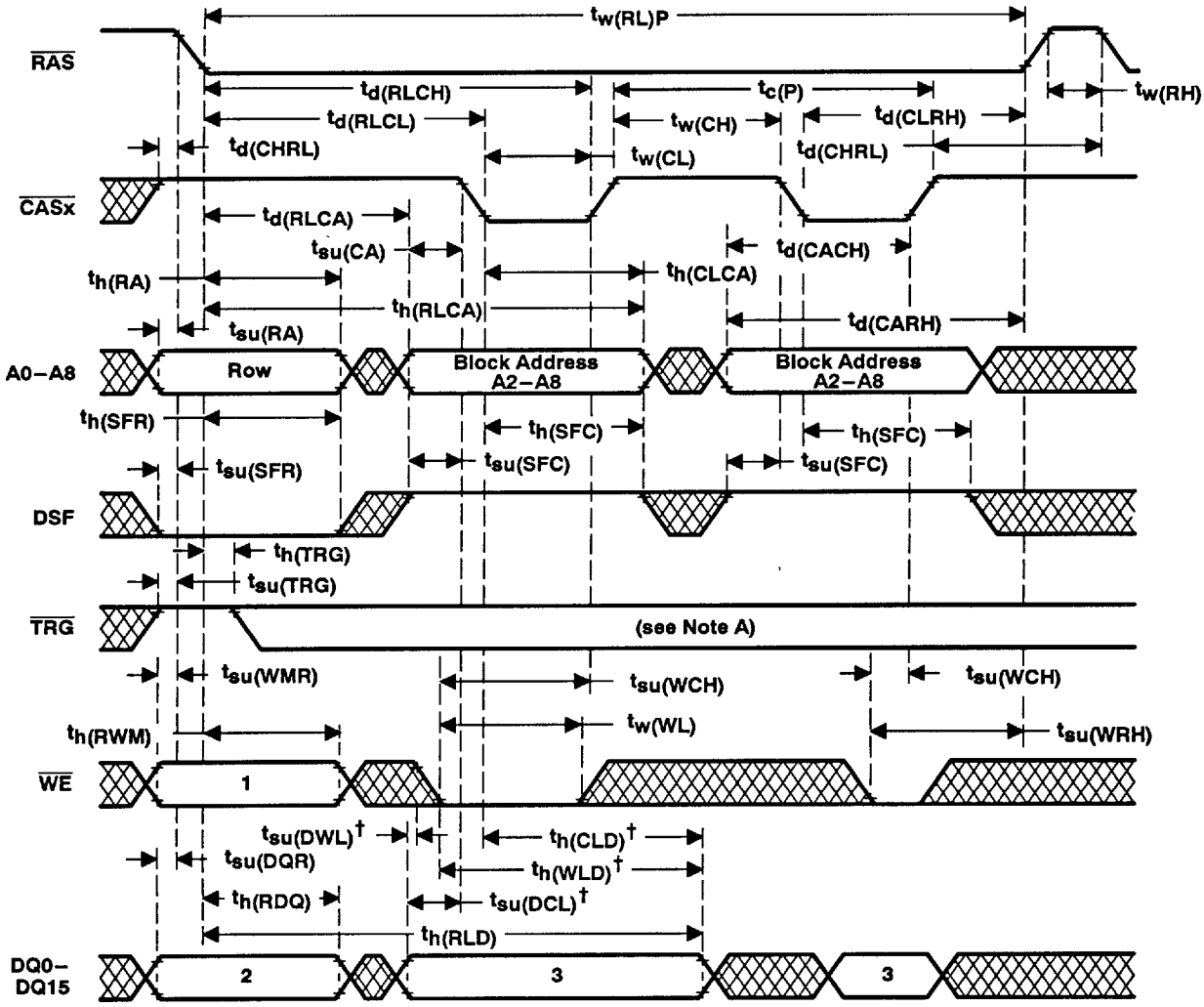
Table 12. Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable
Column-mask data DQi – DQi+3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION



† Referenced to the first falling edge of $\overline{CASx}$ or the falling edge of $\overline{WE}$, whichever occurs later.

NOTE A: To assure page-mode cycle time, $\overline{TRG}$ must remain high throughout the entire page-mode operation if the late-write feature is used. If the early-write cycle timing is used, the state of $\overline{TRG}$ is a don't care after the minimum period $t_{h(TRG)}$ from the falling edge of $\overline{RAS}$.

Figure 42. Enhanced-Page-Mode Block-Write-Cycle Timing

Table 13. Enhanced-Page-Mode Block-Write-Cycle State Table

CYCLE	STATE		
	1	2	3
Block-write operation (nonmasked)	H	Don't care	Column mask
Block-write operation with nonpersistent write-per-bit	L	Write mask	Column mask
Block-write operation with persistent write-per-bit	L	Don't care	Column mask

Write-mask data 0: I/O write disable
1: I/O write enable

Column-mask data DQi – DQi+3 (i = 0, 4, 8, 12) 0: column write disable
1: column write enable

Example:
DQ0 — column 0 (address A1 = 0, A0 = 0)
DQ1 — column 1 (address A1 = 0, A0 = 1)
DQ2 — column 2 (address A1 = 1, A0 = 0)
DQ3 — column 3 (address A1 = 1, A0 = 1)

PARAMETER MEASUREMENT INFORMATION

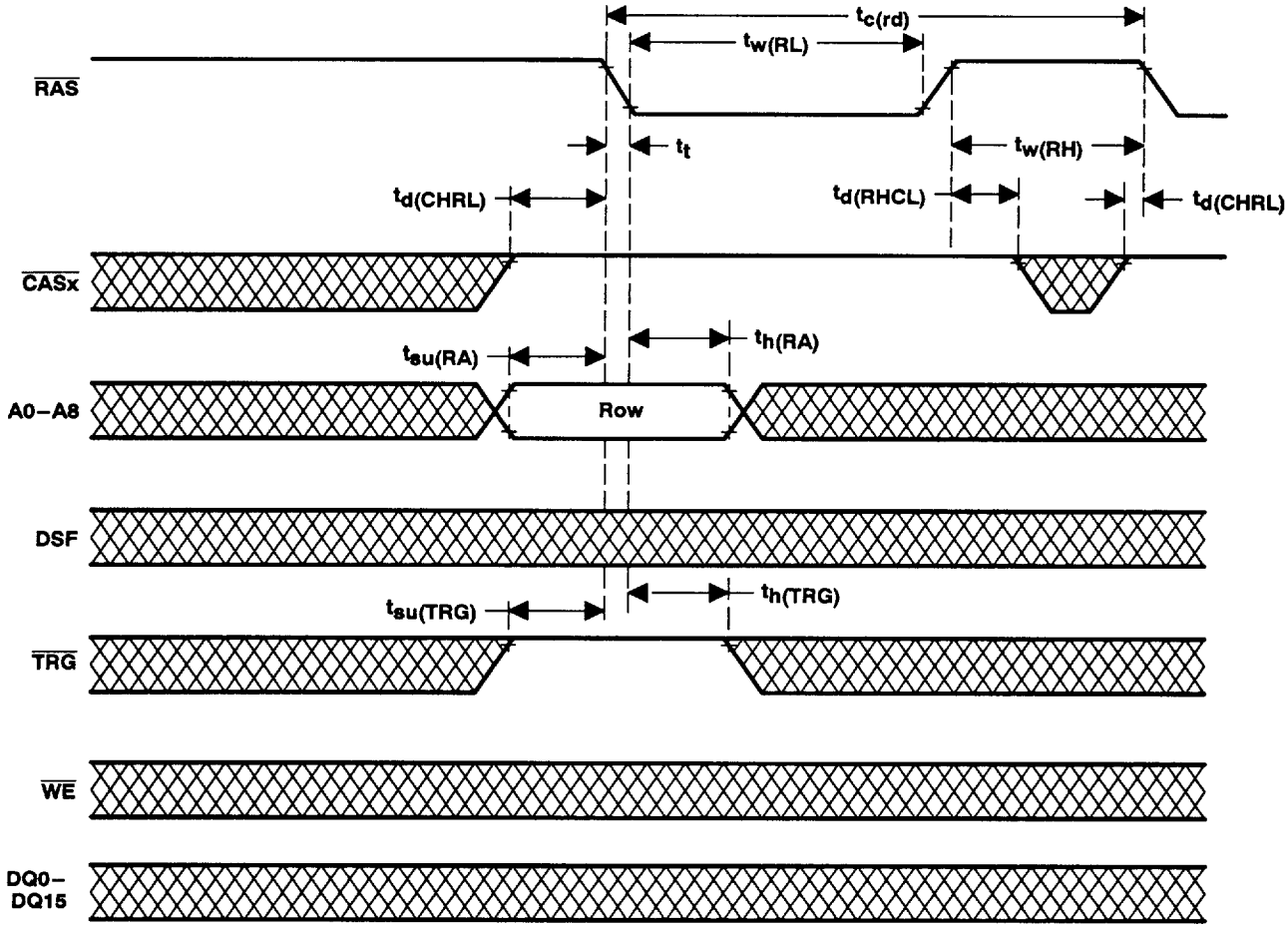


Figure 43. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

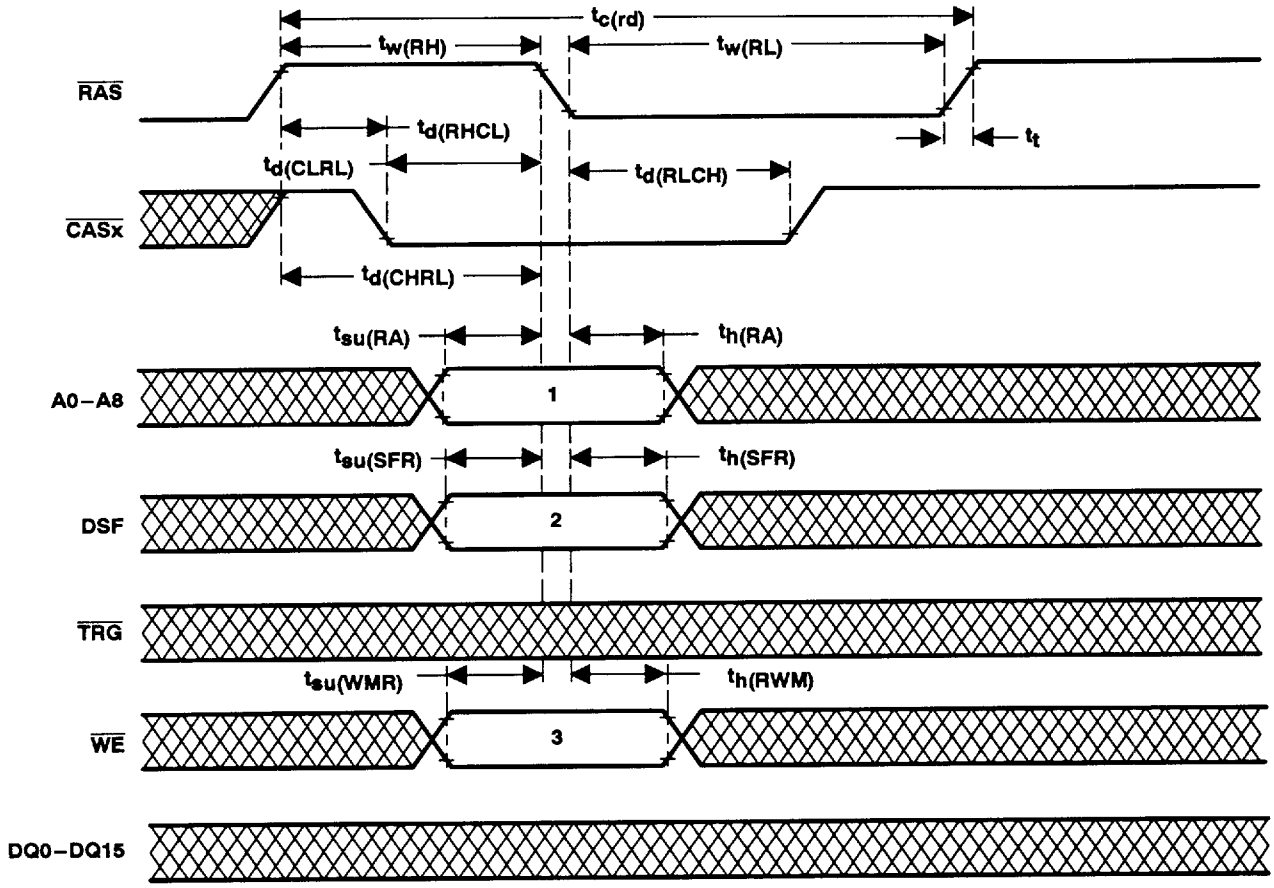


Figure 44. $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh-Cycle Timing

Table 14. CBR-Cycle State Table

CYCLE	STATE		
	1	2	3
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh with option reset	Don't care	L	H
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh with no reset	Don't care	H	H
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh with stop point set and no reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION

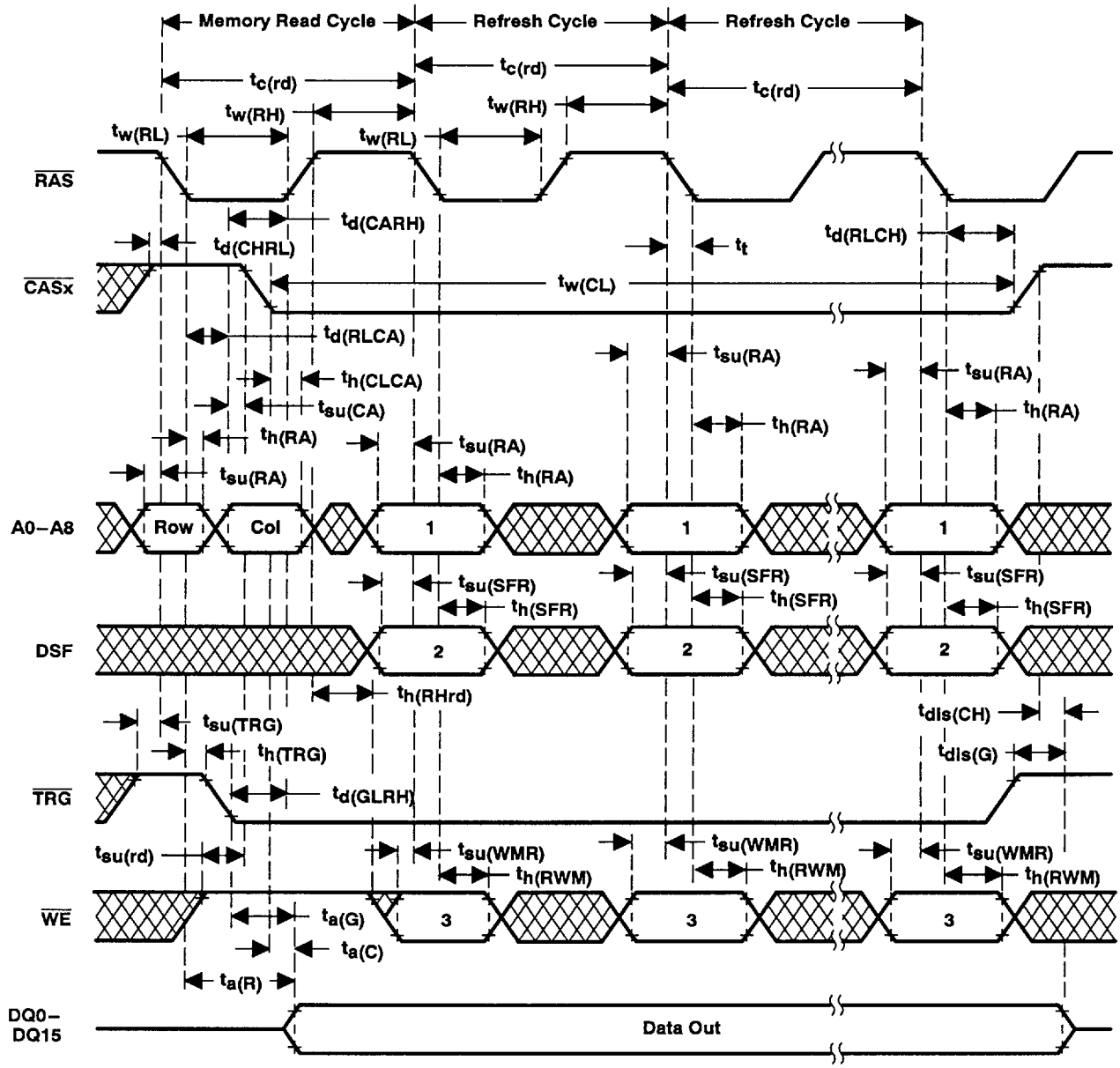
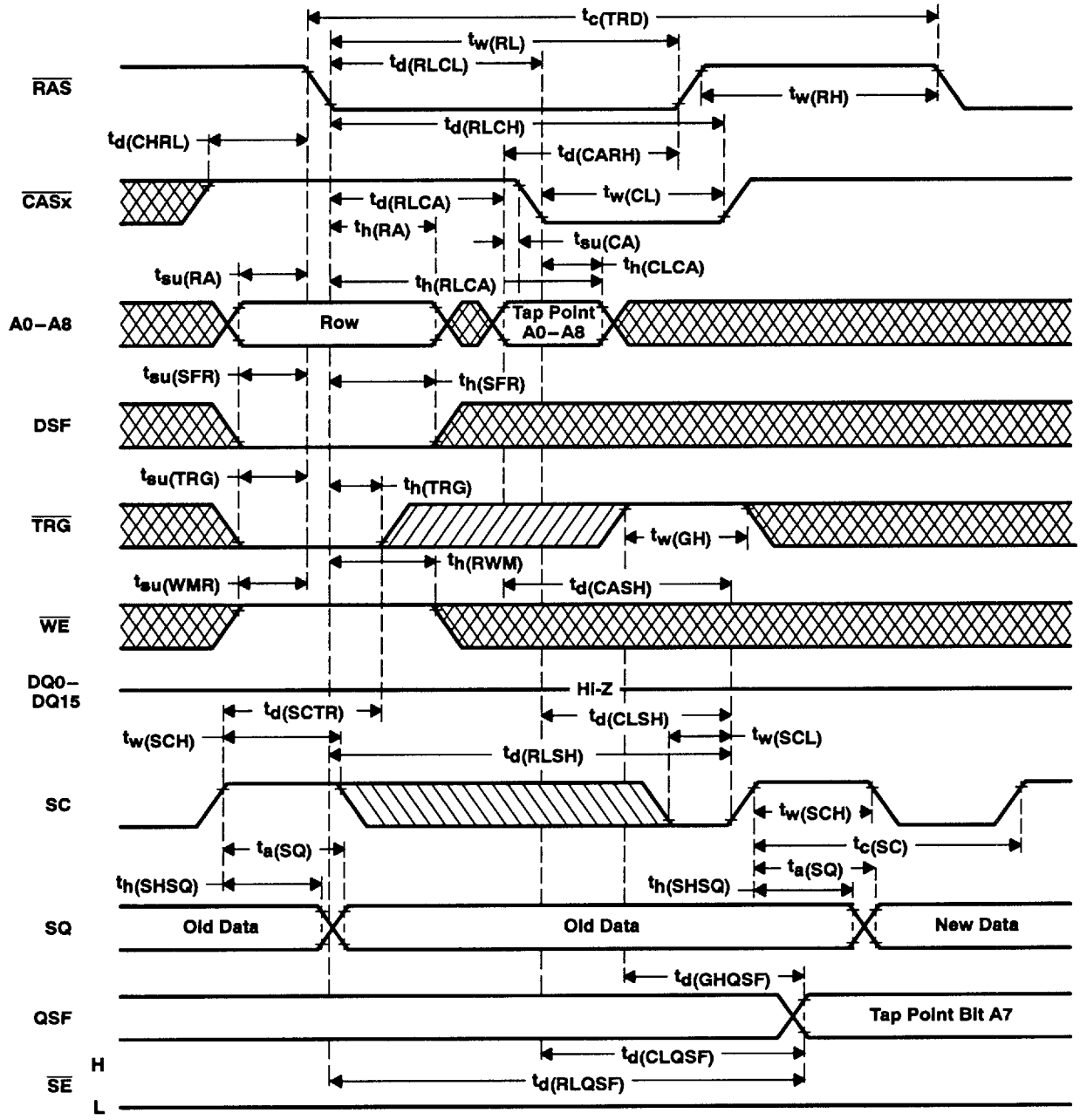


Figure 45. Hidden-Refresh-Cycle Timing

Table 15. Hidden-Refresh-Cycle State Table

CYCLE	STATE		
	1	2	3
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh with option reset	Don't care	L	H
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh with no reset	Don't care	H	H
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh with stop point set and no option reset	Stop address	H	L

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

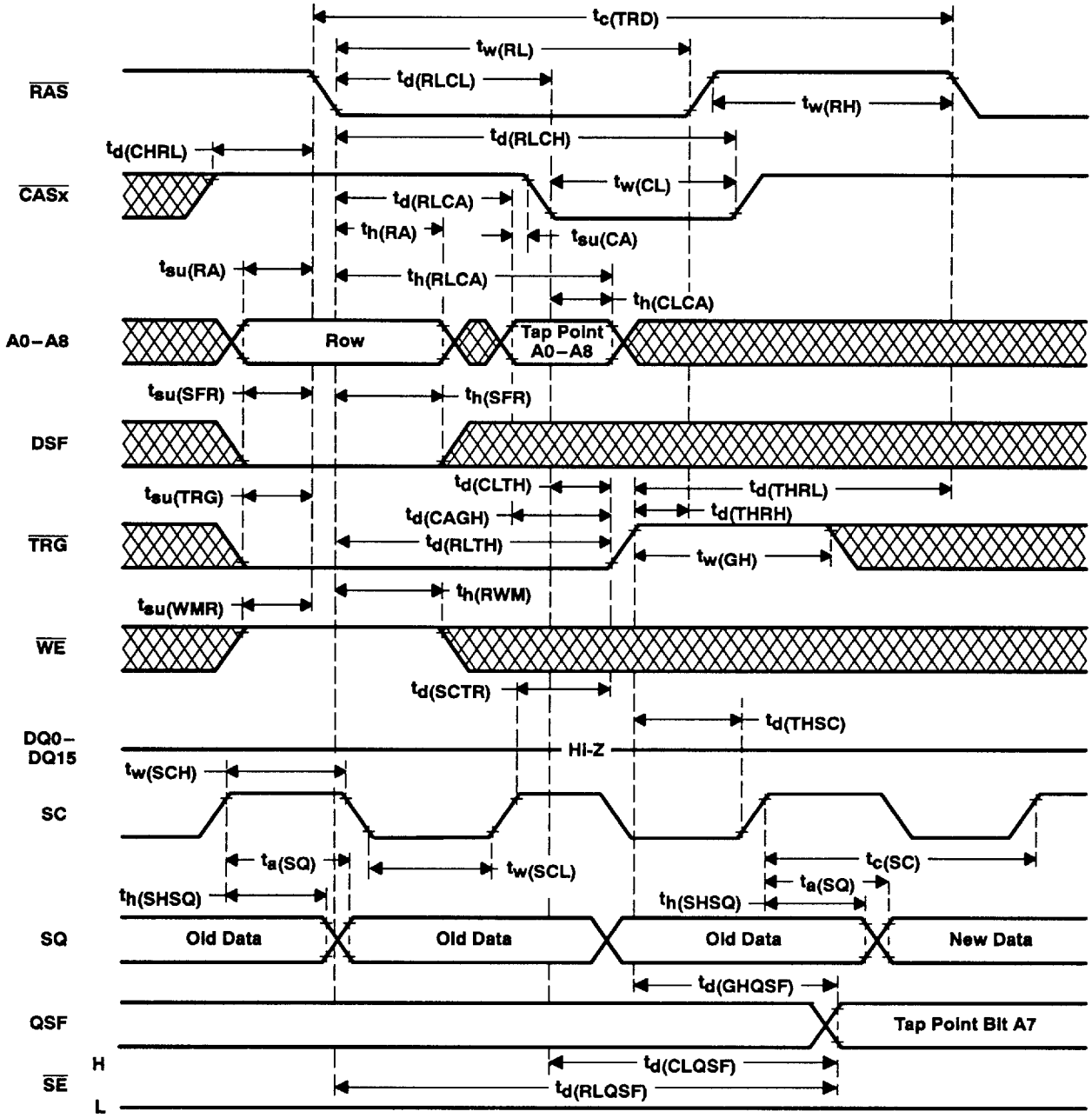
B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0 – A7: register tap point; A8: identifies the half of the transferred row

D. Early-load operation is defined as $t_{h(TRG)}$ min < $t_{h(TRG)}$ < $t_{d(RLTH)}$ min.

Figure 46. Full-Register Transfer Read Timing, Early-Load Operations

PARAMETER MEASUREMENT INFORMATION



NOTES: A. DQ outputs remain in the high-impedance state for the entire memory-to-data-register transfer cycle. The memory-to-data-register transfer cycle is used to load the data registers in parallel from the memory array. The 256 locations in each data register are written into from the 256 corresponding columns of the selected row.

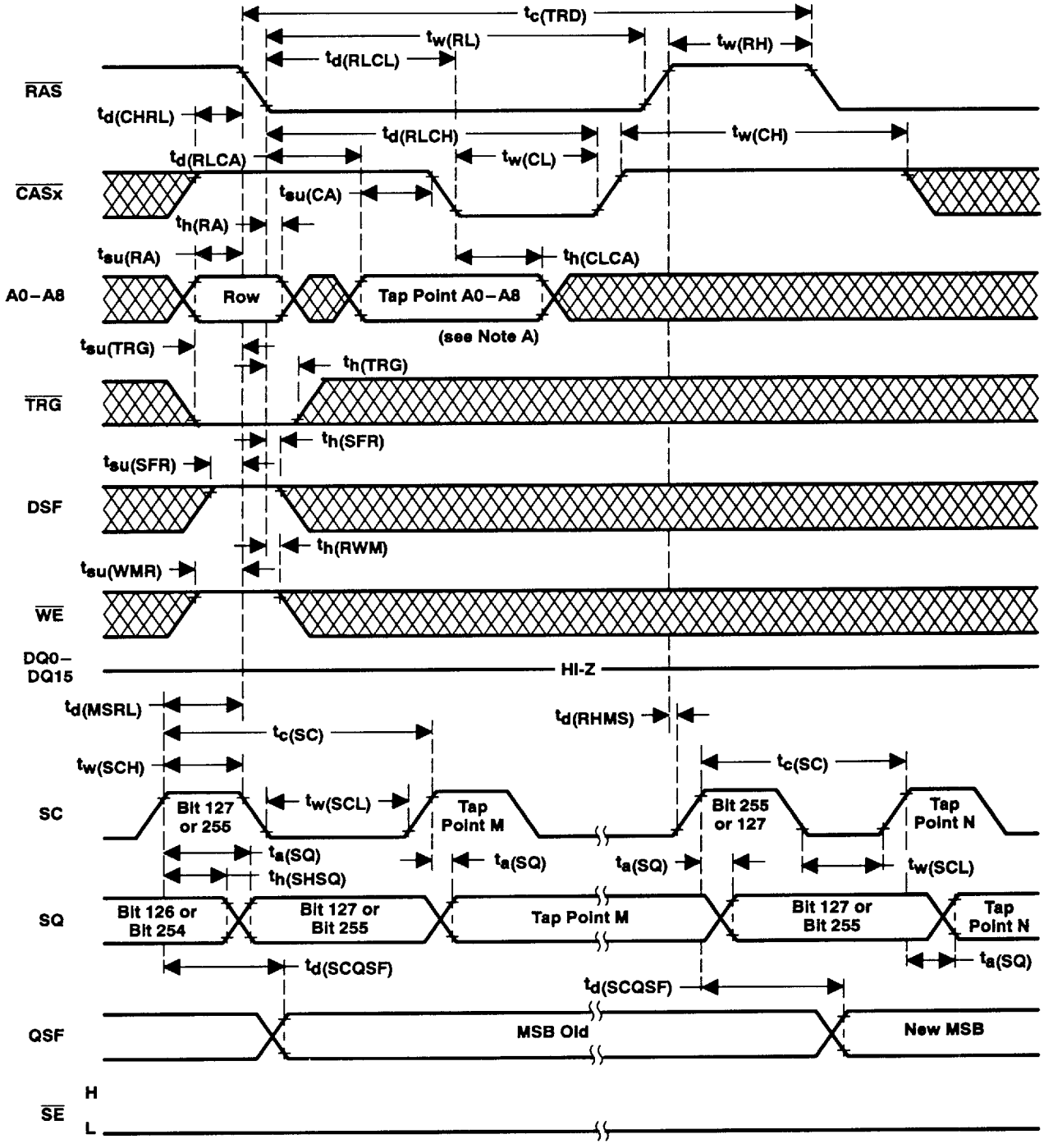
B. Once data is transferred into the data registers, the SAM is in the serial read mode (i.e., SQ is enabled), allowing data to be shifted out of the registers. Also, the first bit to read from the data register after $\overline{TRG}$ has gone high must be activated by a positive transition of SC.

C. A0–A7: register tap point; A8: identifies the half of the transferred row

D. Late load operation is defined as $t_{d(THRH)} < 0$ ns.

Figure 47. Full-Register Transfer Read Timing, Real-Time Load Operation/Late-Load Operation

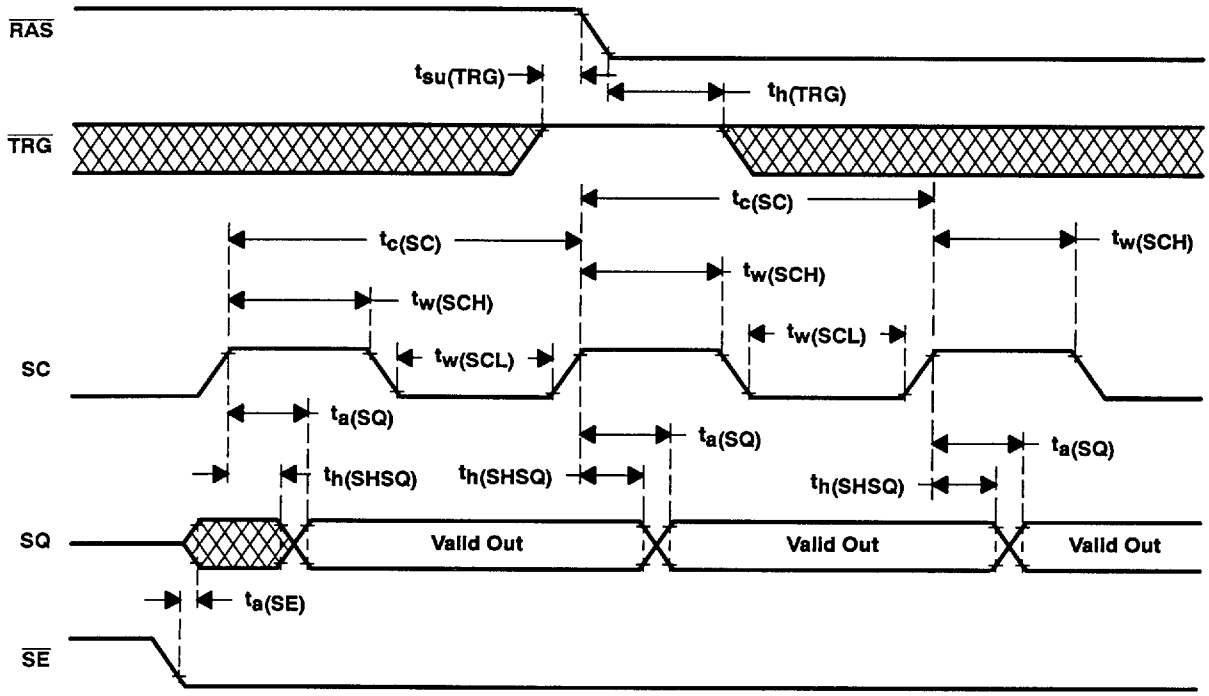
PARAMETER MEASUREMENT INFORMATION



NOTE A: A0–A6: tap point of the given half; A7: don't care; A8: identifies the DRAM row half

Figure 48. Split-Register Transfer Read Timing

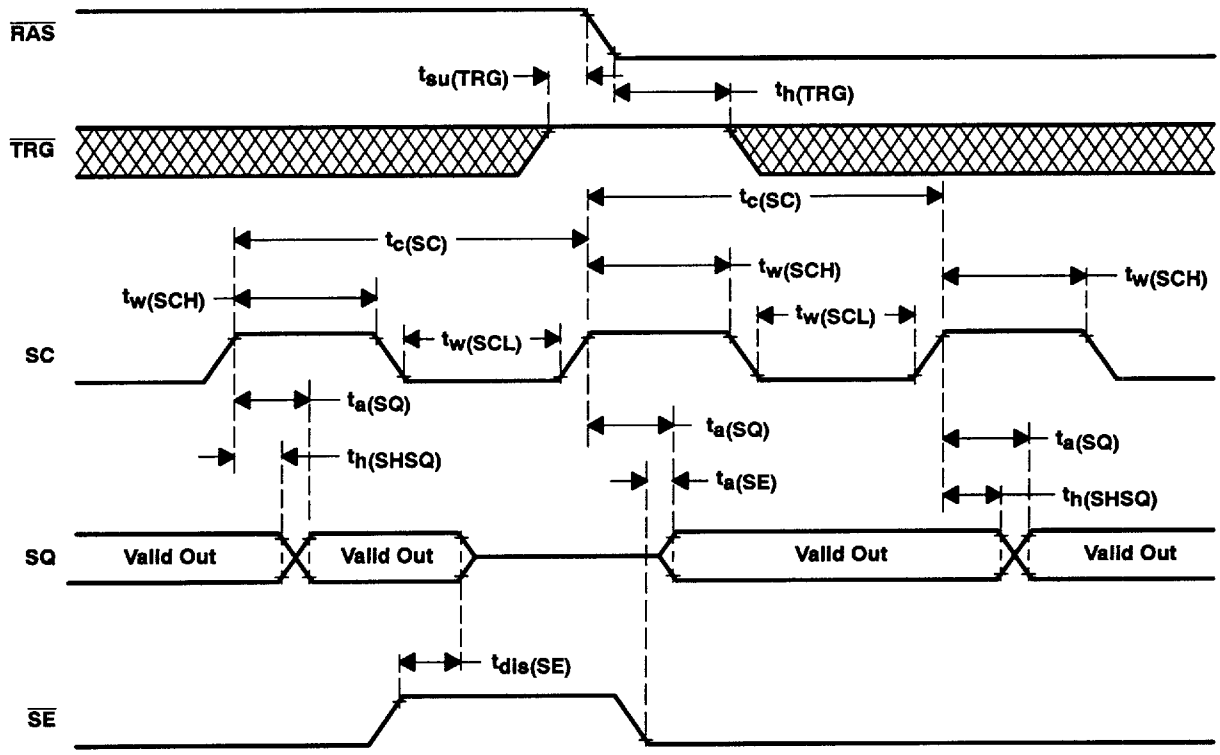
PARAMETER MEASUREMENT INFORMATION



NOTE A: While the data is being read through the serial-data register, $\overline{TRG}$ is a don't care, except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

Figure 49. Serial-Read-Cycle Timing ($\overline{SE}$ = V_{IL})

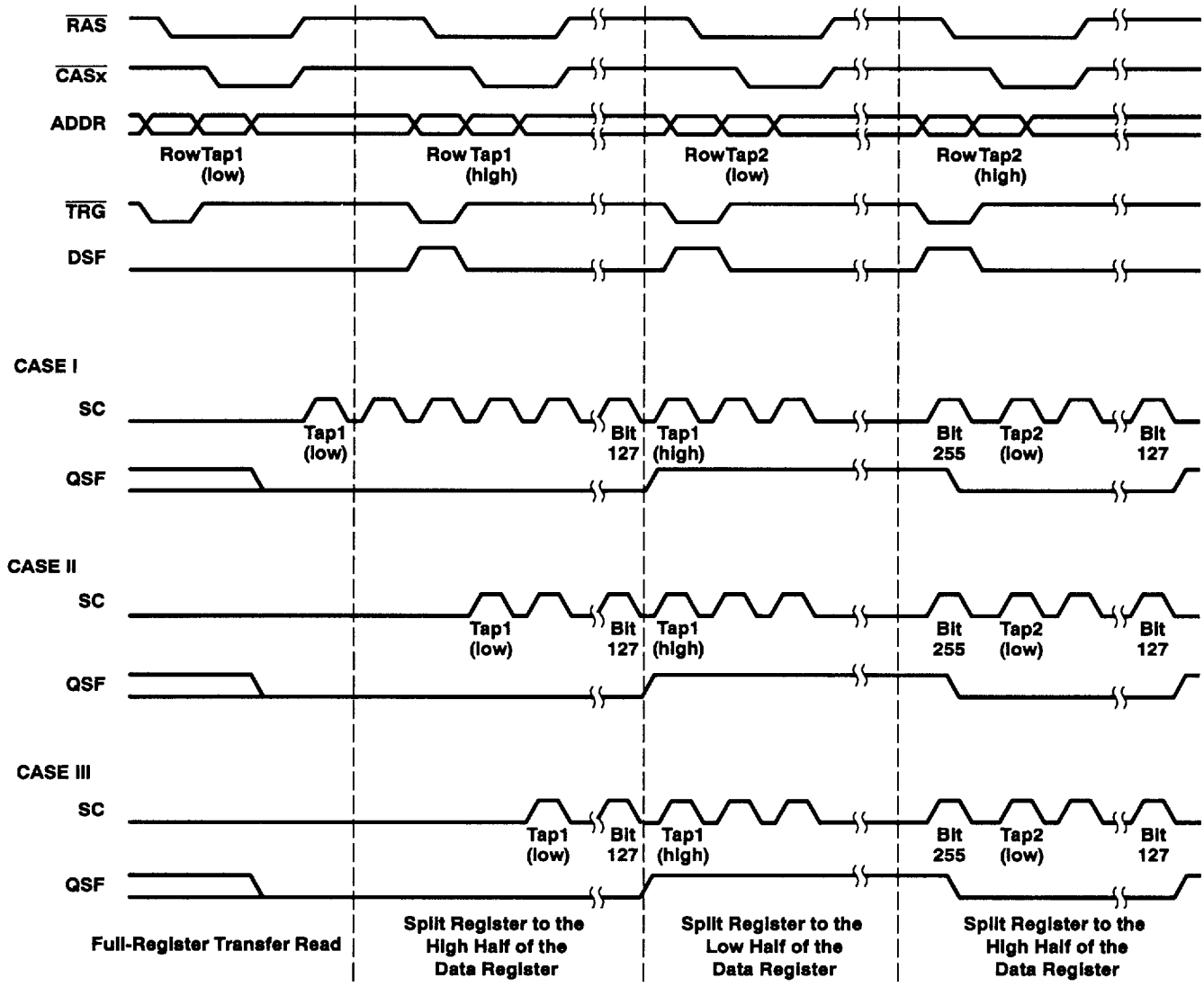
PARAMETER MEASUREMENT INFORMATION



NOTE A: While the data is being read through the serial-data register, $\overline{TRG}$ is a don't care except $\overline{TRG}$ must be held high when $\overline{RAS}$ goes low. This is to avoid the initiation of a register-data transfer operation.

Figure 50. Serial-Read-Cycle Timing ($\overline{SE}$-Controlled Read)

PARAMETER MEASUREMENT INFORMATION



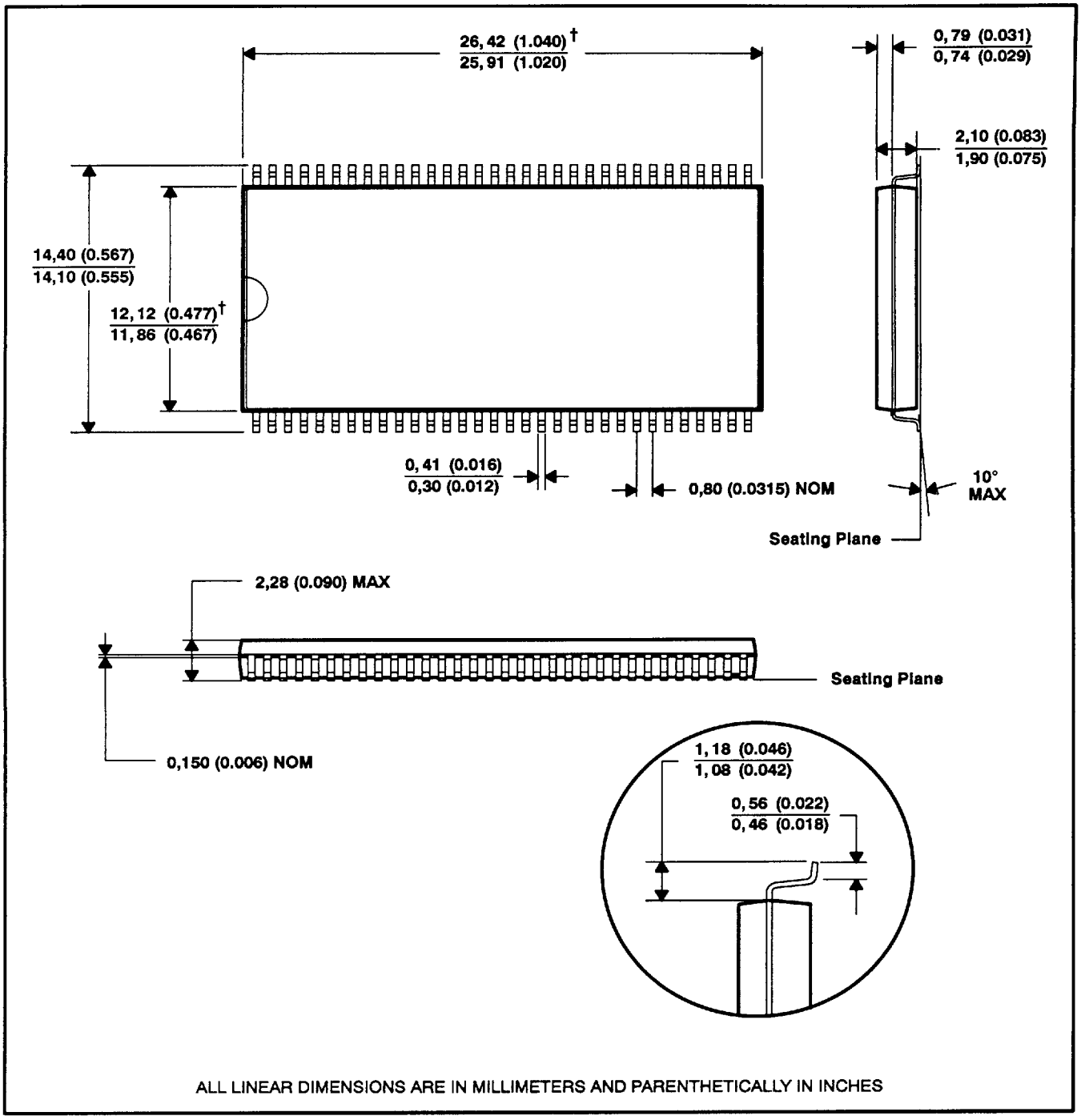
NOTES: A. In order to achieve proper split-register operation, a full-register transfer read should be performed before the first split-register transfer cycle. This is necessary to initialize the data register and the starting tap location. First serial access can then begin either after the full-register transfer read cycle (CASE I), during the first split-register transfer cycle (CASE II), or even after the first split-register transfer cycle (CASE III). There is no minimum requirement of SC clock between the full-register transfer read cycle and the first split-register cycle.

B. A split-register transfer into the inactive half is not allowed until $t_{d(MSRL)}$ is met. $t_{d(MSRL)}$ is the minimum delay time between the rising edge of the serial clock of the last bit (bit 127 or 255) and the falling edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half. After the $t_{d(MSRL)}$ requirement is met, the split-register transfer into the inactive half must also satisfy the minimum $t_{d(RHMS)}$ requirement. $t_{d(RHMS)}$ is the minimum delay time between the rising edge of $\overline{RAS}$ of the split-register transfer cycle into the inactive half and the rising edge of the serial clock of the last bit (bit 127 or 255).

Figure 51. Split-Register Operating Sequence

MECHANICAL DATA

DGH–64 LEAD THIN SMALL-OUTLINE PACKAGE **R–PDSO–G64**



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

† Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0,254 mm (0.010 inches) from the edge of the package bottom plastic.

device symbolization