

P-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
- 60	0.015 at V _{GS} = - 10 V	- 50 ^d
	0.020 at V _{GS} = - 4.5 V	- 50 ^d

FEATURES

- TrenchFET® Power MOSFET
- Material categorization:
For definitions of compliance please see
www.vishay.com/doc?99912

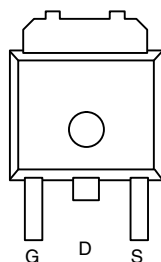


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Switch

TO-252



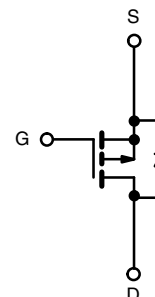
Drain Connected to Tab

Top View

Ordering Information

SUD50P06-15-GE3 (Lead (Pb)-free and Halogen-free)

SUD50P06-15-T4-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 60	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 175 °C)	I _D	T _C = 25 °C - 50 ^d	A
		T _C = 125 °C - 27.5	
Pulsed Drain Current	I _{DM}	- 80	
Avalanche Current	I _{AS}	- 50	
Single Pulse Avalanche Energy ^a	E _{AS}	125	mJ
Power Dissipation	P _D	T _C = 25 °C 113 ^c	W
		T _A = 25 °C 2.5 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient ^b	R _{thJA}	t ≤ 10 s 15	18	°C/W
		Steady State 40	50	
Junction-to-Case	R _{thJC}	0.82	1.1	

Notes:

a. Duty cycle ≤ 1 %.

b. When mounted on 1" square PCB (FR-4 material).

c. See SOA curve for voltage derating.

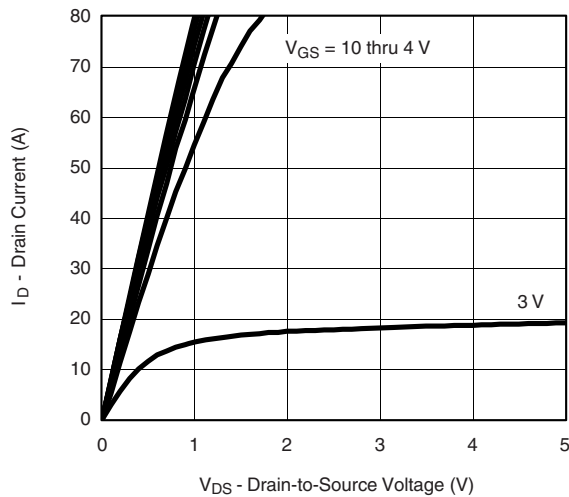
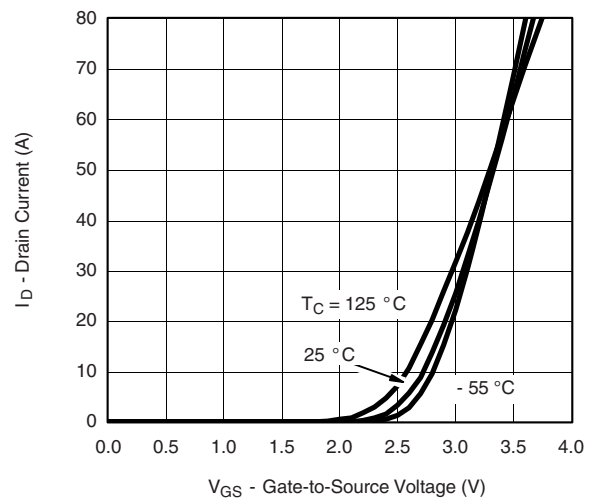
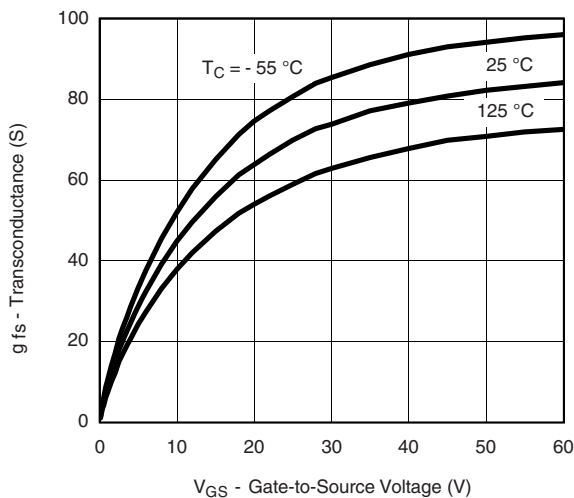
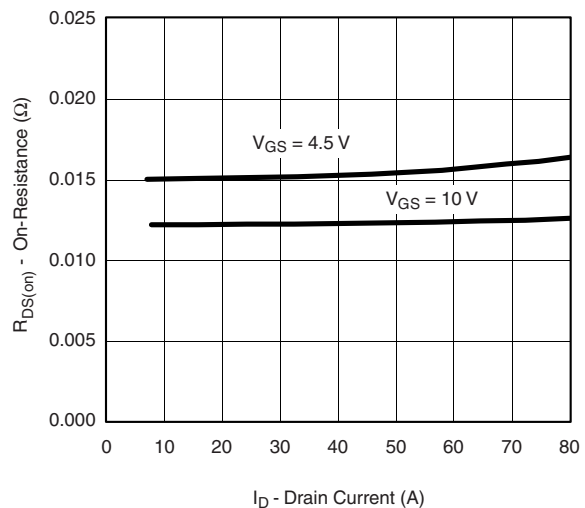
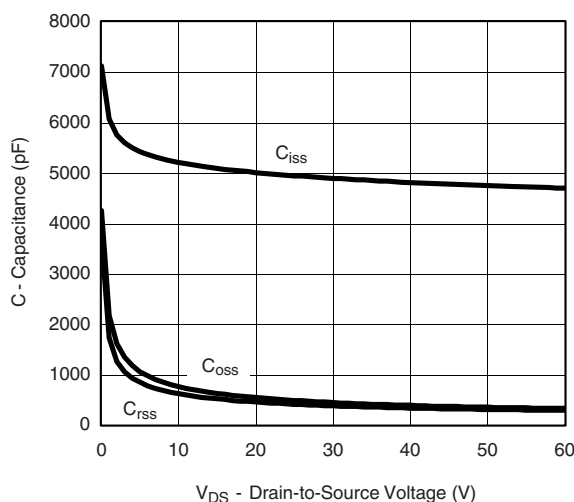
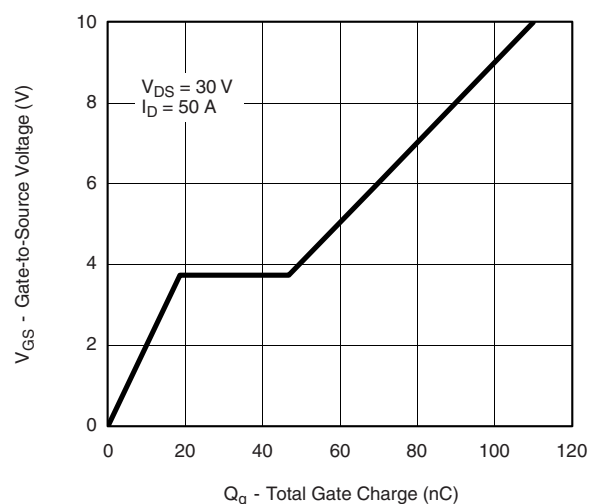
d. Package limited.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 1		- 3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 60 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 60 V, V _{GS} = 0 V, T _J = 125 °C			- 50	
		V _{DS} = - 60 V, V _{GS} = 0 V, T _J = 150 °C			- 100	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = - 5 V, V _{GS} = - 10 V	- 50			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 10 V, I _D = - 17 A		0.012	0.015	Ω
		V _{GS} = - 10 V, I _D = - 50 A, T _J = 125 °C			0.025	
		V _{GS} = - 10 V, I _D = - 50 A, T _J = 150 °C			0.028	
		V _{GS} = - 4.5 V, I _D = - 14 A			0.020	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 15 V, I _D = - 17 A		61		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1 MHz		4950		pF
Output Capacitance	C _{oss}			480		
Reverse Transfer Capacitance	C _{rss}			405		
Total Gate Charge ^c	Q _g	V _{DS} = - 30 V, V _{GS} = - 10 V, I _D = - 50 A		110	165	nC
Gate-Source Charge ^c	Q _{gs}			19		
Gate-Drain Charge ^c	Q _{gd}			28		
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = - 30 V, R _L = 0.6 Ω I _D ≅ - 50 A, V _{GEN} = - 10 V, R _G = 6 Ω		15	23	ns
Rise Time ^c	t _r			70	105	
Turn-Off Delay Time ^c	t _{d(off)}			175	260	
Fall Time ^c	t _f			175	260	
Source-Drain Diode Ratings and Characteristics T _C = 25 °C ^b						
Continuous Current	I _S				- 50	A
Pulsed Current	I _{SM}				- 80	
Forward Voltage ^a	V _{SD}	I _F = - 50 A, V _{GS} = 0 V		- 1	- 1.6	V
Reverse Recovery Time	t _{rr}	I _F = - 50 A, dI/dt = 100 A/μs		45	70	ns

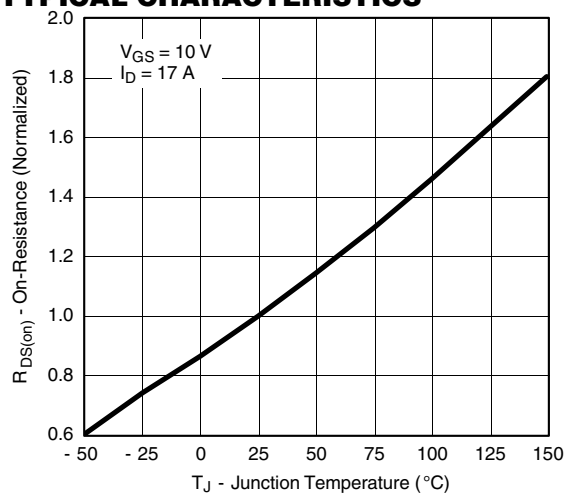
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

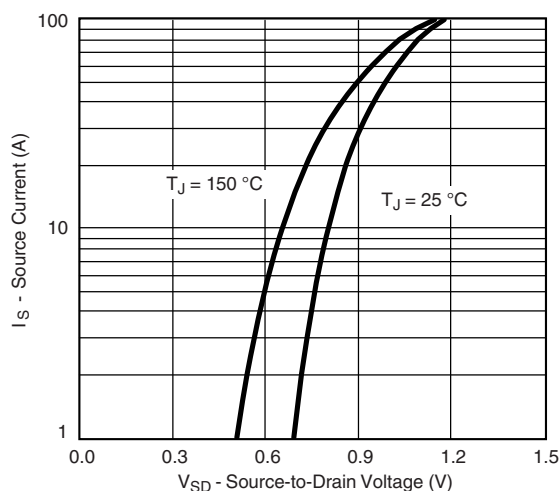
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

Transconductance

On-Resistance vs. Drain Current

Capacitance

Gate Charge

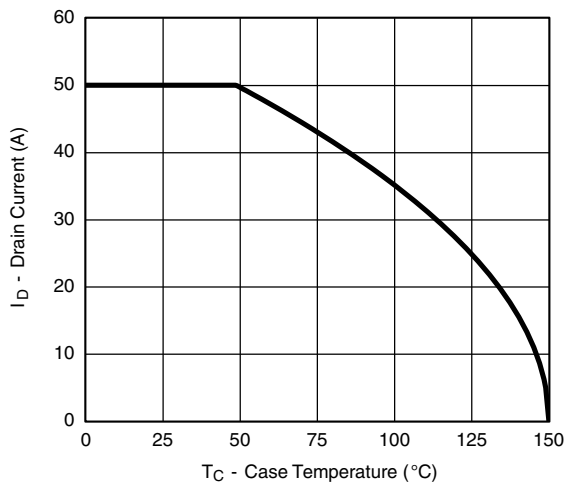
TYPICAL CHARACTERISTICS



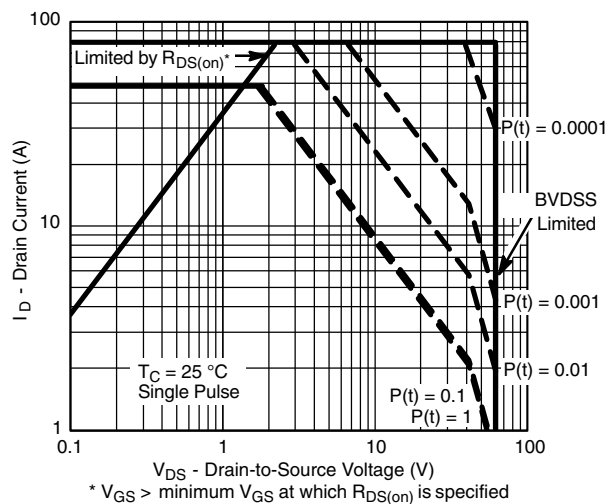
On-Resistance vs. Junction Temperature



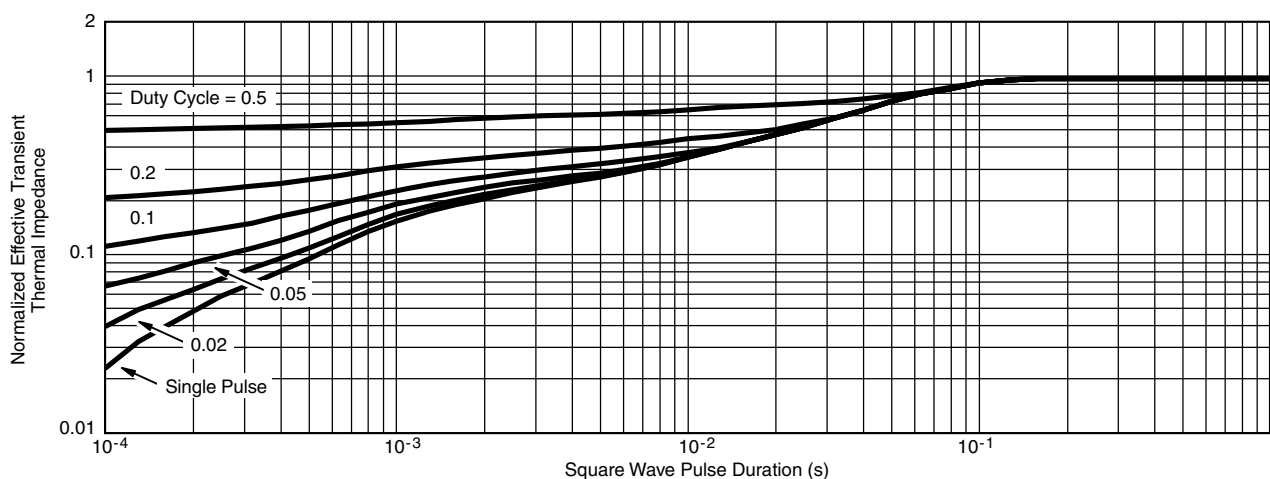
Source-Drain Diode Forward Voltage

THERMAL RATINGS (25 $^{\circ}\text{C}$, unless otherwise noted)

Drain Current vs. Case Temperature



Safe Operating Area

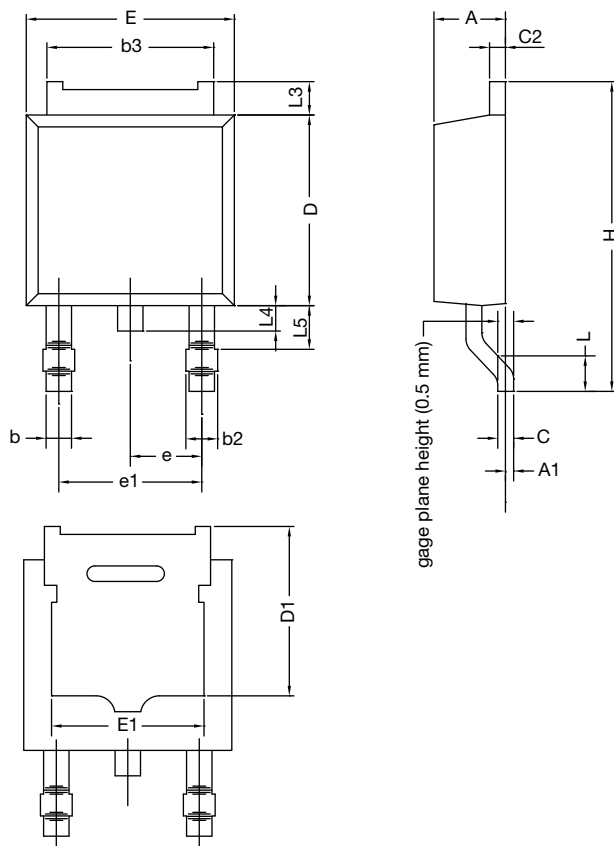


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68940.



TO-252AA Case Outline

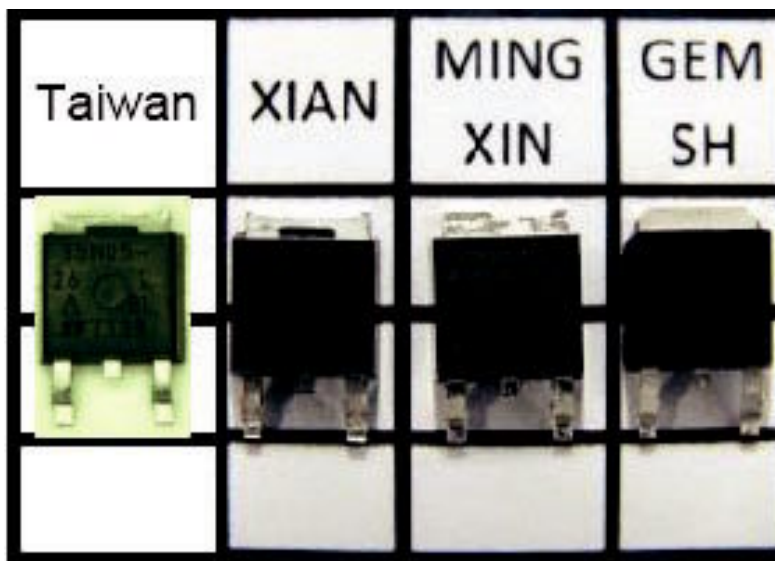


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060

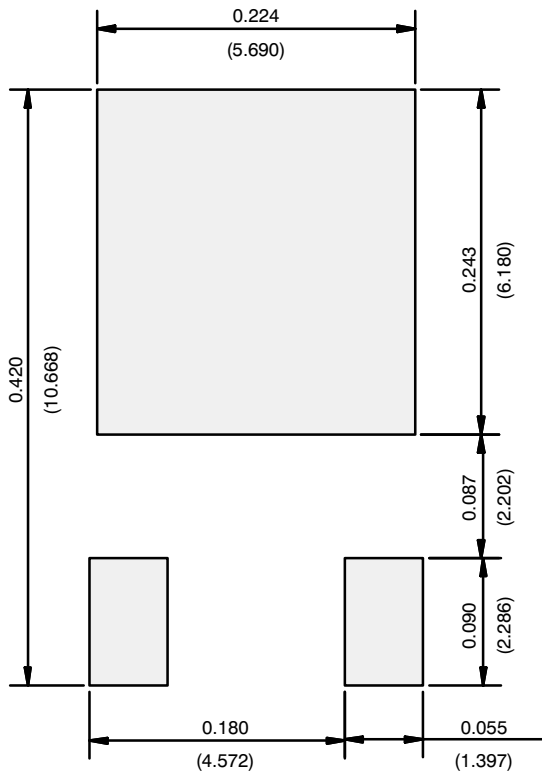
ECN: T13-0359-Rev. O, 03-Jun-13
DWG: 5347

Notes

- Dimension L3 is for reference only.
- Xi'an, Mingxin, and GEM SH actual photo.



RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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