

# HD74LS373

## Octal D-type Transparent Latches (with three-state outputs)

REJ03D0482-0200

Rev.2.00

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The HD74LS373, 8-bit register features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capacity of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

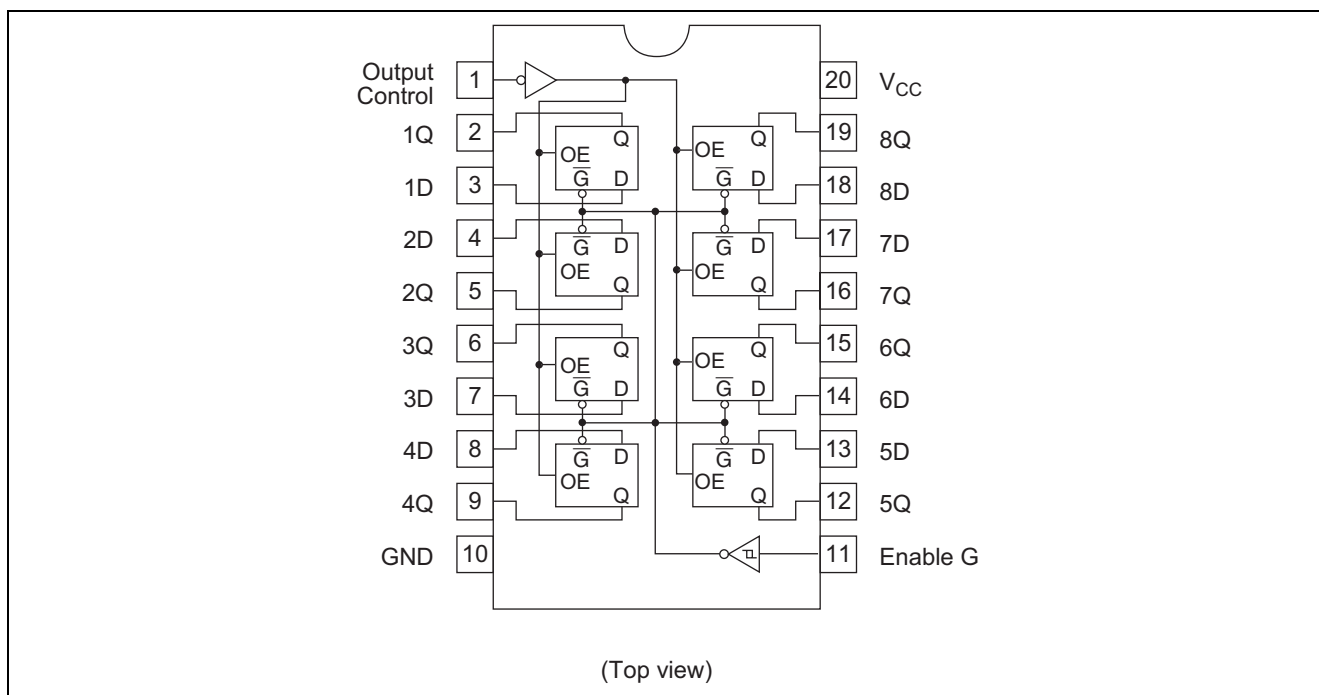
### Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS373P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74LS373FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74LS373RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Pin Arrangement



## Function Table

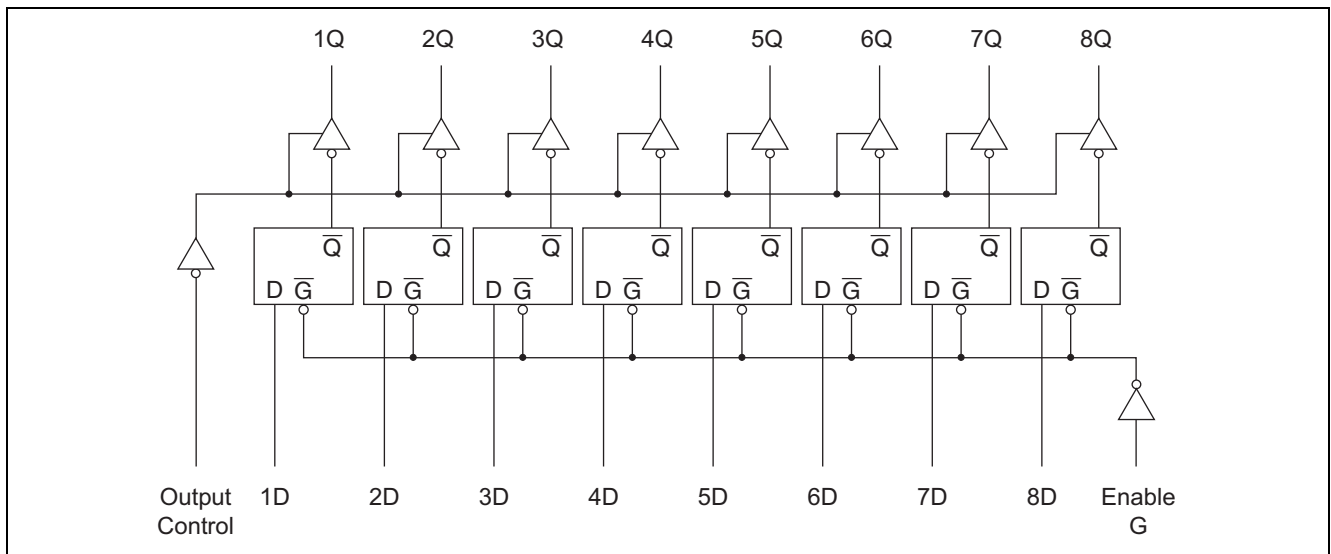
Inputs			Output
Output control	Enable G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z

Notes: H; high level, L; low level, X; irrelevant

Q<sub>0</sub>; level of Q before the indicated steady-state input conditions were established

Z; off (high-impedance) state of a three-state output

## Block Diagram



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V <sub>CC</sub>	7	V
Input voltage	V <sub>IN</sub>	7	V
Power dissipation	P <sub>T</sub>	400	mW
Storage temperature	T <sub>stg</sub>	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

## Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.00	5.25	V
Output voltage	V <sub>OH</sub>	—	—	5.5	V
Output current	I <sub>OH</sub>	—	—	-2.6	mA
	I <sub>OL</sub>	—	—	24	mA
Operating temperature	T <sub>opr</sub>	-20	25	75	°C
Enable pulse width	"H" Level	t <sub>w</sub>	15	—	ns
	"L" Level		15	—	ns
Data setup time	t <sub>su</sub>	5↓	—	—	ns
Data hold time	t <sub>h</sub>	20↓	—	—	ns

## Electrical Characteristics

(Ta = -20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition
Input voltage	V <sub>IH</sub>	2.0	—	—	V	
	V <sub>IL</sub>	—	—	0.7	V	Data inputs
		—	—	0.8		G, Output control inputs
Output voltage	V <sub>OH</sub>	2.4	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL max</sub> I <sub>OH</sub> = -2.6 mA
	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 12 mA
		—	—	0.5		I <sub>OL</sub> = 24 mA
Output current	I <sub>OZH</sub>	—	—	20	μA	V <sub>O</sub> = 2.7 V
	I <sub>OZL</sub>	—	—	-20		V <sub>O</sub> = 0.4 V
Input current	I <sub>IH</sub>	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V
	I <sub>IL</sub>	—	—	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V
	I <sub>I</sub>	—	—	0.1	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 7 V
Short-circuit output current	I <sub>OS</sub>	-30	—	-130	mA	V <sub>CC</sub> = 5.25 V
Supply current	I <sub>CC</sub>	—	24	40	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 4.5 V (Output control)
Input clamp voltage	V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA

Note: \* V<sub>CC</sub> = 5 V, Ta = 25°C

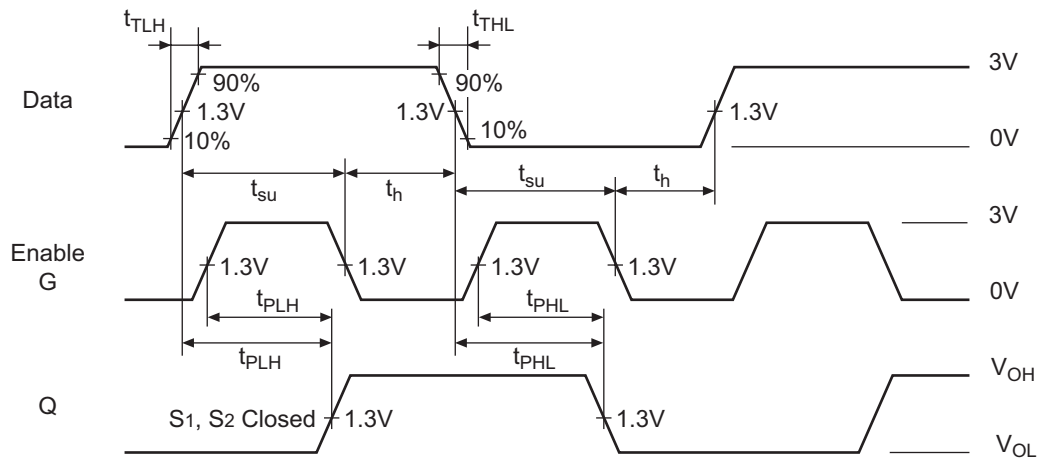
## Switching Characteristics

(V<sub>CC</sub> = 5 V, Ta = 25°C)

Item	Symbol	Input	Output	min.	typ.	max.	Unit	Condition
Propagation delay time	t <sub>PLH</sub>	D	Q	—	12	18	ns	C <sub>L</sub> = 45 pF, R <sub>L</sub> = 667 Ω
	t <sub>PHL</sub>			—	12	18		
	t <sub>PLH</sub>	G	Q	—	20	30		
	t <sub>PHL</sub>			—	18	30		
Output enable time	t <sub>ZH</sub>	OC	Q	—	15	28		C <sub>L</sub> = 5 pF, R <sub>L</sub> = 667 Ω
	t <sub>ZL</sub>			—	25	36		
Output disable time	t <sub>HZ</sub>	OC	Q	—	12	20		
	t <sub>LZ</sub>			—	15	25		

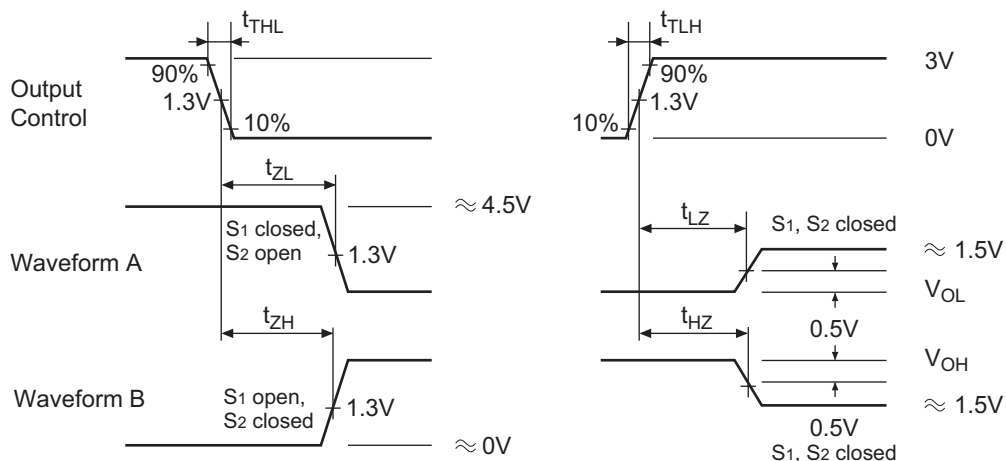


## Waveforms 2



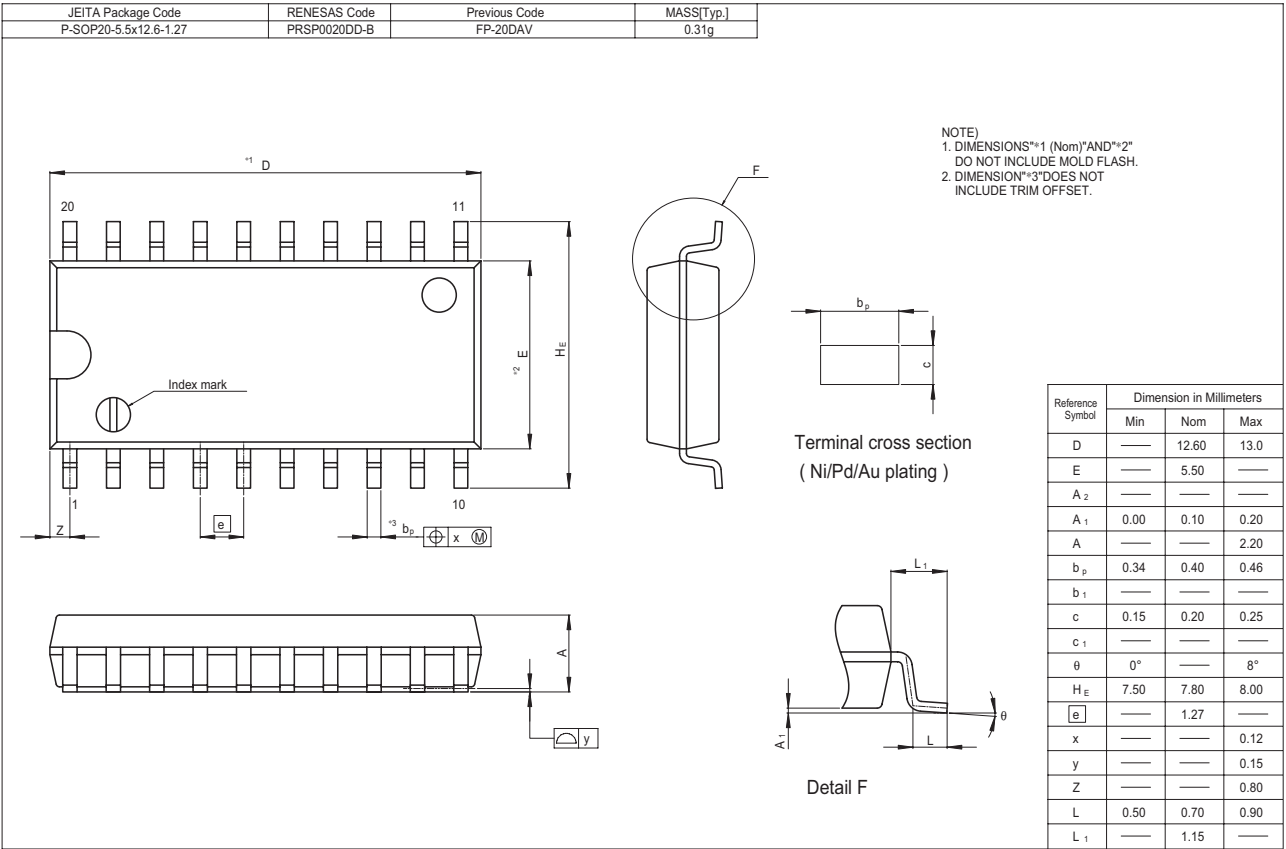
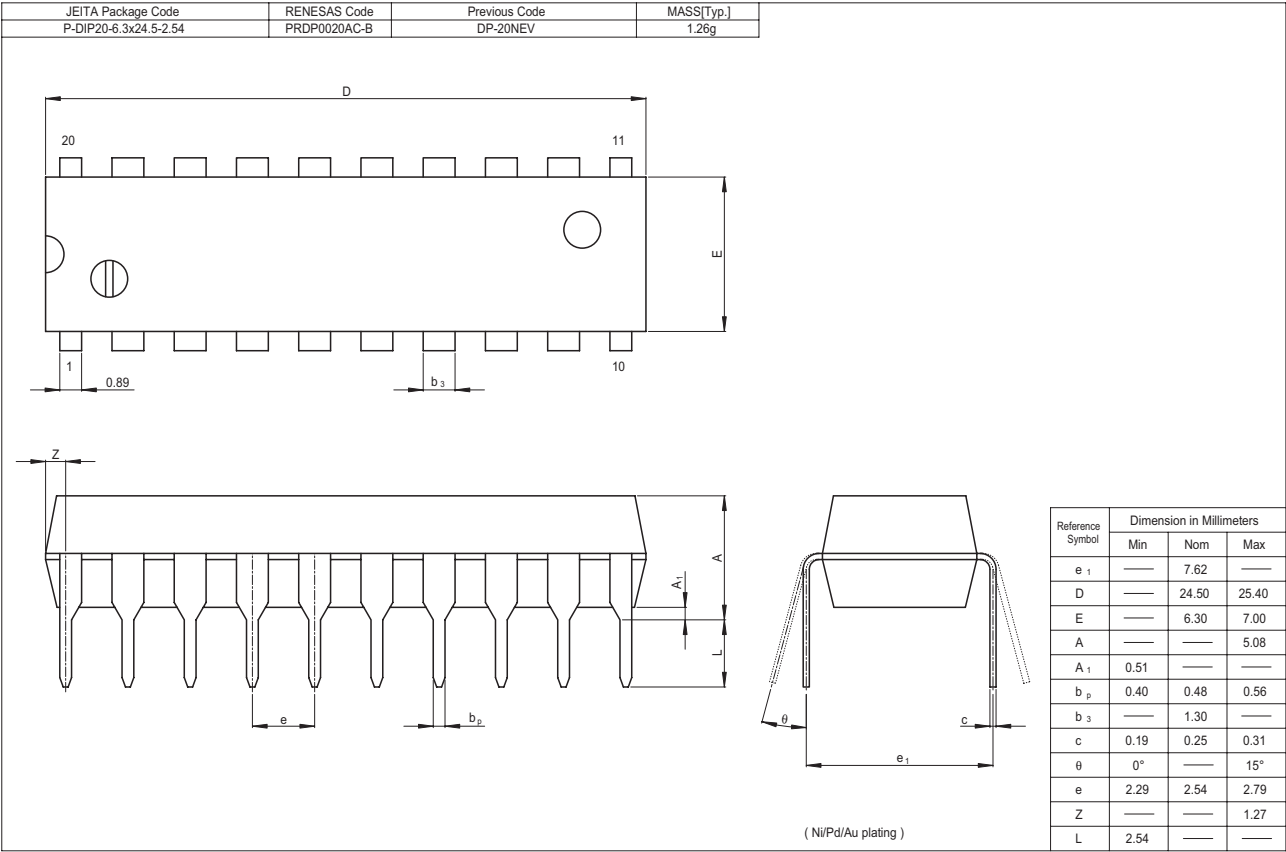
Note: Enable input pulse;  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, PRR = 1 MHz  
Data input pulse;  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, PRR = 1 MHz, G input is high

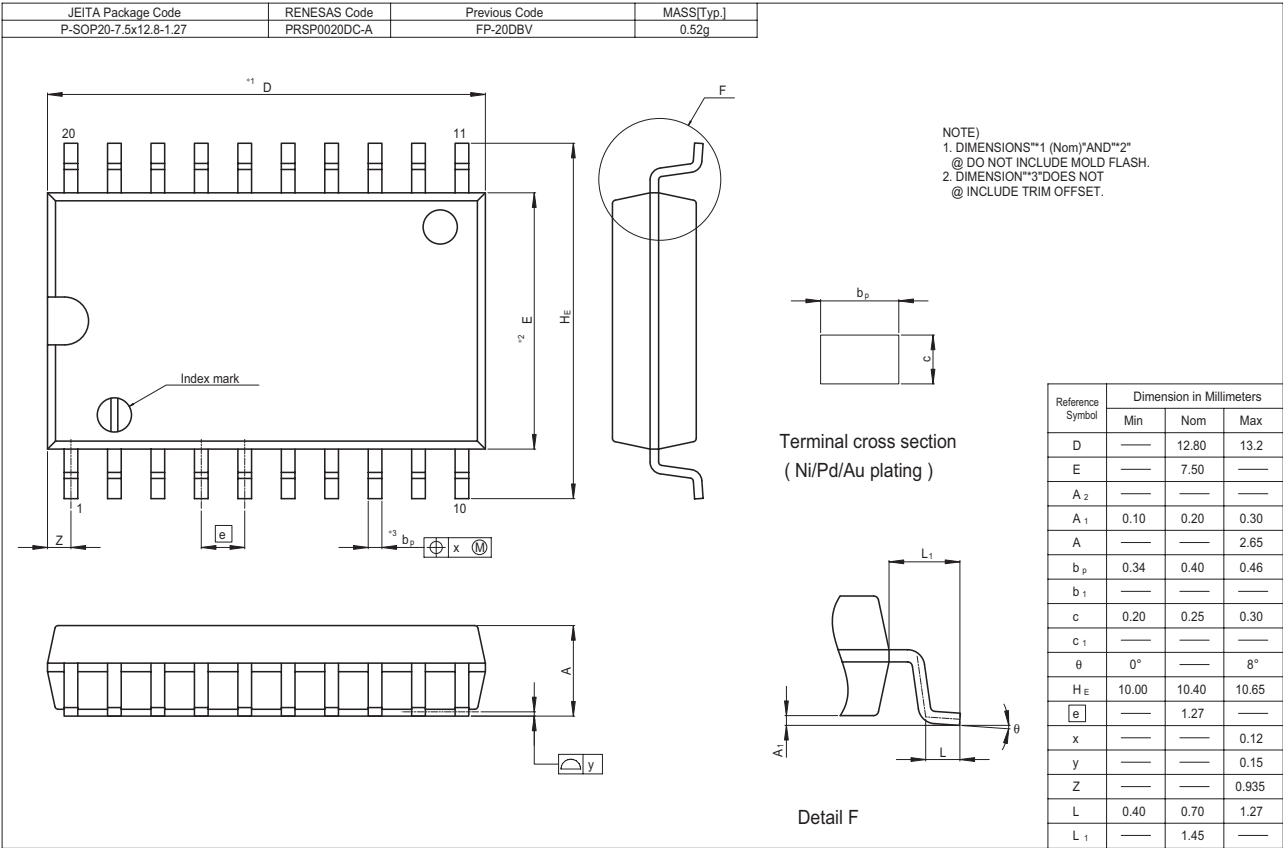
## Waveforms 3



- Notes:
1. Input pulse;  $t_{TLH} \leq 15$  ns,  $t_{THL} \leq 6$  ns, PRR = 1 MHz, duty cycle 50%
  2. Waveform A is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

Package Dimensions





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