

9097248 TOSHIBA (LOGIC/MEMORY)

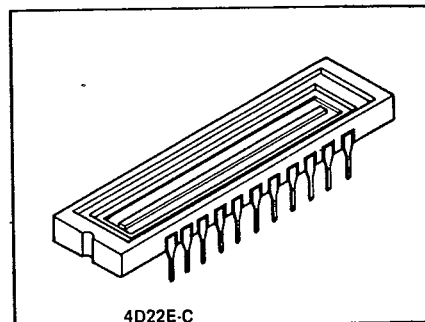
CCD IMAGE SENSOR
CCD (Charge Coupled Device)

TCD101AC

67C 09511 D T-41-55

The TCD101AC is a high resolution and high sensitivity 1728 element linear image sensor. The device is designed for facsimile readers, optical character recognition and other imaging applications.

The device is operated by only 12V power supply, and mounted in 22 pin dual-in-line package with hermetic sealed optical glass window.



4D22E-C

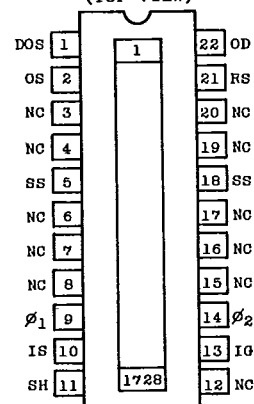
FEATURES:

- . Number of Image Sensing Elements : 1728
- . Image Sensing Element Size : 15 μ m by 15 μ m on 15 μ m centers
- . Photo Sensing Region : High sensitive pn photodiode
- . Clock : 2 Phase
- . Dynamic Range : 600 (Typ.)
- . Package : 22 pin DIP

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Clock Pulse Voltage	V_{ϕ}	-0.3 ~ 15	V
Shift Pulse Voltage	V_{SH}		
Reset Pulse Voltage	V_{RS}		
Output Transistor Drain Voltage	V_{OD}		
Input Gate Voltage	V_{IG}		
Input Source Voltage	V_{IS}	-25 ~ 60	°C
Operating Temperature	T_{opr}		
Storage Temperature	T_{stg}		

Note : All voltage are with respect to SS terminal (Ground)

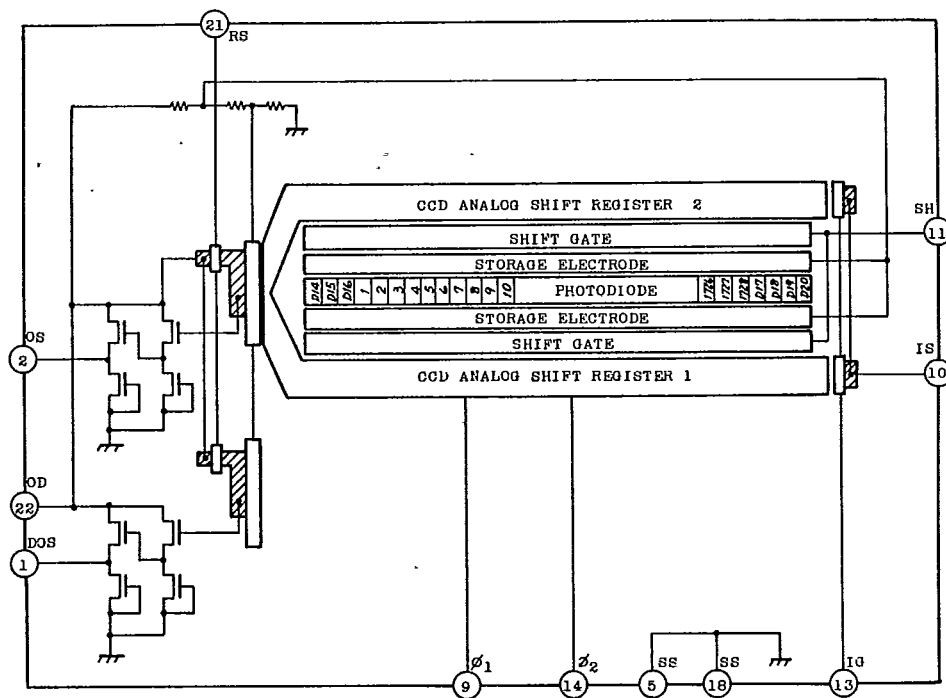
**PIN CONNECTIONS
(TOP VIEW)**

9097248 TOSHIBA (LOGIC/MEMORY)

67C 09512

D

T-41-55

TCD101AC**CIRCUIT DIAGRAM****PIN NAME**

ϕ_1	Clock (Phase 1)
ϕ_2	Clock (Phase 2)
SH	Shift Gate
RS	Reset Gate
OS	Output Transistor Source
DOS	Compensation Transistor Source
OD	Output Transistor Drain
SS	Substrate (Ground)
IS	Input Source (Test Point)
IG	Input Gate (Test Point)
NC	Non Connection

9097248 TOSHIBA (LOGIC/MEMORY)

67C 09513 D

T-41-55

TCD101AC

OPTICAL/ELECTRICAL CHARACTERISTICS

$T_a=25^\circ\text{C}$, $V_{OD}=V_{IS}=12\text{V}$, $V_{IC}=0\text{V}$, $V_\phi=V_{SH}=V_{RS}=12\text{V}$ (Pulse),

$f_\phi=0.5\text{MHz}$, $f_{RS}=1.0\text{MHz}$, t_{INT} (INTEGRATION TIME) = 10msec,

LIGHT SOURCE = DAYLIGHT FLUORESCENT LAMP.

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Responsivity	R	-	0.6	0.8	1.0	V/ $\mu\text{x}\cdot\text{sec}$
Photo Response Non Uniformity	PRNU	Note (1)	-	-	± 10	%
Saturation Output Voltage	V_{SAT}	$V_{OD}=11.4\text{V}$	0.8	1.0	-	V
Saturation Exposure	SE	V_{SAT}/R	0.8	1.25	-	$\mu\text{x}\cdot\text{sec}$
Dark Signal Voltage	V_{DRK}	$V_{OD}=13\text{V}$	-	1.0	6	mV
DC Power Dissipation	P_D	$V_{OD}=13\text{V}$	-	30	58	mW
Total Transfer Efficiency	TTE	-	92	95	-	%
Output Impedance	Z_o	-	-	1.2	3.5	k Ω
Dynamic Range (V_{SAT}/V_{DRK})	DR	V_{SAT}/V_{DRK}	-	600	-	
DC Mismatch Voltage	$ V_{OS}-V_{DOS} $	-	-	-	150	mV

Note (1) : Measured at 50% of SE (Typ.)

PRNU is defined as follows, $PRNU = \frac{\Delta x}{\bar{x}} \times 100 (\%)$

where $\bar{x}$ is average of total photodiode outputs and Δx is deviation of photodiode output under uniform illumination.

9097248 TOSHIBA (LOGIC/MEMORY)

67C 09514

D

T-41-55

TCD101AC

OPERATING CONDITION (Ta=25°C)

CHARACTERISTIC		SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Voltage	H-Level	V_{ϕ}	11	12	13	V
	L-Level		0	0.5	0.8	V
Shift Pulse Voltage	H-Level	V_{SH}	11	12	13	V
	L-Level		0	0.5	0.8	V
Reset Pulse Voltage	H-Level	V_{RS}	11	12	13	V
	L-Level		0	0.5	0.8	V
Output Transistor Drain Voltage		V_{OD}	11.4	12	13	V
Input Gate Voltage		V_{IG}	0	0	1	V
Input Source Voltage		V_{IS}	11	12	13	V

CLOCK CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Pulse Frequency	f_{ϕ}	-	0.5	-	MHz
Reset Pulse Frequency	f_{RS}	-	1.0	-	MHz
Clock Capacitance	C_{ϕ}	-	750	-	pF
Shift Gate Capacitance	C_{SH}	-	250	-	pF
Reset Gate Capacitance	C_{RS}	-	10	-	pF

9097248 TOSHIBA (LOGIC/MEMORY)

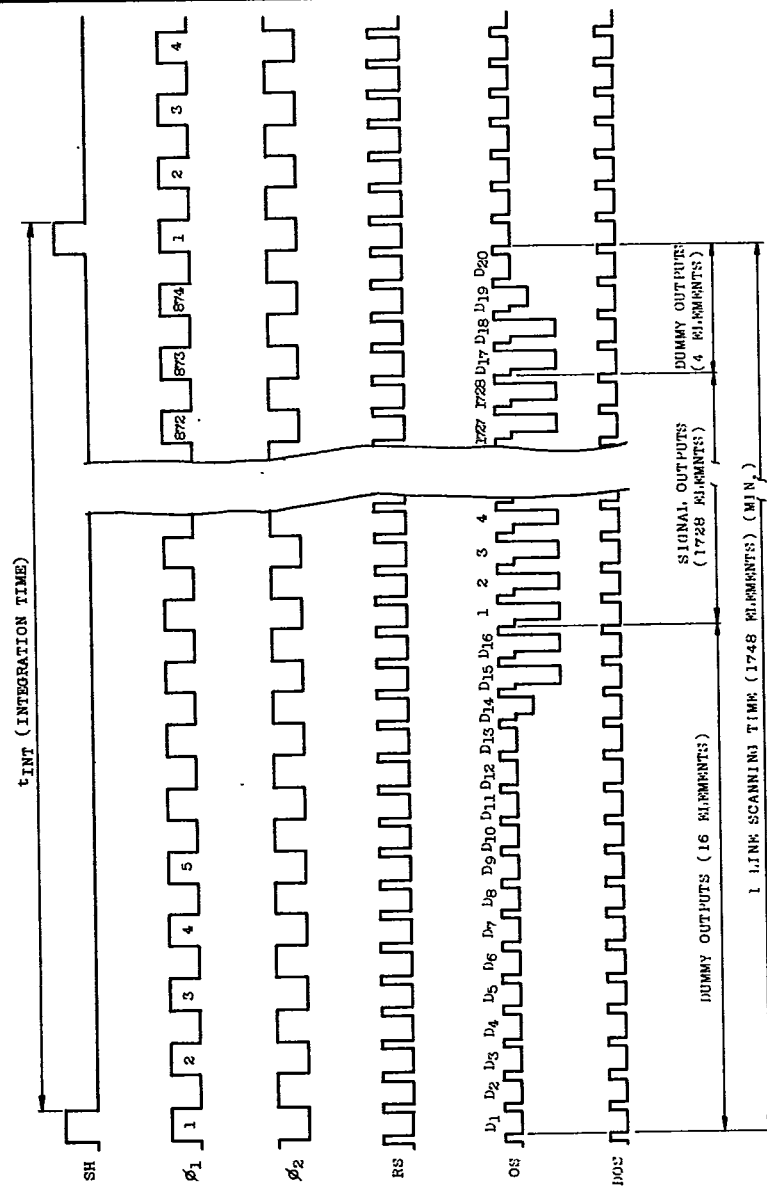
67C 09515

D

T-41-55

TCD101AC

TIMING CHART



9097248 TOSHIBA (LOGIC/MEMORY)

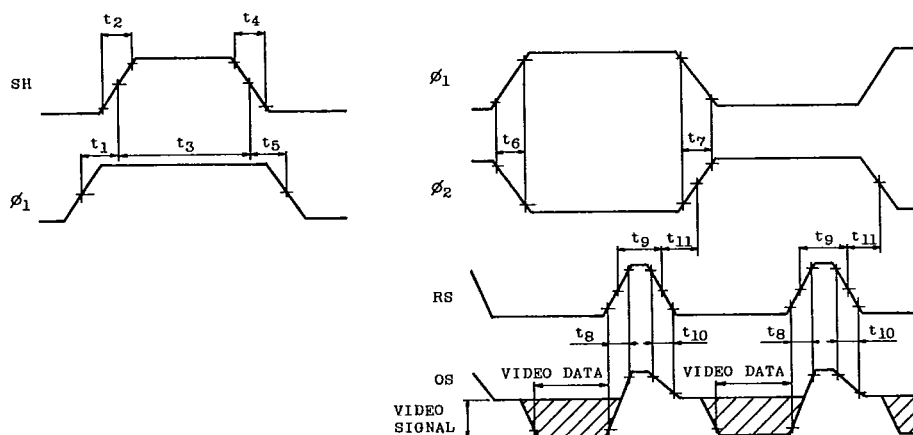
67C 09516

D

T-41-55

TCD101AC

TIMING REQUIREMENTS



CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Pulse Timing of SH and ϕ_1	t_1, t_5	0	100	-	nsec
SH Pulse Rise Time, Fall Time	t_2, t_4	0	50	-	nsec
SH Pulse Width	t_3	60	300	-	nsec
ϕ_1, ϕ_2 Pulse Rise Time, Fall Time	t_6, t_7	0	100	-	nsec
RS Pulse Rise Time, Fall Time	t_8, t_{10}	0	20	-	nsec
RS Pulse Width	t_9	40	250	-	nsec
Pulse Timing of ϕ_1, ϕ_2 and RS	t_{11}	20	250	-	nsec

Note : $f_{RS}=1\text{MHz(Typ.)}$

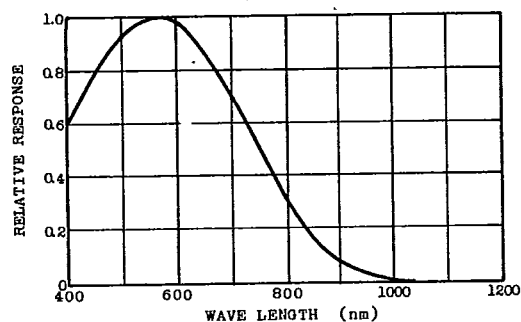
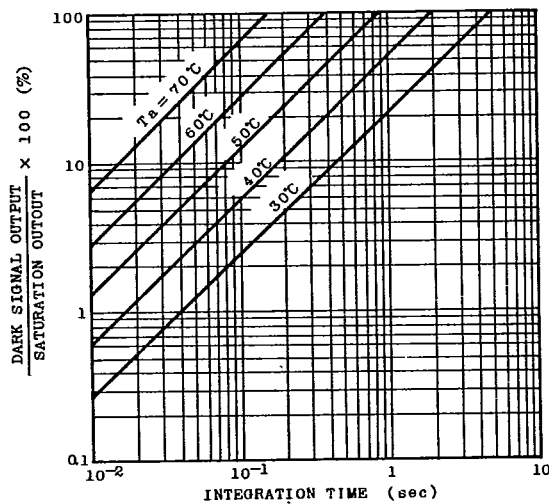
9097248 TOSHIBA (LOGIC/MEMORY)

67C 09517

D

T-41-55

TCD101AC

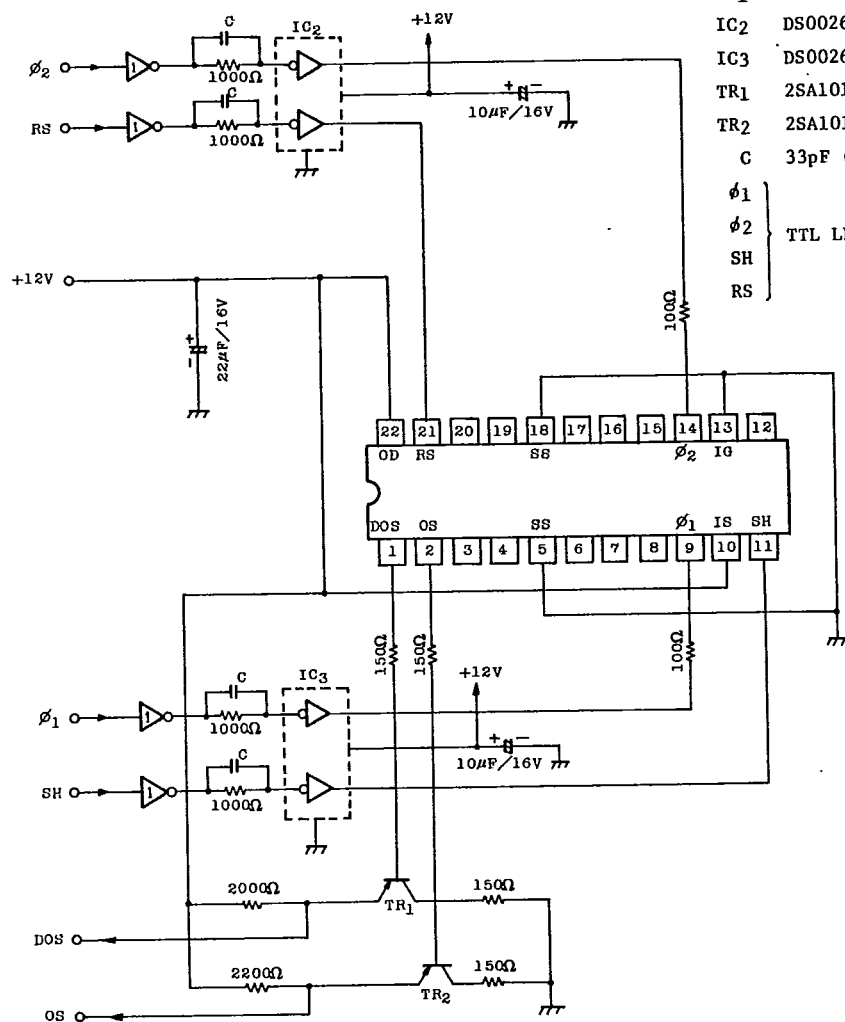
TYPICAL SPECTRAL RESPONSE. ($T_a = 25^\circ\text{C}$)AVERAGE DARK SIGNAL—INTEGRATION TIME
AT DIFFERENT TEMPERATURES

D

TCD101AC

IC ₁	SN74LS04
IC ₂	DS0026CN
IC ₃	DS0026CN
TR ₁	2SA1015
TR ₂	2SA1015
C	33pF (Typ.)

ϕ_1 }
 ϕ_2 } TTL LEVEL INPUT
SH }
RS }



9097248 TOSHIBA (LOGIC/MEMORY)

67C 09519

D

T-41-55

TCD101AC

CAUTION

1. Window Glass

The dust and stain on the glass window of the package degrade optical performance of CCD sensor.

Keep the glass window clean by saturating a cotton swab in alcohol and lightly wiping the surface, and allow the glass to dry, by blowing with filtered dry N₂ or Freon Gas.

Care should be taken to avoid mechanical or thermal shock because the glass window is easily to damage.

2. Electrostatic Breakdown

Store in sgorting clip or in conductive foam to avoid electrostatic breakdown.

3. Incident Light

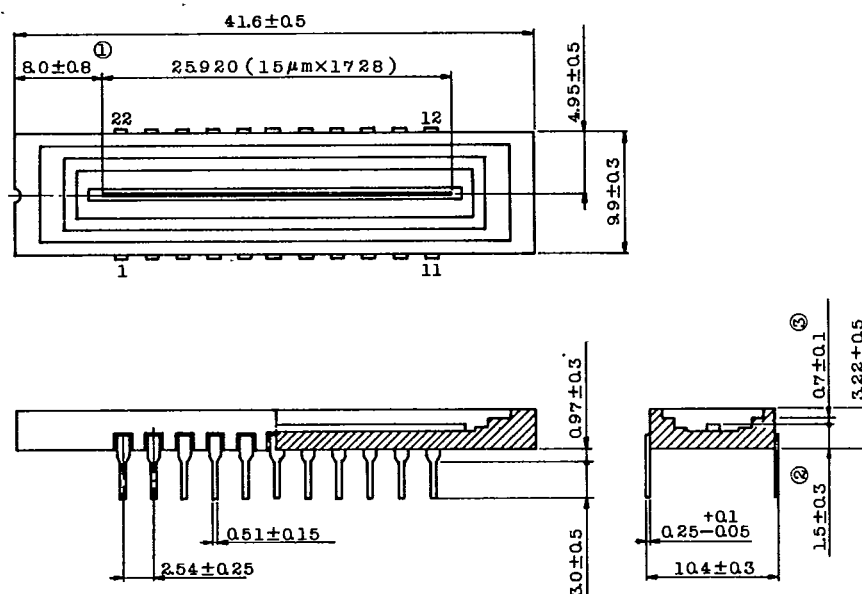
CCD sensor is sensitive to infrared light.

Note that infrared light component degrades resolution and PRNU of CCD sensor.

9097248 TOSHIBA (LOGIC/MEMORY)
67C 09520 D T-41-55
TCD101AC

PACKAGE OUTLINE (4D22E-C)

Unit in mm



- ① No. 1 SENSOR ELEMENT(S1) TO EDGE OF PACKAGE.
- ② TOP OF CHIP TO BOTTOM OF CERAMIC.
- ③ GLASS THICKNESS ($n=1.5$)