Z-Accel 2.4 GHz ZigBee® Processor

Accelerate your ZigBee Development

Applications

- *ZigBee™ systems*
- *Home/Building automation*
- *Industrial control and monitoring*
- *Low power wireless sensor networks*
- *Set-top boxes and remote controls*
- *Automated Meter Reading*

Description

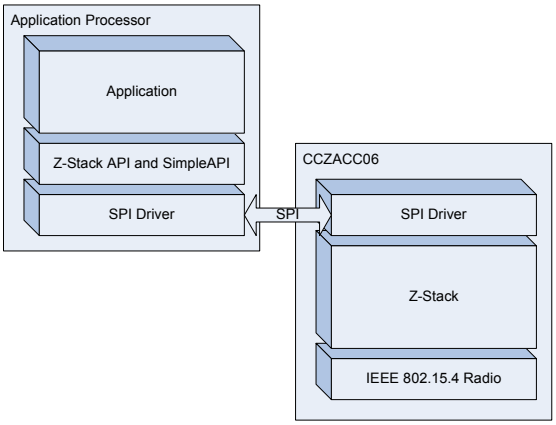
The ***CCZACC06*** is a cost-effective, low power, Z-Accel ZigBee Processor that provides full ZigBee functionality with a minimal development effort.

Z-Accel is a solution where TI's ZigBee stack, Z-Stack, runs on a ZigBee Processor and the application runs on an external microcontroller. The ***CCZACC06*** handles all the timing critical and processing intensive ZigBee protocol tasks, and leaves the resources of the application microcontroller free to handle the application.

Z-Accel makes it easy to add ZigBee to new or existing products at the same time as it provides great flexibility in choice of microcontroller.

CCZACC06 interfaces any microcontroller through an SPI or UART interface. There is no need to learn a new microcontroller or new tools. ***CCZACC06*** can for example be combined with an MSP430.

CCZACC06 supports TI's SimpleAPI. SimpleAPI has only 10 API calls to learn, which drastically simplifies the development of ZigBee applications.



Key Features

- Simple integration of ZigBee into any design
- Running the mature and stable ZigBee 2006 compliant TI Z-Stack
- SPI or UART interface to any microcontroller running the application
- Simple API and full ZigBee API supported
- Can implement any type of ZigBee device: Coordinator, Router or End Device
- Automatically enters low power mode (<0.5 uA) in idle periods when configured as End Device
- Radio
  - Fully integrated and robust IEEE 802.15.4-compliant 2.4 GHz DSSS RF transceiver
  - Excellent receiver sensitivity and best in class robustness to interferers
- Power Supply
  - Wide supply voltage range (2.0V – 3.6V)
  - Low current consumption (RX: 27 mA, TX: 27 mA) and fast transition times.
- External System
  - Very few external components
  - RoHS compliant 7x7mm QLP48 package
- Peripherals and Supporting Functions
  - Port expander with 4 general I/O pins, two with increased sink/source capability
  - Battery monitor and temperature sensor
  - 7-12 bits ADC with two channels
  - Robust power-on-reset and brown-out-reset circuitry
- Tools and Development
  - Packet sniffer PC software
  - Reference designs

Table Of Contents

1 Abbreviations

ADC	Analog to Digital Converter
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
API	Application Programming Interface
ARIB	Association of Radio Industries and Businesses
BOD	Brown Out Detector
BOM	Bill of Materials
CCA	Clear Channel Assessment
CFR	Code of Federal Regulations
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSMA-CA	Carrier Sense Multiple Access with Collision Avoidance
CW	Continuous Wave
DAC	Digital to Analog Converter
DC	Direct Current
DNL	Differential Nonlinearity
DSM	Delta Sigma Modulator
DSSS	Direct Sequence Spread Spectrum
EM	Evaluation Module
ENOB	Effective Number of bits
ESD	Electro Static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVM	Error Vector Magnitude
FCC	Federal Communications Commission
FCF	Frame Control Field
FCS	Frame Check Sequence
I/O	Input / Output
I/Q	In-phase / Quadrature-phase
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
INL	Integral Nonlinearity
ISM	Industrial, Scientific and Medical
JEDEC	Joint Electron Device Engineering Council
KB	1024 bytes
kbps	kilo bits per second
LFSR	Linear Feedback Shift Register
LNA	Low-Noise Amplifier
LO	Local Oscillator
LQI	Link Quality Indication
LSB	Least Significant Bit / Byte
LSB	Least Significant Byte
MAC	Medium Access Control
MISO	Master In Slave Out
MOSI	Master Out Slave In
MPDU	MAC Protocol Data Unit
MSB	Most Significant Byte
MUX	Multiplexer
NA	Not Available
NC	Not Connected
O-QPSK	Offset - Quadrature Phase Shift Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PER	Packet Error Rate
PHY	Physical Layer
PLL	Phase Locked Loop
PM{0-3}	Power Mode 0-3
POR	Power On Reset
PWM	Pulse Width Modulator
QLP	Quad Leadless Package
RAM	Random Access Memory
RC	Resistor-Capacitor
RCOSC	RC Oscillator
RF	Radio Frequency
RoHS	Restriction on Hazardous Substances
RSSI	Receive Signal Strength Indicator
RX	Receive
SCK	Serial Clock
SFD	Start of Frame Delimiter
SHR	Synchronization Header
SINAD	Signal-to-noise and distortion ratio
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
ST	Sleep Timer
T/R	Tape and reel
T/R	Transmit / Receive
TBD	To Be Decided / To Be Defined
THD	Total Harmonic Distortion
TI	Texas Instruments
TX	Transmit
UART	Universal Asynchronous Receiver/Transmitter
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
VGA	Variable Gain Amplifier
XOSC	Crystal Oscillator

2 References

[1] IEEE std. 802.15.4 - 2006: Wireless Medium Access Control (MAC) and Physical Layer (PHY) specifications for Low Rate Wireless Personal Area Networks (LR-WPANs).
http://standards.ieee.org/getieee802/download/802.15.4-2006.pdf

[2] CCZACC06 Interface Specification
http://www.ti.com/lit/pdf/swra175

3 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings given in Table 1 be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Table 1: Absolute Maximum Ratings

Parameter	Min	Max	Units	Condition
Supply voltage, VDD	–0.3	3.9	V	All supply pins must have the same voltage
Voltage on any digital pin	–0.3	VDD+0.3, max 3.9	V	
Voltage on the 1.8V pins (pin no. 22, 25-40 and 42)	–0.3	2.0	V	
Input RF level		10	dBm	
Storage temperature range	–50	150	°C	Device not programmed
Reflow soldering temperature		260	°C	According to IPC/JEDEC J-STD-020C
ESD		<500	V	On RF pads (RF_P, RF_N, AVDD_RF1, and AVDD_RF2), according to Human Body Model, JEDEC STD 22, method A114
		700	V	All other pads, according to Human Body Model, JEDEC STD 22, method A114
		200	V	According to Charged Device Model, JEDEC STD 22, method C101

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

4 Operating Conditions

The operating conditions for ***CCZACC06*** are listed in Table 2.

Table 2: Operating Conditions

Parameter	Min	Max	Unit	Condition
Operating ambient temperature range, T_A	-40	85	°C	
Operating supply voltage	2.0	3.6	V	The supply pins to the radio part must be driven by the 1.8 V on-chip regulator

5 Electrical Specifications

Measured on Texas Instruments ***CCZACC06*** EM reference design with T_A=25°C and VDD=3.0V unless stated otherwise.

Table 3: Electrical Specifications

Parameter	Min	Typ	Max	Unit	Condition
Current Consumption					
CPU Active Mode, 16 MHz, low CPU activity		4.3		mA	Digital regulator on. 16 MHz RCOSC running. No radio, crystals, or peripherals active. Low CPU activity: no flash access (i.e. only cache hit), no RAM access.
CPU Active Mode, 16 MHz, medium CPU activity		5.1		mA	Digital regulator on. 16 MHz RCOSC running. No radio, crystals, or peripherals active. Medium CPU activity: normal flash access[1], minor RAM access.
CPU Active Mode, 16 MHz, high CPU activity		5.7		mA	Digital regulator on. 16 MHz RCOSC running. No radio, crystals, or peripherals active. High CPU activity: normal flash access, extensive RAM access and heavy CPU load.
CPU Active Mode, 32 MHz, low CPU activity		9.5		mA	32 MHz XOSC running. No radio or peripherals active. Low CPU activity : no flash access (i.e. only cache hit), no RAM access
CPU Active Mode, 32 MHz, medium CPU activity		10.5		mA	32 MHz XOSC running. No radio or peripherals active. Medium CPU activity: normal flash access, minor RAM access.
CPU Active Mode, 32 MHz, high CPU activity		12.3		mA	32 MHz XOSC running. No radio or peripherals active. High CPU activity: normal flash access, extensive RAM access and heavy CPU load.
CPU Active and RX Mode		26.7		mA	CPU running at full speed (32MHz), 32MHz XOSC running, radio in RX mode, -50 dBm input power. No peripherals active. Low CPU activity.
CPU Active and TX Mode, 0dBm		26.9		mA	CPU running at full speed (32MHz), 32MHz XOSC running, radio in TX mode, 0dBm output power. No peripherals active. Low CPU activity.
Power mode 1		190		µA	Digital regulator on, 16 MHz RCOSC and 32 MHz crystal oscillator off. 32.768 kHz XOSC, POR and ST active. RAM retention.
Power mode 2		0.5		µA	Digital regulator off, 16 MHz RCOSC and 32 MHz crystal oscillator off. 32.768 kHz XOSC, POR and ST active. RAM retention.
Power mode 3		0.3		µA	No clocks. RAM retention. POR active.
Peripheral Current Consumption					Adds to the figures above if the peripheral unit is activated
Sleep Timer		0.2		µA	Including 32.753 kHz RCOSC.
ADC		1.2		mA	When converting.
Flash write		3		mA	Estimated value
Flash erase		3		mA	Estimated value

[1] Normal Flash access means that the code used exceeds the cache storage so cache misses will happen frequently.

5.1 General Characteristics

Measured on Texas Instruments ***CCZACC06*** EM reference design with T_A=25°C and VDD=3.0V unless stated otherwise.

Table 4: General Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
Wake-Up and Timing					
Power mode 1 → power mode 0		4.1		µs	Digital regulator on, 16 MHz RCOSC and 32 MHz crystal oscillator off. Start-up of 16 MHz RCOSC.
Power mode 2 or 3 → power mode 0		120		µs	Digital regulator off, 16 MHz RCOSC and 32 MHz crystal oscillator off. Start-up of regulator and 16 MHz RCOSC.
Active → TX or RX 32MHz XOSC initially OFF. Voltage regulator initially OFF		525		µs	Time from enabling radio part in power mode 0, until TX or RX starts. Includes start-up of voltage regulator and crystal oscillator in parallel. Crystal ESR=16Ω.
Active → TX or RX Voltage regulator initially OFF		320		µs	Time from enabling radio part in power mode 0, until TX or RX starts. Includes start-up of voltage regulator.
Active → RX or TX			192	µs	Radio part already enabled. Time until RX or TX starts.
RX/TX turnaround			192	µs	
Radio part					
RF Frequency Range	2400		2483.5	MHz	Programmable in 1 MHz steps, 5 MHz between channels for compliance with [1]
Radio bit rate		250		kbps	As defined by [1]
Radio chip rate		2.0		MChip/s	As defined by [1]

5.2 RF Receive Section

Measured on Texas Instruments ***CCZACC06*** EM reference design with T_A=25°C and VDD=3.0V unless stated otherwise.

Table 5: RF Receive Parameters

Parameter	Min	Typ	Max	Unit	Condition/Note
Receiver sensitivity		-92		dBm	PER = 1%, as specified by [1] Measured in 50 Ω single endedly through a balun. [1] requires –85 dBm
Saturation (maximum input level)		10		dBm	PER = 1%, as specified by [1] Measured in 50 Ω single endedly through a balun. [1] requires –20 dBm
Adjacent channel rejection + 5 MHz channel spacing		41		dB	Wanted signal -88dBm, adjacent modulated channel at +5 MHz, PER = 1 %, as specified by [1]. [1] requires 0 dB
Adjacent channel rejection - 5 MHz channel spacing		30		dB	Wanted signal -88dBm, adjacent modulated channel at -5 MHz, PER = 1 %, as specified by [1]. [1] requires 0 dB
Alternate channel rejection + 10 MHz channel spacing		55		dB	Wanted signal -88dBm, adjacent modulated channel at +10 MHz, PER = 1 %, as specified by [1] [1] requires 30 dB
Alternate channel rejection - 10 MHz channel spacing		53		dB	Wanted signal -88dBm, adjacent modulated channel at -10 MHz, PER = 1 %, as specified by [1] [1] requires 30 dB
Channel rejection ≥ + 15 MHz ≤ - 15 MHz		 55 53		 dB dB	Wanted signal @ -82 dBm. Undesired signal is an 802.15.4 modulated channel, stepped through all channels from 2405 to 2480 MHz. Signal level for PER = 1%. Values are estimated.
Co-channel rejection		-6		dB	Wanted signal @ -82 dBm. Undesired signal is 802.15.4 modulated at the same frequency as the desired signal. Signal level for PER = 1%.
Blocking / Desensitization + 5 MHz from band edge + 10 MHz from band edge + 20 MHz from band edge + 50 MHz from band edge - 5 MHz from band edge - 10 MHz from band edge - 20 MHz from band edge - 50 MHz from band edge		 -42 -29 -26 -22 -31 -36 -24 -25		 dBm dBm dBm dBm dBm dBm dBm dBm	Wanted signal 3 dB above the sensitivity level, CW jammer, PER = 1%. Measured according to EN 300 440 class 2.
Spurious emission 30 – 1000 MHz 1 – 12.75 GHz			 −64 −75	 dBm dBm	Conducted measurement in a 50 Ω single ended load. Complies with EN 300 328, EN 300 440 class 2, FCC CFR47, Part 15 and ARIB STD-T-66.
Frequency error tolerance		±140		ppm	Difference between centre frequency of the received RF signal and local oscillator frequency. [1] requires minimum 80 ppm
Symbol rate error tolerance		±900		ppm	Difference between incoming symbol rate and the internally generated symbol rate [1] requires minimum 80 ppm

5.3 RF Transmit Section

Measured on Texas Instruments ***CCZACC06*** EM reference design with T_A=25°C, VDD=3.0V, and nominal output power unless stated otherwise.

Table 6: RF Transmit Parameters

Parameter	Min	Typ	Max	Unit	Condition/Note
Nominal output power		0		dBm	Delivered to a single ended 50 Ω load through a balun. [1] requires minimum –3 dBm
Harmonics 2nd harmonic 3rd harmonic 4th harmonic 5th harmonic		 -50.7 -55.8 -54.2 -53.4		 dBm dBm dBm dBm	Measurement conducted with 100 kHz resolution bandwidth on spectrum analyzer. Output Delivered to a single ended 50 Ω load through a balun.
Spurious emission 30 - 1000 MHz 1– 12.75 GHz 1.8 – 1.9 GHz 5.15 – 5.3 GHz		 -47 -43 -58 -56		 dBm dBm dBm dBm	Maximum output power. Texas Instruments ***CCZACC06*** EM reference design complies with EN 300 328, EN 300 440, FCC CFR47 Part 15 and ARIB STD-T-66. Transmit on 2480MHz under FCC is supported by duty-cycling The peak conducted spurious emission is -47 dBm @ 192 MHz which is in an EN 300 440 restricted band limited to -54 dBm. All radiated spurious emissions are within the limits of ETSI/FCC/ARIB. Conducted spurious emission (CSE) can be reduced with a simple band pass filter connected between matching network and RF connector (1.8 pF in parallel with 1.6 nH reduces the CSE by 20 dB), this filter must be connected to good RF ground.
EVM		11		%	Measured as defined by [1] [1] requires max. 35 %
Optimum load impedance		60 + j164		Ω	Differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna[2].

5.4 32 MHz Crystal Oscillator

Measured on Texas Instruments ***CCZACC06*** EM reference design with T_A=25°C and VDD=3.0V unless stated otherwise.

Table 7: 32 MHz Crystal Oscillator Parameters

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency		32		MHz	
Crystal frequency accuracy requirement	- 40		40	ppm	Including aging and temperature dependency, as specified by [1]
ESR	6	16	60	Ω	Simulated over operating conditions
C_0	1	1.9	7	pF	Simulated over operating conditions
C_L	10	13	16	pF	Simulated over operating conditions
Start-up time		212		µs	

5.5 32.768 kHz Crystal Oscillator

Measured on Texas Instruments ***CCZACC06*** EM reference design with T_A=25°C and VDD=3.0V unless stated otherwise.

[2] This is for 2440MHz

Table 8: 32.768 kHz Crystal Oscillator Parameters

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency		32.768		kHz	
Crystal frequency accuracy requirement	–40		40	ppm	Including aging and temperature dependency, as specified by [1]
ESR		40	130	kΩ	Simulated over operating conditions
C_0		0.9	2.0	pF	Simulated over operating conditions
C_L		12	16	pF	Simulated over operating conditions
Start-up time		400		ms	Value is simulated.

5.6 32 kHz RC Oscillator

Measured on Texas Instruments ***CCZACC06*** EM reference design with T_A=25°C and VDD=3.0V unless stated otherwise.

Table 9: 32 kHz RC Oscillator parameters

Parameter	Min	Typ	Max	Unit	Condition/Note
Calibrated frequency		32.753		kHz	The calibrated 32 kHz RC Oscillator frequency is the 32 MHz XTAL frequency divided by 977
Frequency accuracy after calibration		±0.2		%	Value is estimated.
Temperature coefficient		+0.4		% / °C	Frequency drift when temperature changes after calibration. Value is estimated.
Supply voltage coefficient		+3		% / V	Frequency drift when supply voltage changes after calibration. Value is estimated.
Initial calibration time		1.7		ms	When the 32 kHz RC Oscillator is enabled, calibration is continuously done in the background as long as the 32 MHz crystal oscillator is running.

5.7 16 MHz RC Oscillator

Measured on Texas Instruments ***CCZACC06*** EM reference design with T_A=25°C and VDD=3.0V unless stated otherwise.

Table 10: 16 MHz RC Oscillator parameters

Parameter	Min	Typ	Max	Unit	Condition/Note
Frequency		16		MHz	The calibrated 16 MHz RC Oscillator frequency is the 32 MHz XTAL frequency divided by 2
Uncalibrated frequency accuracy		±18		%	
Calibrated frequency accuracy		±0.6	±1	%	
Start-up time			10	µs	
Temperature coefficient			-325	ppm / °C	Frequency drift when temperature changes after calibration
Supply voltage coefficient			28	ppm / mV	Frequency drift when supply voltage changes after calibration
Initial calibration time		50		µs	When the 16 MHz RC Oscillator is enabled it will be calibrated continuously when the 32MHz crystal oscillator is running.

5.8 Frequency Synthesizer Characteristics

Measured on Texas Instruments ***CCZACC06*** EM reference design with T_A=25°C and VDD=3.0V unless stated otherwise.

Table 11: Frequency Synthesizer Parameters

Parameter	Min	Typ	Max	Unit	Condition/Note
Phase noise					Unmodulated carrier
		−116		dBc/Hz	At ±1.5 MHz offset from carrier
		−117		dBc/Hz	At ±3 MHz offset from carrier
		−118		dBc/Hz	At ±5 MHz offset from carrier
PLL lock time			192	µs	The startup time until RX/TX turnaround. The crystal oscillator is running.

5.9 Analog Temperature Sensor

Measured on Texas Instruments ***CCZACC06*** EM reference design with T_A=25°C and VDD=3.0V unless stated otherwise.

Table 12: Analog Temperature Sensor Parameters

Parameter	Min	Typ	Max	Unit	Condition/Note
Output voltage at –40°C		0.648		V	Value is estimated
Output voltage at 0°C		0.743		V	Value is estimated
Output voltage at +40°C		0.840		V	Value is estimated
Output voltage at +80°C		0.939		V	Value is estimated
Temperature coefficient		2.45		mV/°C	Fitted from –20°C to +80°C on estimated values.
Absolute error in calculated temperature		–8		°C	From –20°C to +80°C when assuming best fit for absolute accuracy on estimated values: 0.743V at 0°C and 2.45mV / °C.
Error in calculated temperature, calibrated	-2	0	2	°C	From –20°C to +80°C when using 2.45mV / °C, after 1-point calibration at room temperature. Values are estimated. Indicated min/max with 1-point calibration is based on simulated values for typical process parameters
Current consumption increase when enabled		280		µA	

5.10 ADC

Measured with T_A=25°C and VDD=3.0V. Note that other data may result when using Texas Instruments' ***CCZACC06*** EM reference design.

Table 13: ADC Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
Input voltage	0		VDD	V	VDD is voltage on AVDD_SOC pin
Input resistance, signal		197		kΩ	Simulated using 4 MHz clock speed.
Full-Scale Signal[3]		2.97		V	Peak-to-peak, defines 0dBFS

[3] Measured with 300 Hz Sine input and VDD as reference.

Parameter	Min	Typ	Max	Unit	Condition/Note
ENOB		5.7		bits	7-bits setting.
Single ended input		7.5			9-bits setting.
		9.3			10-bits setting.
		10.8			12-bits setting.
ENOB[Error! Bookmark not defined.]		6.5		bits	7-bits setting.
Differential input		8.3			9-bits setting.
		10.0			10-bits setting.
		11.5			12-bits setting.
Useful Power Bandwidth		0-20		kHz	7-bits setting
THD					
-Single ended input		-75.2		dB	12-bits setting, -6dBFS
-Differential input		-86.6		dB	12-bits setting, -6dBFS
Signal To Non-Harmonic Ratio					
-Single ended input		70.2		dB	12-bits setting
-Differential input		79.3		dB	12-bits setting
Spurious Free Dynamic Range					
-Single ended input		78.8		dB	12-bits setting, -6dBFS
-Differential input		88.9		dB	12-bits setting, -6dBFS
CMRR, differential input		<-84		dB	12- bit setting, 1 kHz Sine (0dBFS), limited by ADC resolution
Crosstalk, single ended input		<-84		dB	12- bit setting, 1 kHz Sine (0dBFS), limited by ADC resolution
Offset		-3		mV	Mid. Scale
Gain error		0.68		%	
DNL		0.05		LSB	12-bits setting, mean
		0.9		LSB	12-bits setting, max
INL		4.6		LSB	12-bits setting, mean
		13.3		LSB	12-bits setting, max
SINAD		35.4		dB	7-bits setting.
Single ended input		46.8		dB	9-bits setting.
(-THD+N)		57.5		dB	10-bits setting.
		66.6		dB	12-bits setting.
SINAD[Error! Bookmark not defined.]		40.7		dB	7-bits setting.
Differential input		51.6		dB	9-bits setting.
(-THD+N)		61.8		dB	10-bits setting.
		70.8		dB	12-bits setting.
Conversion time		20		µs	7-bits setting.
		36		µs	9-bits setting.
		68		µs	10-bits setting.
		132		µs	12-bits setting.
Power Consumption		1.2		mA	

5.11 Control AC Characteristics

T_A= -40°C to 85°C, VDD=2.0V to 3.6V if nothing else stated.

Table 14: Control Inputs AC Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
System clock, f_{SYSCLK} t_{SYSCLK}= 1/ f_{SYSCLK}	16		32	MHz	System clock is 32 MHz when crystal oscillator is used. System clock is 16 MHz when calibrated 16 MHz RC oscillator is used.
RESET_N low width	250			ns	See item 1, Figure 1. This is the shortest pulse that is guaranteed to be recognized as a complete reset pin request. Note that shorter pulses may be recognized but will not lead to complete reset of all modules within the chip.
Interrupt pulse width	t_{SYSCLK}			ns	See item 2, Figure 1.This is the shortest pulse that is guaranteed to be recognized as an interrupt request. In PM2/3 the internal synchronizers are bypassed so this requirement does not apply in PM2/3.

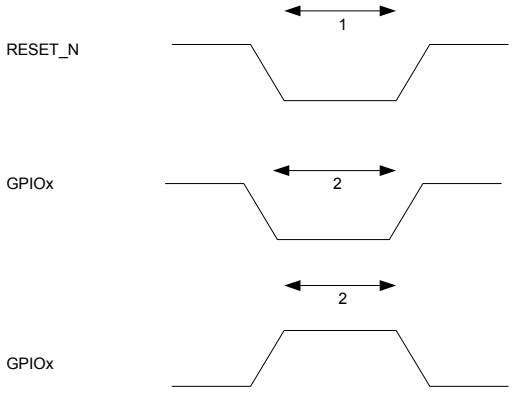


Figure 1: Control Inputs AC Characteristics

5.12 SPI AC Characteristics

T_A= -40°C to 85°C, VDD=2.0V to 3.6V if nothing else stated.

Table 15: SPI AC Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
SSN low to SCK	$2*t_{SYSCLK}$				See item 5 Figure 2
SCK to SSN high	30			ns	See item 6 Figure 2
SCK period	100			ns	See item 1 Figure 2
SCK duty cycle		50%			
SI setup	10			ns	See item 2 Figure 2
SI hold	10			ns	See item 3 Figure 2
SCK to SO			25	ns	See item 4 Figure 2, load = 10 pF

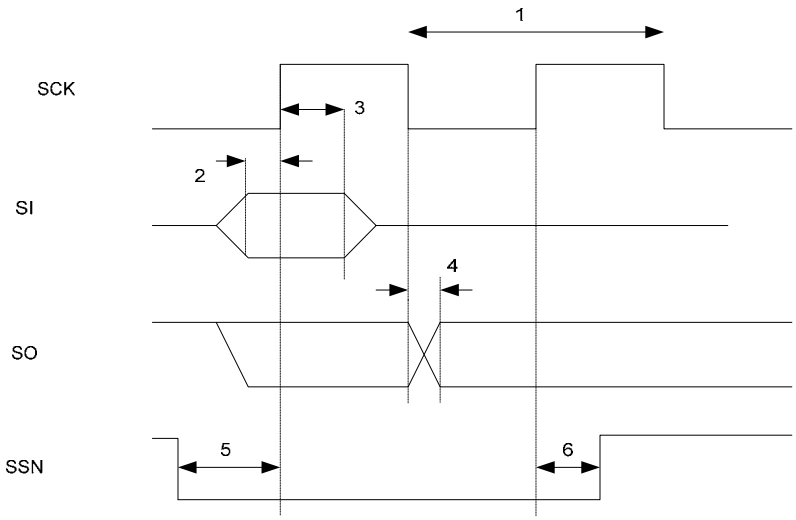


Figure 2: SPI AC Characteristics

5.13 Port Outputs AC Characteristics

T_A= 25°C, VDD=3.0V if nothing else stated.

Table 16: Port Outputs AC Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
GPIO/USART output rise time (SC=0/SC=1)		3.15/ 1.34		ns	Load = 10 pF Timing is with respect to 10% VDD and 90% VDD levels. Values are estimated
fall time (SC=0/SC=1)		3.2/ 1.44			Load = 10 pF Timing is with respect to 90% VDD and 10% VDD. Values are estimated

5.14 DC Characteristics

The DC Characteristics of ***CCZACC06*** are listed in Table 17 below.

T_A=25°C, VDD=3.0V if nothing else stated.

Table 17: DC Characteristics

Digital Inputs/Outputs	Min	Typ	Max	Unit	Condition
Logic "0" input voltage			30	%	Of VDD supply (2.0 – 3.6 V)
Logic "1" input voltage	70			%	Of VDD supply (2.0 – 3.6 V)
Logic "0" input current per pin	NA		12	nA	Input equals 0V
Logic "1" input current	NA		12	nA	Input equals VDD
Total logic “0” input current all pins			70	nA	
Total logic “1” input current all pins			70	nA	
I/O pin pull-up and pull-down resistor		20		kΩ	

6 Pin and I/O Port Configuration

The ***CCZACC06*** pinout is shown in Figure 3 with details in Table 18.

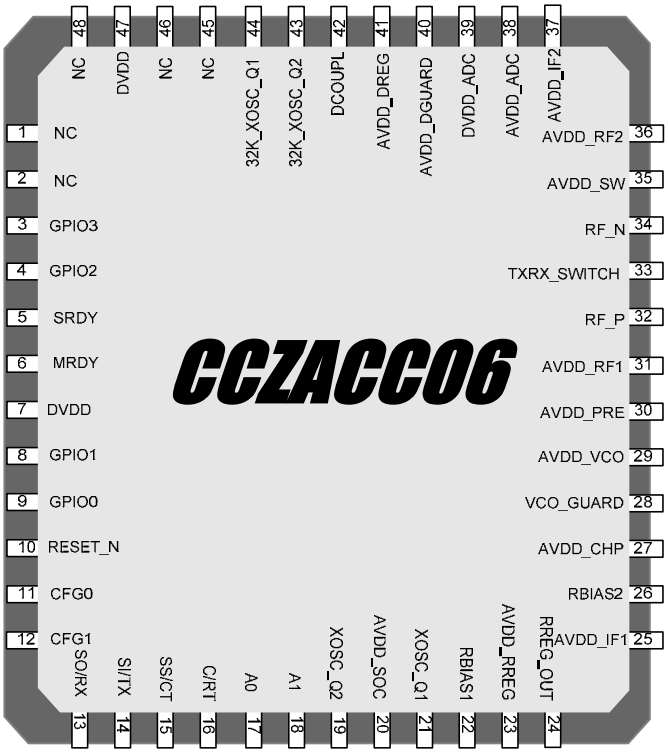


Figure 3: Pinout top view

Note: The exposed die attach pad **must** be connected to a solid ground plane as this is the ground connection for the chip.

Table 18: Pinout overview

Pin	Pin name	Pin type	Description
-	GND	Ground	The exposed die attach pad must be connected to a solid ground plane
1	NC	N/A	
2	NC	N/A	
3	GPIO3	Digital I/O	General I/O pin 3
4	GPIO2	Digital I/O	General I/O pin 2
5	SRDY	Digital Output	Slave ready. Mandatory for SPI, optional for UART.
6	MRDY	Digital Input	Master ready. Optional for SPI and UART.
7	DVDD	Power (Digital)	2.0V-3.6V digital power supply for digital I/O
8	GPIO1	Digital I/O	General I/O pin 1 – increased drive capability
9	GPIO0	Digital I/O	General I/Opin 0 – increased drive capability
10	RESET_N	Digital input	Reset, active low
11	CFG0	Digital Input	Configuration input 0
12	CFG1	Digital Input	Configuration input 1
13	SO/RX	Digital Input	SPI slave output or UART RX data
14	SI/TX	Digital Output	SPI slave input or UART TX data
15	SS/CT	Digital I/O	SPI slave select (in) or UART CTS (out)
16	C/RT	Digital Input	SPI clock or UART RTS
17	A0	Analog Input	ADC input A0
18	A1	Analog Input	ADC input A1
19	XOSC_Q2	Analog I/O	32 MHz crystal oscillator pin 2
20	AVDD_SOC	Power (Analog)	2.0V-3.6V analog power supply connection
21	XOSC_Q1	Analog I/O	32 MHz crystal oscillator pin 1, or external clock input
22	RBIAS1	Analog I/O	External precision bias resistor for reference current
23	AVDD_RREG	Power (Analog)	2.0V-3.6V analog power supply connection
24	RREG_OUT	Power output	1.8V Voltage regulator power supply output. Only intended for supplying the analog 1.8V part (power supply for pins 25, 27-31, 35-40).
25	AVDD_IF1	Power (Analog)	1.8V Power supply for the receiver band pass filter, analog test module, global bias and first part of the VGA
26	RBIAS2	Analog output	External precision resistor, 43 kΩ, ±1 %
27	AVDD_CHP	Power (Analog)	1.8V Power supply for phase detector, charge pump and first part of loop filter
28	VCO_GUARD	Power (Analog)	Connection of guard ring for VCO (to AVDD) shielding
29	AVDD_VCO	Power (Analog)	1.8V Power supply for VCO and last part of PLL loop filter
30	AVDD_PRE	Power (Analog)	1.8V Power supply for Prescaler, Div-2 and LO buffers
31	AVDD_RF1	Power (Analog)	1.8V Power supply for LNA, front-end bias and PA
32	RF_P	RF I/O	Positive RF input signal to LNA during RX. Positive RF output signal from PA during TX
33	TXRX_SWITCH	Power (Analog)	Regulated supply voltage for PA
34	RF_N	RF I/O	Negative RF input signal to LNA during RX Negative RF output signal from PA during TX
35	AVDD_SW	Power (Analog)	1.8V Power supply for LNA / PA switch
36	AVDD_RF2	Power (Analog)	1.8V Power supply for receive and transmit mixers
37	AVDD_IF2	Power (Analog)	1.8V Power supply for transmit low pass filter and last stages of VGA
38	AVDD_ADC	Power (Analog)	1.8V Power supply for analog parts of ADCs and DACs
39	DVDD_ADC	Power (Digital)	1.8V Power supply for digital parts of ADCs
40	AVDD_DGUARD	Power (Digital)	Power supply connection for digital noise isolation
41	AVDD_DREG	Power (Digital)	2.0V-3.6V digital power supply for digital core voltage regulator
42	DCOUPL	Power (Digital)	1.8V digital power supply decoupling. Do not use for supplying external circuits.
43	32K_XOSC_Q2	Analog I/O	32.768 kHz XOSC
44	32K_XOSC_Q1	Analog I/O	32.768 kHz XOSC
45	NC	N/A	
46	NC	N/A	
47	DVDD	Power (Digital)	2.0V-3.6V digital power supply for digital I/O
48	NC	N/A	

7 Circuit Description

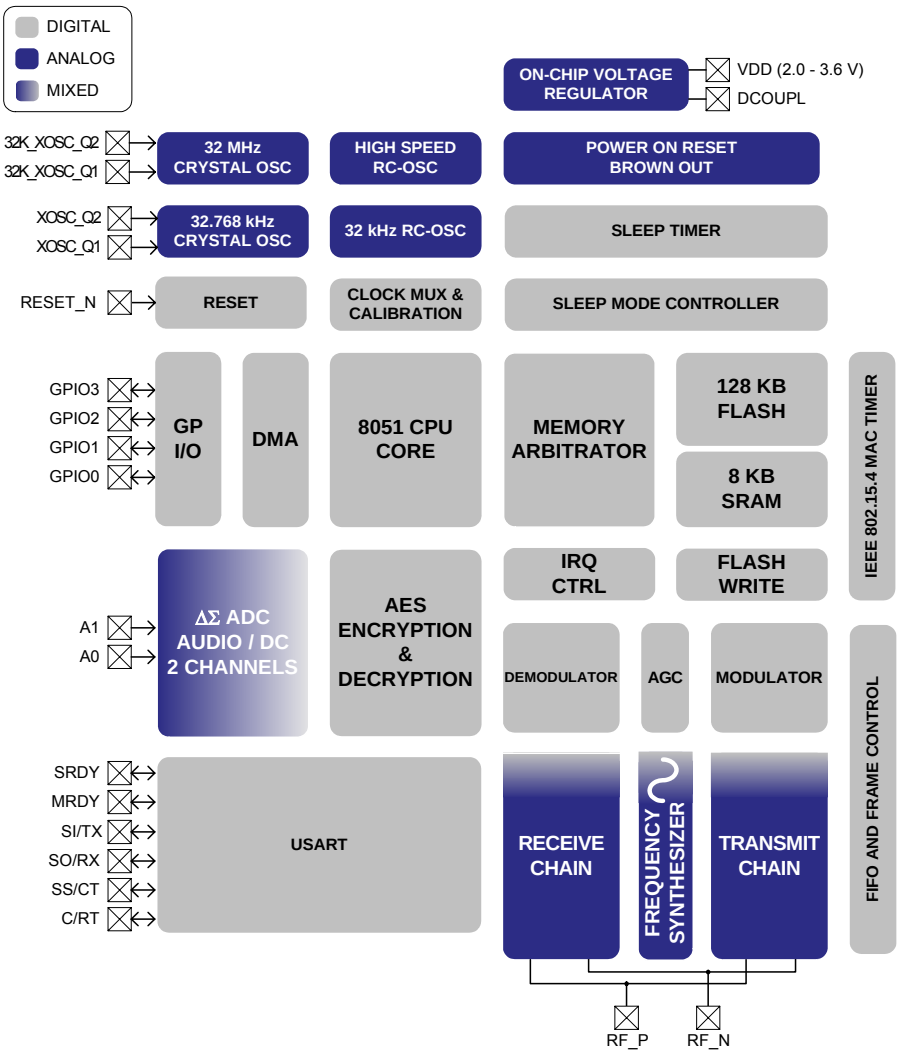


Figure 4: CCZACC06 Block Diagram

A block diagram of ***CCZACC06*** is shown in Figure 4. The modules can be roughly divided into one of three categories: CPU-related modules, modules related to power and clock distribution, and radio-related modules. ***CCZACC06*** features an IEEE 802.15.4 compliant radio based on the leading ***CC2420*** transceiver. See Section 10 for details.

8 Application Circuit

Few external components are required for the operation of ***CCZACC06***. A typical application circuit is shown in Figure 5. Typical values and description of external components are shown in Table 19.

8.1 Input / output matching

The RF input/output is high impedance and differential. The optimum differential load for the RF port is 60 + j164 Ω[4].

When using an unbalanced antenna such as a monopole, a balun should be used in order to optimize performance. The balun can be implemented using low-cost discrete inductors and capacitors. The recommended balun shown, consists of C341, L341, L321 and L331 together with a PCB microstrip transmission line (λ/2-dipole), and will match the RF input/output to 50 Ω. An internal T/R switch circuit is used to switch between the LNA (RX) and the PA (TX). See Input/output matching section on page 33 for more details.

If a balanced antenna such as a folded dipole is used, the balun can be omitted. If the antenna also provides a DC path from TXRX_SWITCH pin to the RF pins, inductors are not needed for DC bias.

Figure 5 shows a suggested application circuit using a differential antenna. The antenna type is a standard folded dipole. The dipole has a virtual ground point; hence bias is provided without degradation in antenna performance. Also refer to the section Antenna Considerations on page 35.

[4] This is for 2440MHz.

8.2 Bias resistors

The bias resistors are R221 and R261. The bias resistor R221 is used to set an accurate bias current for the 32 MHz crystal oscillator.

8.3 Crystal

An external 32 MHz crystal, XTAL1, with two loading capacitors (C191 and C211) is used for the 32 MHz crystal oscillator. See page 10 for details. The load capacitance seen by the 32 MHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{191}} + \frac{1}{C_{211}}} + C_{parasitic}$$

XTAL2 is an optional 32.768 kHz crystal, with two loading capacitors (C441 and C431), used for the 32.768 kHz crystal oscillator. The 32.768 kHz crystal oscillator is used in applications where you need both very low sleep current consumption and accurate wake up times. The load capacitance seen by the 32.768 kHz crystal is given by:

$$C_L = \frac{1}{\frac{1}{C_{441}} + \frac{1}{C_{431}}} + C_{parasitic}$$

A series resistor may be used to comply with the ESR requirement.

8.4 Voltage regulators

The on chip voltage regulators supply all 1.8 V power supply pins and internal power supplies. C241 and C421 are required for stability of the regulators.

8.5 Power supply decoupling and filtering

Proper power supply decoupling must be used for optimum performance. The placement and size of the decoupling capacitors and the power supply filtering are very important to achieve the best performance in an application. TI provides a compact reference design that should be followed very closely.

Refer to the section PCB Layout Recommendation on page 35.

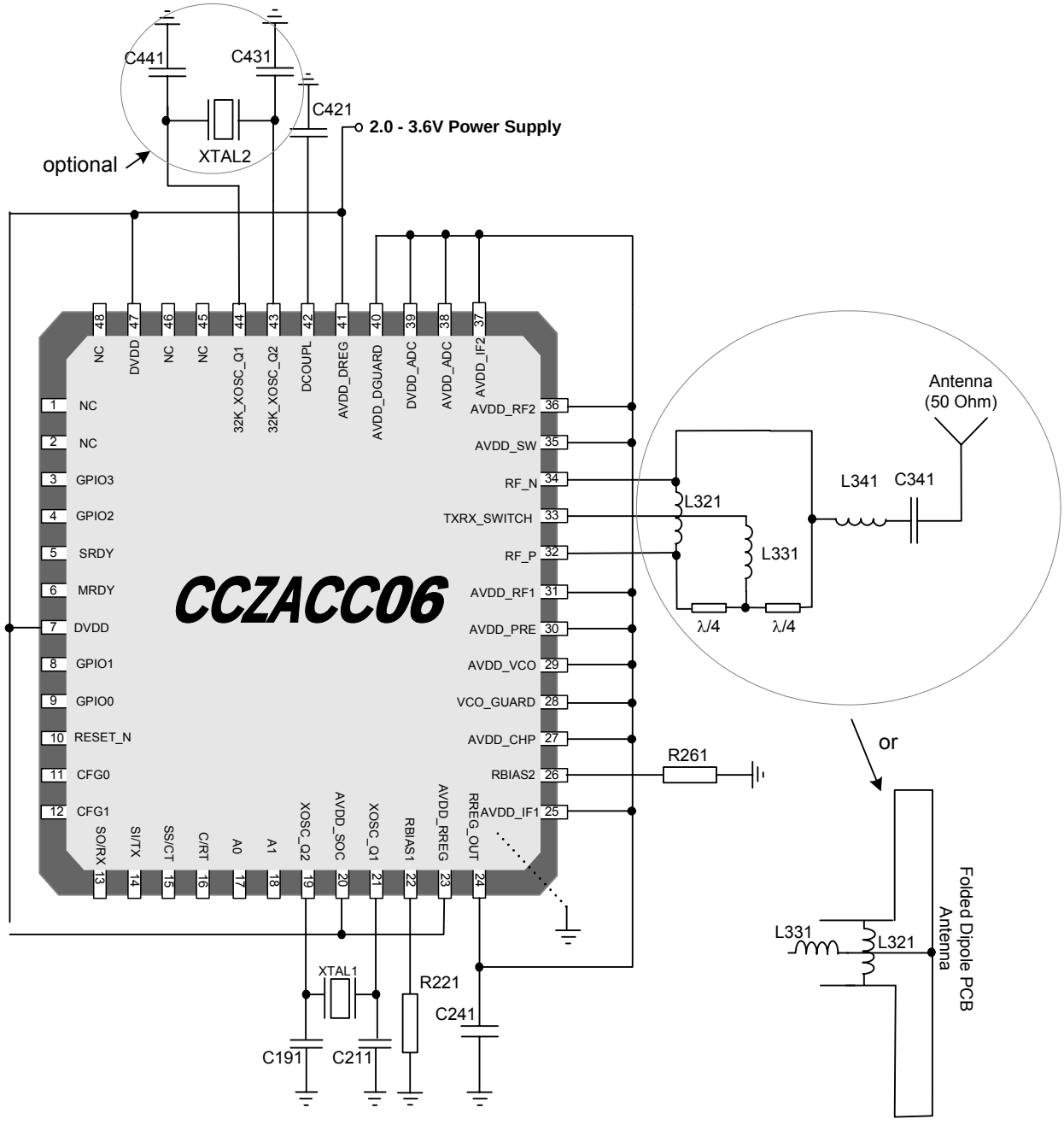


Figure 5: CCZACC06 Application Circuit. (Digital I/O and ADC interface not connected). Decoupling capacitors not shown.

Table 19: Overview of external components (excluding supply decoupling capacitors)

Component	Description	Single Ended 50Ω Output	Differential Antenna
C191	32 MHz crystal load capacitor	33 pF, 5%, NP0, 0402	33 pF, 5%, NP0, 0402
C211	32 MHz crystal load capacitor	27 pF, 5%, NP0, 0402	27 pF, 5%, NP0, 0402
C241	Load capacitance for analogue power supply voltage regulators	220 nF, 10%, 0402	220 nF, 10%, 0402
C421	Load capacitance for digital power supply voltage regulators	1 µF, 10%, 0402	1 µF, 10%, 0402
C341	DC block to antenna and match Note: For RF connector a LP filter can be connected between this C, the antenna and good ground in order to remove conducted spurious emission by using 1.8pF in parallel with 1.6nH	5.6 pF, 5%, NP0, 0402	Not used
		1.8 pF, Murata COG 0402, GRM15 1.6 nH, Murata 0402, LQG15HS1N6S02	
C431, C441	32.768 kHz crystal load capacitor (if low-frequency crystal is needed in application)	15 pF, 5%, NP0, 0402	15 pF, 5%, NP0, 0402
L321	Discrete balun and match	6.8 nH, 5%, Monolithic/multilayer, 0402	12 nH 5%, Monolithic/multilayer, 0402
L331	Discrete balun and match	22 nH, 5%, Monolithic/multilayer, 0402	27 nH, 5%, Monolithic/multilayer, 0402
L341	Discrete balun and match	1.8 nH, +/-0.3 nH, Monolithic/multilayer, 0402	Not used
R221	Precision resistor for current reference generator to system-on-chip part	56 kΩ, 1%, 0402	56 kΩ, 1%, 0402
R261	Precision resistor for current reference generator to RF part	43 kΩ, 1%, 0402	43 kΩ, 1%, 0402
XTAL1	32 MHz Crystal	32 MHz crystal, ESR < 60 Ω	32 MHz crystal, ESR < 60 Ω
XTAL2	Optional 32.768 kHz watch crystal (if low-frequency crystal is needed in application)	32.768 kHz crystal, Epson MC 306.	32.768 kHz crystal, Epson MC 306.

9 Peripherals

In the following sub-sections the user-accessible ***CCZACC06*** peripheral modules are described in detail.

9.1 Reset

The ***CCZACC06*** has four reset sources. The following events generate a reset:

- Forcing RESET_N input pin low
- A power-on reset condition
- A brown-out reset condition
- A firmware-generated reset (SYS_RESET_REQ [2])

The initial conditions after a reset are as follows:

- I/O pins are configured as inputs with pull-up
- See the ***CCZACC06*** user guide [2] for a description of the interaction between CCZACC06 and the host processor after reset.

9.1.1 Power On Reset and Brown Out Detector

The ***CCZACC06*** includes a Power On Reset (POR) providing correct initialization during device power-on. Also includes is a Brown Out Detector (BOD) operating on the regulated 1.8V digital power supply only, The BOD will protect the memory contents during supply voltage variations which cause the regulated 1.8V power to drop below the minimum level required by flash memory and SRAM.

When power is initially applied to the ***CCZACC06*** the Power On Reset (POR) and Brown Out Detector (BOD) will hold the device in reset state until the supply voltage reaches above the Power On Reset and Brown Out voltages.

Figure 6 shows the POR/BOD operation with the 1.8V (typical) regulated supply voltage together with the active low reset signals BOD_RESET and POR_RESET shown in the bottom of the figure (note that signals are not available, just for illustration of events).

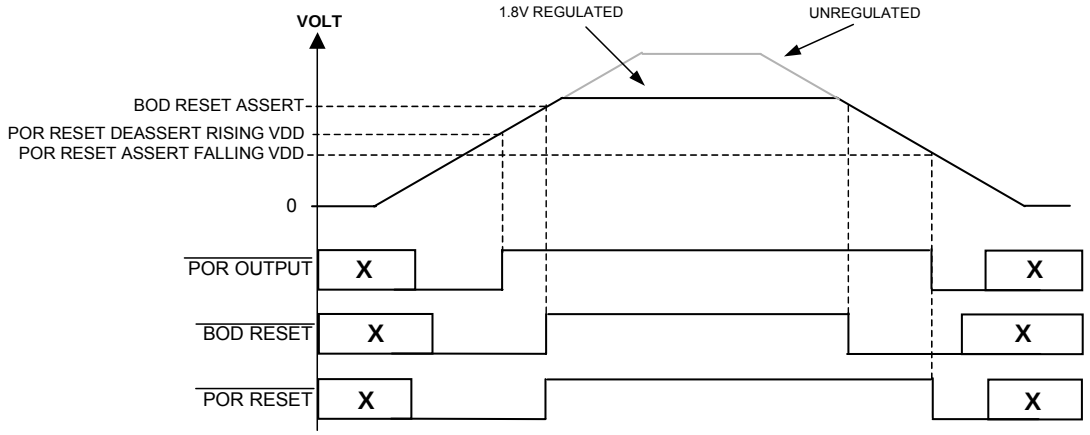


Figure 6 : Power On Reset and Brown Out Detector Operation

9.2 I/O ports

The ***CCZACC06*** has digital input/output pins that have the following key features:

- General purpose I/O or peripheral I/O
- Pull-up or pull-down capability on inputs
- External interrupt capability

Two of the I/O pins have external interrupts that can be used to wake up the device from sleep modes.

9.2.1 Unused I/O pins

Unused I/O pins should have a defined level and not be left floating. One way to do this is to leave the pin unconnected and configured with pull-up resistor. This is also the state of all pins after reset.

9.2.2 Low I/O Supply Voltage

In applications where the digital I/O power supply voltage pin DVDD is below 2.6 V, the SC bit should be set to 1 in order to obtain output DC characteristics specified in section 5.14. See the ***CCZACC06*** user guide [2] for a description of how to do this.

9.2.3 General Purpose I/O

See the ***CCZACC06*** user guide [2] for a description of how to configure and use the GPIO pins.

The output drive strength is 4 mA on all outputs, except for the two high-drive outputs, GPIO0 and GPIO1, which each have ~20 mA output drive strength.

When used as an input, the general purpose I/O port pins can be configured to have a pull-up, pull-down or tri-state mode of operation. By default, after a reset, inputs are configured as inputs with pull-up. Please note that GPIO0 and GPIO1 do not have pull-up or pull-down capabilities.

In power modes PM2 and PM3 the I/O pins retain the I/O mode and output value (if applicable) that was set when PM2/3 was entered

9.3 ADC

9.3.1 ADC Introduction

The ADC supports up to 12-bit analog-to-digital conversion. The ADC includes an analog multiplexer with up to two individually configurable channels and reference voltage generator.

The main features of the ADC are as follows:

- Selectable decimation rates which also sets the resolution (7 to 12 bits).
- Two individual input channels, single-ended or differential
- Internal voltage reference
- Temperature sensor input
- Battery measurement capability

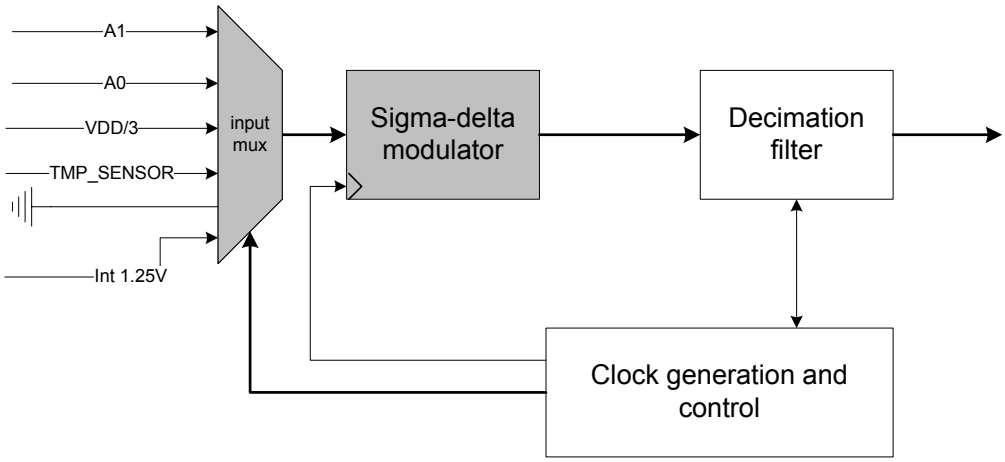


Figure 7: ADC block diagram.

9.3.2 ADC Operation

This section describes the general setup and operation of the ADC.

9.3.2.1 ADC Core

The ADC includes an ADC capable of converting an analog input into a digital representation with up to 12 bits resolution.

The ADC uses a selectable positive reference voltage.

9.3.2.2 ADC Inputs

The signals from input pins A0 and A1 are used as single-ended ADC inputs. The ADC automatically performs a sequence of conversions when the SYS_ADC_READ command is issued.

In addition to the input pins A0-1, the output of an on-chip temperature sensor can be selected as an input to the ADC for temperature measurements.

It is also possible to select a voltage corresponding to AVDD_SOC/3 as an ADC input. This input allows the implementation of e.g. a battery monitor in applications where this feature is required.

9.3.2.3 ADC conversion sequences

The ***CCZACC06*** has two ADC channels that are connected to external pins. Additionally, the ADC can measure the chip voltage and temperature.

The ADC conversions are done channel by channel incrementally.

The two external pin inputs A0 and A1 can be used as single-ended or differential inputs.

In the case where differential inputs are selected, the differential inputs consist of the input pair A0-1. Note that no negative supply can be applied to these pins, nor a supply larger than VDD (unregulated power). It is the difference between the pairs that are converted in differential mode.

In addition to the input pins A0-1, the output of an on-chip temperature sensor can be selected as an input to the ADC for temperature measurements.

It is also possible to select a voltage corresponding to AVDD_SOC/3 as an ADC input. This input allows the implementation of e.g. a battery monitor in applications where this feature is required.

9.3.2.4 ADC Operating Modes

This section describes the operating modes and initialization of conversions.

The ADC uses an internal voltage reference for single-ended conversions.

The decimation rate (and thereby also the resolution and time required to complete a conversion and sample rate) is configurable from 7-12 bits.

9.3.2.5 ADC Conversion Results

The digital conversion result is represented in two's complement form. The result is always positive. This is because the result is the difference between ground and input signal which is always posivitely signed (Vconv=Vinp-Vinn, where Vinn=0V). The maximum value is reached when the input amplitude is equal VREF, the internal voltage reference.

For differential configurations the difference between the pins is converted and this difference can be negatively signed. For 12-bit resolution the digital conversion result is 2047 when the analog input, Vconv, is equal to VREF, and the conversion result is -2048 when the analog input is equal to –VREF.

9.3.2.6 ADC Reference Voltage

The positive reference voltage for analog-to-digital conversions is an internally generated 1.25V voltage.

9.3.2.7 ADC Conversion Timing

The ADC is run on the 32MHz system clock, which is divided by 8 to give a 4 MHz clock.

The time required to perform a conversion depends on the selected decimation rate. When the decimation rate is set to for instance 128, the decimation filter uses exactly 128 of the 4 MHz clock periods to calculate the result. When a conversion is started, the input multiplexer is allowed 16 4 MHz clock cycles to settle in case the channel has been changed since the previous conversion. The 16 clock cycles settling time applies to all decimation rates. Thus in general, the conversion time is given by:

Tconv = (decimation rate + 16) x 0.25 µs.

9.4 Random Number Generator

9.4.1 Introduction

The random number generator has the following features.

- Generate pseudo-random bytes which can be read by the external microprocessor.

The random number generator is a 16-bit Linear Feedback Shift Register (LFSR) with polynomial $X^{16} + X^{15} + X^{2} + 1$ (i.e. CRC16). It uses different levels of unrolling depending on the operation it performs. The basic version (no unrolling) is shown in Figure 8.

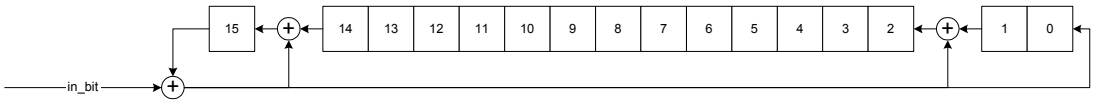


Figure 8: Basic structure of the Random Number Generator

9.4.2 Semi random sequence generation

The operation is to clock the LFSR once (13x unrolling) each time the external microprocessor reads the random value. This leads to the availability of a fresh pseudo-random byte from the LSB end of the LFSR.

9.5 USART

The USART is a serial communications interface that can be operated in either asynchronous UART mode or in synchronous SPI mode.

9.5.1 UART mode

For asynchronous serial interfaces, the UART mode is provided. In the UART mode the interface uses a two-wire or four-wire interface consisting of the pins RXD, TXD and optionally RTS and CTS. The UART mode of operation is as follows:

- Baud rate: 115200.
- Hardware (RTS/CTS) flow control.
- 8N1 byte format.
- DCE signal connection.

The UART mode provides full duplex asynchronous transfers, and the synchronization of bits in the receiver does not interfere with the transmit function. A UART byte transfer consists of a start bit, eight data bits, a parity bit, and one stop bit.

9.5.2 SPI Mode

This section describes the SPI mode of operation for synchronous communication. In SPI mode, the USART communicates with an external system through a 3-wire or 4-wire interface. The interface consists of the pins SI, SO, SCK and SS_N. The SPI mode is as follows:

- SPI slave.
- Clock speed up to 4 MHz.
- Clock polarity 0 and clock phase 0 on ***CCZACC06***.
- Bit order: MSB first.

9.5.2.1 SPI Slave Operation

An SPI byte transfer in slave mode is controlled by the external system. The data on the SI input is shifted into the receive register controlled by the serial clock SCK which is an input in slave mode. At the same time the byte in the transmit register is shifted out onto the SO output.

9.5.3 SSN Slave Select Pin

When the USART is operating in SPI mode, configured as an SPI slave, a 4-wire interface is used with the Slave Select (SSN) pin as an input to the SPI (edge controlled). At falling edge of SSN the SPI slave is active and receives data on the SI input and outputs data on the SO output. At rising edge of SSN, the SPI slave is inactive and will not receive data. Note that the SO output is not tri-stated after rising edge on SSn. This could be achieved using an external buffer. Also note that release of SSn (rising edge) must be aligned to end of byte recived or sent. If released in a byte the next received byte will not be received properly as information about previous byte is present in SPI system.

10 Radio

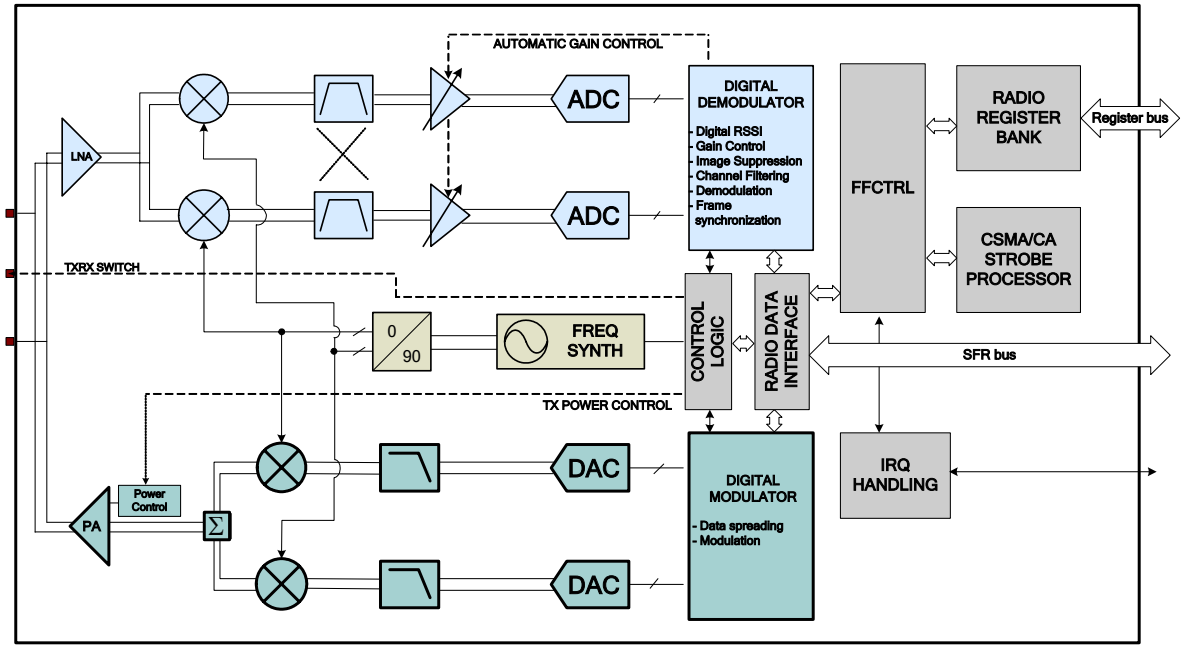


Figure 9: CCZACC06 Radio Module

A simplified block diagram of the IEEE 802.15.4 compliant radio inside ***CCZACC06*** is shown in Figure 9. The radio core is based on the industry leading ***CC2420*** RF transceiver.

CCZACC06 features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF (2 MHz), the complex I/Q signal is filtered and amplified, and then digitized by the RF receiver ADCs.

The ***CCZACC06*** transmitter is based on direct up-conversion. The preamble and start of frame delimiter are generated in hardware. Each symbol (4 bits) is spread using the IEEE 802.15.4 spreading sequence to 32 chips and output to the digital-to-analog converters (DACs).

An analog low pass filter passes the signal to the quadrature (I and Q) up-conversion mixers.

The RF signal is amplified in the power amplifier (PA) and fed to the antenna.

The internal T/R switch circuitry makes the antenna interface and matching easy. The RF connection is differential. A balun may be used for single-ended antennas. The biasing of the PA and LNA is done by connecting TXRX_SWITCH to RF_P and RF_N through an external DC path.

The frequency synthesizer includes a completely on-chip LC VCO and a 90 degrees phase splitter for generating the I and Q LO signals to the down-conversion mixers in receive mode and up-conversion mixers in transmit mode. The VCO operates in the frequency range 4800 – 4966 MHz, and the frequency is divided by two when split into I and Q signals.

An on-chip voltage regulator delivers the regulated 1.8 V supply voltage.

10.1 IEEE 802.15.4 Modulation Format

This section is meant as an introduction to the 2.4 GHz direct sequence spread spectrum (DSSS) RF modulation format defined in IEEE 802.15.4. For a complete description, please refer to [1].

The modulation and spreading functions are illustrated at block level in Figure 10 [1]. Each byte is divided into two symbols, 4 bits each. The least significant symbol is transmitted first. For multi-byte fields, the least significant byte is transmitted first.

Each symbol is mapped to one out of 16 pseudo-random sequences, 32 chips each. The symbol to chip mapping is shown in Table 20. The chip sequence is then transmitted at 2 MChips/s, with the least significant chip (C_0) transmitted first for each symbol.

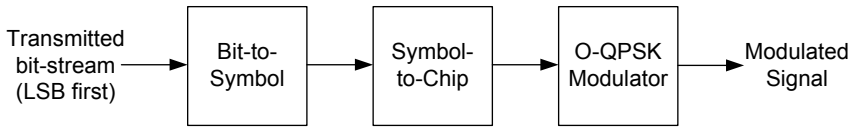


Figure 10: Modulation and spreading functions [1]

The modulation format is Offset – Quadrature Phase Shift Keying (O-QPSK) with half-sine chip shaping. This is equivalent to MSK modulation. Each chip is shaped as a half-sine, transmitted alternately in the I and Q channels with one half chip period offset. This is illustrated for the zero-symbol in Figure 11.

Table 20: IEEE 802.15.4 symbol-to-chip mapping [1]

Symbol	Chip sequence (C_0, C_1, C_2, … , C_{31})
0	1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0
1	1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0
2	0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0
3	0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1
4	0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1
5	0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0
6	1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1
7	1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1
8	1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1
9	1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1
10	0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1
11	0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0
12	0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0
13	0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1
14	1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0
15	1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0

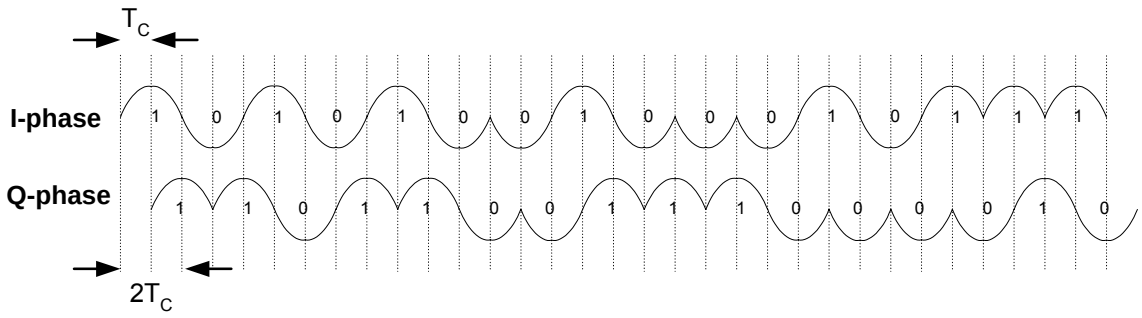


Figure 11: I / Q Phases when transmitting a zero-symbol chip sequence, T_C = 0.5 µs

10.2 Demodulator, Symbol Synchronizer and Data Decision

The block diagram for the ***CCZACC06*** demodulator is shown in Figure 12. Channel filtering and frequency offset compensation is performed digitally. The signal level in the channel is estimated to generate the RSSI level. Data filtering is also included for enhanced performance.

With the ±40 ppm frequency accuracy requirement from [1], a compliant receiver must be able to compensate for up to 80 ppm or 200 kHz. The ***CCZACC06*** demodulator tolerates up to 300 kHz offset without significant degradation of the receiver performance.

Soft decision is used at the chip level, i.e. the demodulator does not make a decision for each chip, only for each received symbol. De-spreading is performed using over-sampling symbol correlators. Symbol synchronization is achieved by a continuous start of frame delimiter (SFD) search.

The ***CCZACC06*** demodulator also handles symbol rate errors in excess of 120 ppm without performance degradation. Resynchronization is performed continuously to adjust for error in the incoming symbol rate.

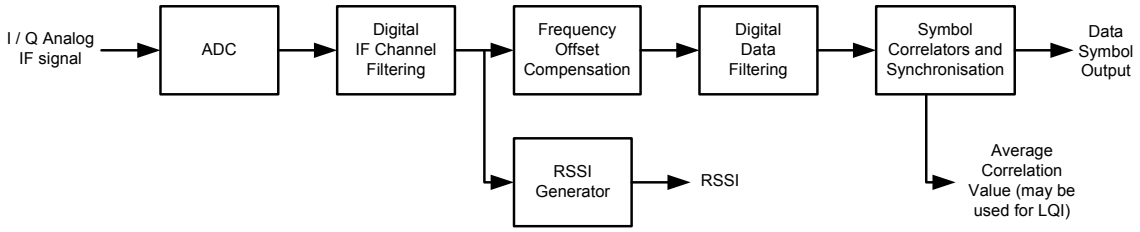


Figure 12: Demodulator Simplified Block Diagram

10.3 Frame Format

CCZACC06 has hardware support for parts of the IEEE 802.15.4 frame format. This section gives a brief summary to the IEEE 802.15.4 frame format, and describes how ***CCZACC06*** is set up to comply with this.

Figure 13 [1] shows a schematic view of the IEEE 802.15.4 frame format. Similar figures describing specific frame formats (data frames, beacon frames, acknowledgment frames and MAC command frames) are included in [1].

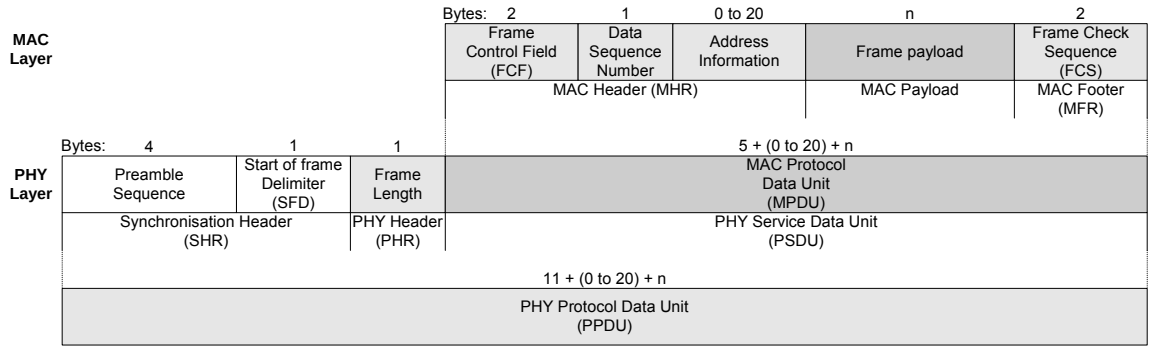


Figure 13: Schematic view of the IEEE 802.15.4 Frame Format [1]

10.4 Synchronization header

The synchronization header (SHR) consists of the preamble sequence followed by the start of frame delimiter (SFD). In [1], the preamble sequence is defined to be four bytes of 0x00. The SFD is one byte, set to 0xA7.

A synchronization header is always transmitted first in all transmit modes.

In receive mode ***CCZACC06*** uses the preamble sequence for symbol synchronization and frequency offset adjustments. The SFD is used for byte synchronization.

10.5 MAC protocol data unit

The FCF, data sequence number and address information follows the length field as shown in Figure 13. Together with the MAC data payload and Frame Check Sequence, they form the MAC Protocol Data Unit (MPDU).

The format of the FCF is shown in Figure 14. Please refer to [1] for details.

Bits: 0-2	3	4	5	6	7-9	10-11	12-13	14-15
Frame Type	Security Enabled	Frame Pending	Acknowledge request	Intra PAN	Reserved	Destination addressing mode	Reserved	Source addressing mode

Figure 14: Format of the Frame Control Field (FCF) [1]

10.6 Frame check sequence

A 2-byte frame check sequence (FCS) follows the last MAC payload byte as shown in Figure 13. The FCS is calculated over the MPDU, i.e. the length field is not part of the FCS.

The FCS polynomial is [1]:

$$x^{16} + x^{12} + x^5 + 1$$

The ***CCZACC06*** hardware implementation is shown in Figure 15. Please refer to [1] for further details.

In transmit mode the FCS is appended at the correct position defined by the length field.

The most significant bit in the last byte of each frame is set high if the CRC of the received frame is correct and low otherwise.

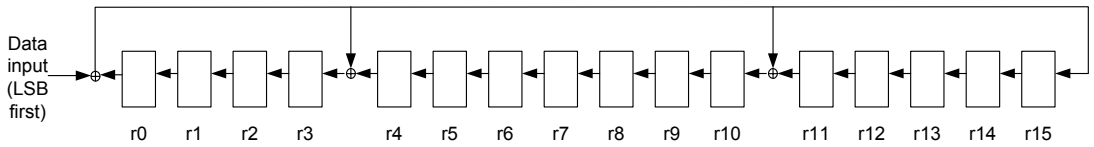


Figure 15: *CCZACC06* Frame Check Sequence (FCS) hardware implementation [1]

10.7 Linear IF and AGC Settings

CCZACC06 is based on a linear IF chain where the signal amplification is done in an analog VGA (variable gain amplifier). The gain of the VGA is digitally controlled.

The AGC (Automatic Gain Control) loop ensures that the ADC operates inside its dynamic range by using an analog/digital feedback loop.

10.8 Clear Channel Assessment

The clear channel assessment signal is based on the measured RSSI value and a programmable threshold. The clear channel assessment function is used to implement the CSMA-CA functionality specified in [1]. CCA is valid when the receiver has been enabled for at least 8 symbol periods.

10.9 VCO and PLL Self-Calibration

10.9.1 VCO

The VCO is completely integrated and operates at 4800 – 4966 MHz. The VCO frequency is divided by 2 to generate frequencies in the desired band (2400-2483.5 MHz).

10.9.2 PLL self-calibration

The VCO's characteristics will vary with temperature, changes in supply voltages, and the desired operating frequency.

In order to ensure reliable operation the VCO's bias current and tuning range are automatically calibrated every time the RX mode or TX mode is enabled.

10.10 Input / Output Matching

The RF input / output is differential (RF_N and RF_P). In addition there is supply switch output pin (TXRX_SWITCH) that must have an external DC path to RF_N and RF_P.

In RX mode the TXRX_SWITCH pin is at ground and will bias the LNA. In TX mode the TXRX_SWITCH pin is at supply rail voltage and will properly bias the internal PA.

The RF output and DC bias can be done using different topologies. Some are shown in Figure 5 on page 21.

Component values are given in Table 19 on page 22. If a differential antenna is implemented, no balun is required.

If a single ended output is required (for a single ended connector or a single ended antenna), a balun should be used for optimum performance.

10.11 System Considerations and Guidelines

10.11.1 SRD regulations

International regulations and national laws regulate the use of radio receivers and transmitters. SRDs (Short Range Devices) for license free operation are allowed to operate in the 2.4 GHz band worldwide. The most important regulations are ETSI EN 300 328 and EN 300 440 (Europe), FCC CFR-47 part 15.247 and 15.249 (USA), and ARIB STD-T66 (Japan).

10.11.2 Frequency hopping and multi-channel systems

The 2.4 GHz band is shared by many systems both in industrial, office and home environments. ***CCZACC06*** uses direct sequence spread spectrum (DSSS) as defined by [1] to spread the output power, thereby making the communication link more robust even in a noisy environment.

10.11.3 Crystal accuracy and drift

A crystal accuracy of ±40 ppm is required for compliance with IEEE 802.15.4 [1]. This accuracy must also take ageing and temperature drift into consideration.

A crystal with low temperature drift and low aging could be used without further compensation. A trimmer capacitor in the crystal oscillator circuit (in parallel with C191 in Figure 5) could be used to set the initial frequency accurately.

For non-IEEE 802.15.4 systems, the robust demodulator in ***CCZACC06*** allows up to 140 ppm total frequency offset between the transmitter and receiver. This could e.g. relax the accuracy requirement to 60 ppm for each of the devices.

Optionally in a star network topology, the full-function device (FFD) could be equipped with a more accurate crystal thereby relaxing the requirement on the reduced-function device (RFD). This can make sense in systems where the reduced-function devices ship in higher volumes than the full-function devices.

10.11.4 Communication robustness

CCZACC06 provides very good adjacent, alternate and co channel rejection, image frequency suppression and blocking properties. The ***CCZACC06*** performance is significantly better than the requirements imposed by [1]. These are highly important parameters for reliable operation in the 2.4 GHz band, since an increasing number of devices/systems are using this license free frequency band.

10.11.5 Communication security

The hardware encryption and authentication operations in ***CCZACC06*** enable secure communication, which is required for many applications. Security operations require a lot of data processing, which is costly in an 8-bit microcontroller system. The hardware support within ***CCZACC06*** enables a high level of security with minimum CPU processing requirements.

10.11.6 Low cost systems

As the ***CCZACC06*** provides 250 kbps multi-channel performance without any external filters, a very low cost system can be made (e.g. two layer PCB with single-sided component mounting). A differential antenna will eliminate the need for a balun, and the DC biasing can be achieved in the antenna topology.

10.11.7 Battery operated systems

In low power applications, the ***CCZACC06*** should be placed in the low-power modes PM2 or PM3 when not active. Ultra low power consumption may be achieved since the voltage regulators are turned off.

10.12 PCB Layout Recommendation

In the Texas Instruments reference design, the top layer is used for signal routing, and the open areas are filled with metallization connected to ground using several vias. The area under the chip is used for grounding and must be well connected to the ground plane with several vias.

The ground pins should be connected to ground as close as possible to the package pin using individual vias. The de-coupling capacitors should also be placed as close as possible to the supply pins and connected to the ground plane by separate vias. Supply power filtering is very important.

The external components should be as small as possible (0402 is recommended) and surface mount devices must be used.

If using any external high-speed digital devices, caution should be used when placing these in order to avoid interference with the RF circuitry.

It is strongly advised that this reference layout is followed very closely in order to obtain the best performance.

The schematic, BOM and layout Gerber files for the reference designs are all available from the TI website.

10.13 Antenna Considerations

CCZACC06 can be used together with various types of antennas. A differential antenna like a dipole would be the easiest to interface not needing a balun (balanced to un-balanced transformation network).

The length of the λ/2-dipole antenna is given by:

$$L = 14250 / f$$

where f is in MHz, giving the length in cm. An antenna for 2450 MHz should be 5.8 cm. Each arm is therefore 2.9 cm.

Other commonly used antennas for short-range communication are monopole, helical and loop antennas. The single-ended monopole and helical would require a balun network between the differential output and the antenna.

Monopole antennas are resonant antennas with a length corresponding to one quarter of the electrical wavelength (λ/4). They are very easy to design and can be implemented simply as a “piece of wire” or even integrated into the PCB.

The length of the λ/4-monopole antenna is given by:

$$L = 7125 / f$$

where f is in MHz, giving the length in cm. An antenna for 2450 MHz should be 2.9 cm.

Non-resonant monopole antennas shorter than λ/4 can also be used, but at the expense of range. In size and cost critical applications such an antenna may very well be integrated into the PCB.

Enclosing the antenna in high dielectric constant material reduces the overall size of the antenna. Many vendors offer such antennas intended for PCB mounting.

Helical antennas can be thought of as a combination of a monopole and a loop antenna. They are a good compromise in size critical applications. Helical antennas tend to be more difficult to optimize than the simple monopole.

Loop antennas are easy to integrate into the PCB, but are less effective due to difficult impedance matching because of their very low radiation resistance.

For low power applications the differential antenna is recommended giving the best range and because of its simplicity.

The antenna should be connected as close as possible to the IC. If the antenna is located away from the RF pins the antenna should be matched to the feeding transmission line (50Ω).

11 Voltage Regulators

The ***CCZACC06*** includes two low drop-out voltage regulators. These are used to provide a 1.8 V power supply to the ***CCZACC06*** analog and digital power supplies.

Note: It is recommended that the voltage regulators are not used to provide power to external circuits. This is because of limited power sourcing capability and due to noise considerations. External circuitry can be powered if they can be used when internal power consumption is low and can be set I PD mode when internal power consumption I high.

The analog voltage regulator input pin AVDD_RREG is to be connected to the unregulated 2.0 to 3.6 V power supply. The regulated 1.8 V voltage output to the analog parts, is available on the RREG_OUT pin. The digital regulator input pin AVDD_DREG is also to be connected to the unregulated 2.0 to 3.6 V power supply. The output of the digital regulator is connected internally within the ***CCZACC06*** to the digital power supply.

The voltage regulators require external components as described in section 8 on page 20.

11.1 Voltage Regulators Power-on

When the analog voltage regulator is powered-on before use of the radio, there will be a delay before the regulator is enabled.

The digital voltage regulator is disabled when the ***CCZACC06*** is placed in low power modes to reduce power consumption.

12 Package Description (QLP 48)

All dimensions are in millimeters, angles in degrees. NOTE: The ***CCZACC06*** is available in RoHS lead-free package only. Compliant with JEDEC MS-020.

Table 21: Package dimensions

Quad Leadless Package (QLP)										
		D	D1	E	E1	e	b	L	D2	E2
QLP 48	Min	6.9	6.65	6.9	6.65		0.18	0.3	5.05	5.05
		7.0	6.75	7.0	6.75	0.5		0.4	5.10	5.10
	Max	7.1	6.85	7.1	6.85		0.30	0.5	5.15	5.15
The overall package height is 0.85 +/- 0.05 All dimensions in mm										

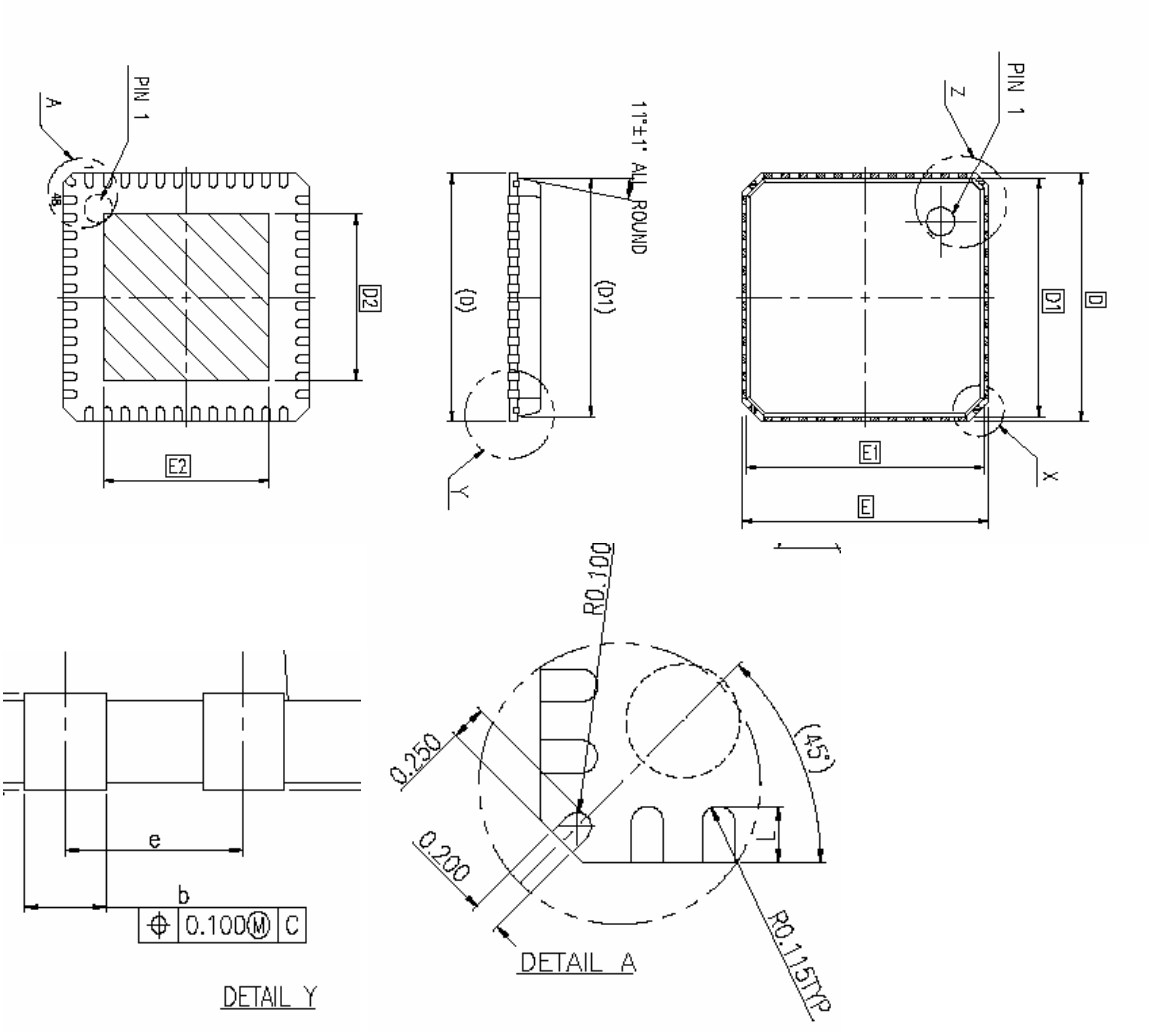


Figure 16: Package dimensions drawing

12.1 Recommended PCB layout for package (QLP 48)

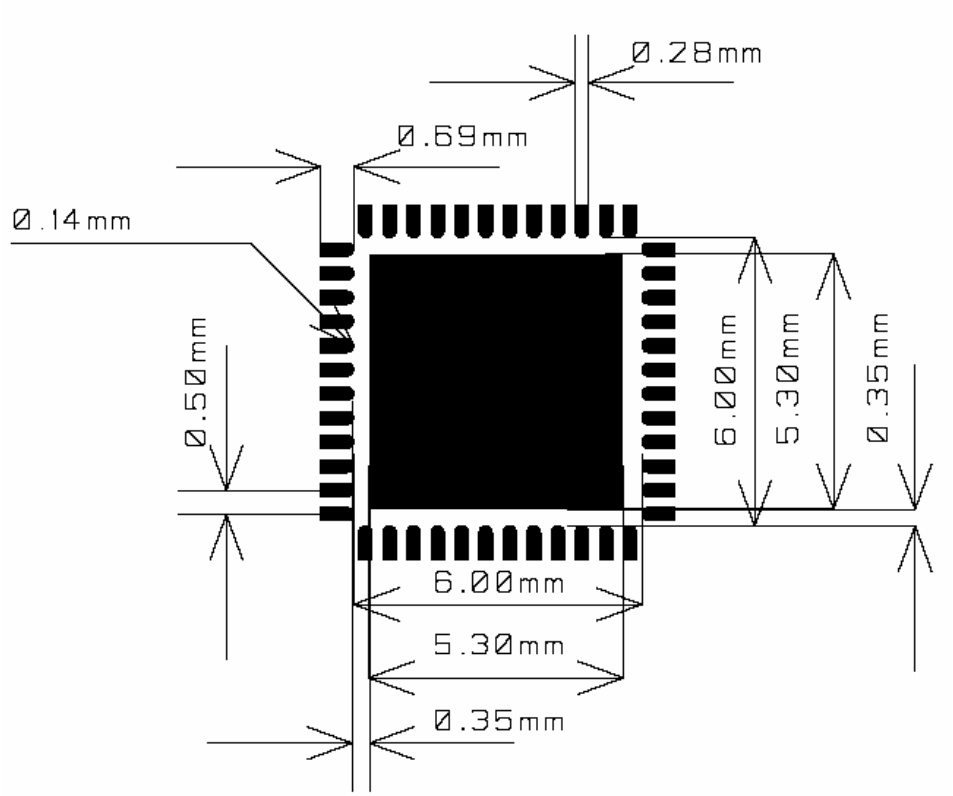


Figure 17: Recommended PCB layout for QLP 48 package

Note: The figure is an illustration only and not to scale. There are nine 14 mil diameter via holes distributed symmetrically in the ground pad under the package. See also the ***CCZACC06*** EM reference design

12.2 Package thermal properties

Table 22: Thermal properties of QLP 48 package

Thermal resistance	
Air velocity [m/s]	0
Rth,j-a [K/W]	25.6

12.3 Soldering information

The recommendations for lead-free solder reflow in IPC/JEDEC J-STD-020C should be followed.

12.4 Tray specification

Table 23: Tray specification

Tray Specification				
Package	Tray Width	Tray Height	Tray Length	Units per Tray
QLP 48	135.9mm ± 0.25mm	7.62mm ± 0.13mm	322.6mm ± 0.25mm	260

12.5 Carrier tape and reel specification

Carrier tape and reel is in accordance with EIA Specification 481.

Table 24: Carrier tape and reel specification

Tape and Reel Specification					
Package	Tape Width	Component Pitch	Hole Pitch	Reel Diameter	Units per Reel
QLP 48	16mm	12mm	4mm	13 inches	2500

13 Ordering Information

Table 25: Ordering Information

Ordering part number	Description	MOQ
CCZACC06A1RTC	CCZACC06, QLP48 package, RoHS compliant Pb-free assembly, trays with 260 pcs per tray, ZigBee 2006 Network Processor.	260
CCZACC06A1RTCR	CCZACC06, QLP48 package, RoHS compliant Pb-free assembly, T&R with 2500 pcs per reel, ZigBee 2006 Network Processor.	2,500
eZ430-RFZACC06	CCZACC06 Demonstration Board based on the eZ430-RF platform	1

MOQ = Minimum Order Quantity T&R = tape and reel

14 General Information

14.1 Document History

Table 26: Document History

Revision	Date	Description/Changes
1.0	2008-03-02	First data sheet for released product.

15 Address Information

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16 TI Worldwide Technical Support

Internet

TI Semiconductor Product Information Center Home Page: support.ti.com
TI Semiconductor KnowledgeBase Home Page: support.ti.com/sc/knowledgebase

Product Information Centers

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Fax: +1(972) 927-6377
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	Domestic	www.tij.co.jp/pic

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	Philippines	1-800-765-7404
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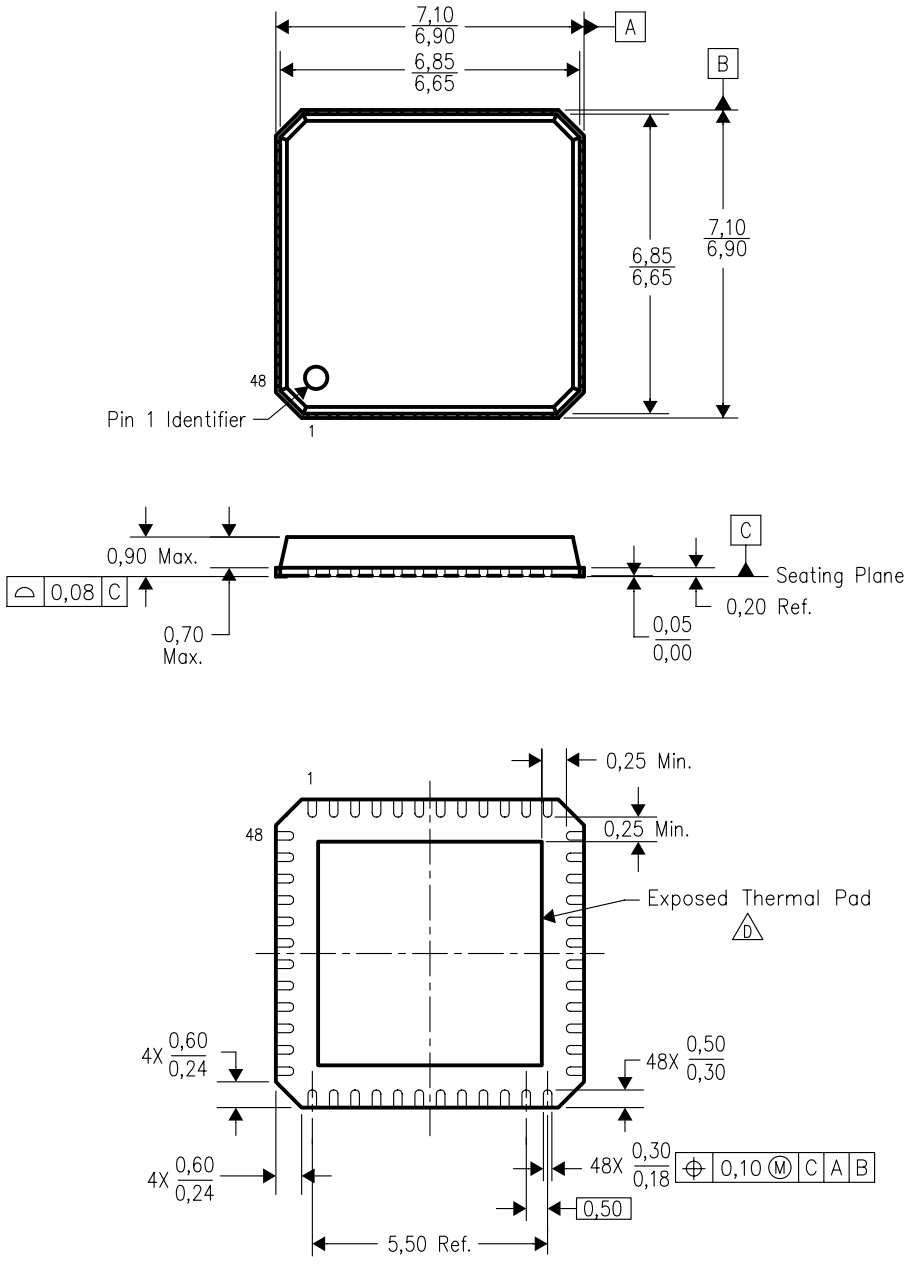
Internet		support.ti.com/sc/pic/asia.htm

RTC (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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