

52Mbps Precision Delay RS485 Quad Line Receivers

FEATURES

- **Precision Propagation Delay: $18.5\text{ns} \pm 3.5\text{ns}$ Over 0°C to 70°C Temperature Range**
- **High Data Rate: 52Mbps**
- **Low t_{PLH}/t_{PHL} Skew: 500ps Typ**
- **Low Channel-to-Channel Skew: 500ps Typ**
- **Guaranteed Fail-Safe Operation over the Entire Common Mode Range**
- **-7V to 12V RS485 Input Common Mode Range**
- **Input Resistance $\geq 22\text{k}$, Even When Unpowered**
- **Hot Swap™ Capable**
- **High Common Mode Rejection to 26MHz**
- **Short-Circuit Protection: 10mA Typ Output Current for an Indefinite Short**
- **Three-State Output Capability**
- **Will Not Oscillate with Slow Moving Input Signals**
- **Single 5V Supply**
- **Pin Compatible with LTC488, LTC489**

APPLICATIONS

- High Speed RS485/RS422 Receivers
- STS-1/OC-1 Data Receivers
- PECL Line Receivers
- Level Translators
- Fast-20/Fast-40 SCSI Receiver

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 Hot Swap is a trademark of Linear Technology Corporation.

DESCRIPTION

The LTC®1518/LTC1519 are high speed, precision delay differential quad bus/line receivers that can operate at data rates as high as 52Mbps. They are pin compatible with the LTC488/LTC489 RS485 line receivers and operate over the entire -7V to 12V common mode range. A unique architecture provides very stable propagation delays and low skew over wide input common mode, input overdrive and ambient temperature ranges. Propagation delay is $18.5\text{ns} \pm 3.5\text{ns}$ over the commercial temperature range. Typical t_{PLH}/t_{PHL} and channel-to-channel skew is 500ps.

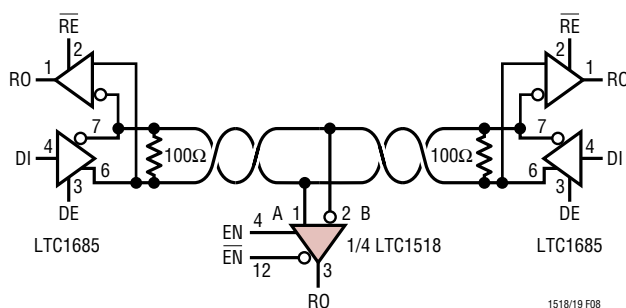
Each receiver translates differential input levels ($|V_{ID}| \geq 300\text{mV}$) into valid CMOS and TTL output levels. Its high input resistance ($\geq 22\text{k}$) allows many receivers to be connected to the same driver. The receiver outputs go into a high impedance state when disabled.

The receivers have a fail-safe feature that guarantees a high output state when the inputs are shorted or left floating. Other protection features include thermal shutdown and a controlled maximum short-circuit current (50mA Max). Input resistance remains $\geq 22\text{k}$ when the device is unpowered or disabled, thus allowing hot swapping without loading the data lines.

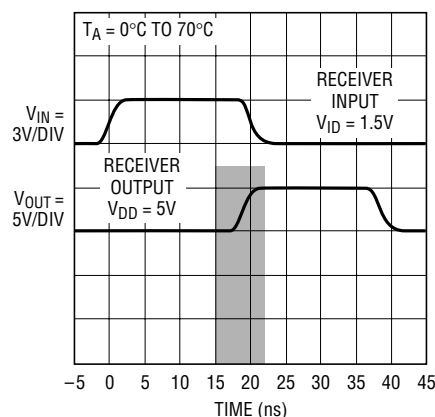
The LTC1518/LTC1519 operate from a single 5V supply and draw 12mA of supply current.

TYPICAL APPLICATION

52Mbps Data Communication over Twisted Pair



Propagation Delay Guaranteed to Fail
Within Shaded Area ($\pm 3.5\text{ns}$)



1518/19 TA02

LTC1518/LTC1519

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 10V
 Digital Input Currents –100mA to 100mA
 Digital Input Voltages –0.5V to 10V
 Receiver Input Voltages $\pm 14V$
 Receiver Output Voltages –0.5V to $V_{DD} + 0.5V$
 Receiver Input Differential 10V

Short-Circuit Duration Indefinite
 Operating Temperature Range
 LTC1518C/LTC1519C 0°C to 70°C
 LTC1518I/LTC1519I –40°C to 85°C
 Storage Temperature Range –65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

	ORDER PART NUMBER LTC1518CS LTC1518IS		ORDER PART NUMBER LTC1519CS LTC1519IS
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Consult factory for Military grade parts.

DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{DD} = 5V \pm 5\%$ (Notes 2, 3) per receiver, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V _{CM}	Input Common Mode Voltage	A, B Inputs	●	−7		12	V
V _{IH}	Input High Voltage	EN, $\overline{\text{EN}}$, EN12, EN34	●	2			V
V _{IL}	Input Low Voltage	EN, $\overline{\text{EN}}$, EN12, EN34	●			0.8	V
I _{IN1}	Input Current	EN, $\overline{\text{EN}}$, EN12, EN34	●	−1		1	μA
I _{IN2}	Input Current (A, B)	V _A , V _B = 12V V _A , V _B = −7V	● ●			500	μA μA
R _{IN}	Input Resistance	−7V ≤ V _{CM} ≤ 12V (Figure 5)	●	22			kΩ
C _{IN}	Input Capacitance	(Note 4)			3		pF
V _{OC}	Open-Circuit Input Voltage	V _{DD} = 5V (Note 4) (Figure 5)	●	3.2	3.3	3.4	V
V _{ID(MIN)}	Differential Input Threshold Voltage	−7V ≤ V _{CM} ≤ 12V	●	−0.3		0.3	V
dV _{ID}	Input Hysteresis	V _{CM} = 2.5V			25		mV
V _{OH}	Output High Voltage	I _{OUT} = −4mA, V _{ID} = 0.3V, V _{DD} = 5V	●	4.6			V
V _{OL}	Output Low Voltage	I _{OUT} = 4mA, V _{ID} = −0.3V, V _{DD} = 5V	●			0.4	V
I _{OZR}	Three-State Output Current	0V < V _{OUT} < 5V	●	−10		10	μA
I _{DD}	Total Supply Current All 4 Receivers	V _{ID} > 0.3V, No Load, Device Enabled	●		12	20	mA
I _{OSR}	Short-Circuit Current	V _{OUT} = 0V, V _{OUT} = 5V (Note 7)	●	−50		50	mA

DC ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{DD} = 5V \pm 5\%$ (Notes 2, 3) per receiver, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Max V_{ID} for Fail-Safe Detection	$-7V \leq V_{CM} \leq 12V$		25		mV
	Min Time to Detect Fault Condition			2		μs
CMRR	Common Mode Rejection Ratio	$V_{CM} = 2.5V$, $f = 26\text{MHz}$ (Note 4)		45		dB

SWITCHING TIME CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_{DD} = 5V \pm 5\%$ (Notes 2, 3) $V_{ID} = 1.5V$, $V_{CM} = 2.5V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH} , t_{PHL}	Input-to-Output Propagation Delay	$C_L = 15\text{pF}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Figure 1) ● $C_L = 15\text{pF}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ (Figure 1) ●	15 12	18.5	22 25	ns ns
t_r , t_f	Rise/Fall Times	$C_L = 15\text{pF}$		2.5		ns
t_{SKD}	$ t_{PLH} - t_{PHL} $ Skew	$C_L = 15\text{pF}$, Same Receiver (Note 5)		500		ps
t_{ZL}	Enable to Output Low	$C_L = 15\text{pF}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Figure 2) ● $C_L = 15\text{pF}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ (Figure 2)		10 15	35	ns ns
t_{ZH}	Enable to Output High	$C_L = 15\text{pF}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Figure 2) ● $C_L = 15\text{pF}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ (Figure 2)		10 15	35	ns ns
t_{LZ}	Disable from Output Low	$C_L = 15\text{pF}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Figure 2) ● $C_L = 15\text{pF}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ (Figure 2)		20 25	35	ns ns
t_{HZ}	Disable from Output High	$C_L = 15\text{pF}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Figure 2) ● $C_L = 15\text{pF}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ (Figure 2)		20 25	35	ns ns
t_{CH-CH}	Channel-to-Channel Skew	$C_L = 15\text{pF}$ (Figure 3, Note 6)		500		ps
$t_{PKG-PKG}$	Package-to-Package Skew	$C_L = 15\text{pF}$, Same Temperature (Figure 4, Note 4)		1.5		ns
t_r , t_f Input	Maximum Input Rise or Fall Time	(Note 4) ●			2000	ns
	Minimum Input Pulse Width	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Note 4) ● $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ (Note 4) ●		12 16	19.2 25	ns ns
$f_{IN(MAX)}$	Maximum Input Frequency	Square Wave, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Note 4) ● Square Wave, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ (Note 4) ●	26 20	40 30		MHz MHz
	Maximum Data Rate	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ (Note 4) ● $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ (Note 4) ●	52 40	80 65		Mbps Mbps
C_L	Load Capacitance	(Note 4)			500	pF

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into the device pins are positive; all currents out of the device pins are negative.

Note 3: All typicals are given for $V_{DD} = 5V$, $T_A = 25^\circ\text{C}$.

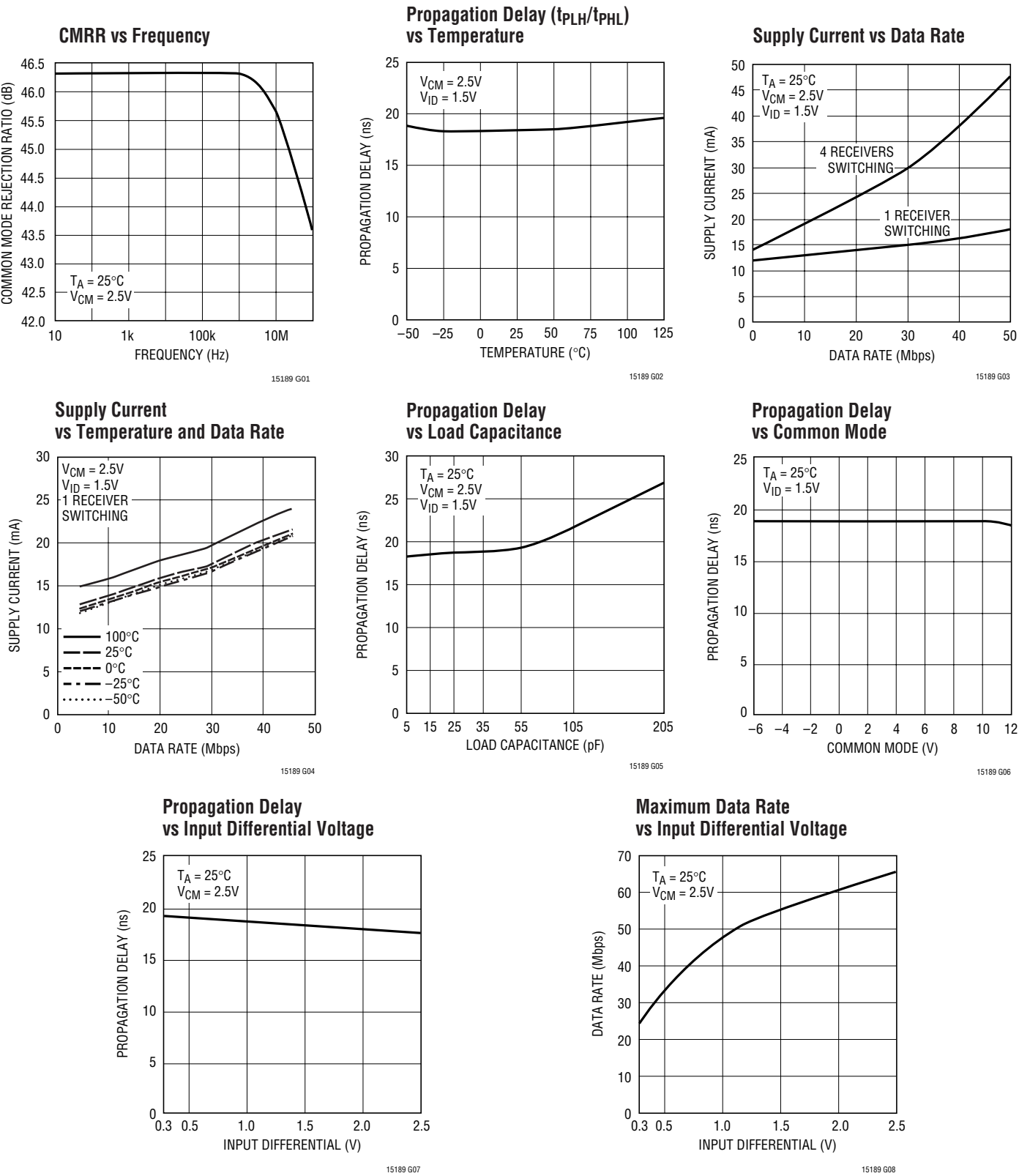
Note 4: Guaranteed by design, but not tested.

Note 5: Worst-case $|t_{PLH} - t_{PHL}|$ skew for a single receiver in a package over the full operating temperature range.

Note 6: Maximum difference between any two t_{PLH} or t_{PHL} transitions in a single package over the full operating temperature range.

Note 7: Short-circuit current does not represent output drive capability. When the output detects a short-circuit condition, output drive current is significantly reduced until the short is removed.

TYPICAL PERFORMANCE CHARACTERISTICS



PIN FUNCTIONS

LTC1518

B1 (Pin 1): Receiver 1 Inverting Input.

A1 (Pin 2): Receiver 1 Noninverting Input.

OUT 1 (Pin 3): Receiver 1 Output.

EN (Pin 4): A high enables all outputs; a low on Pin 4 and a high on Pin 12 will put all outputs into a high impedance state. Do not float.

OUT 2 (Pin 5): Receiver 2 Output.

A2 (Pin 6): Receiver 2 Noninverting Input.

B2 (Pin 7): Receiver 2 Inverting Input.

GND (Pin 8): Ground Pin. A ground plane is recommended for all LTC1518 applications.

B3 (Pin 9): Receiver 3 Inverting Input.

A3 (Pin 10): Receiver 3 Noninverting Input.

OUT 3 (Pin 11): Receiver 3 Output.

EN (Pin 12): A low enables all outputs; a low on Pin 4 and a high on Pin 12 will put all outputs into a high impedance state. Do not float.

OUT 4 (Pin 13): Receiver 4 Output.

A4 (Pin 14): Receiver 4 Noninverting Input.

B4 (Pin 15): Receiver 4 Inverting Input.

V_{DD} (Pin 16): Power Supply Input. This pin should be decoupled with a 0.1μF ceramic capacitor as close as possible to the pin. Recommended: $V_{DD} = 5V \pm 5\%$.

LTC1519

B1 (Pin 1): Receiver 1 Inverting Input.

A1 (Pin 2): Receiver 1 Noninverting Input.

OUT 1 (Pin 3): Receiver 1 Output.

EN12 (Pin 4): A high enables receivers 1 and 2; a low will put the outputs of receivers 1 and 2 into a high impedance state. Do not float.

OUT 2 (Pin 5): Receiver 2 Output.

A2 (Pin 6): Receiver 2 Noninverting Input.

B2 (Pin 7): Receiver 2 Inverting Input.

GND (Pin 8): Ground Pin. A ground plane is recommended for all LTC1519 applications.

B3 (Pin 9): Receiver 3 Inverting Input.

A3 (Pin 10): Receiver 3 Noninverting Input.

OUT 3 (Pin 11): Receiver 3 Output.

EN34 (Pin 12): A high enables receivers 3 and 4; a low will put the outputs of receivers 3 and 4 into a high impedance state. Do not float.

OUT 4 (Pin 13): Receiver 4 Output.

A4 (Pin 14): Receiver 4 Noninverting Input.

B4 (Pin 15): Receiver 4 Inverting Input.

V_{DD} (Pin 16): Power Supply Input. This pin should be decoupled with a 0.1μF ceramic capacitor as close as possible to the pin. Recommended: $V_{DD} = 5V \pm 5\%$.

SWITCHING TIME WAVEFORMS $t_r = t_f \leq 3\text{ns}$ for all input and enable signals.

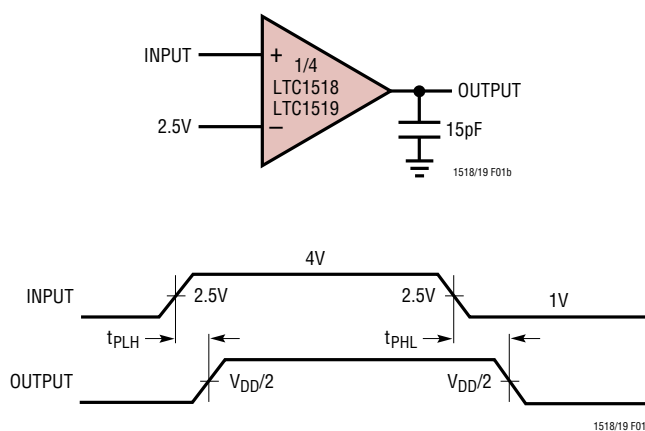


Figure 1. Propagation Delay Test Circuit and Waveforms

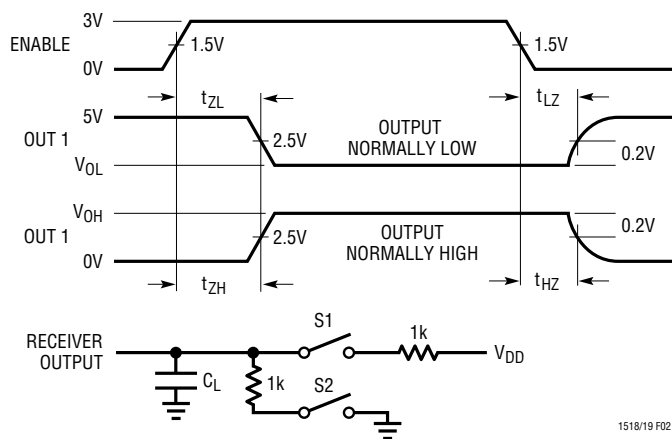


Figure 2. Receiver Enable and Disable Timing Test Circuit and Waveforms

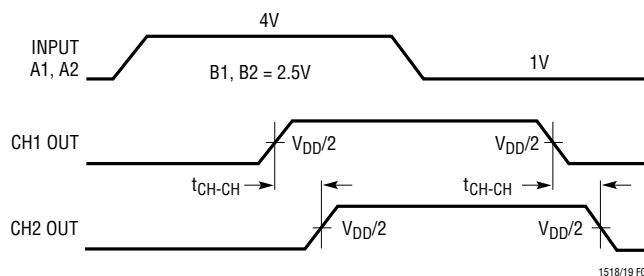


Figure 3. Any Channel to Any Channel Skew, Same Package

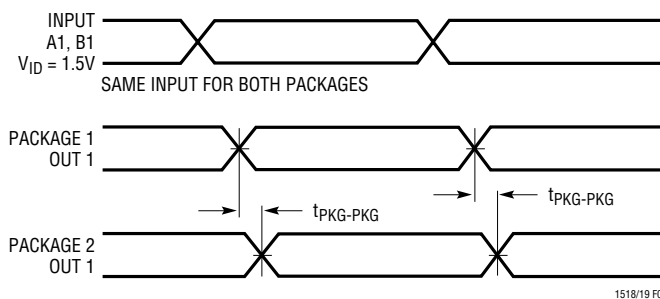


Figure 4. Package-to-Package Propagation Delay Skew

EQUIVALENT INPUT NETWORKS

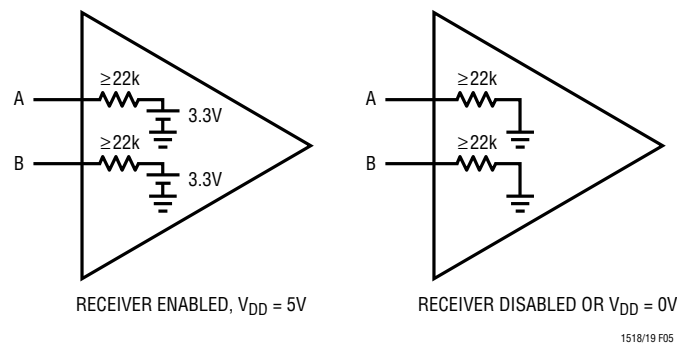


Figure 5. Input Thevenin Equivalent

APPLICATIONS INFORMATION

Theory of Operation

Unlike typical line receivers whose propagation delay can vary by as much as 500% from package to package and show significant temperature drift, the LTC1518/LTC1519 employ a novel architecture that produces a tightly controlled and temperature compensated propagation delay. The differential timing skew is also minimized between rising and falling output edges, and the propagation delays of any two receivers within a package are very tightly matched.

The precision timing features of the LTC1518/LTC1519 reduce overall system timing constraints by providing a narrow $\pm 3.5\text{ns}$ window during which valid data appears at the receiver output. This output timing window applies to all receivers in all packages over the commercial operating temperature range, thereby making the LTC1518/LTC1519 well suited for high speed data transmission.

In clocked data systems, the low skew minimizes duty cycle distortion of the clock signal. The LTC1518/LTC1519 can propagate signals at frequencies of 26MHz (52Mbps) with less than 5% duty cycle distortion. When a clock signal is used to retime parallel data, the maximum recommended data transmission rate is 25Mbps to avoid timing errors due to clock distortion.

Thermal shutdown and short-circuit protection prevent latchup damage to the LTC1518/LTC1519 during fault conditions.

Fail-Safe Features

The LTC1518/LTC1519 have a fail-safe feature that guarantees the output to be in a logic HIGH state when the inputs are either shorted or left open (note that when inputs are left open, any external large leakage current might override the fail-safe). The fail-safe feature detects shorted inputs over the entire common mode range. When a fault is detected, the output will typically go high in $2\mu\text{s}$.

When some of the receivers within a package are not used, the open fail-safe feature will allow the user to let the receiver inputs float and maintain a high logic state at the output. Without the open fail-safe feature, any noise at the input would cause unwanted glitches at the output. When the inputs are left "open," one must make sure that there are no sources of leakage current connected to one or both of the inputs. This can happen if the device is being driven single-endedly and both the signal and the DC bias are disconnected. If the capacitor used to bypass the DC bias is left connected to the input of the device and is leaky ($>1\mu\text{A}$), the output of the device might not be the desired high logic state. Also keep in mind that the inputs are high impedance ($\geq 22\text{k}\Omega$). When left open, noisy traces should be kept away from the receiver inputs to minimize capacitive coupling of undesired signals. Even with the open fail-safe feature, for maximum noise immunity, grounding the negative input of unused receivers is recommended.

APPLICATIONS INFORMATION

When the inputs are accidentally shorted (by cutting through a cable, for example), the short-circuit fail-safe feature will guarantee a high output logic level. Note also that if the line driver is removed and the termination resistors are left in place, the receiver will see this as a “short” and output a logic high.

Both of these fail-safe features will keep the receiver from outputting false data pulses under fault conditions.

Single-Ended Applications

Over short distances, the LTC1518/LTC1519 can be configured to receive single-ended data by tying one input to a fixed bias voltage and connecting the other input to the driver output. In such applications, standard high speed CMOS logic may be used as a driver for the LTC1518/LTC1519. With a 22k minimum input resistance, the receiver trip points may be easily adjusted to

accommodate different driver output swings by changing the resistor divider at the fixed input. Figure 6a shows a single-ended receiver configuration with the driver and receiver connected via PC traces. Note that at very high speeds, transmission line and driver ringing effects must be considered. Motorola's *MECL System Design Handbook* serves as an excellent reference for transmission line and termination effects. To mitigate transmission errors and duty cycle distortion due to driver ringing, a small output filter or a dampening resistor on the driver's V_{DD} may be needed as shown in Figure 6b. With an open circuit voltage of 3.3V at both inputs, the receivers can be used without an external bias applied to the fixed inputs. The fixed input should be bypassed with a 0.01 μ F ceramic capacitor. The positive input should be driven with a 5V CMOS part in order to minimize the skew caused by the 3.3V threshold. Figure 6c shows this configuration.

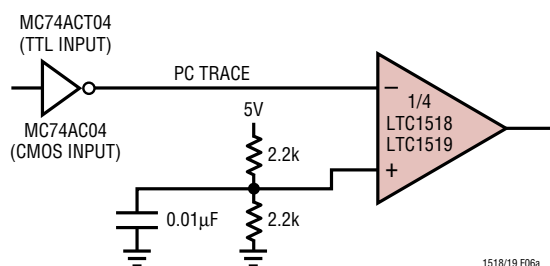


Figure 6a. Single-Ended Receiver

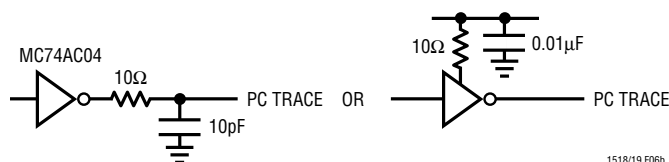


Figure 6b. Techniques to Minimize Driver Ringing

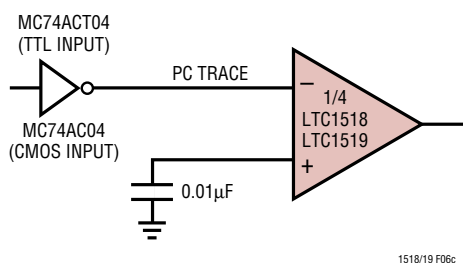


Figure 6c. Self Biased Single Ended Receiver

APPLICATIONS INFORMATION

Note that due to the increased skew, this configuration might not operate at the highest data rates. To transmit single-ended data over short to medium distances, twisted pair is recommended with the unused wire grounded at both ends (Figure 7).

Differential Transmission

Data rates up to 52Mbps can be transmitted over 100 feet of high quality category 5 twisted pair. Figure 8 shows the LTC1518 receiving differential data from an LTC1685 transceiver. As in the single-ended configurations, care must be taken to properly terminate the differential data lines to avoid unwanted reflections, etc.

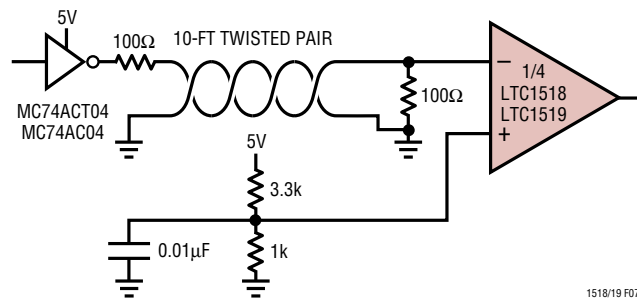


Figure 7. Medium Distance Single-Ended Transmission Using a CMOS Driver

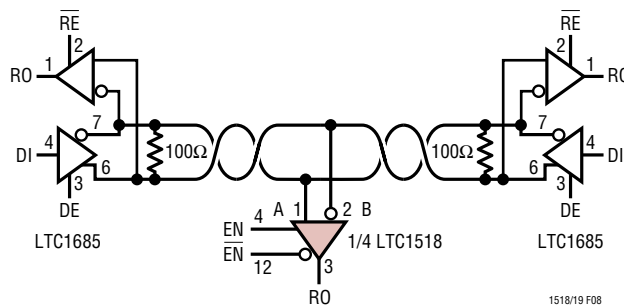


Figure 8. LTC1518 Connected to LTC1685 High Speed RS485 Transceiver

APPLICATIONS INFORMATION

Figure 9 shows a trace with 100ft category 5 UTP between an LTC1685 driver and an LTC1518 receiver. Notice that at the far end of the cable, the signal to the LTC1518 input has been reduced. Figure 10 shows a 52Mbps square wave.

Output Short-Circuit Protection

The LTC1518/LTC1519 employ voltage sensing short-circuit protection at the output terminals. For a given input differential, this circuitry determines what the correct

output level should be. For example, if the input differential is $\geq 300\text{mV}$, it expects the output to be a logic high. If the output is subsequently shorted to a voltage below $V_{DD}/2$, this circuitry shuts off the output devices and turns on a smaller device in its place. A timeout period of about 50ns is used in order to maintain normal high frequency operation, even under heavy capacitive loads ($>100\text{mA}$ transient current into the load).

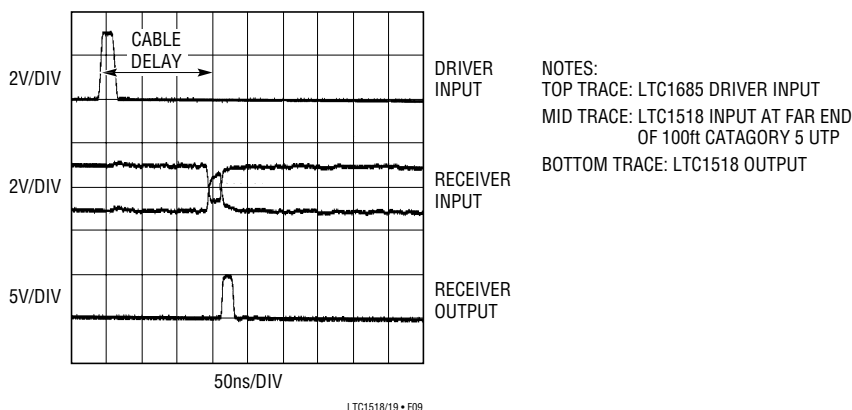


Figure 9. 20ns Pulse Propagating Down 100ft of Category 5 UTP

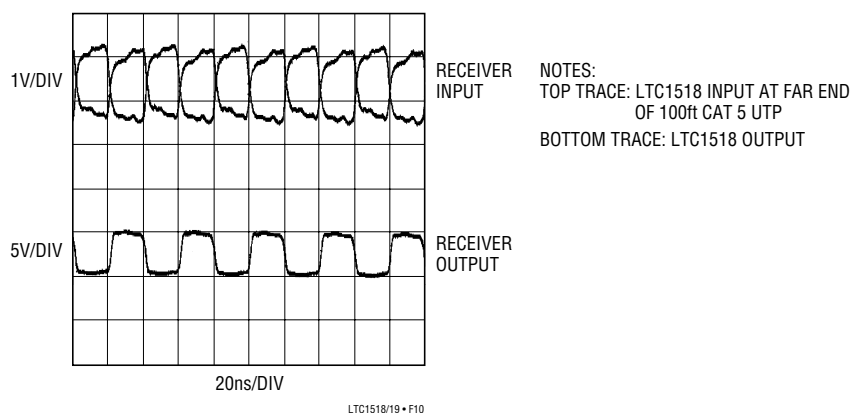
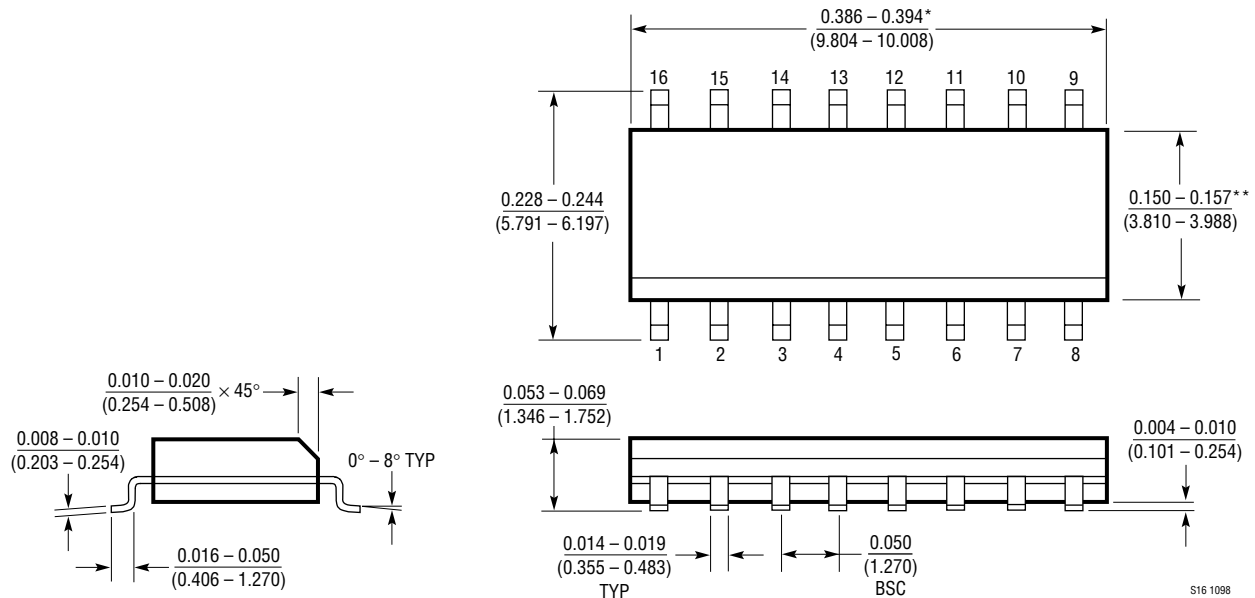


Figure 10. 52Mbps Pulse Train Over 100ft of Category 5 UTP

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
 (LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

The schematic diagram illustrates the internal circuitry of the plug-in card. Key components and connections include:

- Power and Ground:** V_{CC} (5V, 5A) and GND are connected to the BACK PLANE and PLUG-IN CARD connectors.
- Connectors:** CONNECTOR 1 and CONNECTOR 2 are used for interfacing with the back plane and the plug-in card.
- LTC1422 Comparator:** This IC is configured with V_{CC} ON (pin 8), SENSE (pin 7), GATE (pin 6), FB (pin 5), RESET (pin 1), TIMER (pin 3), and GND (pin 4). It is biased by a network of resistors (R1, R2, R3, R4) and capacitors (C1, C2).
- LTC1518 Quad Differential Line Driver:** Two instances of this IC are used to drive the data bus (D0-D7). Each instance has pins 1, 2, 6, 7, 10, 9, 14, 15, 8, 16, 4, and 3.
- Microprocessor (μP):** The RESET pin of the μP is connected to the RESET pin of the LTC1422.
- Passive Components:** Resistors R1 (0.005Ω), R2 (10Ω, 5%), R3 (6.81k, 1%), and R4 (2.43k, 1%) are used for biasing and signal conditioning. Capacitors C1 (0.1μF), C2 (0.33μF), and C4 (2200μF) are used for timing and decoupling.

RELATED PARTS

UltraFast is a trademark of Linear Technology Corporation.