

# MC74HCT273A

## Octal D Flip-Flop with Common Clock and Reset with LSTTL-Compatible Inputs

### High-Performance Silicon-Gate CMOS

The MC74HCT273A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

The HCT273A is identical in pinout to the LS273.

This device consists of eight D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active low.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 V to 5.5 V
- Low Input Current: 1.0  $\mu$ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 284 FETs or 71 Equivalent Gates
- These Devices are Pb-Free and are RoHS Compliant

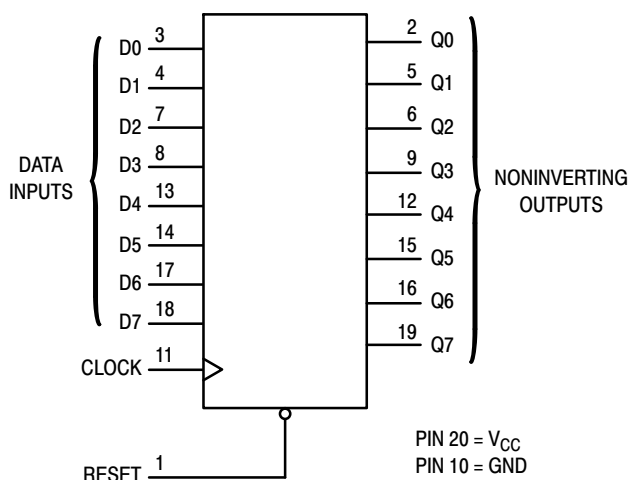


Figure 1. Logic Diagram

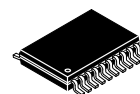


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SOIC-20W  
DW SUFFIX  
CASE 751D

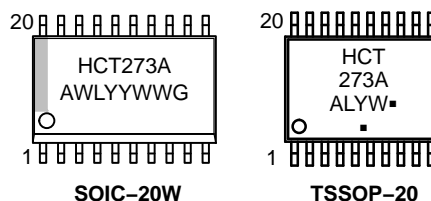


TSSOP-20  
DT SUFFIX  
CASE 948E

#### PIN ASSIGNMENT

RESET	1	20	V <sub>CC</sub>
Q0	2	19	Q7
D0	3	18	D7
D1	4	17	D6
Q1	5	16	Q6
Q2	6	15	Q5
D2	7	14	D5
D3	8	13	D4
Q3	9	12	Q4
GND	10	11	CLOCK

#### MARKING DIAGRAMS



SOIC-20W

TSSOP-20

A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Package  
(Note: Microdot may be in either location)

#### FUNCTION TABLE

Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	↗	H	H
H	↘	L	L
H	L	X	No Change
H	↔	X	No Change

X = Don't Care  
Z = High Impedance

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
$V_{in}$	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air SOIC Package†	500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-55	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				−55 to 25°C	≤ 85°C	≤ 125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> − 0.1 V  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA	4.5	3.98	3.84	3.7	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 4.0 mA	4.5	0.26	0.33	0.4	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND	5.5	±0.1	±1.0	±1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	5.5	4.0	40	160	μA
ΔI <sub>CC</sub>	Additional Quiescent Supply Current	V <sub>in</sub> = 2.4 V, Any One Input V <sub>in</sub> = V <sub>CC</sub> or GND, Other Inputs I <sub>out</sub> = 0 μA	5.5	≥ −55°C	25°C to 125°C		mA
				2.9	2.4		

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## AC ELECTRICAL CHARACTERISTICS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ , $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6.0 \text{ ns}$ )

Symbol	Parameter	Fig.	Guaranteed Limit			Unit
			−55 to 25°C	≤ 85°C	≤ 125°C	
f <sub>max</sub>	Maximum Clock Frequency (50% Duty Cycle)	2, 5	30	24	20	MHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Clock to Q	2, 5	25	28	35	ns
t <sub>PHL</sub>	Maximum Propagation Delay, Reset to Q		25	28	35	ns
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output	2, 5	18	20	22	ns
C <sub>PD</sub>	Power Dissipation Capacitance (Per Gate)*	Typical @ 25°C, V <sub>CC</sub> = 5.0 V				pF
		30				

\* Used to determine the no-load dynamic power consumption:  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ .

## TIMING REQUIREMENTS ( $V_{CC} = 5.0 \text{ V} \pm 10\%$ , $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6.0 \text{ ns}$ )

Symbol	Parameter	Fig.	Guaranteed Limit						Unit
			−55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t <sub>su</sub>	Minimum Setup Time, Data to Clock		10		12		15		ns
t <sub>h</sub>	Minimum Hold Time, Clock to Data		3.0		3.0		3.0		ns
t <sub>rec</sub>	Minimum Recovery Time, Set or Reset Inactive to Clock		5.0		5.0		5.0		ns
t <sub>w</sub>	Minimum Pulse Width, Clock	2	12		15		18		ns
t <sub>w</sub>	Minimum Pulse Width, Set or Reset		12		15		18		ns
t <sub>r</sub> , t <sub>f</sub>	Maximum Input Rise and Fall Times	2		500		500		500	ns

## SWITCHING WAVEFORMS

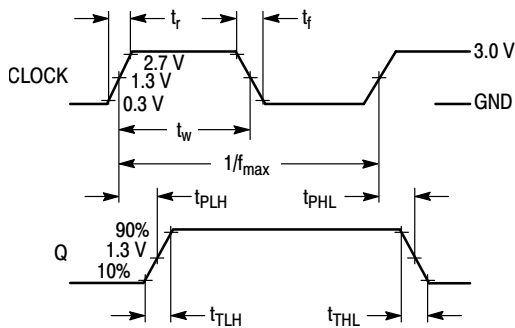


Figure 2.

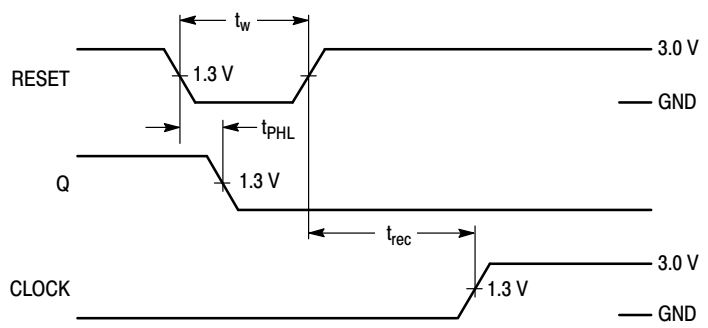


Figure 3.

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## SWITCHING WAVEFORMS

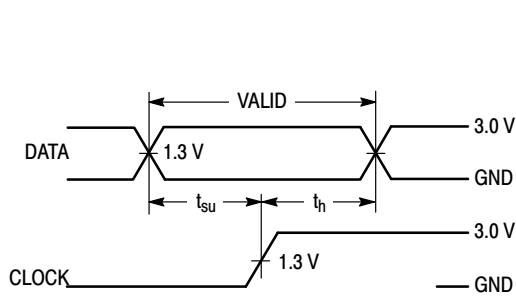
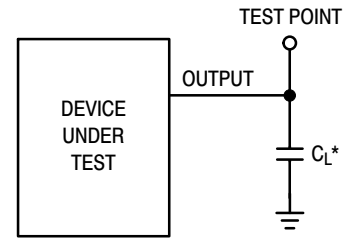


Figure 4.



\*Includes all probe and jig capacitance

Figure 5. Test Circuit

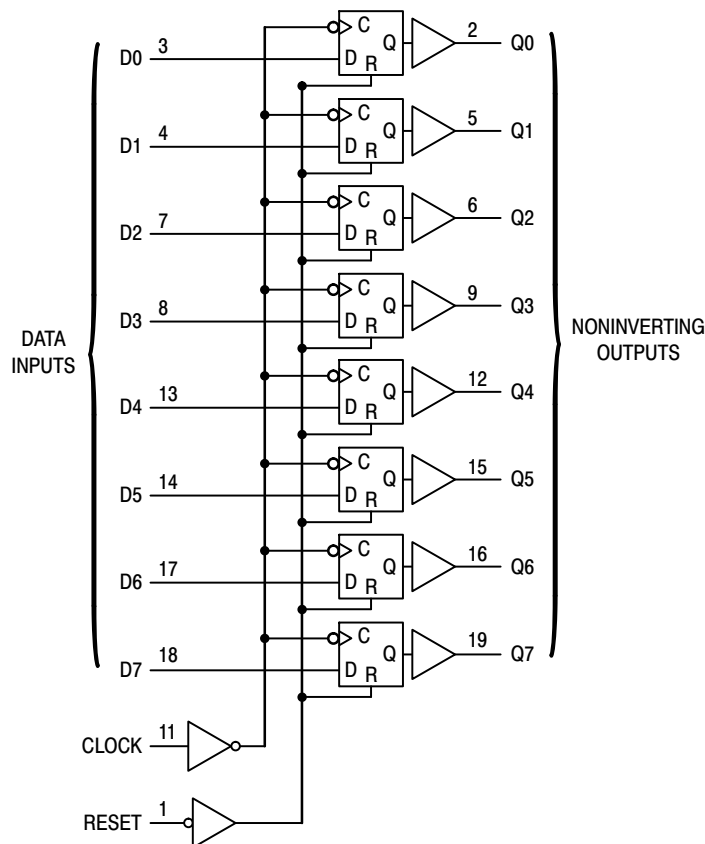


Figure 6. Expanded Logic Diagram

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MC74HCT273ADWG	SOIC-20 (Pb-Free)	38 Units / Rail
MC74HCT273ADWR2G	SOIC-20 (Pb-Free)	1000 / Tape & Reel
MC74HCT273ADTR2G	TSSOP-20 (Pb-Free)	2500 / Tape & Reel

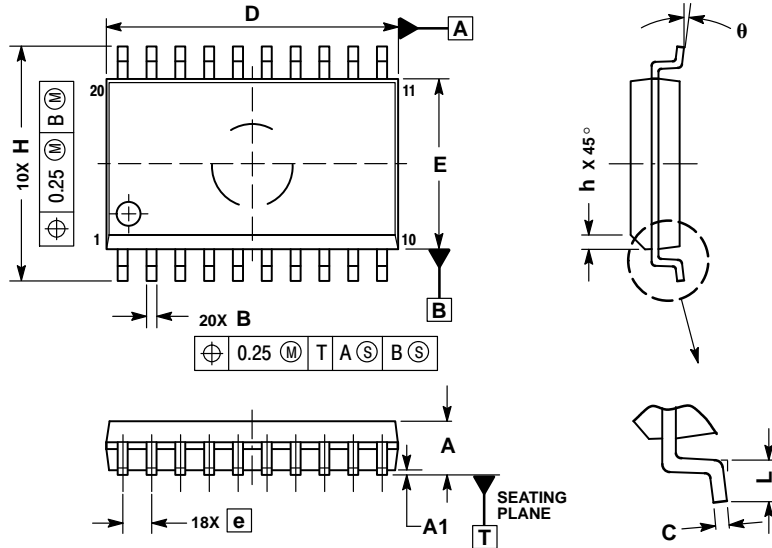
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



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## PACKAGE DIMENSIONS


SOIC-20W  
DW SUFFIX  
CASE 751D-05  
ISSUE G



### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27	BSC
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

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