1.5MHz/2.25MHz, 600mA Synchronous Step-Down Regulator with LDO Mode

FEATURES

- **High Efficiency: Up to 96%**
- **Very Low Quiescent Supply Current: 32µA During Linear Regulator Operation**
- **600mA Output Current (Buck Converter)**
- **Optionally Operates as Linear Regulator Below 3mA—External or Automatic ON/OFF**
- **2.5V to 5.5V Input Voltage Range**
- **1.5MHz or 2.25MHz Constant Frequency Operation or External Synchronization**
- **No Schottky Diode Required**
- **Low Dropout Operation: 100% Duty Cycle**
- 0.6V Reference Allows Low Output Voltages
- Shutdown Mode Draws <1µA Supply Current
- Current Mode Operation for Excellent Line and Load Transient Response
- Overtemperature Protected
- Low Profile (3mm × 3mm) 8-Lead DFN and 8-Lead MSOP Packages

APPLICATIONS

- Cellular Telephones
- Personal Information Appliances
- Wireless and DSL Modems
- Digital Still Cameras
- MP3 Players
- Portable Instruments

DESCRIPTION

The LTC®3448 is a high efficiency, monolithic, synchronous buck regulator using a constant frequency, current mode architecture. Supply current during operation is only 32µA (linear regulator mode) and drops to <1µA in shutdown. The 2.5V to 5.5V input voltage range makes the LTC3448 ideally suited for single Li-Ion battery-powered applications. 100% duty cycle provides low dropout operation, extending battery life in portable systems. At moderate output load levels, PWM pulse skipping mode operation provides very low output ripple voltage for noise sensitive applications.

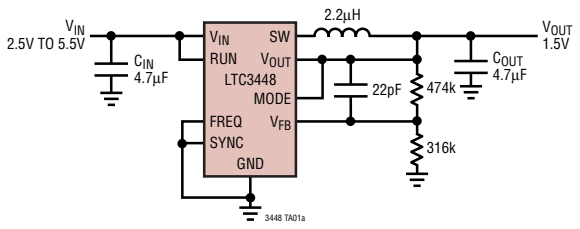
The LTC3448 automatically switches into linear regulator operation at very low load currents to maintain <5mV$_{P-P}$ output voltage ripple. Supply current in this mode is typically 32µA. The switch to linear regulator mode occurs at a threshold of 3mA. Linear regulator operation can be set to on, off or automatic turn on/off.

Switching frequency is selectable at either 1.5MHz or 2.25MHz, allowing the use of small surface mount inductors and capacitors.

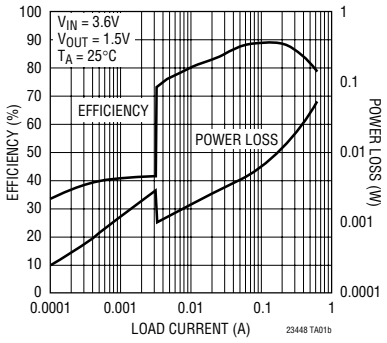
The internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. Low output voltages are easily supported with the 0.6V feedback reference voltage. The LTC3448 is available in a low profile 3mm × 3mm DFN package or thermally enhanced 8-lead MSOP.

TYPICAL APPLICATION

1.5V High Efficiency Regulator with Automatic LDO Mode



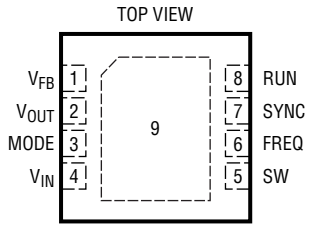
Efficiency and Power Loss vs Load Current



ABSOLUTE MAXIMUM RATINGS (Note 1)

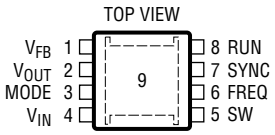
Input Supply Voltage ..... –0.3V to 6V
RUN, SYNC Voltages ..... –0.3V to (V_{IN} + 0.3V)
MODE Voltage ..... –0.3V to (V_{IN} + 0.3V)
FREQ, V_{FB} Voltages ..... –0.3V to (V_{IN} + 0.3V)
SW Voltage ..... –0.3V to (V_{IN} + 0.3V)
V_{OUT} Voltage ..... –0.3V to (V_{IN} + 0.3V)
P-Channel Switch Source Current (DC) 800mA
N-Channel Switch Sink Current (DC) 800mA
V_{OUT} (LDO) Source Current 25mA
Peak SW Sink and Source Current 1.3A
Operating Temperature Range (Note 2) .. –40°C to 85°C
Junction Temperature (Notes 3, 7) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
MSOP Only ..... 300°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 9) IS GND
MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LTC3448EDD
DD PART MARKING
LBMJ



MS8E PACKAGE
8-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 9) IS GND
MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LTC3448EMS8E
MS8 PART MARKING
LTBMK

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 3.6V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VFB}	Feedback Current		●			±30	nA
V_{FB}	Regulated Feedback Voltage (Note 4)	T_A = 25°C 0°C ≤ T_A ≤ 85°C –40°C ≤ T_A ≤ 85°C	 ●	0.5880 0.5865 0.5850	0.6 0.6 0.6	0.6120 0.6135 0.6150	V V V
ΔV_{FB}	Reference Voltage Line Regulation	V_{IN} = 2.5V to 5.5V (Note 4)	●		0.2	0.4	%/V
ΔV_{OVL}	Output Overvoltage Lockout	$\Delta V_{OVL} = V_{OVL} - V_{FB}$ $\Delta V_{OVL} = (V_{OVL} - V_{OUT}) \bullet 100/V_{OUT}$		15 2.5	35 5.8	55 9.2	mV %
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 2.5V to 5.5V (LDO)			0.1	0.8	%/V
I_{PK}	Peak Inductor Current	V_{FB} = 0.5V or V_{OUT} = 90%, Duty Cycle < 35%		0.7	1	1.3	A
$V_{LOADREG}$	Output Voltage Load Regulation	LDO, 1mA to 10mA			0.5		%/V
$V_{OUT(MAX)}$	Maximum Output Voltage	(Note 9)		V_{IN} – 0.7	V_{IN} – 0.3		V
V_{IN}	Input Voltage Range		●	2.5		5.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 3.6V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	Input DC Bias Current Active Mode (Pulse Skip, No LRO)	V_{IN} = 3.6V (Note 5) V_{FB} = 0.5V or V_{OUT} = 90%, I_{LOAD} = 0A, 1.5MHz V_{FB} = 0.5V or V_{OUT} = 90%, I_{LOAD} = 0A, 2.25MHz			 250 275	 375 400	 µA µA
	Linear Regulator Operation (LRO)	$I_{LOAD} \le I_{LDO(ON)}$			32	43	µA
	Shutdown	V_{RUN} = 0V, V_{IN} = 5.5V			0.1	1	µA
f_{OSC}	Oscillator Frequency	FREQ = Low, V_{IN} = 3.6V FREQ = High	● ●	1.2 1.8	1.5 2.25	1.8 2.7	MHz MHz
f_{SYNC}	Synchronization Frequency	(Note 6)		1.5		>4	MHz
$V_{TH(SYNC)}$	SYNC Activation Input Threshold				1	1.3	V
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET	I_{SW} = 100mA			0.4		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET	I_{SW} = –150mA			0.35		Ω
I_{LSW}	SW Leakage	V_{RUN} = 0V, V_{SW} = 0V or 5V, V_{IN} = 5V			±0.01	±1	µA
V_{RUNH}	RUN Threshold High		●	1.5			V
V_{RUNL}	RUN Threshold Low		●			0.3	V
I_{RUN}	RUN Leakage Current		●		±0.01	±1	µA
V_{FREQH}	FREQ Threshold High		●	V_{IN} – 1			V
V_{FREQL}	FREQ Threshold Low		●			1	V
I_{FREQ}	FREQ Leakage Current		●		±0.01	±1	µA
V_{MODEH}	MODE Threshold High		●	V_{IN} – 0.15			V
V_{MODEL}	MODE Threshold Low		●			0.12	V
I_{MODE}	MODE Leakage Current		●		±0.1	±1	µA
I_{SYNC}	SYNC Leakage Current		●		±0.01	±1	µA
$I_{LDO(ON)}$	LRO ON Load Current Threshold	2.2mH Inductor (Note 8)			3	5	mA
$I_{LDO(OFF)}$	LRO OFF Load Current Threhold			8	11	17	mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3448E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D)(43°C/W)$

Note 4: The LTC3448 is tested in a proprietary test mode that connects V_{FB} to the output of the error amplifier.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. LRO is "linear regulator operation."

Note 6: 4MHz operation is guaranteed by design but is not production tested and is subject to duty cycle limitations.

Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

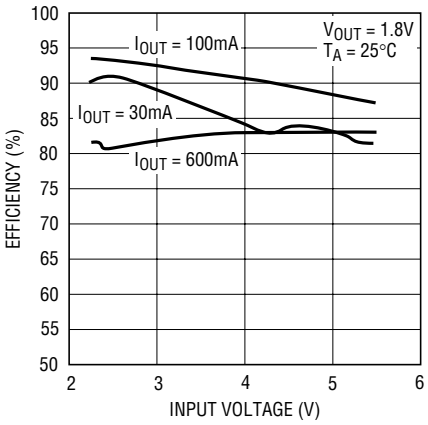
Note 8: The load current below which the switching regulator turns off and the LDO turns on is, to first order, inversely proportional to the value of the inductor. This effect is covered in more detail in the Operation section. This parameter is not production tested but is guaranteed by design.

Note 9: For 2.5V < V_{IN} < 2.7V the output voltage is limited to V_{IN} – 0.7V to ensure regulation in linear regulator mode. This parameter is not production tested but is guaranteed by design.

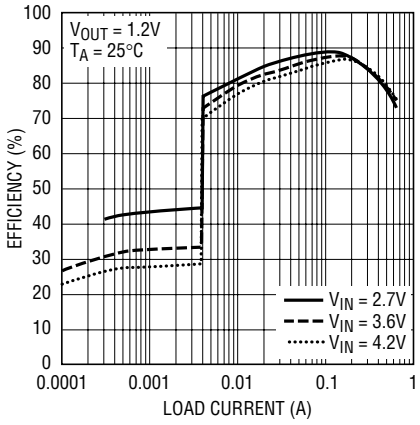
TYPICAL PERFORMANCE CHARACTERISTICS

(From Figure1a Except for the Resistive Divider Resistor Values)

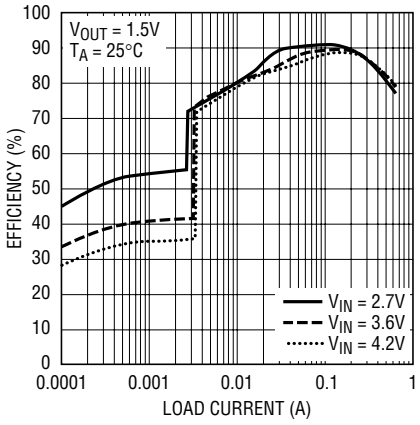
Efficiency vs Input Voltage



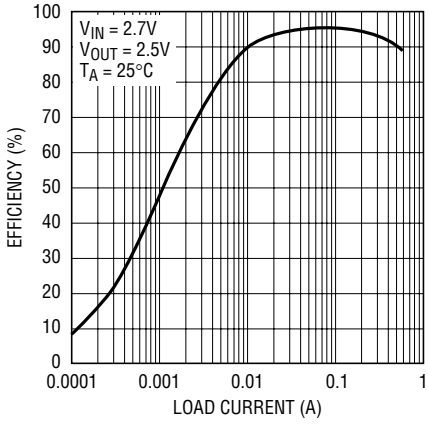
Efficiency vs Load Current



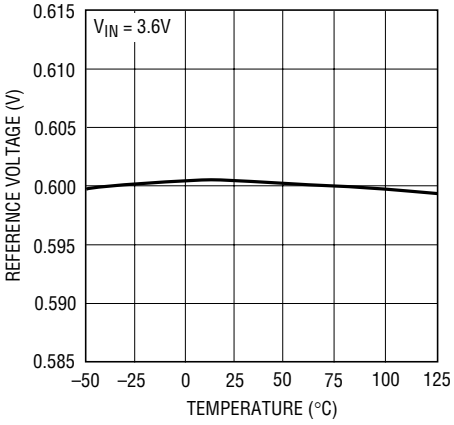
Efficiency vs Load Current



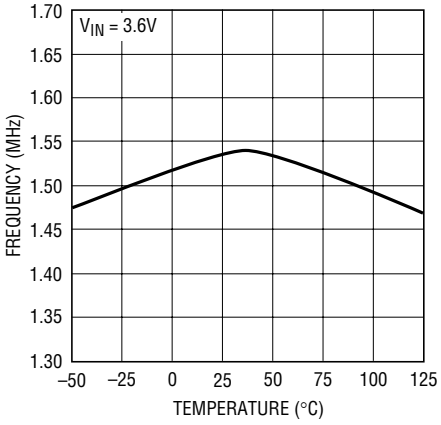
Efficiency vs Load Current (Switcher Only)



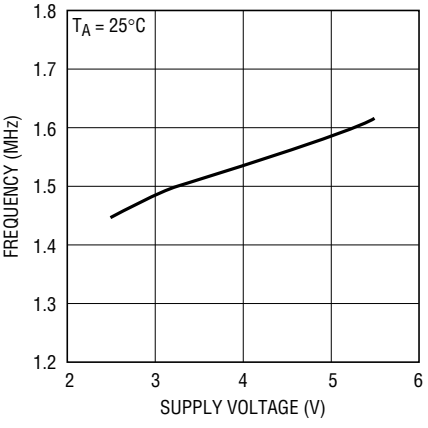
Reference Voltage vs Temperature



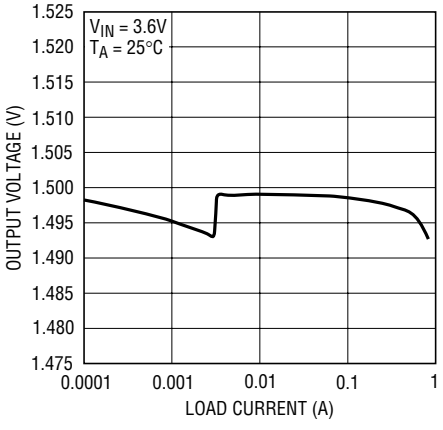
Oscillator Frequency vs Temperature



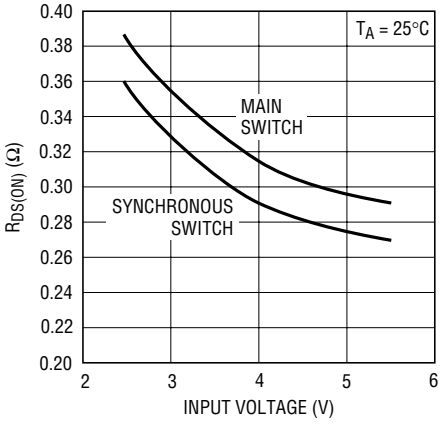
Oscillator Frequency vs Supply Voltage



Output Voltage vs Load Current



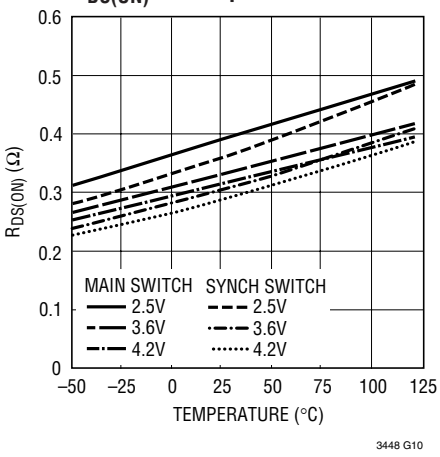
$R_{DS(ON)}$ vs Input Voltage



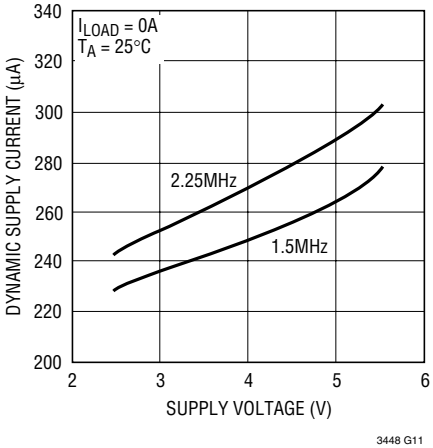
TYPICAL PERFORMANCE CHARACTERISTICS

(From Figure1a Except for the Resistive Divider Resistor Values)

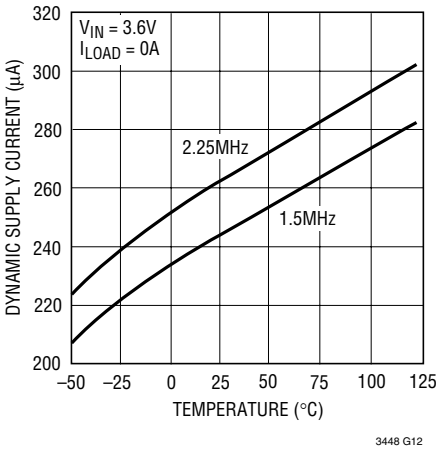
$R_{DS(ON)}$ vs Temperature



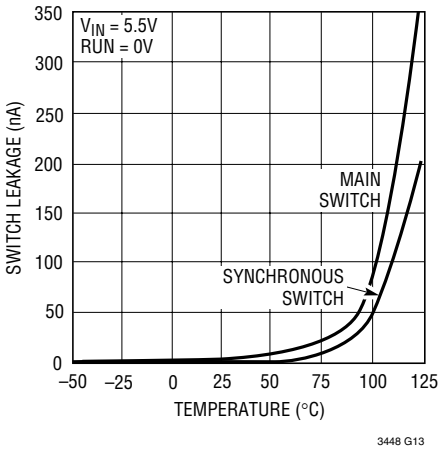
Dynamic Supply Current vs Supply Voltage



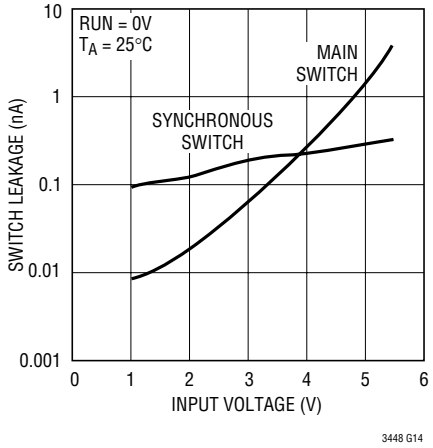
Dynamic Supply Current vs Temperature



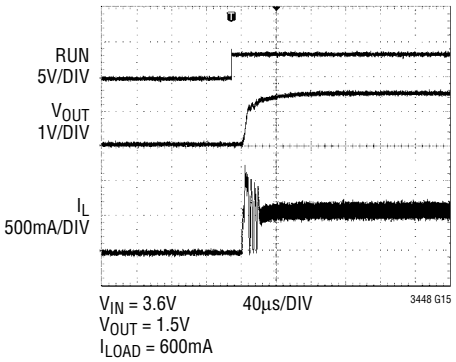
Switch Leakage vs Temperature



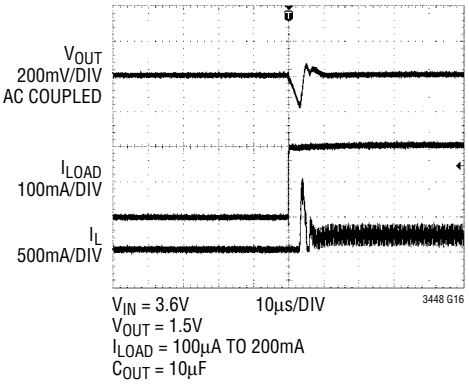
Switch Leakage vs Input Voltage



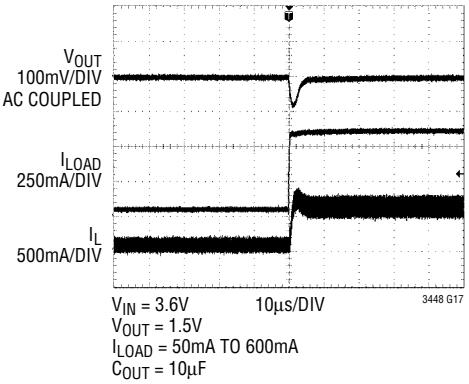
Start-Up from Shutdown



Load Step



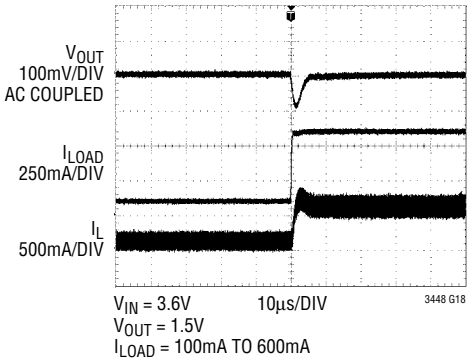
Load Step



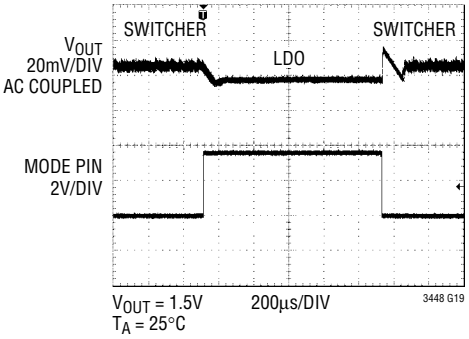
TYPICAL PERFORMANCE CHARACTERISTICS

(From Figure 1a Except for the Resistive Divider Resistor Values)

Load Step



External Mode Control (Constant 1mA Load)



PIN FUNCTIONS

V_{FB} (Pin 1): Feedback Pin. This pin receives the feedback voltage from an external resistive divider across the output.

V_{OUT} (Pin 2): Output Pin. This pin connects to an external resistor divider and the linear regulator output. Connect externally to the inductor and the output capacitor. The internal linear regulator will supply current up to the $I_{LDO(OFF)}$ current. Load currents above that are supplied by the buck regulator. Internal circuitry automatically enables the buck switching regulator at load currents higher than the $I_{LDO(OFF)}$. The minimum required capacitance on this pin is 2µF.

MODE (Pin 3): Linear Regulator Control. Grounding this pin turns off the linear regulator. Setting this pin to V_{IN} turns on the linear regulator regardless of the load current. Tying this pin midrange (i.e., to V_{OUT}) will place the linear regulator in auto mode, where turn on/off is a function of the load current. In applications where MODE is externally driven high or low, this pin should be held low for 50µs after the RUN pin is pulled high.

V_{IN} (Pin 4): Main Supply Pin. This pin must be closely decoupled to GND with a 2.2µF or greater ceramic capacitor.

SW (Pin 5): Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.

FREQ (Pin 6): Frequency Select. Switching frequency is set to 1.5MHz when FREQ = 0V and to 2.25MHz when FREQ = V_{IN}. Do not float this pin.

SYNC (Pin 7): External Synchronization Pin. The oscillation frequency can be synchronized to an external oscillator applied to this pin. For external frequencies above 2.2MHz, pull FREQ high.

RUN (Pin 8): Run Control Input. Forcing this pin above 1.5V enables the part. Forcing this pin below 0.3V shuts down the device. In shutdown, all functions are disabled drawing <1µA supply current. Do not leave RUN floating.

Exposed Pad (Pin 9): Ground. This pin must be soldered to PCB.

FUNCTIONAL DIAGRAM

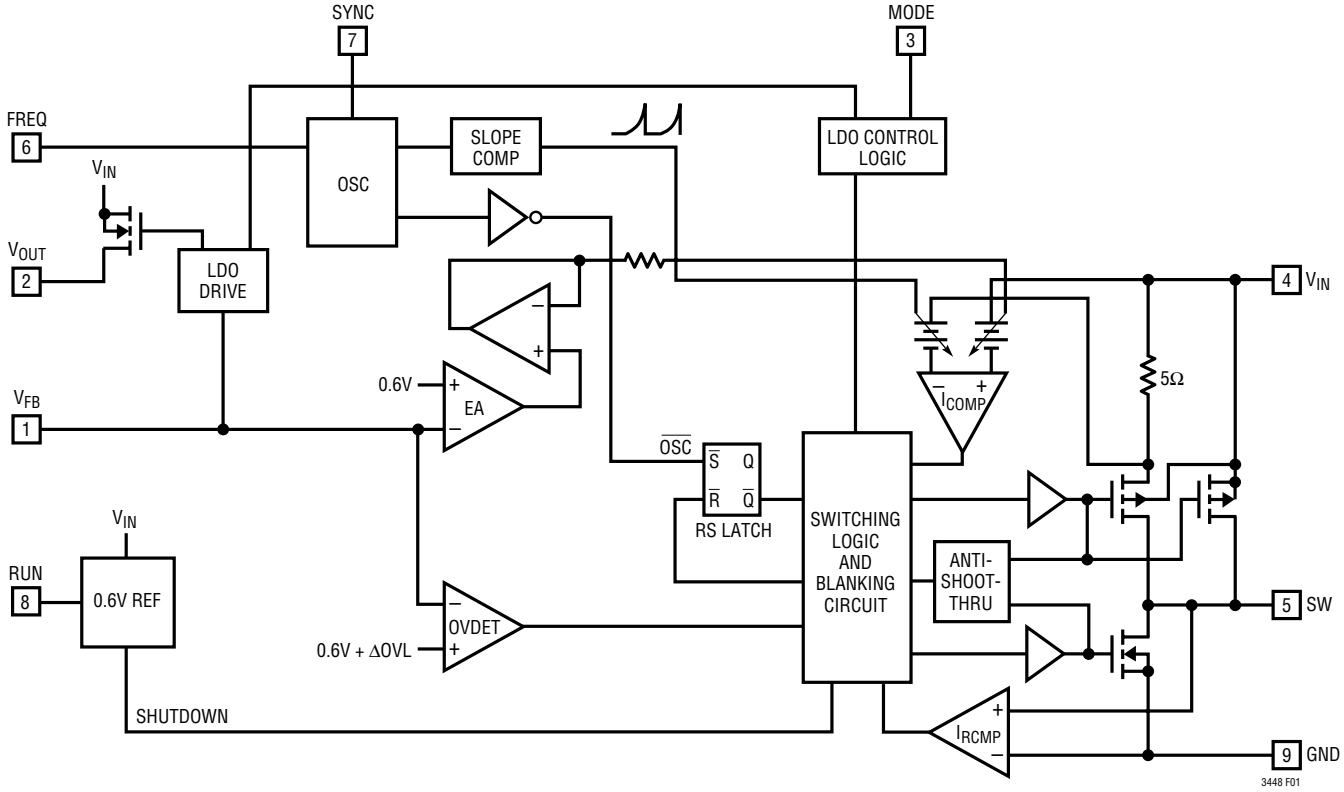


Figure 1

OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3448 uses a constant frequency, current mode, step-down architecture. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, I_{COMP}, resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch, is controlled by the output of error amplifier EA. When the load current increases, it causes a slight decrease in the feedback voltage FB_{INT} relative to the 0.6V reference, which in turn, causes the EA amplifier's output voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator I_{RCMP}, or the beginning of the next clock cycle. The comparator OVDET guards against transient overshoots 5.8% by turning off the main switch and keeping it off until the fault is removed.

Pulse Skipping Mode Operation

At light loads, the inductor current may reach zero or reverse on each pulse. The bottom MOSFET is turned off by the current reversal comparator, I_{RCMP}, and the switch voltage will ring. This is discontinuous mode operation, and is normal behavior for the switching regulator. At very light loads, the LTC3448 will automatically skip pulses to maintain output regulation.

Low Ripple LDO Mode Operation

At load currents below $I_{LDO(ON)}$, and when enabled, the LTC3448 will switch into very low ripple, linear regulating operation (LRO). In this mode, the current is sourced from

OPERATION (Refer to Functional Diagram)

the V_{OUT} pin and both the main and synchronous switches are turned off. The control loop is stabilized by the load capacitor and requires a minimum value of 2µF. The LTC3448 will change back to switching mode and turn off the LDO when the load current exceeds approximately 11mA.

When MODE is connected to an intermediate voltage level (i.e., V_{OUT}), this switchover is automatic. If MODE is pulled high to V_{IN}, the LDO remains on and the switcher off regardless of the load current. The LDO is capable of providing a maximum of approximately 15mA before the load regulation will degrade to unacceptable levels. If MODE is pulled to GND, the switcher remains on and the LDO off regardless of the load current.

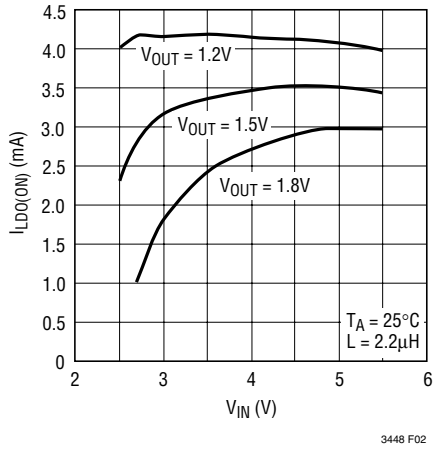


Figure 2. $I_{LDO(ON)}$ vs V_{IN}, V_{OUT}

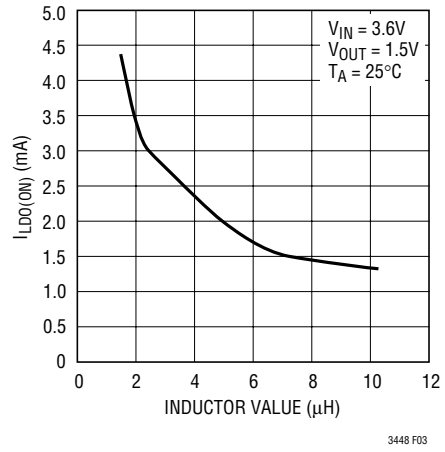


Figure 3. $I_{LDO(ON)}$ vs L_{OUT}

Some applications may be able to anticipate the transition from high to low and low to high load currents. In these cases it may be desirable to switch between modes by controlling the MODE pin with a processor signal. In these applications it is important that the MODE pin is pulled high no earlier than 50µs after the RUN pin is pulled high. This will ensure proper start-up of internal reference circuitry.

The load current $I_{LDO(ON)}$ below which the switcher will automatically turn off and the LDO turn on is independent of the external capacitor, and to first order, independent of supply and output voltage. There is an inverse relationship between $I_{LDO(ON)}$ and the value of the inductor. These dependencies are shown in Figures 2 and 3. Automatic operation with inductor values below 1µH is not recommended.

At the low load currents at which the switcher to linear regulator transition occurs, the switcher is operating in pulse skipping mode. During each switching cycle in this mode, while the synchronous switch (bottom MOSFET) is on, the inductor current decays until the reverse current comparator is triggered. At this occurrence, the bottom MOSFET is turned off. Ideally, this occurs when the inductor current is precisely zero. In reality, because of on-chip delays, this current will be negative at higher output voltages.

The internal algorithm which controls the LDO turn-on load current level makes certain assumptions about the amount of charge transferred to the output on each switching cycle. These assumptions are no longer met when the inductor current begins to reverse. This causes the load current at which the transition takes place to move to lower levels at higher output voltages. For this reason use of the LDO auto mode is not recommended for output levels above 2V. For output voltages above 2V, the MODE pin should be driven externally.

Short-Circuit Protection

When the output is shorted to ground, the main switch cycle will be skipped, and the synchronous switch will remain on for a longer duration. This allows the inductor current more time to decay, thereby preventing runaway.

OPERATION (Refer to Functional Diagram)

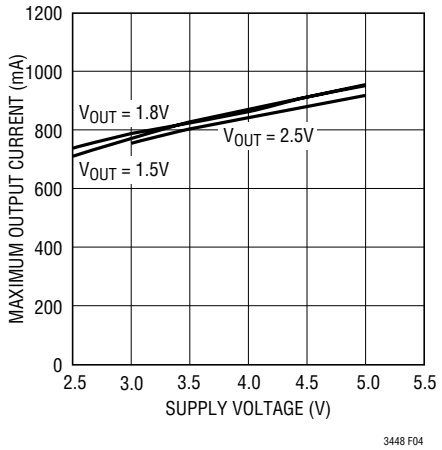


Figure 4. Maximum Output Current vs Input Voltage

Dropout Operation

As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor.

An important detail to remember is that at low input supply voltages, the $R_{DS(ON)}$ of the P-channel switch increases (see Typical Performance Characteristics). Therefore, the user should calculate the power dissipation when the LTC3448 is used at 100% duty cycle with low input voltage (See Thermal Considerations in the Applications Information section).

Low Supply Operation

The LTC3448 will operate with input supply voltages as low as 2.5V, but the maximum allowable output current is reduced at this low voltage. Figure 4 shows the reduction in the maximum output current as a function of input voltage for various output voltages.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. This normally results in a reduction of maximum inductor peak current for duty cycles >40%. However, the LTC3448 uses a patent-pending scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

APPLICATIONS INFORMATION

The basic LTC3448 application circuit is shown on the first page of this data sheet. External component selection is driven by the load requirement and begins with the selection of L followed by C_{IN} and C_{OUT}.

Inductor Selection

For most applications, the value of the inductor will fall in the range of 1µH to 4.7µH. Its value is chosen based on the desired ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation 1. A reasonable starting point for setting ripple current is ΔI_L = 240mA (40% of 600mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 720mA rated inductor should be enough for most applications (600mA + 120mA). For better efficiency, choose a low DC-resistance inductor.

If the LTC3448 is to be used in auto LDO mode, inductor values less than 1µH should not be used.

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Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3448 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3448 applications.

Table 1. Representative Surface Mount Inductors

PART NUMBER	VALUE (μH)	DCR (Ω MAX)	MAX DC CURRENT (A)	SIZE W × L × H (mm³)
Sumida CDRH3D16	1.5	0.043	1.55	3.8 × 3.8 × 1.8
	2.2	0.075	1.20	
	3.3	0.110	1.10	
	4.7	0.162	0.90	
Sumida CMD4D06	2.2	0.116	0.950	3.5 × 4.3 × 0.8
	3.3	0.174	0.770	
	4.7	0.216	0.750	
Coilcraft ME3220	2.2	0.104	1.8	2.5 × 3.2 × 2.0
	3.3	0.138	1.3	
	4.7	0.190	1.2	
Murata LQH3C	1.0	0.060	1.00	2.5 × 3.2 × 2.0
	2.2	0.097	0.79	
	4.7	0.150	0.65	

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{required}\ I_{RMS} \cong I_{OMAX}\frac{\left[V_{OUT}\left(V_{IN}-V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. In any case, if LDO mode is enabled, the value of C_{OUT} must have a minimum value of 2μF to ensure loop stability. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L\left(ESR+\frac{1}{8fC_{OUT}}\right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3448's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used **freely** to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At

APPLICATIONS INFORMATION

worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN}, large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

The output voltage is set by tying V_{FB} to a resistive divider according to the following formula:

$$V_{OUT} = 0.6V\left(1+\frac{R2}{R1}\right) \quad (2)$$

The external resistive divider is connected to the output, allowing remote voltage sensing as shown in Figure 5.

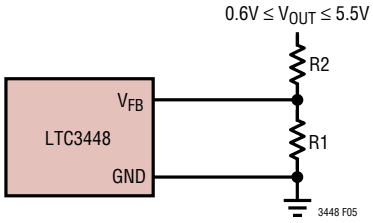

Figure 5. Setting the LTC3448 Output Voltage

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in LTC3448 circuits: V_{IN} quiescent current and I^2R losses. When in switching mode, V_{IN} quiescent current loss dominates the efficiency loss at low load currents, whereas the I^2R loss dominates the efficiency loss at medium to high load currents. At very low load currents with the part operating in LDO mode, efficiency can be dominated by I^2R losses in the pass transistor and is a strong function of ($V_{IN} – V_{OUT}$). In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of little consequence as illustrated in Figure 6.

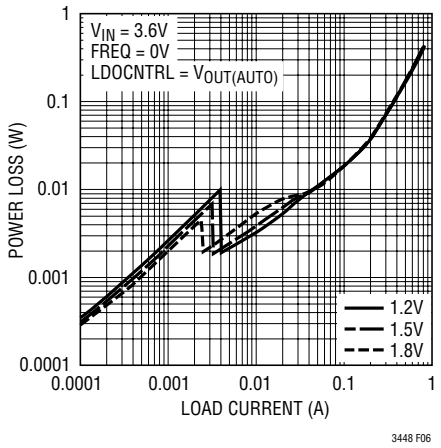

Figure 6. Power Loss vs Load Current

1. The V_{IN} quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from V_{IN} to ground. The resulting dQ/dt is the current out of V_{IN} that is typically larger than the DC bias current and proportional to frequency. Both the DC bias and gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.
2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode, the average output current flowing through inductor L is “chopped” between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both

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top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current.

3. At load currents below the selected threshold the LTC3448 will switch into low ripple LDO mode if enabled. In this case the losses are due to the DC bias currents as given in the electrical characteristics and I^2R losses due to the $(V_{IN} - V_{OUT})$ voltage drop across the internal pass transistor.

Other losses when in switching operation, including C_{IN} and COUT ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

The LTC3448 requires the package backplane metal (GND pin) to be well soldered to the PC board. This gives the DFN and MSOP packages exceptional thermal properties, making it difficult in normal operation to exceed the maximum junction temperature of the part. In most applications the LTC3448 does not dissipate much heat due to its high efficiency. In applications where the LTC3448 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part if it is not well thermally grounded. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3448 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = P_D\theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, T_J, is given by:

$$T_J = T_A + T_R$$

where T_A is the ambient temperature.

As an example, consider the LTC3448 in dropout at an input voltage of 2.7V, a load current of 600mA and an ambient temperature of 70°C. From the typical performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 70°C is approximately 0.52Ω. Therefore, power dissipated by the part is:

$$P_D = I_{LOAD}^2 \bullet R_{DS(ON)} = 187.2mW$$

For the 3mm × 3mm DFN package, the θ_{JA} is 43°C/W. Thus, the junction temperature of the regulator is:

$$T_J = 85°C + (0.1872)(43) = 93°C$$

which is well below the maximum junction temperature of 125°C.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance $R_{DS(ON)}$.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $(\Delta I_{LOAD} \bullet ESR)$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. For a detailed explanation of switching control loop theory, see Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel

APPLICATIONS INFORMATION

with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25 • C_{LOAD}). Thus, a 10µF capacitor charging to 3.3V would require a 250µs rise time, limiting the charging current to about 130mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3448. These items are also illustrated graphically in Figures 7 and 8. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace and the V_{IN} trace should be kept short, direct and wide.
2. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1/R2 must be connected between the (+) plate of C_{OUT} and ground.
3. Does the (+) plate of C_{IN} connect to V_{IN} as closely as possible? This capacitor provides the AC current to the internal power MOSFETs.
4. Keep the switching node, SW, away from the sensitive V_{FB} node.
5. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.

Design Example

As a design example, assume the LTC3448 is used in a single lithium-ion battery-powered cellular phone application. The V_{IN} will be operating from a maximum of 4.2V down to about 2.7V. The load current requirement is a maximum of 0.6A but most of the time it will be in standby mode, requiring only 2mA. Efficiency at both low

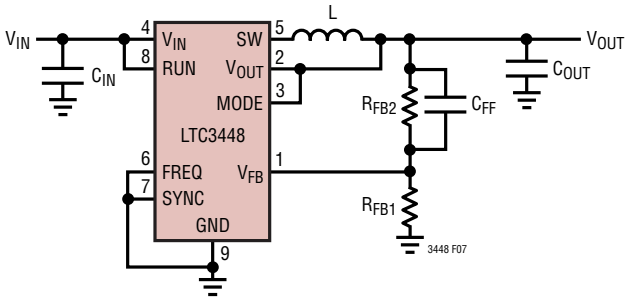


Figure 7. LTC3448 Layout Design

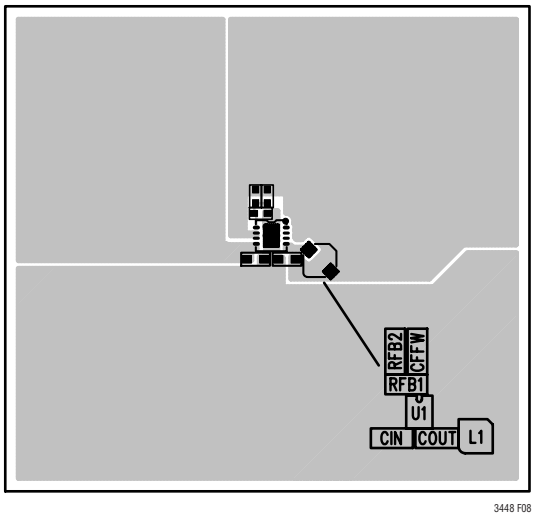


Figure 8. LTC3448 Layout

APPLICATIONS INFORMATION

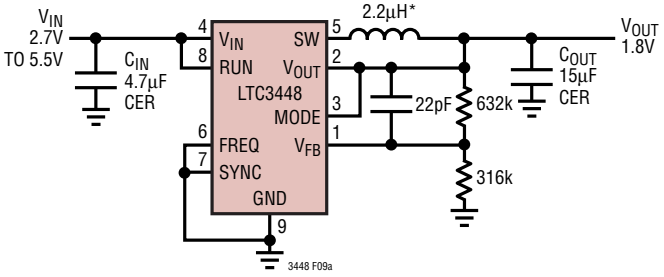
and high load currents is important. Output voltage is 1.8V. With this information we can calculate L using Equation (1),

$$L = \frac{1}{(f)(\Delta I_L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Substituting V_{OUT} = 1.8V, V_{IN} = 4.2V, ΔI_L = 240mA and f = 1.5MHz in Equation (3) gives:

$$L = \frac{1.8V}{1.5MHz(240mA)}\left(1 - \frac{1.8V}{4.2V}\right) = 2.86\mu H$$

A 2.2µH inductor works well for this application. For best efficiency choose a 720mA or greater inductor with less than 0.2Ω series resistance.



C_{IN}: TAIYO YUDEN JMK212BJ475MG
C_{OUT}: TAIYO YUDEN JMK212BJ475MG
*MURATA LQH32CN2R2M11

Figure 9a

C_{IN} will require an RMS current rating of at least 0.3A ≅ $I_{LOAD(MAX)}/2$ at temperature and C_{OUT} will require an ESR of less than 0.25Ω. In most cases, a ceramic capacitor will satisfy this requirement.

For the feedback resistors, choose R1 = 316k. R2 can then be calculated from Equation (2) to be:

$$R2 = \left(\frac{V_{OUT}}{0.6} - 1\right)R1 = 632k$$

Figure 9 shows the complete circuit along with its efficiency curve.

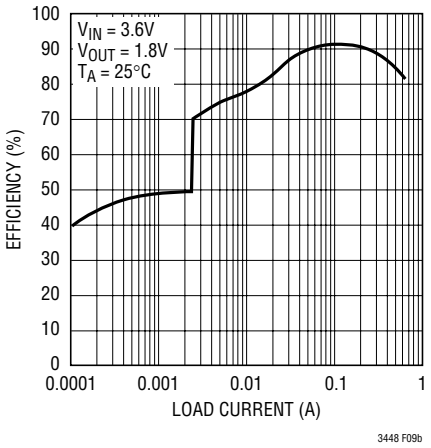


Figure 9b

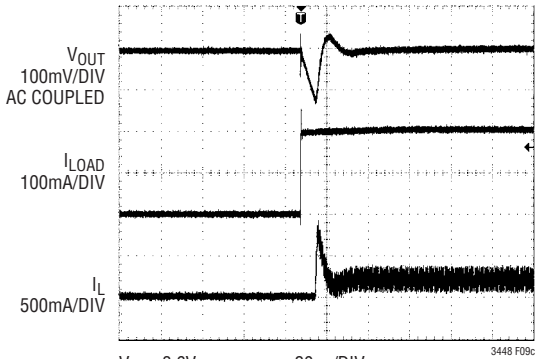


Figure 9c

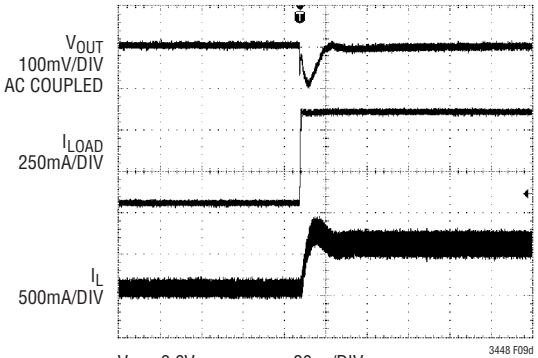
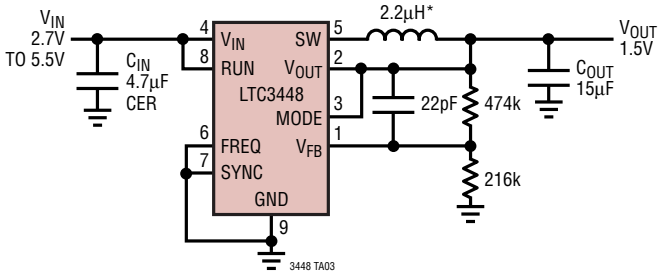


Figure 9d

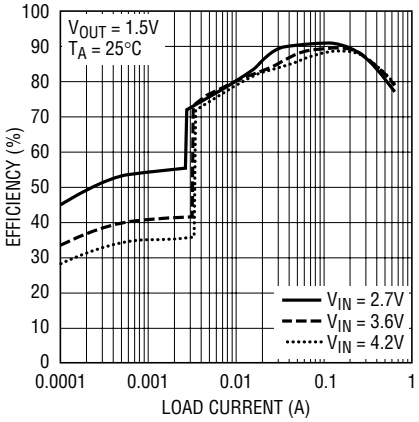
TYPICAL APPLICATIONS

Single Li-Ion 1.5V/600mA Regulator for High Efficiency and Small Footprint

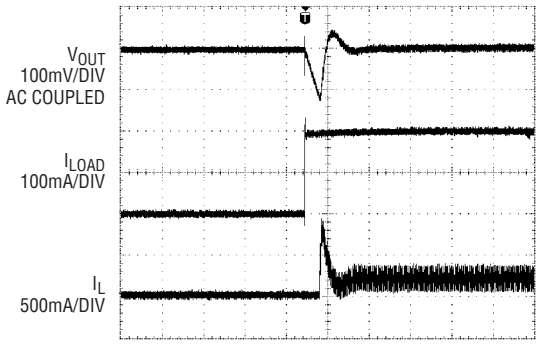


C_{IN}: TAIYO YUDEN CERAMIC JMK212BJ475MG
C_{OUT}: TAIYO YUDEN CERAMIC JMK212BJ475MG
*MURATA LQH32CN2R2M33

Efficiency vs Output Current

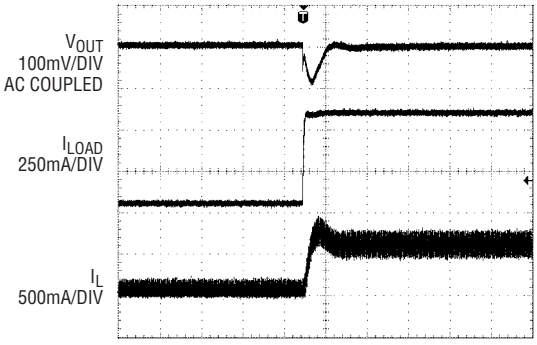


Load Step



V_{IN} = 3.6V 20µs/DIV
V_{OUT} = 1.5V
I_{LOAD} = 100µA TO 200mA

Load Step

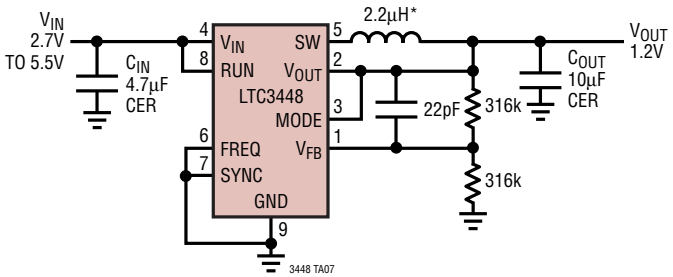


V_{IN} = 3.6V 20µs/DIV
V_{OUT} = 1.5V
I_{LOAD} = 50mA TO 600mA

Note: Performance data measured on the LTC3448 with external resistors

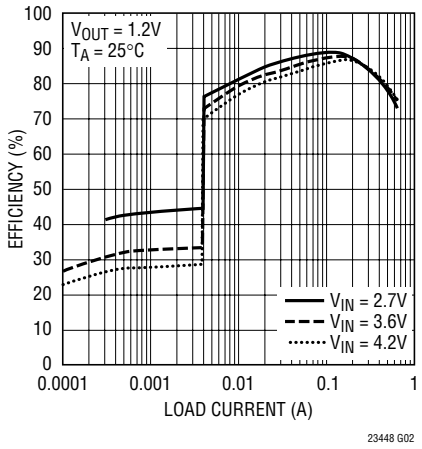
TYPICAL APPLICATIONS

Single Li-Ion 1.2V/600mA Regulator for High Efficiency and Small Footprint

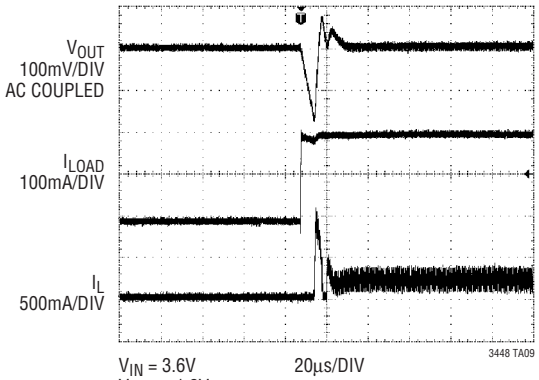


C_{IN}: TAIYO YUDEN JMK212BJ475MG
C_{OUT}: TAIYO YUDEN JMK212BJ475MG
*MURATA LQH32CN2R2M33

Efficiency vs Output Current

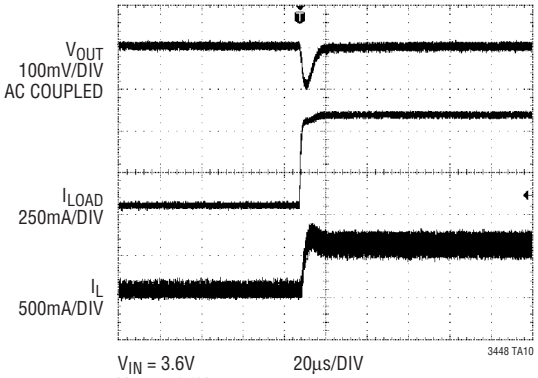


Load Step



V_{IN} = 3.6V 20µs/DIV
V_{OUT} = 1.2V
I_{LOAD} = 100µA TO 200mA

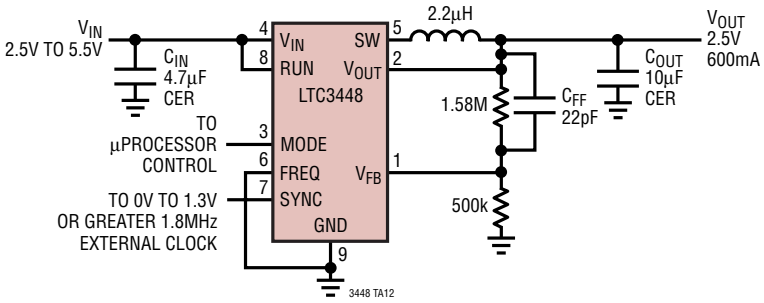
Load Step



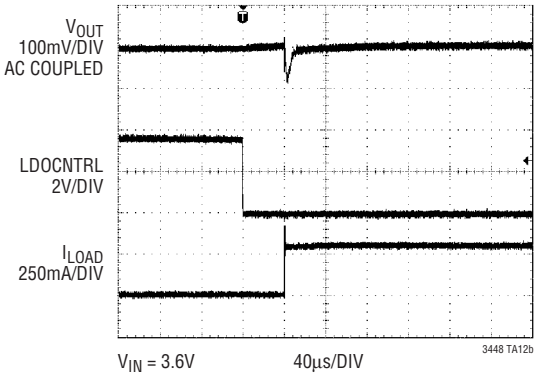
V_{IN} = 3.6V 20µs/DIV
V_{OUT} = 1.2V
I_{LOAD} = 50mA TO 600mA

TYPICAL APPLICATIONS

Single Li-Ion 2.5V/600mA Regulator with 1.8MHz External Synchronization and External MODE

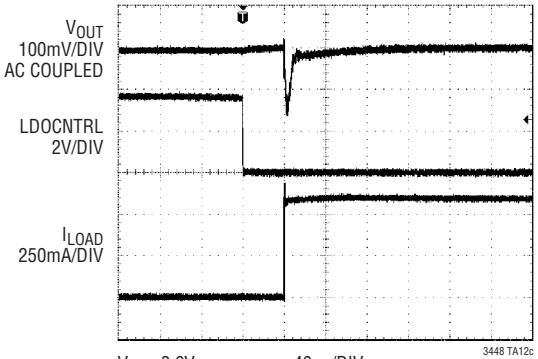


Load Step



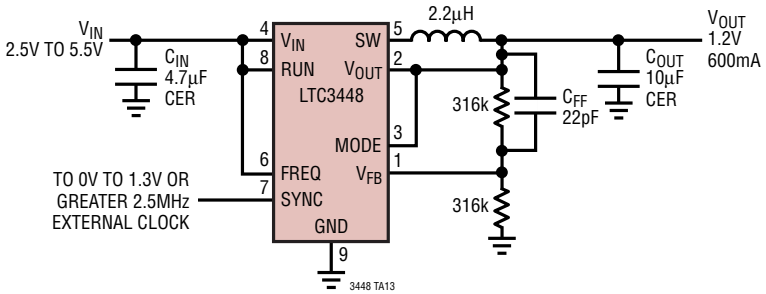
VIN = 3.6V
VOUT = 2.5V
ILOAD = 100µA TO 300mA
40µs/DIV

Load Step



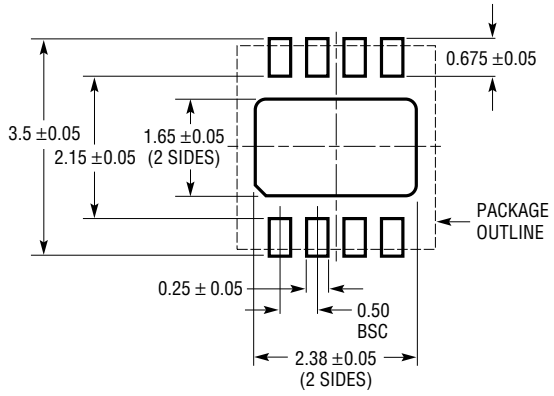
VIN = 3.6V
VOUT = 2.5V
ILOAD = 100µA TO 600mA
40µs/DIV

Single Li-Ion 1.2V/600mA Regulator with 2.5MHz External Synchronization

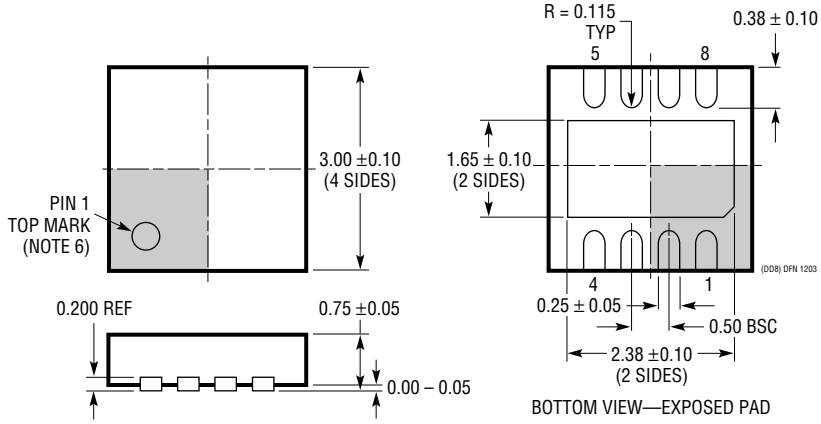


PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

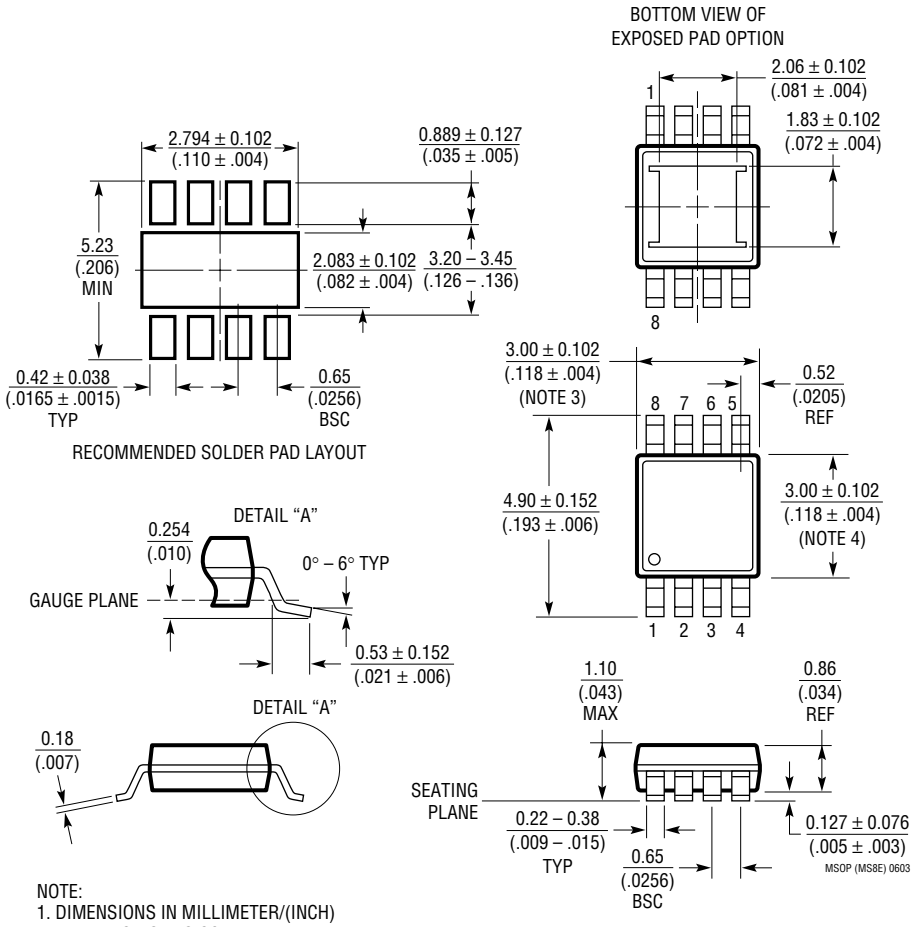


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MS8E Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1662)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1616	500mA (I_{OUT}), 1.4MHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN} = 3.6V to 25V, $V_{OUT} \geq$ 1.25V, I_Q = 1.9mA, I_{SD} = <1µA, ThinSOT Package
LT1776	500mA (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	90% Efficiency, V_{IN} = 7.4V to 40V, $V_{OUT} \geq$ 1.24V, I_Q = 3.2mA, I_{SD} = 30µA, N8, S8 Packages
LTC1877	600mA (I_{OUT}), 550kHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.7V to 10V, $V_{OUT} \geq$ 0.8V, I_Q = 10µA, I_{SD} = <1µA, MS8 Package
LTC1879	1.2A (I_{OUT}), 550kHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.7V to 10V, $V_{OUT} \geq$ 0.8V, I_Q = 15µA, I_{SD} = <1µA, TSSOP-16 Package
LTC3403	600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter with Bypass Transistor	96% Efficiency, V_{IN} = 2.5V to 5.5V, V_{OUT} = Dynamically Adjustable, I_Q = 20µA, I_{SD} = <1µA, DFN Package
LTC3405/LTC3405A	300mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN} = 2.5V to 5.5V, $V_{OUT} \geq$ 0.8V, I_Q = 20µA, I_{SD} = <1µA, ThinSOT Package
LTC3406	600mA (I_{OUT}), 1.5MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN} = 2.5V to 5.5V, $V_{OUT} \geq$ 0.6V, I_Q = 20µA, I_{SD} = <1µA, ThinSOT Package
LTC3406B-2	600mA (I_{OUT}), 2.25MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN} = 2.5V to 5.5V, $V_{OUT} \geq$ 0.6V, I_Q = 300µA, I_{SD} = <1µA, ThinSOT Package
LTC3407/LTC3407-2	Dual 600mA/800mA (I_{OUT}), 1.5MHz/2.25MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN} = 2.5V to 5.5V, $V_{OUT} \geq$ 0.6V, I_Q = 40µA, I_{SD} = <1µA, MS10, DFN Packages
LTC3409	600mA Low V_{IN} Buck Regulator	95% Efficiency, V_{IN} = 1.6V to 5.5V, I_Q = 65µA I_{SD} = <1µA, DFN Package
LTC3411	1.25A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.5V to 5.5V, $V_{OUT} \geq$ 0.8V, I_Q = 60µA, I_{SD} = <1µA, MS Package
LTC3412	2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN} = 2.5V to 5.5V, $V_{OUT} \geq$ 0.8V, I_Q = 60µA, I_{SD} = <1µA, TSSOP-16E Package
LTC3440	600mA (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN} = 2.5V to 5.5V, $V_{OUT} \geq$ 2.5V, I_Q = 25µA, I_{SD} = <1µA, MS Package
LTC3441	1.2A (I_{OUT}), 1MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN} = 2.4V to 5.5V, $V_{OUT} \geq$ 2.4V to 5.25V, I_Q = 25µA, I_{SD} = <1µA, DFN Package
LTC3442	1.2A (I_{OUT}), 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN} = 2.4V to 5.5V, $V_{OUT} \geq$ 2.4V to 5.25V, I_Q = 35µA, I_{SD} = <1µA, DFN Package
LTC3443	1.2A (I_{OUT}), 600kHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN} = 2.4V to 5.5V, $V_{OUT} \geq$ 2.4V to 5.25V, I_Q = 28µA, I_{SD} = <1µA, DFN Package

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