

# Intel<sup>®</sup> Xeon<sup>®</sup> Processor 7200 Series and 7300 Series

Datasheet

---

*September 2008*

**Notice:** The Intel<sup>®</sup> Xeon<sup>®</sup> Processor 7200 Series and 7300 Series may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.



INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The Intel® Xeon® Processor 7200 Series and 7300 Series may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com>.

Intel, Pentium, Intel Xeon, Intel SpeedStep, Intel Core, and Intel Virtualization Technology, are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

Intel® 64 requires a computer system with a processor, chipset, BIOS, OS, device drivers and applications enabled for Intel® 64. Processor will not operate (including 32-bit operation) without an Intel® 64-enabled BIOS. Performance will vary depending on your hardware and software configurations. Intel® 64-enabled OS, BIOS, device drivers and applications may not be available. Check with your vendor for more information.

\* Other names and brands may be claimed as the property of others.

Copyright © 2006 - 2008, Intel Corporation



# Contents

---

|          |                                                                   |     |
|----------|-------------------------------------------------------------------|-----|
| <b>1</b> | <b>Introduction</b>                                               | 9   |
| 1.1      | Terminology                                                       | 11  |
| 1.2      | State of Data                                                     | 13  |
| 1.3      | References                                                        | 13  |
| <b>2</b> | <b>Electrical Specifications</b>                                  | 15  |
| 2.1      | Front Side Bus and GTLREF                                         | 15  |
| 2.2      | Decoupling Guidelines                                             | 15  |
| 2.2.1    | VCC Decoupling                                                    | 16  |
| 2.2.2    | VTT Decoupling                                                    | 16  |
| 2.2.3    | Front Side Bus AGTL+ Decoupling                                   | 16  |
| 2.3      | Front Side Bus Clock (BCLK[1:0]) and Processor Clocking           | 16  |
| 2.3.1    | Front Side Bus Frequency Select Signals (BSEL[2:0])               | 17  |
| 2.3.2    | PLL Power Supply                                                  | 17  |
| 2.4      | Voltage Identification (VID)                                      | 17  |
| 2.5      | Reserved, Unused, or Test Signals                                 | 20  |
| 2.6      | Front Side Bus Signal Groups                                      | 20  |
| 2.7      | CMOS Asynchronous and Open Drain Asynchronous Signals             | 22  |
| 2.8      | Test Access Port (TAP) Connection                                 | 22  |
| 2.9      | Mixing Processors                                                 | 23  |
| 2.10     | Absolute Maximum and Minimum Ratings                              | 23  |
| 2.11     | Processor DC Specifications                                       | 24  |
| 2.11.1   | Flexible Motherboard Guidelines (FMB)                             | 25  |
| 2.11.2   | Platform Environmental Control Interface (PECI) DC Specifications | 35  |
| 2.11.3   | VCC Overshoot Specification                                       | 37  |
| 2.11.4   | AGTL+ FSB Specifications                                          | 38  |
| 2.12     | Front Side Bus AC Specifications                                  | 40  |
| 2.13     | Processor AC Timing Waveforms                                     | 45  |
| <b>3</b> | <b>Mechanical Specifications</b>                                  | 57  |
| 3.1      | Package Mechanical Drawing                                        | 57  |
| 3.2      | Processor Component Keepout Zones                                 | 60  |
| 3.3      | Package Loading Specifications                                    | 66  |
| 3.4      | Package Handling Guidelines                                       | 67  |
| 3.5      | Package Insertion Specifications                                  | 67  |
| 3.6      | Processor Mass Specifications                                     | 67  |
| 3.7      | Processor Materials                                               | 67  |
| 3.8      | Processor Markings                                                | 68  |
| 3.9      | Processor Pin-Out Coordinates                                     | 69  |
| <b>4</b> | <b>Pin Listing</b>                                                | 71  |
| 4.1      | Pin Assignments                                                   | 71  |
| 4.1.1    | Pin Listing by Pin Name                                           | 71  |
| 4.1.2    | Pin Listing by Pin Number                                         | 79  |
| <b>5</b> | <b>Signal Definitions</b>                                         | 87  |
| 5.1      | Signal Definitions                                                | 87  |
| <b>6</b> | <b>Thermal Specifications</b>                                     | 95  |
| 6.1      | Package Thermal Specifications                                    | 95  |
| 6.1.1    | Thermal Specifications                                            | 95  |
| 6.1.2    | Thermal Metrology                                                 | 102 |
| 6.2      | Processor Thermal Features                                        | 103 |
| 6.2.1    | Thermal Monitor Features                                          | 103 |
| 6.2.2    | Thermal Monitor                                                   | 103 |



|          |                                                                          |            |
|----------|--------------------------------------------------------------------------|------------|
| 6.2.3    | Thermal Monitor 2 .....                                                  | 104        |
| 6.2.4    | On-Demand Mode .....                                                     | 105        |
| 6.2.5    | PROCHOT# Signal .....                                                    | 106        |
| 6.2.6    | FORCEPR# Signal .....                                                    | 106        |
| 6.2.7    | THERMTRIP# Signal .....                                                  | 106        |
| 6.3      | Platform Environment Control Interface (PECI) .....                      | 107        |
| 6.3.1    | Introduction .....                                                       | 107        |
| 6.3.2    | PECI Specifications .....                                                | 108        |
| <b>7</b> | <b>Features .....</b>                                                    | <b>111</b> |
| 7.1      | Power-On Configuration Options .....                                     | 111        |
| 7.2      | Clock Control and Low Power States .....                                 | 111        |
| 7.2.1    | Normal State .....                                                       | 112        |
| 7.2.2    | HALT or Extended HALT State .....                                        | 112        |
| 7.2.3    | Stop-Grant State .....                                                   | 114        |
| 7.2.4    | Extended HALT Snoop or HALT Snoop State, Stop Grant<br>Snoop State ..... | 115        |
| 7.3      | Enhanced Intel SpeedStep® Technology .....                               | 115        |
| 7.4      | System Management Bus (SMBus) Interface .....                            | 116        |
| 7.4.1    | SMBus Device Addressing .....                                            | 117        |
| 7.4.2    | PIROM and Scratch EEPROM Supported SMBus Transactions .....              | 118        |
| 7.4.3    | Processor Information ROM (PIROM) .....                                  | 119        |
| 7.4.4    | Checksums .....                                                          | 137        |
| 7.4.5    | Scratch EEPROM .....                                                     | 137        |
| <b>8</b> | <b>Boxed Processor Specifications .....</b>                              | <b>139</b> |
| 8.1      | Introduction .....                                                       | 139        |
| 8.2      | Thermal Specifications .....                                             | 139        |
| 8.2.1    | Boxed Processor Cooling Requirements .....                               | 139        |
| <b>9</b> | <b>Debug Tools Specifications .....</b>                                  | <b>141</b> |
| 9.1      | Debug Port System Requirements .....                                     | 141        |
| 9.2      | Logic Analyzer Interface (LAI) .....                                     | 141        |
| 9.2.1    | Mechanical Considerations .....                                          | 141        |
| 9.2.2    | Electrical Considerations .....                                          | 142        |



## Figures

|      |                                                                                                                  |     |
|------|------------------------------------------------------------------------------------------------------------------|-----|
| 2-1  | Quad-Core Intel® Xeon® L7345 Processor Load Current versus Time .....                                            | 27  |
| 2-2  | Dual-Core Dual-Core Intel® Xeon® Processor 7200 Series Load Current versus Time.....                             | 28  |
| 2-3  | Quad-Core Intel® Xeon® Processor 7200 Series and 7300 Series Load Current versus Time28                          |     |
| 2-4  | Quad-Core <b>Intel® Xeon® X7350 Processor</b> Load Current versus Time .....                                     | 29  |
| 2-5  | Quad-Core Intel® Xeon® Processor 7200 Series and 7300 Series VCC Static and Transient Tolerance Load Lines ..... | 31  |
| 2-6  | Quad-Core <b>Intel® Xeon® X7350 Processor</b> VCC Static and Transient Tolerance Load Lines.....                 | 32  |
| 2-7  | Quad-Core Intel® Xeon® L7345 Processor V <sub>CC</sub> Static and Transient Tolerance Load Lines.....            | 33  |
| 2-8  | Dual-Core Intel® Xeon® Processor 7200 Series VCC Static and Transient Tolerance Load Lines .....                 | 34  |
| 2-9  | Input Device Hysteresis .....                                                                                    | 37  |
| 2-10 | VCC Overshoot Example Waveform.....                                                                              | 38  |
| 2-11 | Electrical Test Circuit .....                                                                                    | 46  |
| 2-12 | TCK Clock Waveform .....                                                                                         | 46  |
| 2-13 | Differential Clock Waveform .....                                                                                | 47  |
| 2-14 | Differential Clock Crosspoint Specification .....                                                                | 47  |
| 2-15 | BCLK Waveform at Processor Pad and Pin .....                                                                     | 48  |
| 2-16 | FSB Common Clock Valid Delay Timing Waveform .....                                                               | 48  |
| 2-17 | FSB Source Synchronous 2X (Address) Timing Waveform .....                                                        | 49  |
| 2-18 | FSB Source Synchronous 4X (Data) Timing Waveform .....                                                           | 50  |
| 2-19 | TAP Valid Delay Timing Waveform .....                                                                            | 51  |
| 2-20 | Test Reset (TRST#), Async GTL+ Input, and PROCHOT# Timing Waveform .....                                         | 51  |
| 2-21 | THERMTRIP# Power Down Sequence .....                                                                             | 51  |
| 2-22 | SMBus Timing Waveform.....                                                                                       | 52  |
| 2-23 | SMBus Valid Delay Timing Waveform .....                                                                          | 52  |
| 2-24 | Voltage Sequence Timing Requirements .....                                                                       | 53  |
| 2-25 | FERR#/PBE# Valid Delay Timing .....                                                                              | 54  |
| 2-26 | VID Step Timings .....                                                                                           | 54  |
| 2-27 | VID Step Times and Vcc Waveforms .....                                                                           | 55  |
| 3-1  | Processor Package Assembly Sketch .....                                                                          | 57  |
| 3-2  | Processor Package Drawing (Sheet 1 of 2) .....                                                                   | 58  |
| 3-3  | Processor Package Drawing (Sheet 2 of 2) .....                                                                   | 59  |
| 3-4  | Top Side Board Keepout Zones (Part 1) .....                                                                      | 61  |
| 3-5  | Top Side Board Keepout Zones (Part 2) .....                                                                      | 62  |
| 3-6  | Bottom Side Board Keepout Zones.....                                                                             | 63  |
| 3-7  | Board Mounting-Hole Keepout Zones .....                                                                          | 64  |
| 3-8  | Volumetric Height Keep-Ins .....                                                                                 | 65  |
| 3-9  | Processor Topside Markings .....                                                                                 | 68  |
| 3-10 | Processor Bottom-Side Markings .....                                                                             | 68  |
| 3-11 | Processor Pin-Out Coordinates, Top View .....                                                                    | 69  |
| 6-1  | Quad-Core Intel® Xeon® E7300 Processor Thermal Profile .....                                                     | 97  |
| 6-2  | Quad-Core Intel® Xeon® X7350 Processor Thermal Profile.....                                                      | 98  |
| 6-3  | Quad-Core Intel® Xeon® L7345 Processor Thermal Profile .....                                                     | 100 |
| 6-4  | Dual-Core Intel® Xeon® Processor 7200 Series Thermal Profile .....                                               | 101 |
| 6-5  | Case Temperature (TCASE) Measurement Location .....                                                              | 103 |
| 6-6  | Thermal Monitor 2 Frequency and Voltage Ordering .....                                                           | 105 |
| 6-7  | PECI Topology .....                                                                                              | 107 |



|     |                                                                |     |
|-----|----------------------------------------------------------------|-----|
| 6-8 | Conceptual Fan Control Diagram For a PECI-Based Platform ..... | 108 |
| 7-1 | Stop Clock State Machine.....                                  | 114 |
| 7-2 | Logical Schematic of SMBus Circuitry.....                      | 117 |

## Tables

|      |                                                                           |     |
|------|---------------------------------------------------------------------------|-----|
| 1-1  | Quad-Core Intel® Xeon® Processor 7300 Series Processor Features .....     | 10  |
| 1-2  | Dual-Core Intel® Xeon® Processor 7200 Series Processor Features .....     | 10  |
| 2-1  | Core Frequency to FSB Multiplier Configuration .....                      | 17  |
| 2-2  | BSEL[2:0] Frequency Table .....                                           | 17  |
| 2-3  | Voltage Identification Definition .....                                   | 19  |
| 2-4  | FSB Signal Groups .....                                                   | 21  |
| 2-5  | AGTL+ Signal Description Table .....                                      | 22  |
| 2-6  | Non AGTL+ Signal Description Table.....                                   | 22  |
| 2-7  | Signal Reference Voltages.....                                            | 22  |
| 2-8  | Processor Absolute Maximum Ratings .....                                  | 23  |
| 2-9  | Voltage and Current Specifications .....                                  | 25  |
| 2-10 | VCC Static and Transient Tolerance .....                                  | 30  |
| 2-11 | AGTL+ Signal Group DC Specifications.....                                 | 34  |
| 2-12 | CMOS Signal Input/Output Group DC Specifications.....                     | 35  |
| 2-13 | Open Drain Signal Group DC Specifications .....                           | 35  |
| 2-14 | SMBus Signal Group DC Specifications.....                                 | 35  |
| 2-15 | PECI DC Electrical Limits.....                                            | 36  |
| 2-16 | VCC Overshoot Specifications .....                                        | 37  |
| 2-17 | AGTL+ Bus Voltage Definitions .....                                       | 39  |
| 2-18 | FSB Differential BCLK Specifications .....                                | 39  |
| 2-19 | Front Side Bus Differential Clock AC Specifications .....                 | 40  |
| 2-20 | Front Side Bus Common Clock AC Specifications .....                       | 40  |
| 2-21 | FSB Source Synchronous AC Specifications.....                             | 41  |
| 2-22 | Miscellaneous GTL+ AC Specifications.....                                 | 42  |
| 2-23 | Front Side Bus AC Specifications (Reset Conditions) .....                 | 42  |
| 2-24 | TAP Signal Group AC Specifications .....                                  | 42  |
| 2-25 | VID Signal Group AC Specifications .....                                  | 44  |
| 2-26 | SMBus Signal Group AC Specifications .....                                | 44  |
| 3-1  | Processor Loading Specifications .....                                    | 66  |
| 3-2  | Package Handling Guidelines .....                                         | 67  |
| 3-3  | Processor Materials .....                                                 | 67  |
| 4-1  | Pin Listing by Pin Name .....                                             | 71  |
| 4-2  | Pin Listing by Pin Number .....                                           | 79  |
| 5-1  | Signal Definitions.....                                                   | 87  |
| 6-1  | Quad-Core Intel® Xeon® E7300 Processor Thermal Specifications .....       | 96  |
| 6-2  | Quad-Core Intel® Xeon® E7300 Processor Thermal Profile Table .....        | 97  |
| 6-3  | Quad-Core Intel® Xeon® X7350 Processor Thermal Specifications .....       | 98  |
| 6-4  | Quad-Core Intel® Xeon® X7350 Processor Thermal Profile Table .....        | 99  |
| 6-5  | Quad-Core Intel® Xeon® L7345 Processor Thermal Specifications .....       | 99  |
| 6-6  | Quad-Core Intel® Xeon® L7345 Processor Thermal Profile.....               | 100 |
| 6-7  | Dual-Core Intel® Xeon® Processor 7200 Series Thermal Specifications ..... | 101 |
| 6-8  | Dual-Core Intel® Xeon® Processor 7200 Series Thermal Profile.....         | 102 |
| 6-9  | BREQ# signal assertion during power on.....                               | 109 |
| 6-10 | PECI Address assigned to processor .....                                  | 109 |
| 6-11 | GetTemp0() and GetTemp1() Error Codes .....                               | 110 |
| 7-1  | Power-On Configuration Option pins .....                                  | 111 |



|     |                                               |     |
|-----|-----------------------------------------------|-----|
| 7-2 | Extended HALT Maximum Power.....              | 113 |
| 7-3 | Memory Device SMBus Addressing.....           | 118 |
| 7-4 | Read Byte SMBus Packet .....                  | 118 |
| 7-5 | Write Byte SMBus Packet .....                 | 118 |
| 7-6 | Processor Information ROM Data Sections ..... | 119 |
| 7-7 | 128 Byte ROM Checksum Values .....            | 137 |



## Revision History

---

| Document Number | Revision | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Date           |
|-----------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| 318080          | -001     | <ul style="list-style-type: none"><li>Initial Release</li></ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | September 2007 |
| 318080          | -002     | <ul style="list-style-type: none"><li>Changed Product Name to Intel® Xeon® Processor 7200 Series and 7300 Series</li><li>Updated Power Specifications</li><li>The character byte ordering was reversed for the following fields:<br/>SQNUM: S-Spec QDF Number<br/>PREV: Package Revision<br/>PPN: Processor Part Number</li><li>Updated the Processor Mechanical drawings to add an optional small shallow depression in the top right-hand side corner of the integrated heat spreader (IHS). This feature, which supports anti-mixing, may be seen on some processor packages. There are no major electrical, mechanical, or thermal differences in the form, fit or function of the processors with or without this feature.</li><li>Updated PROC_ID[1:0] Definition</li></ul> | September 2008 |

### §



# 1 Introduction

---

## ALL INFORMATION IN THIS DOCUMENT IS SUBJECT TO CHANGE.

The Intel® Xeon® Processor 7200 Series and 7300 Series are multi-processor servers utilizing four Intel® Core™ microarchitecture cores. These processors are based on Intel's 65 nanometer process technology combining high performance with the power efficiencies of a low-power microarchitecture. The Quad-Core Intel® Xeon® 7300 Series consists of two die, each die containing two processor cores. The Dual-Core Intel® Xeon® 7200 Series consists of two die, each die containing one processor core. All processors maintain the tradition of compatibility with IA-32 software. Some key features include on-die, 64 KB Level 1 instruction data caches per die and 2x4MB shared Level 2 cache with Advanced Transfer Cache Architecture. The processor's Data Prefetch Logic speculatively fetches data to the L2 cache before an L1 cache requests occurs, resulting in reduced bus cycle penalties and improved performance. The 1066 MHz Front Side Bus (FSB) is a quad-pumped bus running off a 266 MHz system clock making 8.5 GBytes per second data transfer rates possible. The Quad-Core Intel® Xeon® X7350 processor offers higher clock frequencies than the other Quad-Core Intel® Xeon® Processor 7300 Series for platforms that are targeted for the performance optimized segment. The Quad-Core Intel® Xeon® L7345 Processor is a lower voltage, lower power processor.

Enhanced thermal and power management capabilities are implemented including Thermal Monitor (TM1), Thermal Monitor 2 (TM2) and Enhanced Intel SpeedStep® Technology. TM1 and TM2 provide efficient and effective cooling in high temperature situations. Enhanced Intel SpeedStep Technology allows trade-offs to be made between performance and power consumption. This may lower average power consumption (in conjunction with OS support).

The Intel® Xeon® Processor 7200 Series and 7300 Series features include Advanced Dynamic Execution, enhanced floating point and multi-media units, Streaming SIMD Extensions 2 (SSE2) and Streaming SIMD Extensions 3 (SSE3). Advanced Dynamic Execution improves speculative execution and branch prediction internal to the processor. The floating point and multi-media units include 128-bit wide registers and a separate register for data movement. SSE3 instructions provide highly efficient double-precision floating point, SIMD integer, and memory management operations.

The Intel® Xeon® Processor 7200 Series and 7300 Series support Intel® 64 as an enhancement to Intel's IA-32 architecture. This enhancement allows the processor to execute operating systems and applications written to take advantage of the 64-bit extension technology. Further details on Intel® 64 Technology and its programming model can be found in the Intel® 64 and IA-32 Architectures Software Developer's Manual.

In addition, the Intel® Xeon® Processor 7200 Series and 7300 Series support the Execute Disable Bit functionality. When used in conjunction with a supporting operating system, Execute Disable allows memory to be marked as executable or non executable. This feature can prevent some classes of viruses that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. Further details on Execute Disable can be found at

<http://www.intel.com/cd/ids/developer/asmo-na/eng/149308.htm>.



The Intel® Xeon® Processor 7200 Series and 7300 Series support Intel® Virtualization Technology for hardware-assisted virtualization within the processor. Intel Virtualization Technology is a set of hardware enhancements that can improve virtualization solutions. Intel Virtualization Technology is used in conjunction with Virtual Machine Monitor software enabling multiple, independent software environments inside a single platform. Further details on Intel Virtualization Technology can be found at <http://developer.intel.com/technology/vt>.

The Intel® Xeon® Processor 7200 Series and 7300 Series are intended for high performance multi-processor server systems. The processors support a Multi Independent Bus (MIB) architecture with one processor on each bus. The MIB architecture provides improved performance by allowing increased FSB speeds and bandwidth. All versions of the Intel® Xeon® Processor 7200 Series and 7300 Series will include manageability features. Components of the manageability features include an OEM EEPROM and Processor Information ROM which are accessed through an SMBus interface and contain information relevant to the particular processor and system in which it is installed. The Intel® Xeon® Processor 7200 Series and 7300 Series is packaged in a 604-pin Flip Chip Micro Pin Grid Array (FC-mPGA6) package and utilizes a surface-mount Zero Insertion Force (ZIF) mPGA604 socket. The Intel® Xeon® Processor 7200 Series and 7300 Series support 40-bit addressing.

**Table 1-1. Quad-Core Intel® Xeon® Processor 7300 Series Processor Features**

| # of Processor Cores | L1 Cache per core               | L2 Advanced Transfer Cache                      | Front Side Bus Frequency | Package  |
|----------------------|---------------------------------|-------------------------------------------------|--------------------------|----------|
| 4                    | 32 KB instruction<br>32 KB data | 4M Shared L2<br>Cache per die<br>8M Total Cache | 1066 MHz                 | FC-mPGA6 |

**Table 1-2. Dual-Core Intel® Xeon® Processor 7200 Series Processor Features**

| # of Processor Cores | L1 Cache per core               | L2 Advanced Transfer Cache            | Front Side Bus Frequency | Package  |
|----------------------|---------------------------------|---------------------------------------|--------------------------|----------|
| 2                    | 32 KB instruction<br>32 KB data | 4M L2 Cache per die<br>8M Total Cache | 1066 MHz                 | FC-mPGA6 |

Intel® Xeon® Processor 7200 Series and 7300 Series-based platforms implement independent core voltage ( $V_{CC}$ ) power planes for each processor. FSB termination voltage ( $V_{TT}$ ) is shared and must connect to all FSB agents. The processor core voltage utilizes power delivery guidelines specified by VRM/EVRD 11.0 and its associated load line (see *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines* for further details). VRM/EVRD 11.0 will support the power requirements of all frequencies of the processors including Flexible Motherboard Guidelines (FMB) (see [Section 2.11.1](#)). Refer to the appropriate platform design guidelines for implementation details.

The Intel® Xeon® Processor 7200 Series and 7300 Series supports 1066 MHz Front Side Bus operation. The FSB utilizes a split-transaction, deferred reply protocol and Source-Synchronous Transfer (SST) of address and data to improve performance. The processor transfers data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a 'double-clocked' or a 2X address bus. In addition, the Request Phase completes in one clock cycle. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 8.5 GBytes per second. The FSB is also used to deliver interrupts.



Signals on the FSB use Assisted Gunning Transceiver Logic (AGTL+) level voltages. [Section 2.1](#) contains the electrical specifications of the FSB while implementation details are fully described in the appropriate platform design guidelines (refer to [Section 1.3](#)).

## 1.1 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating a signal is in the asserted state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as address or data), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

Commonly used terms are explained here for clarification:

- **Enhanced Intel SpeedStep® Technology** — Enhanced Intel SpeedStep® Technology is the next generation implementation of the Geyserville technology which extends power management capabilities of servers.
- **FC-mPGA6** — The Intel® Xeon® Processor 7200 Series and 7300 Series package is available in a Flip-Chip Micro Pin Grid Array 6 package, consisting of a processor core mounted on a pinned substrate with an integrated heat spreader (IHS). This packaging technology employs a 1.27 mm [0.05 in] pitch for the substrate pins.
- **mPGA604** — The Intel® Xeon® Processor 7200 Series and 7300 Series package mates with the system board through this surface mount, 604-pin, zero insertion force (ZIF) socket.
- **Processor core** — Processor core with integrated L1 cache. L2 cache and system bus interface are shared between the two cores on the die. All AC timing and signal integrity specifications are at the pads of the processor die.
- **FSB (Front Side Bus)** — The electrical interface that connects the processor to the chipset. Also referred to as the processor system bus or the system bus. All memory and I/O transactions as well as interrupt messages pass between the processor and chipset over the FSB.
- **Multi Independent Bus (MIB)** — A front side bus architecture with one processor on each bus, rather than a FSB shared between multiple processor agents. The MIB architecture provides improved performance by allowing increased FSB speeds and bandwidth.
- **Flexible Motherboard Guidelines (FMB)** — Are estimates of the maximum values the Intel® Xeon® Processor 7200, 7300 Series will have over certain time periods. The values are only estimates and actual specifications for future processors may differ.
- **Functional Operation** — Refers to the normal operating conditions in which all processor specifications, including DC, AC, FSB, signal quality, mechanical and thermal are satisfied.
- **Storage Conditions** — Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor pins should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.



- **Processor Information ROM (PIROM)** — A memory device located on the processor and accessible via the System Management Bus (SMBus) which contains information regarding the processor's features. This device is shared with the Scratch EEPROM, is programmed during manufacturing, and is write-protected.
- **Scratch EEPROM (Electrically Erasable, Programmable Read-Only Memory)** — A memory device located on the processor and addressable via the SMBus which can be used by the OEM to store information useful for system management.
- **SMBus** — System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system. It is based on the principals of the operation of the I<sup>2</sup>C\* two-wire serial bus from Phillips Semiconductor.

**Note:** I<sup>2</sup>C is a two-wire communications bus/protocol developed by Phillips. SMBus is a subset of the I<sup>2</sup>C bus/protocol and was developed by Intel. Implementations of the I<sup>2</sup>C bus/protocol or the SMBus bus/protocol may require licenses from various entities, including Phillips Electronics N.V. and North American Phillips Corporation.

- **Priority Agent** – The priority agent is the host bridge to the processor and is typically known as the chipset.
- **Symmetric Agent** – A symmetric agent is a processor which shares the same I/O subsystem and memory array, and runs the same operating system as another processor in a system. Systems using symmetric agents are known as Symmetric Multiprocessing (SMP) systems.
- **Integrated Heat Spreader (IHS)** – A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **Thermal Design Power** – Processor thermal solutions should be designed to meet this target. It is the highest expected sustainable power while running known power intensive real applications. TDP is not the maximum power that the processor can dissipate.
- **Intel® 64** – Instruction set architecture and programming environment of Intel's 64-bit processors, which are a superset of and compatible with IA-32. This 64-bit instruction set architecture was formerly known as IA-32 with EM64T or Intel® EM64T.
- **Platform Environment Control Interface (PECI)** – A proprietary one-wire bus interface that provides a communication channel between Intel processor and chipset components to external thermal monitoring devices, for use in fan speed control. PECI communicates readings from the processor's Digital Thermal Sensors (DTS). The DTS replaces the thermal diode available in previous processors.
- **Intel® Virtualization Technology** – Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
- **VRM (Voltage Regulator Module)** – DC-DC converter built onto a module that interfaces with a card edge socket and supplies the correct voltage and current to the processor based on the logic state of the processor VID bits.
- **EVRD (Enterprise Voltage Regulator Down)** – DC-DC converter integrated onto the system board that provides the correct voltage and current to the processor based on the logic state of the processor VID bits.
- **V<sub>CC</sub>** – The processor core power supply.
- **V<sub>SS</sub>** – The processor ground.
- **V<sub>TT</sub>** – FSB termination voltage.



## 1.2 State of Data

This document contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel sales office that you have the latest datasheet before finalizing a design

## 1.3 References

Material and concepts available in the following documents may be beneficial when reading this document:

| Document                                                                                                                                                                                                                                                                                      | Document Number <sup>1</sup>                   | Notes |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|-------|
| AP-485, Intel® Processor Identification and the CPUID Instruction                                                                                                                                                                                                                             | 241618                                         | 1     |
| Intel® 64 and IA-32 Architectures Software Developer's Manual                                                                                                                                                                                                                                 |                                                | 1     |
| <ul style="list-style-type: none"> <li>Volume 1: Basic Architecture</li> <li>Volume 2A: Instruction Set Reference, A-M</li> <li>Volume 2B: Instruction Set Reference, N-Z</li> <li>Volume 3A: System Programming Guide Part 1</li> <li>Volume 3B: System Programming Guide, Part 2</li> </ul> | 253665<br>253666<br>253667<br>253668<br>253669 |       |
| IA-32 Intel® Architecture and Intel® 64 Software Developer's Manual Documentation Changes                                                                                                                                                                                                     | 252046                                         | 1     |
| IA-32 Intel® Architecture Optimization Reference Manual                                                                                                                                                                                                                                       | 248966                                         | 1     |
| Intel® Extended Memory 64 Technology                                                                                                                                                                                                                                                          |                                                | 1     |
| <ul style="list-style-type: none"> <li>Volume 1</li> <li>Volume 2</li> </ul>                                                                                                                                                                                                                  | 300834<br>300835                               |       |
| Intel® Virtualization Technology for IA-32 Processors (VT-x) Preliminary Specification                                                                                                                                                                                                        | C97063                                         | 1     |
| Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series Specification Update                                                                                                                                                                            | 318081                                         | 1     |
| Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines                                                                                                                                                                                            | 315889                                         | 1     |
| EPS12V Power Supply Design Guide: A Server system Infrastructure (SSI) Specification for Entry Chassis Power Supplies                                                                                                                                                                         |                                                | 2     |
| Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series Thermal / Mechanical Design Guide                                                                                                                                                               | 318086                                         | 1     |
| Intel® Xeon® Processor 7200 Series and 7300 Series Package Mechanical Models                                                                                                                                                                                                                  |                                                | 1     |
| mPGA604 Socket Design Guide                                                                                                                                                                                                                                                                   | 254239                                         | 1     |
| Intel® Xeon® Processor 7200 Series and 7300 Series Enabled Components (CEK) Thermal Models                                                                                                                                                                                                    |                                                | 1     |
| Intel® Xeon® Processor 7200 Series and 7300 Series Enabled Components (CEK) Mechanical Models                                                                                                                                                                                                 |                                                | 1     |
| Intel® Xeon® Processor 7200 Series and 7300 Series Boundary Scan Descriptive Language (BSDL) Model                                                                                                                                                                                            |                                                | 1     |

### Notes:

1. Document is available publicly at <http://developer.intel.com>.
2. Document available on [www.ssiforum.org](http://www.ssiforum.org).





## 2 Electrical Specifications

---

### 2.1 Front Side Bus and GTLREF

Most Intel® Xeon® Processor 7200 Series and 7300 Series FSB signals use Assisted Gunning Transceiver Logic (AGTL+) signaling technology. This technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. AGTL+ buffers are open-drain and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active PMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition. Platforms implement a termination voltage level for AGTL+ signals defined as  $V_{TT}$ . Because platforms implement separate power planes for each processor (and chipset), separate  $V_{CC}$  and  $V_{TT}$  supplies are necessary. This configuration allows for improved noise tolerance as processor frequency increases. Speed enhancements to data and address buses have made signal integrity considerations and platform design methods even more critical than with previous processor families. Design guidelines for the processor FSB are detailed in the appropriate platform design guidelines (refer to [Section 1.3](#)).

The AGTL+ inputs require reference voltages (GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID and GTLREF\_ADD\_END) which are used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF\_DATA\_MID and GTLREF\_DATA\_END are used for the 4X front side bus signaling group and GTLREF\_ADD\_MID and GTLREF\_ADD\_END are used for the 2X and common clock front side bus signaling groups. GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END must be generated on the baseboard (See [Table 2-17](#) for GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID and GTLREF\_ADD\_END specifications). Refer to the applicable platform design guidelines for details. Termination resistors ( $R_{TT}$ ) for AGTL+ signals are provided on the processor silicon and are terminated to  $V_{TT}$ . The on-die termination resistors are always enabled on the processor to control reflections on the transmission line. Intel chipsets also provide on-die termination, thus eliminating the need to terminate the bus on the baseboard for most AGTL+ signals.

Some FSB signals do not include on-die termination ( $R_{TT}$ ) and must be terminated on the baseboard. See [Table 2-4](#) and [Table 2-6](#) for details regarding these signals.

The AGTL+ bus depends on incident wave switching. Therefore, timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the FSB, including trace lengths, is highly recommended when designing a system. Contact your Intel Field Representative to obtain the processor signal integrity models, which includes buffer and package models.

### 2.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Larger bulk storage (CBULK), such as electrolytic capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. Care must be taken in the baseboard design to ensure that the voltage provided to the processor

remains within the specifications listed in [Table 2-9](#). Failure to do so can result in timing violations or reduced lifetime of the component. For further information and guidelines, refer to the appropriate platform design guidelines.

### 2.2.1 $V_{CC}$ Decoupling

$V_{CC}$  regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR). Bulk decoupling must be provided on the baseboard to handle large current swings. The power delivery solution must ensure the voltage and current specifications are met (as defined in [Table 2-9](#)). For further information regarding power delivery, decoupling and layout guidelines, refer to the appropriate platform design guidelines.

### 2.2.2 $V_{TT}$ Decoupling

Bulk decoupling must be provided on the baseboard. Decoupling solutions must be sized to meet the expected load. To ensure optimal performance, various factors associated with the power delivery solution must be considered including regulator type, power plane and trace sizing, and component placement. A conservative decoupling solution consists of a combination of low ESR bulk capacitors and high frequency ceramic capacitors. For further information regarding power delivery, decoupling and layout guidelines, refer to the appropriate platform design guidelines.

### 2.2.3 Front Side Bus AGTL+ Decoupling

The processor integrates signal termination on the die, as well as a portion of the required high frequency decoupling capacitance on the processor package. However, additional high frequency capacitance must be added to the baseboard to properly decouple the return currents from the FSB. Bulk decoupling must also be provided by the baseboard for proper AGTL+ bus operation. Decoupling guidelines are described in the appropriate platform design guidelines.

## 2.3 Front Side Bus Clock (BCLK[1:0]) and Processor Clocking

BCLK[1:0] directly controls the FSB interface speed as well as the core frequency of the processor. As in previous processor generations, the processor core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier is set during manufacturing. The default setting is for the maximum speed of the processor.

The processor core frequency is configured during reset by using values stored internally during manufacturing. The stored value sets the highest bus fraction at which the particular processor can operate. If lower speeds are desired, the appropriate ratio can be configured via the CLOCK\_FLEX\_MAX Model Specific Register (MSR).

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK[1:0] input, with exceptions for spread spectrum clocking. Processor DC and AC specifications for the BCLK[1:0] inputs are provided in [Table 2-18](#) and [Table 2-19](#), respectively. These specifications must be met while also meeting signal integrity requirements as outlined in [Table 2-18](#). The processor utilizes differential clocks. [Table 2-1](#) contains processor core frequency to FSB multipliers and their corresponding core frequencies.

**Table 2-1. Core Frequency to FSB Multiplier Configuration**

| Core Frequency to FSB Multiplier | Core Frequency with 266 MHz FSB Clock | Notes      |
|----------------------------------|---------------------------------------|------------|
| 1/6                              | 1.60 GHz                              | 1, 2, 3, 4 |
| 1/7                              | 1.86 GHz                              | 1, 2, 3    |
| 1/8                              | 2.13 GHz                              | 1, 2, 3    |
| 1/9                              | 2.40 GHz                              | 1, 2, 3    |
| 1/10                             | 2.66 GHz                              | 1, 2, 3    |
| 1/11                             | 2.93 GHz                              | 1, 2, 3    |

**Notes:**

1. Individual processors operate only at or below the frequency marked on the package.
2. Listed frequencies are not necessarily committed production frequencies.
3. For valid processor core frequencies, refer to the *Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series Specification Update*.
4. The lowest bus ratio supported is 1/6.

### 2.3.1 Front Side Bus Frequency Select Signals (BSEL[2:0])

Upon power up, the FSB frequency is set to the maximum supported by the individual processor. BSEL[2:0] are CMOS outputs that are used to select the FSB frequency. Please refer to [Table 2-11](#) for DC specifications. [Table 2-2](#) defines the possible combinations of the signals and the frequency associated with each combination. The frequency is determined by the processor(s), chipset, and clock synthesizer. All FSB agents must operate at the same core and FSB frequency. See the appropriate platform design guidelines for further details.

**Table 2-2. BSEL[2:0] Frequency Table**

| BSEL2 | BSEL1 | BSEL0 | Bus Clock Frequency |
|-------|-------|-------|---------------------|
| 0     | 0     | 0     | 266 MHz             |
| 0     | 0     | 1     | Reserved            |
| 0     | 1     | 0     | Reserved            |
| 0     | 1     | 1     | Reserved            |
| 1     | 0     | 0     | Reserved            |
| 1     | 0     | 1     | Reserved            |
| 1     | 1     | 0     | Reserved            |
| 1     | 1     | 1     | Reserved            |

### 2.3.2 PLL Power Supply

An on-die PLL filter solution is implemented on the processor. The  $V_{CCPLL}$  input is used to provide power to the on chip PLL of the processor. Please refer to [Table 2-9](#) for DC specifications. Refer to the appropriate platform design guidelines for decoupling and routing guidelines.

## 2.4 Voltage Identification (VID)

The Voltage Identification (VID) specification for the processor is defined by the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines*. The voltage set by the VID signals is the reference VR output voltage to be delivered to the processor Vcc pins. VID signals are asynchronous CMOS



outputs. Please refer to [Table 2-12](#) for the DC specifications for these signals. A voltage range is provided in [Table 2-3](#) and changes with frequency. The specifications have been set such that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be calibrated during manufacturing such that two devices at the same core frequency may have different default VID settings. This is reflected by the VID range values provided in [Table 2-3](#).

The processor uses six voltage identification signals, VID[6:1], to support automatic selection of power supply voltages. [Table 2-3](#) specifies the voltage level corresponding to the state of VID[6:1]. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. The definition provided in [Table 2-3](#) is not related in any way to previous Intel® Xeon® processors or voltage regulator designs. If the processor socket is empty (VID[6:1] = 111111), or the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself. See the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines* for further details.

Although the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines* defines VID [7:0], VID 7 and VID 0 are not used on the Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series.

The Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage ( $V_{CC}$ ). This will represent a DC shift in the load line. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target core voltage. Transitions above the specified VID are not permitted. [Table 2-10](#) includes VID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in [Table 2-2](#) and [Table 2-3](#).

The VRM or EVRD utilized must be capable of regulating its output to the value defined by the new VID. DC specifications for dynamic VID transitions are included in [Table 2-9](#) and [Table 2-10](#), while AC specifications are included in [Table 2-25](#). Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines* for further details.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.



Table 2-3. Voltage Identification Definition

| HEX | VID6<br>400<br>mV | VID5<br>200<br>mV | VID4<br>100<br>mV | VID3<br>50<br>mV | VID2<br>25<br>mV | VID1<br>12.5<br>mV | V <sub>CC_MAX</sub> | HEX | VID6<br>400<br>mV | VID5<br>200<br>mV | VID4<br>100<br>mV | VID3<br>50<br>mV | VID2<br>25<br>mV | VID1<br>12.5<br>mV | V <sub>CC_MAX</sub> |
|-----|-------------------|-------------------|-------------------|------------------|------------------|--------------------|---------------------|-----|-------------------|-------------------|-------------------|------------------|------------------|--------------------|---------------------|
| 7A  | 1                 | 1                 | 1                 | 1                | 0                | 1                  | 0.8500              | 3C  | 0                 | 1                 | 1                 | 1                | 1                | 0                  | 1.2375              |
| 78  | 1                 | 1                 | 1                 | 1                | 0                | 0                  | 0.8625              | 3A  | 0                 | 1                 | 1                 | 1                | 0                | 1                  | 1.2500              |
| 76  | 1                 | 1                 | 1                 | 0                | 1                | 1                  | 0.8750              | 38  | 0                 | 1                 | 1                 | 1                | 0                | 0                  | 1.2625              |
| 74  | 1                 | 1                 | 1                 | 0                | 1                | 0                  | 0.8875              | 36  | 0                 | 1                 | 1                 | 0                | 1                | 1                  | 1.2750              |
| 72  | 1                 | 1                 | 1                 | 0                | 0                | 1                  | 0.9000              | 34  | 0                 | 1                 | 1                 | 0                | 1                | 0                  | 1.2875              |
| 70  | 1                 | 1                 | 1                 | 0                | 0                | 0                  | 0.9125              | 32  | 0                 | 1                 | 1                 | 0                | 0                | 1                  | 1.3000              |
| 6E  | 1                 | 1                 | 0                 | 1                | 1                | 1                  | 0.9250              | 30  | 0                 | 1                 | 1                 | 0                | 0                | 0                  | 1.3125              |
| 6C  | 1                 | 1                 | 0                 | 1                | 1                | 0                  | 0.9375              | 2E  | 0                 | 1                 | 0                 | 1                | 1                | 1                  | 1.3250              |
| 6A  | 1                 | 1                 | 0                 | 1                | 0                | 1                  | 0.9500              | 2C  | 0                 | 1                 | 0                 | 1                | 1                | 0                  | 1.3375              |
| 68  | 1                 | 1                 | 0                 | 1                | 0                | 0                  | 0.9625              | 2A  | 0                 | 1                 | 0                 | 1                | 0                | 1                  | 1.3500              |
| 66  | 1                 | 1                 | 0                 | 0                | 1                | 1                  | 0.9750              | 28  | 0                 | 1                 | 0                 | 1                | 0                | 0                  | 1.3625              |
| 64  | 1                 | 1                 | 0                 | 0                | 1                | 0                  | 0.9875              | 26  | 0                 | 1                 | 0                 | 0                | 1                | 1                  | 1.3750              |
| 62  | 1                 | 1                 | 0                 | 0                | 0                | 1                  | 1.0000              | 24  | 0                 | 1                 | 0                 | 0                | 1                | 0                  | 1.3875              |
| 60  | 1                 | 1                 | 0                 | 0                | 0                | 0                  | 1.0125              | 22  | 0                 | 1                 | 0                 | 0                | 0                | 1                  | 1.4000              |
| 5E  | 1                 | 0                 | 1                 | 1                | 1                | 1                  | 1.0250              | 20  | 0                 | 1                 | 0                 | 0                | 0                | 0                  | 1.4125              |
| 5C  | 1                 | 0                 | 1                 | 1                | 1                | 0                  | 1.0375              | 1E  | 0                 | 0                 | 1                 | 1                | 1                | 1                  | 1.4250              |
| 5A  | 1                 | 0                 | 1                 | 1                | 0                | 1                  | 1.0500              | 1C  | 0                 | 0                 | 1                 | 1                | 1                | 0                  | 1.4375              |
| 58  | 1                 | 0                 | 1                 | 1                | 0                | 0                  | 1.0625              | 1A  | 0                 | 0                 | 1                 | 1                | 0                | 1                  | 1.4500              |
| 56  | 1                 | 0                 | 1                 | 0                | 1                | 1                  | 1.0750              | 18  | 0                 | 0                 | 1                 | 1                | 0                | 0                  | 1.4625              |
| 54  | 1                 | 0                 | 1                 | 0                | 1                | 0                  | 1.0875              | 16  | 0                 | 0                 | 1                 | 0                | 1                | 1                  | 1.4750              |
| 52  | 1                 | 0                 | 1                 | 0                | 0                | 1                  | 1.1000              | 14  | 0                 | 0                 | 1                 | 0                | 1                | 0                  | 1.4875              |
| 50  | 1                 | 0                 | 1                 | 0                | 0                | 0                  | 1.1125              | 12  | 0                 | 0                 | 1                 | 0                | 0                | 1                  | 1.5000              |
| 4E  | 1                 | 0                 | 0                 | 1                | 1                | 1                  | 1.1250              | 10  | 0                 | 0                 | 1                 | 0                | 0                | 0                  | 1.5125              |
| 4C  | 1                 | 0                 | 0                 | 1                | 1                | 0                  | 1.1375              | 0E  | 0                 | 0                 | 0                 | 1                | 1                | 1                  | 1.5250              |
| 4A  | 1                 | 0                 | 0                 | 1                | 0                | 1                  | 1.1500              | 0C  | 0                 | 0                 | 0                 | 1                | 1                | 0                  | 1.5375              |
| 48  | 1                 | 0                 | 0                 | 1                | 0                | 0                  | 1.1625              | 0A  | 0                 | 0                 | 0                 | 1                | 0                | 1                  | 1.5500              |
| 46  | 1                 | 0                 | 0                 | 0                | 1                | 1                  | 1.1750              | 08  | 0                 | 0                 | 0                 | 1                | 0                | 0                  | 1.5625              |
| 44  | 1                 | 0                 | 0                 | 0                | 1                | 0                  | 1.1875              | 06  | 0                 | 0                 | 0                 | 0                | 1                | 1                  | 1.5750              |
| 42  | 1                 | 0                 | 0                 | 0                | 0                | 1                  | 1.2000              | 04  | 0                 | 0                 | 0                 | 0                | 1                | 0                  | 1.5875              |
| 40  | 1                 | 0                 | 0                 | 0                | 0                | 0                  | 1.2125              | 02  | 0                 | 0                 | 0                 | 0                | 0                | 1                  | 1.6000              |
| 3E  | 0                 | 1                 | 1                 | 1                | 1                | 1                  | 1.2250              | 00  | 0                 | 0                 | 0                 | 0                | 0                | 0                  | OFF <sup>1</sup>    |

**Notes:**

- When this VID pattern is observed, the voltage regulator output should be disabled.
- Shading denotes the expected VID range of the Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series.
- The VID range includes VID transitions that may be initiated by thermal events, assertion of the FORCEPR# signal (see [Section 6.2.3](#)), Extended HALT state transitions (see [Section 7.2.2](#)), or Enhanced Intel SpeedStep® Technology transitions (see [Section 7.3](#)). **The Extended HALT state must be enabled for the processor to remain within its specifications.**
- Once the VRM/EVRD is operating after power-up, if either the Output Enable signal is de-asserted or a specific VID off code is received, the VRM/EVRD must turn off its output (the output should go to high impedance) within 500 ms and latch off until power is cycled. Refer to Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines.

## 2.5 Reserved, Unused, or Test Signals

All Reserved signals must remain unconnected. Connection of these signals to  $V_{CC}$ ,  $V_{TT}$ ,  $V_{SS}$ , or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See [Section 4](#) for a pin listing of the processor and the location of all Reserved signals.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active high inputs, should be connected through a resistor to ground ( $V_{SS}$ ). Unused outputs can be left unconnected; however, this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within  $\pm 20\%$  of the impedance of the baseboard trace for FSB signals, unless otherwise noticed in the appropriate platform design guidelines. For unused AGTL+ input or I/O signals, use pull-up resistors of the same value as the on-die termination resistors ( $R_{TT}$ ). For details see [Table 2-24](#).

TAP, Asynchronous GTL+ inputs, and Asynchronous GTL+ outputs do not include on-die termination. Inputs and utilized outputs must be terminated on the baseboard. Unused outputs may be terminated on the baseboard or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. Signal termination for these signal types is discussed in the appropriate platform design guidelines.

For each processor socket, connect the TESTIN1 and TESTIN2 signals together, then terminate the net with a 51  $\Omega$  resistor to  $V_{TT}$ .

The TESTHI signal must be tied to the processor  $V_{TT}$  using a matched resistor, where a matched resistor has a resistance value within  $\pm 20\%$  of the impedance of the board transmission line traces. For example, if the trace impedance is 50  $\Omega$ , then a value between 40  $\Omega$  and 60  $\Omega$  is required.

The TESTHI signals may use individual pull-up resistors or be grouped together as detailed below. A matched resistor must be used for each group:

- TESTHI[1:0] - can be grouped together with a single pull-up to  $V_{TT}$

## 2.6 Front Side Bus Signal Groups

The FSB signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END as reference levels. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving. AGTL+ asynchronous outputs can become active anytime and include an active PMOS pull-up transistor to assist during the first clock of a low-to-high voltage transition.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals whose timings are specified with respect to rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as rising edge of BCLK0. Asynchronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. [Table 2-4](#) identifies which signals are common clock, source synchronous and asynchronous.



Table 2-4. FSB Signal Groups

| Signal Group                 | Type                         | Signals <sup>1</sup>                                                                                                                                                                                                                               |                   |
|------------------------------|------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|
| AGTL+ Common Clock Input     | Synchronous to BCLK[1:0]     | BPRI#, DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#;                                                                                                                                                                                                      |                   |
| AGTL+ Common Clock Output    | Synchronous to BCLK[1:0]     | BPM4#, BPM[2:1]#, BPMb[2:1]#                                                                                                                                                                                                                       |                   |
| AGTL+ Common Clock I/O       | Synchronous to BCLK[1:0]     | ADS#, AP[1:0]#, BINIT# <sup>2</sup> , BNR# <sup>2</sup> , BPM5#, BPM3#, BPM0#, BPMb3#, BPMb0#, BR[1:0]#, DBSY#, DP[3:0]#, DRDY#, HIT# <sup>2</sup> , HITM# <sup>2</sup> , LOCK#, MCERR# <sup>2</sup>                                               |                   |
| AGTL+ Source Synchronous I/O | Synchronous to assoc. strobe |                                                                                                                                                                                                                                                    |                   |
|                              |                              | Signals                                                                                                                                                                                                                                            | Associated Strobe |
|                              |                              | REQ[4:0]#<br>A[37:36,16:3]#                                                                                                                                                                                                                        | ADSTB0#           |
|                              |                              | A[39:38, 35:17]#                                                                                                                                                                                                                                   | ADSTB1#           |
|                              |                              | D[15:0]#, DBI0#                                                                                                                                                                                                                                    | DSTBP0#, DSTBN0#  |
|                              |                              | D[31:16]#, DBI1#                                                                                                                                                                                                                                   | DSTBP1#, DSTBN1#  |
|                              |                              | D[47:32]#, DBI2#                                                                                                                                                                                                                                   | DSTBP2#, DSTBN2#  |
|                              |                              | D[63:48]#, DBI3#                                                                                                                                                                                                                                   | DSTBP3#, DSTBN3#  |
|                              |                              |                                                                                                                                                                                                                                                    |                   |
| AGTL+ Strobes I/O            | Synchronous to BCLK[1:0]     | ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#                                                                                                                                                                                                              |                   |
| Open Drain Output            | Asynchronous                 | FERR#/PBE#, IERR#, PROCHOT#, THERMTRIP#, TDO                                                                                                                                                                                                       |                   |
| CMOS Asynchronous Input      | Asynchronous                 | A20M#, FORCEPR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, STPCLK#, TCK, TDI, TMS TRST#                                                                                                                                                 |                   |
| CMOS Asynchronous Output     | Asynchronous                 | BSEL[2:0], VID[6:1]                                                                                                                                                                                                                                |                   |
| FSB Clock                    | Clock                        | BCLK[1:0]                                                                                                                                                                                                                                          |                   |
| SMBus                        | Synchronous to SM_CLK        | SM_CLK, SM_DAT, SM_EP_A[2:0], SM_WP                                                                                                                                                                                                                |                   |
| Power/Other                  | Power/Other                  | COMP[3:0], GTLREF_ADD_MID, GTLREF_ADD_END, GTLREF_DATA_MID, GTLREF_DATA_END, LL_ID[1:0], PROC_ID[1:0], PECl, RESERVED, SKTOCC#,SM_VCC, TESTHI[1:0], TESTIN1, TESTIN2, VCC, VCC_SENSE, VCC_SENSE2, VCCPLL, VSS_SENSE, VSS_SENSE2, VSS, VTT, VTT_SEL |                   |

**Notes:**

1. Refer to [Section 5](#) for signal descriptions.
2. These signals may be driven simultaneously by multiple agents (Wired-OR).



Table 2-5 outlines the signals which include on-die termination ( $R_{TT}$ ). Table 2-6 outlines non AGTL+ signals including open drain signals. Table 2-7 provides signal reference voltages.

**Table 2-5. AGTL+ Signal Description Table**

| AGTL+ signals with $R_{TT}$ <sup>1</sup>                                                                                                                                                                | AGTL+ signals with no $R_{TT}$         |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------|
| A[39:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, HIT#, HITM#, LOCK#, MCERR#, REQ[4:0]#, RS[2:0]#, RSP#, TRDY# | BPM[5:0]#, BPMb[3:0]#, RESET#, BR[1:0] |

**Note:**

1. Signals that have  $R_{TT}$  in the package with 50  $\Omega$  pullup to  $V_{TT}$ .

**Table 2-6. Non AGTL+ Signal Description Table**

| Signals with $R_{TT}$ | Signals with no $R_{TT}$                                                                                                                                                                                                                                                                                                                                                                      |
|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                       | A20M#, BCLK[1:0], BSEL[2:0], COMP[3:0], FERR#/PBE#, FORCEPR#, GTLREF_ADD_MID, GTLREF_ADD_END, GTLREF_DATA_MID, GTLREF_DATA_END, IERR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, LL_ID[1:0], PROC_ID[1:0], PECI, PROCHOT#, PWRGOOD, SKTOCC#, SMI#, STPCLK#, TCK, TDI, TDO, TESTHI[1:0], TESTIN1, TESTIN2, THERMTRIP#, TMS, TRST#, VCC_SENSE, VCC_SENSE2, VID[6:1], VSS_SENSE, VSS_SENSE2, VTT_SEL |

**Table 2-7. Signal Reference Voltages**

| GTLREF                                                                                                                                                                                                                                                     | CMOS                                                                                      |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------|
| A[39:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BPM[5:0]#, BPMb[3:0]#, BPRI#, BR[1:0]#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, FORCEPR#, HIT#, HITM#, LOCK#, MCERR#, RESET#, REQ[4:0]#, RS[2:0]#, RSP#, TRDY# | A20M#, LINT0/INTR, LINT1/NMI, IGNNE#, INIT#, PWRGOOD, SMI#, STPCLK#, TCK, TDI, TMS, TRST# |

## 2.7 CMOS Asynchronous and Open Drain Asynchronous Signals

Legacy input signals such as A20M#, IGNNE#, INIT#, SMI#, and STPCLK# utilize CMOS input buffers. Legacy output signals such as FERR#/PBE#, IERR#, PROCHOT#, THERMTRIP#, and TDO utilize open drain output buffers. All of the CMOS and Open Drain signals are required to be asserted/deasserted for at least eight BCLKs in order for the processor to recognize the proper signal state. See Section 2.11 and Section 2.12 for the DC and AC specifications. See Section 7 for additional timing requirements for entering and leaving the low power states.

## 2.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the processor(s) be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required with each driving a different voltage level.



## 2.9 Mixing Processors

Intel supports and validates multi-processor configurations only in which all processors operate with the same FSB frequency, core frequency, number of cores, and have the same internal cache sizes. Mixing components operating at different internal clock frequencies or number of cores is not supported and will not be validated by Intel.

**Note:** Processors within a system must operate at the same frequency per bits [12:8] of the CLOCK\_FLEX\_MAX MSR; however this does not apply to frequency transitions initiated due to thermal events, Extended HALT, Enhanced Intel SpeedStep technology transitions, or assertion of the FORCEPR# signal (See [Section 6](#)).

Mixing processors of different steppings but the same model (as per CPUID instruction) is supported. Details regarding the CPUID instruction are provided in the *AP-485 Intel® Processor Identification and the CPUID Instruction* application note.

## 2.10 Absolute Maximum and Minimum Ratings

[Table 2-8](#) specifies absolute maximum and minimum ratings only, which lie outside the functional limits of the processor. Only within specified operation limits, can functionality and long-term reliability be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

**Table 2-8. Processor Absolute Maximum Ratings**

| Symbol               | Parameter                                               | Min                           | Max                           | Unit | Notes <sup>1</sup>                                        |
|----------------------|---------------------------------------------------------|-------------------------------|-------------------------------|------|-----------------------------------------------------------|
| V <sub>CC</sub>      | Core voltage with respect to V <sub>SS</sub>            | -0.30                         | 1.55                          | V    |                                                           |
| V <sub>TT</sub>      | FSB termination voltage with respect to V <sub>SS</sub> | -0.30                         | 1.55                          | V    |                                                           |
| T <sub>CASE</sub>    | Processor case temperature                              | See <a href="#">Section 6</a> | See <a href="#">Section 6</a> | °C   |                                                           |
| T <sub>STORAGE</sub> | Storage temperature                                     | -40                           | 85                            | °C   | <a href="#">2</a> , <a href="#">3</a> , <a href="#">4</a> |

**Notes:**

1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
3. This rating applies to the processor and does not include any tray or packaging.
4. Failure to adhere to this specification can affect the long-term reliability of the processor.



## 2.11 Processor DC Specifications

The following notes apply:

- The processor DC specifications in this section are defined at the processor die and not at the package pins unless noted otherwise.
- The notes associated with each parameter are part of the specification for that parameter.
- Unless otherwise noted, all specifications in the tables apply to all frequencies and cache sizes.

See [Section 5](#) for the pin signal definitions. Most of the signals on the processor FSB are in the AGTL+ signal group. The DC specifications for these signals are listed in [Table 2-11](#).

[Table 2-9](#) through [Table 2-17](#) list the DC specifications and are valid only while meeting specifications for case temperature (Tcase as specified in [Section 6](#)), clock frequency, and input voltages.



### 2.11.1 Flexible Motherboard Guidelines (FMB)

The Flexible Motherboard (FMB) guidelines are estimates of the maximum values the Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series will have over certain time periods. The values are only estimates and actual specifications for future processors may differ. Processors may or may not have specifications equal to the FMB value in the foreseeable future. System designers should meet the FMB values to ensure their systems will be compatible with future processors.

**Table 2-9. Voltage and Current Specifications (Sheet 1 of 2)**

| Symbol                 | Parameter                                                                                                            | Min                                                      | Typ   | Max    | Unit | Notes<br>1,17    |
|------------------------|----------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|-------|--------|------|------------------|
| VID                    | VID range                                                                                                            | 1.0000                                                   |       | 1.5000 | V    |                  |
| V <sub>CC</sub>        | V <sub>CC</sub> for processor core<br>Launch - FMB                                                                   | See Table 2-10, Figure 2-5,<br>Figure 2-6 and Figure 2-7 |       |        | V    | 2, 3, 4, 6,<br>9 |
| V <sub>CC_BOOT</sub>   | Default V <sub>CC</sub> Voltage for initial power up                                                                 |                                                          | 1.10  |        | V    | 2                |
| V <sub>VID_STEP</sub>  | VID step size during a transition                                                                                    |                                                          |       | ± 12.5 | mV   |                  |
| V <sub>VID_SHIFT</sub> | Total allowable DC load line shift from<br>VID steps                                                                 |                                                          |       | 450    | mV   | 10               |
| V <sub>TT</sub>        | FSB termination voltage (DC + AC<br>specification)                                                                   | 1.14                                                     | 1.20  | 1.26   | V    | 8, 13            |
| V <sub>CCPLL</sub>     | PLL supply voltage (DC + AC<br>specification)                                                                        | 1.425                                                    | 1.50  | 1.605  | V    |                  |
| SM_VCC                 | SMBus supply voltage                                                                                                 | 3.135                                                    | 3.300 | 3.465  | V    |                  |
| I <sub>CC</sub>        | I <sub>CC</sub> for Quad-Core Intel® Xeon® L7345<br>Processor with multiple VID<br>Launch - FMB                      |                                                          |       | 60     | A    | 4, 5, 6, 9       |
| I <sub>CC_RESET</sub>  | I <sub>CC_RESET</sub> for Quad-Core Intel® Xeon®<br>L7345 Processor with multiple VID<br>Launch - FMB                |                                                          |       | 60     | A    | 17               |
| I <sub>CC</sub>        | I <sub>CC</sub> for Dual-Core Intel® Xeon®<br>Processor 7200 Series with multiple<br>VID<br>Launch - FMB             |                                                          |       | 90     | A    | 4, 5, 6, 9       |
| I <sub>CC_RESET</sub>  | I <sub>CC_RESET</sub> for Dual-Core Intel® Xeon®<br>Processor 7200 Series with multiple<br>VID<br>Launch - FMB       |                                                          |       | 90     | A    | 17               |
| I <sub>CC</sub>        | I <sub>CC</sub> for Intel® Xeon® Processor 7200<br>Series and 7300 Series with multiple<br>VID<br>Launch - FMB       |                                                          |       | 90     | A    | 4, 5, 6, 9       |
| I <sub>CC_RESET</sub>  | I <sub>CC_RESET</sub> for Intel® Xeon® Processor<br>7200 Series and 7300 Series with<br>multiple VID<br>Launch - FMB |                                                          |       | 90     | A    | 17               |
| I <sub>CC</sub>        | I <sub>CC</sub> for Intel® Xeon® X7350 Processor<br>with multiple VID<br>Launch - FMB                                |                                                          |       | 130    | A    | 4, 5, 6, 9       |
| I <sub>CC_RESET</sub>  | I <sub>CC_RESET</sub> for Intel® Xeon® X7350<br>Processor with multiple VID<br>Launch - FMB                          |                                                          |       | 130    | A    | 17               |
| I <sub>SM_VCC</sub>    | I <sub>CC</sub> for SMBus supply                                                                                     |                                                          | 100   | 122.5  | mA   |                  |



Table 2-9. Voltage and Current Specifications (Sheet 2 of 2)

| Symbol             | Parameter                                                                                                                                              | Min | Typ | Max        | Unit | Notes<br>1,17 |
|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|------------|------|---------------|
| $I_{TT}$           | $I_{CC}$ for $V_{TT}$ supply before $V_{CC}$ stable<br>$I_{CC}$ for $V_{TT}$ supply after $V_{CC}$ stable                                              |     |     | 8.0<br>7.0 | A    | 15            |
| $I_{CC\_TDC}$      | Thermal Design Current (TDC) Quad-Core Intel® Xeon® L7345 Processor<br>Launch - FMB                                                                    |     |     | 50         | A    | 6,14          |
| $I_{CC\_TDC}$      | Thermal Design Current (TDC) Dual-Core Intel® Xeon® Processor 7200 Series<br>Launch - FMB                                                              |     |     | 75         | A    | 6,14          |
| $I_{CC\_TDC}$      | Thermal Design Current (TDC) Intel® Xeon® Processor 7200 Series and 7300 Series<br>Launch - FMB                                                        |     |     | 75         | A    | 6,14          |
| $I_{CC\_TDC}$      | Thermal Design Current (TDC) Intel® Xeon® X7350 Processor<br>Launch - FMB                                                                              |     |     | 110        | A    | 6,14          |
| $I_{CC\_VTT\_OUT}$ | DC current that may be drawn from $V_{TT\_OUT}$ per pin                                                                                                |     |     | 580        | mA   | 16            |
| $I_{CC\_GTLREF}$   | $I_{CC}$ for<br>GTLREF_DATA_MID,<br>GTLREF_DATA_END,<br>GTLREF_ADD_MID, and<br>GTLREF_ADD_END                                                          |     |     | 200        | μA   | 7             |
| $I_{CC\_VCCPLL}$   | $I_{CC}$ for PLL supply                                                                                                                                |     |     | 260        | mA   | 12            |
| $I_{TCC}$          | $I_{CC}$ for Quad-Core Intel® Xeon® L7345 Processor during active thermal control circuit (TCC)                                                        |     |     | 60         | A    |               |
| $I_{TCC}$          | $I_{CC}$ for Dual-Core Intel® Xeon® Processor 7200 Series during active thermal control circuit (TCC)                                                  |     |     | 90         | A    |               |
| $I_{TCC}$          | $I_{CC}$ for Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series during active thermal control circuit (TCC) |     |     | 90         | A    |               |
| $I_{TCC}$          | $I_{CC}$ for Intel® Xeon® X7350 Processor during active thermal control circuit (TCC)                                                                  |     |     | 130        | A    |               |

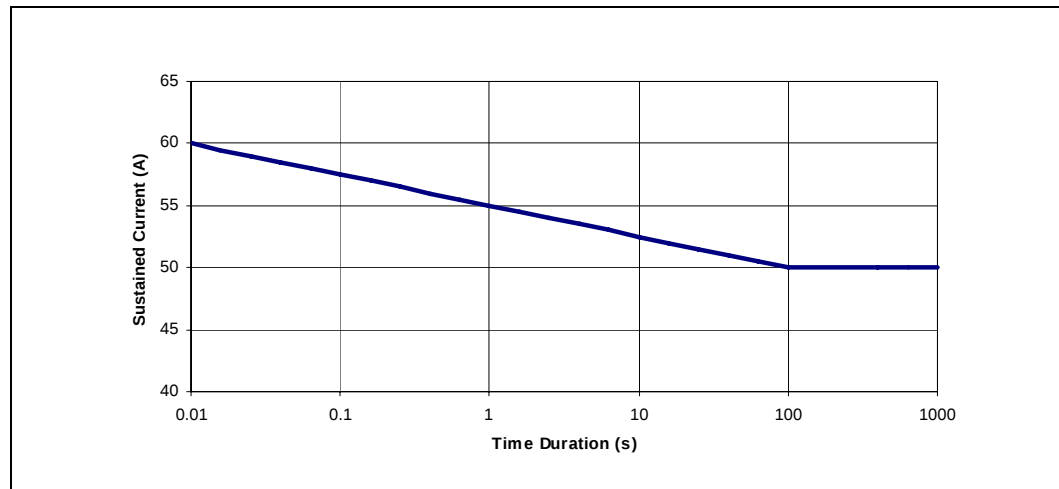
**Notes:**

1. Unless otherwise noted, all specifications in this table apply to all processors and are based on estimates and simulations, not empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See [Section 2.4](#) for more information.
3. The voltage specification requirements are measured across the VCC\_SENSE and VSS\_SENSE pins and across the VCC\_SENSE2 and VSS\_SENSE2 pins with an oscilloscope set to 100 MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
4. The processor must not be subjected to any static  $V_{CC}$  level that exceeds the  $V_{CC\_MAX}$  associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
5.  $I_{CC\_MAX}$  specification is based on maximum  $V_{CC}$  loadline. Refer to [Figure 2-10](#) for details. The processor is capable of drawing  $I_{CC\_MAX}$  for up to 10 ms. Refer to [Figure 2-9](#) for further details on the average processor current draw over various time durations.
6. FMB is the flexible motherboard guideline. These guidelines are for estimation purposes only. See [Section 2.11.1](#) for further details on FMB guidelines.
7. This specification represents the total current for GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END.
8.  $V_{TT}$  must be provided via a separate voltage source and must not be connected to  $V_{CC}$ . This specification is measured at the pin.



9. Minimum VCC and maximum ICC are specified at the maximum processor case temperature (TCASE) shown in [Figure 6-2](#).
10. This specification refers to the total reduction of the load line due to VID transitions below the specified VID.
11. Individual processor VID values may be calibrated during manufacturing such that two devices at the same frequency may have different VID settings.
12. This specification applies to the VCCPLL pin.
13. Baseboard bandwidth is limited to 20 MHz.
14.  $I_{CC\_TDC}$  is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator temperature assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion. Please see the applicable design guidelines for further details. The processor is capable of drawing  $I_{CC\_TDC}$  indefinitely. Refer to [Figure 2-9](#) for further details on the average processor current draw over various time durations. This parameter is based on design characterization and is not tested.
15. This is the maximum total current drawn from the  $V_{TT}$  plane by only one processor with  $R_{TT}$  enabled. This specification does not include the current coming from on-board termination ( $R_{TT}$ ), through the signal line. Refer to the appropriate platform design guide and the Voltage Regulator Design Guidelines to determine the total  $I_{TT}$  drawn by the system. This parameter is based on design characterization and is not tested.
16.  $I_{CC\_VTT\_OUT}$  is specified at 1.2 V.
17.  $I_{CC\_RESET}$  is specified while PWRGOOD and RESET# are asserted. Refer to [Table 2-22](#) for the PWRGOOD to RESET# de-assertion time specification and [Table 2-23](#) for the RESET# Pulse Width specification.

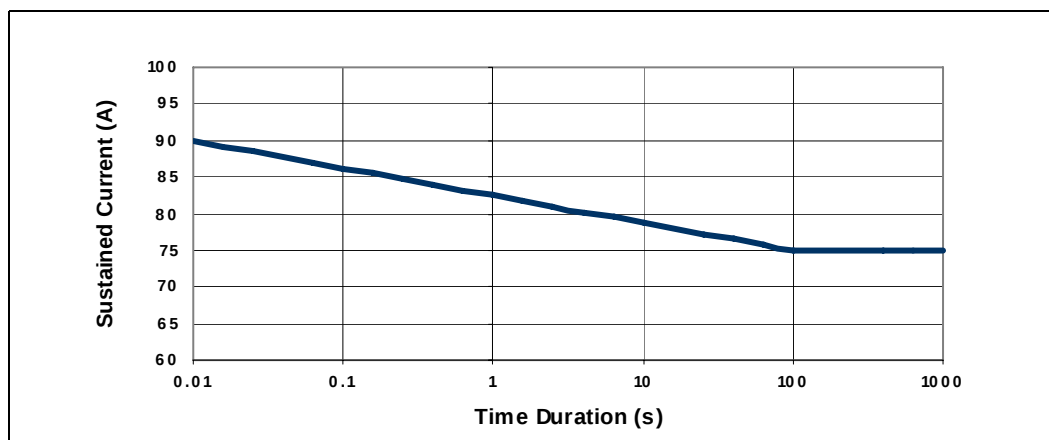
**Figure 2-1. Quad-Core Intel® Xeon® L7345 Processor Load Current versus Time**



**Notes:**

1. Processor or Voltage Regulator thermal protection circuitry should not trip for load currents greater than  $I_{CC\_TDC}$ .
2. Not 100% tested. Specified by design characterization.

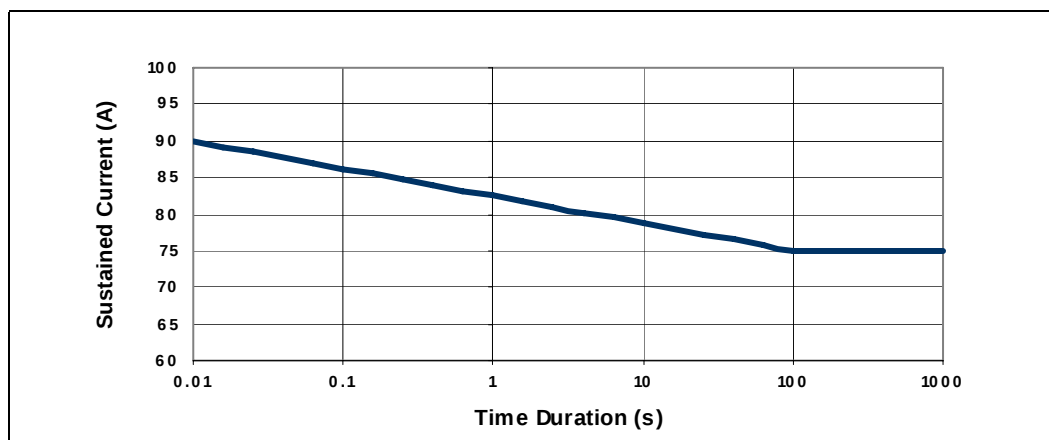
**Figure 2-2. Dual-Core Dual-Core Intel® Xeon® Processor 7200 Series Load Current versus Time**



**Notes:**

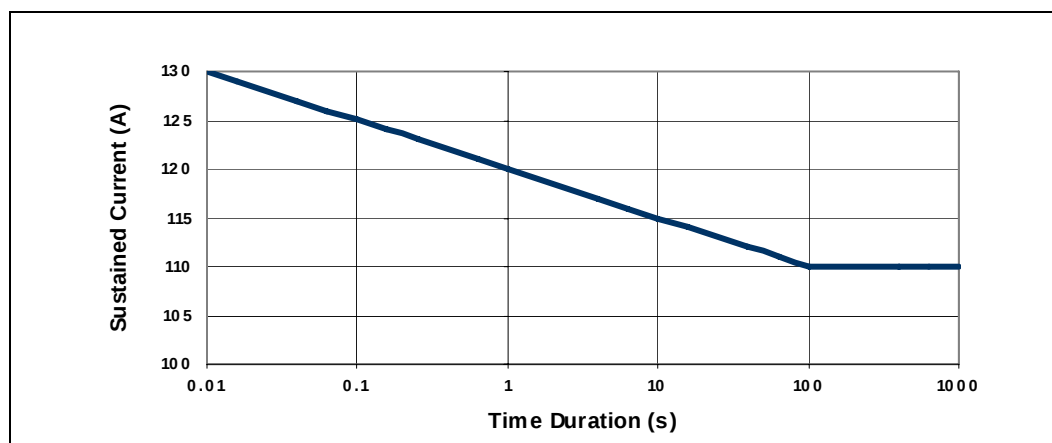
1. Processor or Voltage Regulator thermal protection circuitry should not trip for load currents greater than  $I_{CC\_TDC}$ .
2. Not 100% tested. Specified by design characterization.

**Figure 2-3. Quad-Core Intel® Xeon® Processor 7200 Series and 7300 Series Load Current versus Time**



**Notes:**

1. Processor or Voltage Regulator thermal protection circuitry should not trip for load currents greater than  $I_{CC\_TDC}$ .
2. Not 100% tested. Specified by design characterization.

**Figure 2-4. Quad-Core Intel® Xeon® X7350 Processor Load Current versus Time****Notes:**

1. Processor or Voltage Regulator thermal protection circuitry should not trip for load currents greater than  $I_{CC\_TDC}$ .
2. Not 100% tested. Specified by design characterization.



Table 2-10.  $V_{CC}$  Static and Transient Tolerance

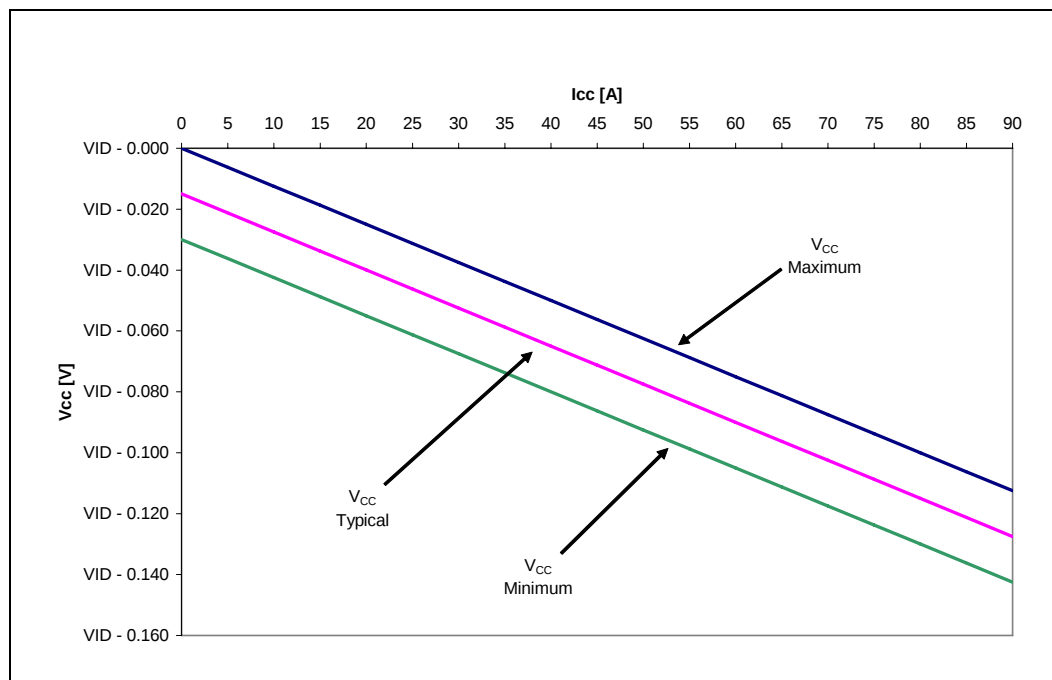
| $I_{CC}$ (A) | $V_{CC\_Max}$ (V) | $V_{CC\_Typ}$ (V) | $V_{CC\_Min}$ (V) | Notes         |
|--------------|-------------------|-------------------|-------------------|---------------|
| 0            | VID - 0.000       | VID - 0.015       | VID - 0.030       | 1, 2, 3       |
| 5            | VID - 0.006       | VID - 0.021       | VID - 0.036       | 1, 2, 3       |
| 10           | VID - 0.013       | VID - 0.028       | VID - 0.043       | 1, 2, 3       |
| 15           | VID - 0.019       | VID - 0.034       | VID - 0.049       | 1, 2, 3       |
| 20           | VID - 0.025       | VID - 0.040       | VID - 0.055       | 1, 2, 3       |
| 25           | VID - 0.031       | VID - 0.046       | VID - 0.061       | 1, 2, 3       |
| 30           | VID - 0.038       | VID - 0.053       | VID - 0.068       | 1, 2, 3       |
| 35           | VID - 0.044       | VID - 0.059       | VID - 0.074       | 1, 2, 3       |
| 40           | VID - 0.050       | VID - 0.065       | VID - 0.080       | 1, 2, 3       |
| 45           | VID - 0.056       | VID - 0.071       | VID - 0.086       | 1, 2, 3       |
| 50           | VID - 0.069       | VID - 0.084       | VID - 0.099       | 1, 2, 3       |
| 55           | VID - 0.069       | VID - 0.077       | VID - 0.093       | 1, 2, 3       |
| 60           | VID - 0.075       | VID - 0.090       | VID - 0.105       | 1, 2, 3       |
| 65           | VID - 0.081       | VID - 0.096       | VID - 0.111       | 1, 2, 3, 4    |
| 70           | VID - 0.087       | VID - 0.103       | VID - 0.118       | 1, 2, 3, 4    |
| 75           | VID - 0.094       | VID - 0.109       | VID - 0.124       | 1, 2, 3, 4    |
| 80           | VID - 0.100       | VID - 0.115       | VID - 0.130       | 1, 2, 3, 4    |
| 85           | VID - 0.106       | VID - 0.121       | VID - 0.136       | 1, 2, 3, 4    |
| 90           | VID - 0.113       | VID - 0.128       | VID - 0.143       | 1, 2, 3, 4    |
| 95           | VID - 0.119       | VID - 0.134       | VID - 0.149       | 1, 2, 3, 4, 5 |
| 100          | VID - 0.125       | VID - 0.140       | VID - 0.155       | 1, 2, 3, 4, 5 |
| 105          | VID - 0.131       | VID - 0.146       | VID - 0.161       | 1, 2, 3, 4, 5 |
| 110          | VID - 0.138       | VID - 0.153       | VID - 0.168       | 1, 2, 3, 4, 5 |
| 115          | VID - 0.144       | VID - 0.159       | VID - 0.174       | 1, 2, 3, 4, 5 |
| 120          | VID - 0.150       | VID - 0.165       | VID - 0.180       | 1, 2, 3, 4, 5 |
| 125          | VID - 0.156       | VID - 0.171       | VID - 0.186       | 1, 2, 3, 4, 5 |
| 130          | VID - 0.163       | VID - 0.178       | VID - 0.193       | 1, 2, 3, 4, 5 |

**Notes:**

1. The  $V_{CC\_MIN}$  and  $V_{CC\_MAX}$  loadlines represent static and transient limits. Please see [Section 2.11.3](#) for  $V_{CC}$  overshoot specifications.
2. This table is intended to aid in reading discrete points on [Figure 2-5](#) for Intel® Xeon® Processor 7200 Series and 7300 Series, [Figure 2-6](#) for Intel® Xeon® X7350 Processor, [Figure 2-7](#) for Quad-Core Intel® Xeon® L7345 Processor and [Figure 2-8](#) for Dual-Core Intel® Xeon® Processor 7200 Series.
3. The loadlines specify voltage limits at the die measured at the  $V_{CC\_SENSE}$  and  $V_{SS\_SENSE}$  pins and across the  $V_{CC\_SENSE2}$  and  $V_{SS\_SENSE2}$  pins. Voltage regulation feedback for voltage regulator circuits must also be taken from processor  $V_{CC\_SENSE2}$  and  $V_{SS\_SENSE2}$  pins. Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator Down (EVRD) 11.0 Design Guidelines* for socket load line guidelines and VR implementation. Please refer to the appropriate platform design guide for details on VR implementation.
4.  $I_{CC}$  values greater than 60 A are not applicable for the Quad-Core Intel® Xeon® L7345 Processor.
5.  $I_{CC}$  values greater than 90 A are not applicable for the Intel® Xeon® Processor 7200 Series and 7300 Series and Dual-Core Intel® Xeon® Processor 7200 Series.



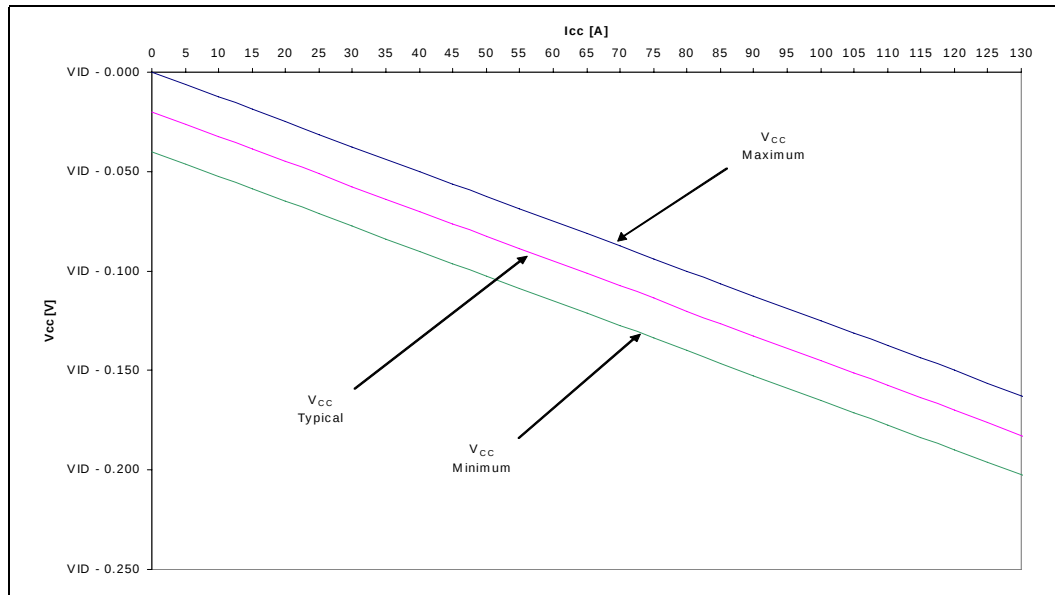
**Figure 2-5. Quad-Core Intel® Xeon® Processor 7200 Series and 7300 Series  $V_{CC}$  Static and Transient Tolerance Load Lines**



**Notes:**

1. The  $V_{CC\_MIN}$  and  $V_{CC\_MAX}$  loadlines represent static and transient limits. Please see [Section 2.11.3](#) for VCC overshoot specifications.
2. Refer to [Table 2-9](#) for processor VID information.
3. Refer to [Table 2-10](#) for  $V_{CC}$  Static and Transient Tolerance
4. The load lines specify voltage limits at the die measured at the VCC\_SENSE and VSS\_SENSE pins and the VCC\_SENSE2 and VSS\_SENSE2 pins. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCC\_SENSE2 and VSS\_SENSE2 pins. Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator Down (EVRD) 11.0 Design Guidelines* for socket load line guidelines and VR implementation. Please refer to the appropriate platform design guide for details on VR implementation.

**Figure 2-6. Quad-Core Intel® Xeon® X7350 Processor VCC Static and Transient Tolerance Load Lines**

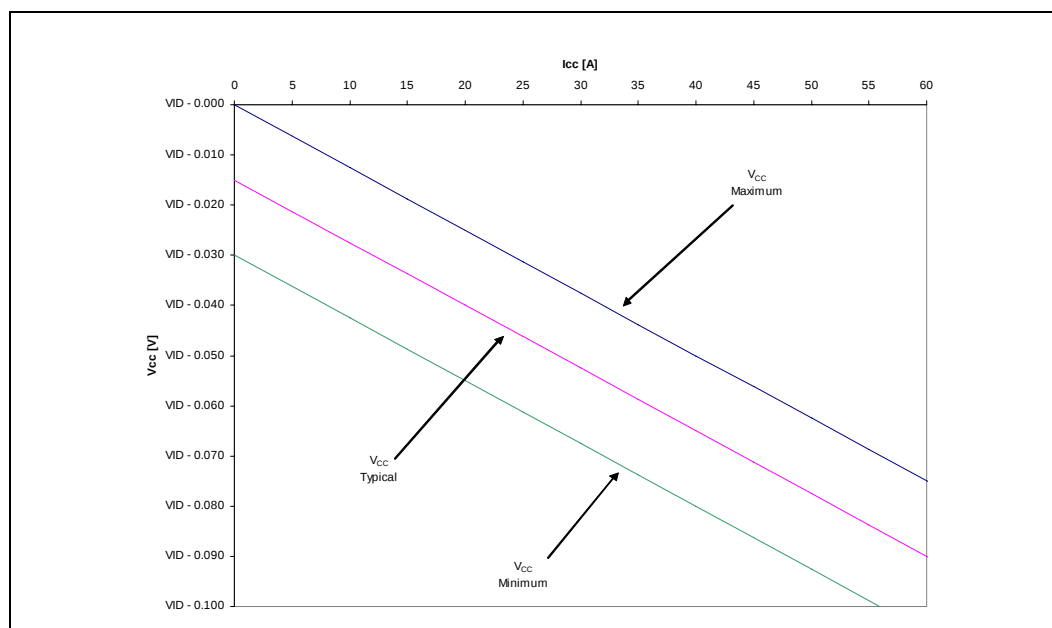


**Notes:**

1. The  $V_{CC\_MIN}$  and  $V_{CC\_MAX}$  loadlines represent static and transient limits. Please see [Section 2.11.3](#) for VCC overshoot specifications.
2. Refer to [Table 2-9](#) for processor VID information.
3. Refer to [Table 2-10](#) for  $V_{CC}$  Static and Transient Tolerance
4. The load lines specify voltage limits at the die measured at the VCC\_SENSE and VSS\_SENSE pins and the VCC\_SENSE2 and VSS\_SENSE2 pins. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCC\_SENSE2 and VSS\_SENSE2 pins. Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator Down (EVRD) 11.0 Design Guidelines* for socket load line guidelines and VR implementation. Please refer to the appropriate platform design guide for details on VR implementation.



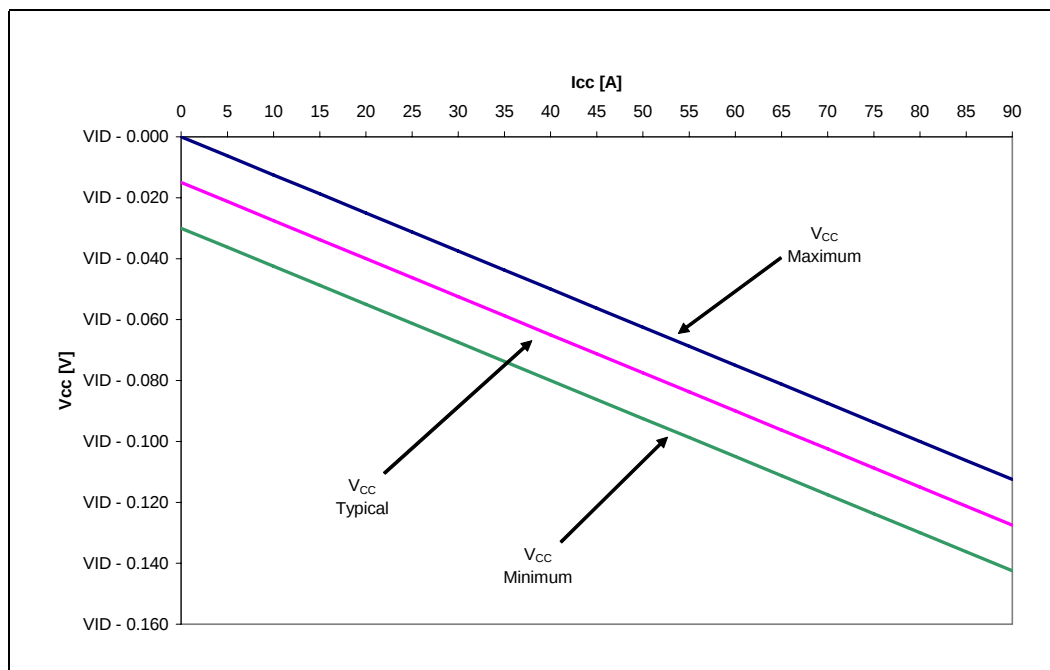
**Figure 2-7. Quad-Core Intel® Xeon® L7345 Processor  $V_{CC}$  Static and Transient Tolerance Load Lines**



**Notes:**

1. The  $V_{CC\_MIN}$  and  $V_{CC\_MAX}$  loadlines represent static and transient limits. Please see [Section 2.11.3](#) for VCC overshoot specifications.
2. Refer to [Table 2-9](#) for processor VID information.
3. Refer to [Table 2-10](#) for  $V_{CC}$  Static and Transient Tolerance
4. The load lines specify voltage limits at the die measured at the VCC\_SENSE and VSS\_SENSE pins and the VCC\_SENSE2 and VSS\_SENSE2 pins. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCC\_SENSE2 and VSS\_SENSE2 pins. Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator Down (EVRD) 11.0 Design Guidelines* for socket load line guidelines and VR implementation. Please refer to the appropriate platform design guide for details on VR implementation

**Figure 2-8. Dual-Core Intel® Xeon® Processor 7200 Series  $V_{CC}$  Static and Transient Tolerance Load Lines**



**Notes:**

1. The  $V_{CC\_MIN}$  and  $V_{CC\_MAX}$  loadlines represent static and transient limits. Please see [Section 2.11.3](#) for VCC overshoot specifications.
2. Refer to [Table 2-9](#) for processor VID information.
3. Refer to [Table 2-10](#) for  $V_{CC}$  Static and Transient Tolerance
4. The load lines specify voltage limits at the die measured at the VCC\_SENSE and VSS\_SENSE pins and the VCC\_SENSE2 and VSS\_SENSE2 pins. Voltage regulation feedback for voltage regulator circuits must also be taken from processor VCC\_SENSE2 and VSS\_SENSE2 pins. Refer to the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator Down (EVRD) 11.0 Design Guidelines* for socket load line guidelines and VR implementation. Please refer to the appropriate platform design guide for details on VR implementation.

**Table 2-11. AGTL+ Signal Group DC Specifications**

| Symbol   | Parameter             | Min             | Typ      | Max           | Units    | Notes <sup>1</sup> |
|----------|-----------------------|-----------------|----------|---------------|----------|--------------------|
| $V_{IL}$ | Input Low Voltage     | -0.10           | 0        | GTLREF-0.10   | V        | 2,4,6              |
| $V_{IH}$ | Input High Voltage    | GTLREF+0.10     | $V_{TT}$ | $V_{TT}+0.10$ | V        | 3,6                |
| $V_{OH}$ | Output High Voltage   | $V_{TT} - 0.10$ | N/A      | $V_{TT}$      | V        | 4,6                |
| $R_{ON}$ | Buffer On Resistance  | 10.00           | 11.50    | 13.00         | $\Omega$ | 5                  |
| $I_{LI}$ | Input Leakage Current | N/A             | N/A      | +/-100        | $\mu A$  | 7,8                |

**Notes:**

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2.  $V_{IL}$  is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3.  $V_{IH}$  is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4.  $V_{IH}$  and  $V_{OH}$  may experience excursions above  $V_{TT}$ . However, input signal drivers must comply with the signal quality specifications.
5. This is the pull down driver resistance. Refer to processor I/O Buffer Models for I/V characteristics. Measured at  $0.31 \cdot V_{TT}$ .  $R_{ON} (min) = 0.225 \cdot R_{TT}$ .  $R_{ON} (typ) = 0.250 \cdot R_{TT}$ .  $R_{ON} (max) = 0.275 \cdot R_{TT}$
6. GTLREF should be generated from  $V_{TT}$  with a 1% tolerance resistor divider. The  $V_{TT}$  referred to in these specifications is the instantaneous  $V_{TT}$ .
7. Specified when on-die  $R_{TT}$  and  $R_{ON}$  are turned off.  $V_{IN}$  between 0 and  $V_{TT}$ .
8. This is the measurement at the pin.



Table 2-12. CMOS Signal Input/Output Group DC Specifications

| Symbol          | Parameter             | Min                 | Typ             | Max                  | Units | Notes <sup>1</sup> |
|-----------------|-----------------------|---------------------|-----------------|----------------------|-------|--------------------|
| V <sub>IL</sub> | Input Low Voltage     | -0.10               | 0.00            | 0.3*V <sub>TT</sub>  | V     | 2,3                |
| V <sub>IH</sub> | Input High Voltage    | 0.7*V <sub>TT</sub> | V <sub>TT</sub> | V <sub>TT</sub> +0.1 | V     | 2                  |
| V <sub>OL</sub> | Output Low Voltage    | -0.10               | 0               | 0.1*V <sub>TT</sub>  | V     | 2                  |
| V <sub>OH</sub> | Output High Voltage   | 0.9*V <sub>TT</sub> | V <sub>TT</sub> | V <sub>TT</sub> +0.1 | V     | 2                  |
| I <sub>OL</sub> | Output Low Current    | 1.70                | N/A             | 4.70                 | mA    | 4                  |
| I <sub>OH</sub> | Output High Current   | 1.70                | N/A             | 4.70                 | mA    | 5                  |
| I <sub>LI</sub> | Input Leakage Current | N/A                 | N/A             | +/- 100              | μA    | 6,7                |

**Notes:**

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V<sub>TT</sub> referred to in these specifications refers to instantaneous V<sub>TT</sub>.
3. Refer to the processor I/O Buffer Models for I/V characteristics.
4. Measured at 0.1\*V<sub>TT</sub>.
5. Measured at 0.9\*V<sub>TT</sub>.
6. For V<sub>in</sub> between 0 V and V<sub>TT</sub>. Measured when the driver is tristated.
7. This is the measurement at the pin.

Table 2-13. Open Drain Signal Group DC Specifications

| Symbol          | Parameter           | Min                 | Typ             | Max                 | Units | Notes <sup>1</sup> |
|-----------------|---------------------|---------------------|-----------------|---------------------|-------|--------------------|
| V <sub>OL</sub> | Output Low Voltage  |                     | N/A             | 0.20                | V     | 3                  |
| V <sub>OH</sub> | Output High Voltage | V <sub>TT</sub> -5% | V <sub>TT</sub> | V <sub>TT</sub> +5% | V     |                    |
| I <sub>OL</sub> | Output Low Current  | 16                  | N/A             | 50                  | mA    | 2                  |
| I <sub>LO</sub> | Leakage Current     | N/A                 | N/A             | +/- 200             | μA    | 4,5                |

**Notes:**

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2\*V<sub>TT</sub>.
3. V<sub>OH</sub> is determined by value of the external pullup resistor to V<sub>TT</sub>. Please refer to platform design guide for details.
4. For V<sub>IN</sub> between 0 V and V<sub>OH</sub>.
5. This is the measurement at the pin.

Table 2-14. SMBus Signal Group DC Specifications

| Symbol           | Parameter              | Min           | Max           | Unit | Notes <sup>1, 2</sup> |
|------------------|------------------------|---------------|---------------|------|-----------------------|
| V <sub>IL</sub>  | Input Low Voltage      | -0.30         | 0.30 * SM_VCC | V    |                       |
| V <sub>IH</sub>  | Input High Voltage     | 0.70 * SM_VCC | 3.465         | V    |                       |
| V <sub>OL</sub>  | Output Low Voltage     | 0             | 0.400         | V    |                       |
| I <sub>OL</sub>  | Output Low Current     | N/A           | 3.0           | mA   |                       |
| I <sub>LI</sub>  | Input Leakage Current  | N/A           | ± 10          | μA   |                       |
| I <sub>LO</sub>  | Output Leakage Current | N/A           | ± 10          | μA   |                       |
| C <sub>SMB</sub> | SMBus Pin Capacitance  |               | 15.0          | pF   | 3                     |

**Notes:**

1. These parameters are based on design characterization and are not tested.
2. All DC specifications for the SMBus signal group are measured at the processor pins.
3. Platform designers may need this value to calculate the maximum loading of the SMBus and to determine maximum rise and fall times for SMBus signals.

## 2.11.2 Platform Environmental Control Interface (PECI) DC Specifications

PECI is an Intel proprietary one-wire bus interface that provides a communication channel between Intel processor and external thermal monitoring devices. The Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor



7300 Series contains Digital Thermal Sensors (DTS) distributed throughout the die. These sensors are implemented as analog-to-digital converters calibrated at the factory for reasonable accuracy to provide a digital representation of relative processor temperature. PECI provides an interface to relay the highest DTS temperature within a die to external management devices for thermal/fan speed control.

### 2.11.2.1 DC Characteristics

A PECI device interface operates at a nominal voltage set by  $V_{TT}$ . The set of DC electrical specifications shown in [Table 2-15](#) is used with devices normally operating from a  $V_{TT}$  interface supply.  $V_{TT}$  nominal levels will vary between processor families. All PECI devices will operate at the  $V_{TT}$  level determined by the processor installed in the system. For specific nominal  $V_{TT}$  levels, refer to [Table 2-11](#).

**Table 2-15. PECI DC Electrical Limits**

| Symbol           | Definition and Conditions                                           | Min              | Max              | Units     | Notes <sup>1</sup> |
|------------------|---------------------------------------------------------------------|------------------|------------------|-----------|--------------------|
| $V_{in}$         | Input Voltage Range                                                 | -0.150           | $V_{TT}$         | V         |                    |
| $V_{hysteresis}$ | Hysteresis                                                          | $0.1 * V_{TT}$   | N/A              | V         |                    |
| $V_n$            | Negative-edge threshold voltage                                     | $0.275 * V_{TT}$ | $0.500 * V_{TT}$ | V         |                    |
| $V_p$            | Positive-edge threshold voltage                                     | $0.550 * V_{TT}$ | $0.762 * V_{TT}$ | V         |                    |
| $I_{source}$     | High level output source<br>( $V_{OH} = 0.75 * V_{TT}$ )            | -6.0             | N/A              | mA        |                    |
| $I_{sink}$       | Low level output sink<br>( $V_{OL} = 0.25 * V_{TT}$ )               | 0.5              | 1.0              | mA        |                    |
| $I_{leak+}$      | High impedance state leakage to $V_{TT}$<br>( $V_{leak} = V_{OL}$ ) | N/A              | 50               | $\mu A$   | 2                  |
| $I_{leak-}$      | High impedance leakage to GND<br>( $V_{leak} = V_{OH}$ )            | N/A              | 10               | $\mu A$   | 2                  |
| $C_{bus}$        | Bus capacitance                                                     | N/A              | 10               | pF        | 3                  |
| $V_{noise}$      | Signal noise immunity above 300 MHz                                 | $0.1 * V_{TT}$   | N/A              | $V_{p-p}$ |                    |

**Note:**

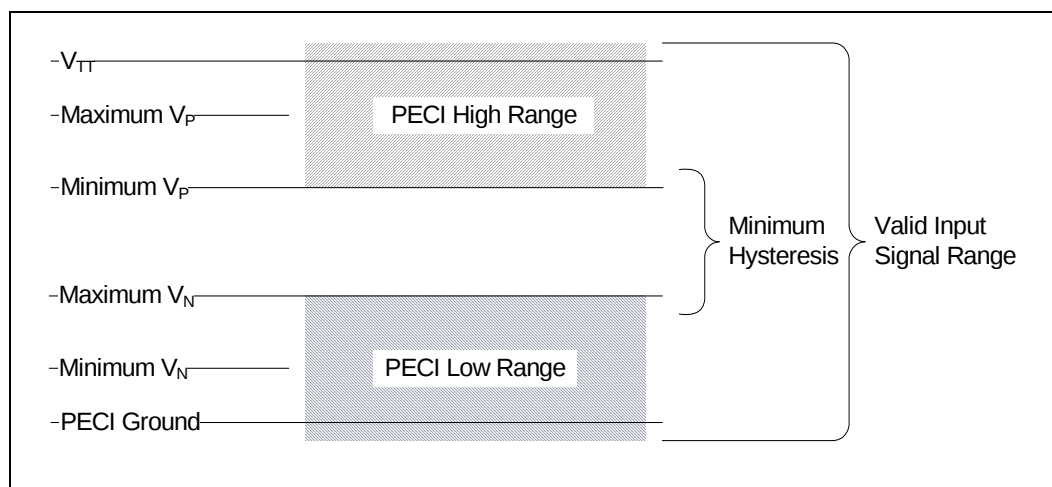
1.  $V_{TT}$  supplies the PECI interface. PECI behavior does not affect  $V_{TT}$  min/max specifications.
2. The leakage specification applies to powered devices on the PECI bus.
3. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.

### 2.11.2.2 Input Device Hysteresis

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use [Figure 2-9](#) as a guide for input buffer design.



Figure 2-9. Input Device Hysteresis



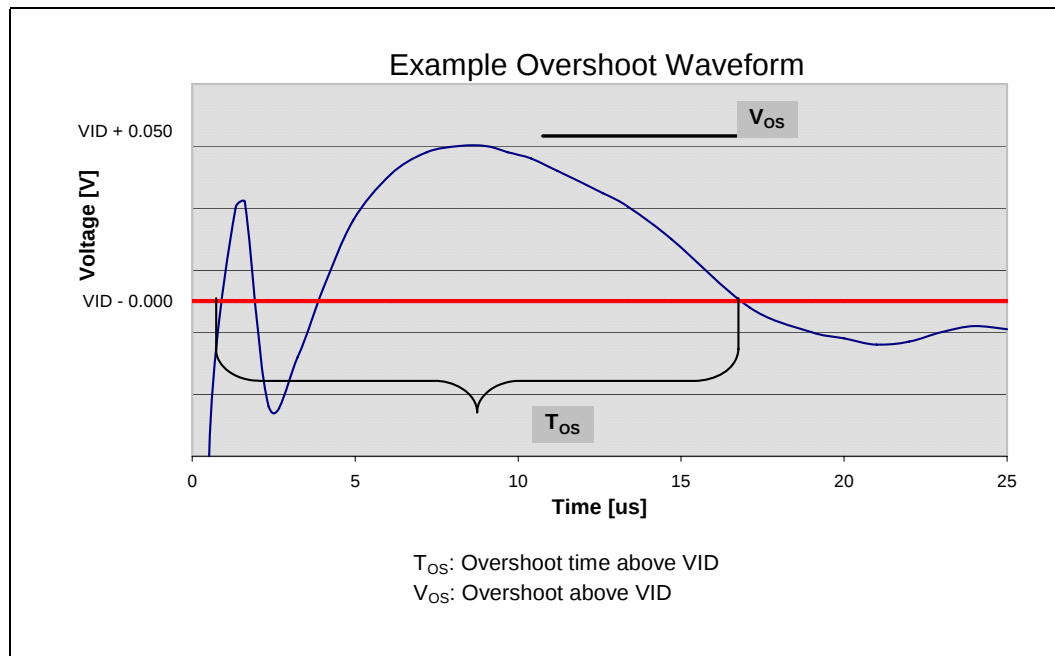
### 2.11.3 $V_{CC}$ Overshoot Specification

Processors can tolerate short transient overshoot events where  $V_{CC}$  exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed  $VID + V_{OS\_MAX}$  ( $V_{OS\_MAX}$  is the maximum allowable overshoot above VID). These specifications apply to the processor die voltage as measured across the  $V_{CC\_SENSE}$  and  $V_{SS\_SENSE}$  pins and across the  $V_{CC\_SENSE2}$  and  $V_{SS\_SENSE2}$  pins.

Table 2-16.  $V_{CC}$  Overshoot Specifications

| Symbol        | Parameter                                     | Min | Max | Units   | Figure | Notes |
|---------------|-----------------------------------------------|-----|-----|---------|--------|-------|
| $V_{OS\_MAX}$ | Magnitude of $V_{CC}$ overshoot above VID     |     | 50  | mV      | 2-10   |       |
| $T_{OS\_MAX}$ | Time duration of $V_{CC}$ overshoot above VID |     | 25  | $\mu$ s | 2-10   |       |

Figure 2-10.  $V_{CC}$  Overshoot Example Waveform



**Notes:**

1.  $V_{OS}$  is the measured overshoot voltage.
2.  $T_{OS}$  is the measured time duration above VID.

### 2.11.3.1 Die Voltage Validation

Core voltage ( $V_{CC}$ ) overshoot events at the processor must meet the specifications in [Table 2-16](#) when measured across the  $V_{CC\_SENSE}$  and  $V_{SS\_SENSE}$  pins and across the  $V_{CC\_SENSE2}$  and  $V_{SS\_SENSE2}$  pins. Overshoot events that are  $< 10$  ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

### 2.11.4 AGTL+ FSB Specifications

Routing topologies are dependent on the processors supported and the chipset used in the design. Please refer to the appropriate platform design guidelines for specific implementation details. In most cases, termination resistors are not required as these are integrated into the processor silicon. See [Table 2-6](#) for details on which signals do not include on-die termination. Please refer to [Table 2-17](#) for  $R_{TT}$  values.

Valid high and low levels are determined by the input buffers via comparing with a reference voltage called  $GTLREF\_DATA\_MID$ ,  $GTLREF\_DATA\_END$ ,  $GTLREF\_ADD\_MID$ , and  $GTLREF\_ADD\_END$ .  $GTLREF\_DATA\_MID$  and  $GTLREF\_DATA\_END$  are the reference voltage for the FSB 4X data signals,  $GTLREF\_ADD\_MID$  and  $GTLREF\_ADD\_END$  are the reference voltage for the FSB 2X address signals and common clock signals. [Table 2-17](#) lists the  $GTLREF\_DATA\_MID$ ,  $GTLREF\_DATA\_END$ ,  $GTLREF\_ADD\_MID$ , and  $GTLREF\_ADD\_END$  specifications.

The AGTL+ reference voltages ( $GTLREF\_DATA\_MID$ ,  $GTLREF\_DATA\_END$ ,  $GTLREF\_ADD\_MID$ , and  $GTLREF\_ADD\_END$ ) must be generated on the baseboard using high precision voltage divider circuits. Refer to the appropriate platform design guidelines for implementation details.



Table 2-17. AGTL+ Bus Voltage Definitions

| Symbol                             | Parameter                        | Min                    | Typ             | Max                    | Units    | Notes <sup>1</sup> |
|------------------------------------|----------------------------------|------------------------|-----------------|------------------------|----------|--------------------|
| GTLREF_DATA_MID<br>GTLREF_DATA_END | Data Bus Reference Voltage       | $0.98 * 0.67 * V_{TT}$ | $0.67 * V_{TT}$ | $1.02 * 0.67 * V_{TT}$ | V        | 2, 3               |
| GTLREF_ADD_MID<br>GTLREF_ADD_END   | Address Bus Reference Voltage    | $0.98 * 0.67 * V_{TT}$ | $0.67 * V_{TT}$ | $1.02 * 0.67 * V_{TT}$ | V        | 2, 3               |
| $R_{TT}$                           | Termination Resistance (pull up) | 45                     | 50              | 55                     | $\Omega$ | 4                  |
| COMP                               | COMP Resistance                  | 49.4                   | 49.9            | 50.4                   | $\Omega$ | 5                  |

**Notes:**

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- The tolerances for this specification have been stated generically to enable system designer to calculate the minimum values across the range of  $V_{TT}$ .
- GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END is generated from  $V_{TT}$  on the baseboard by a voltage divider of 1% resistors. The minimum and maximum specifications account for this resistor tolerance. Refer to the appropriate platform design guidelines for implementation details. The  $V_{TT}$  referred to in these specifications is the instantaneous  $V_{TT}$ .
- $R_{TT}$  is the on-die termination resistance measured at  $V_{OL}$  of the AGTL+ output driver. Measured at  $0.31 * V_{TT}$ .  $R_{TT}$  is connected to  $V_{TT}$  on die. Refer to processor I/O Buffer Models for I/V characteristics.
- COMP resistance must be provided on the system board with +/- 1% resistors. See the applicable platform design guide for implementation details.

Table 2-18. FSB Differential BCLK Specifications

| Symbol                          | Parameter                       | Min                                | Typ   | Max                                | Unit    | Figure        | Notes <sup>1,2</sup> |
|---------------------------------|---------------------------------|------------------------------------|-------|------------------------------------|---------|---------------|----------------------|
| $V_{IL}$                        | Single-ended Input Low Voltage  | -0.150                             | 0.0   | 0.15                               | V       | 2-13          |                      |
| $V_{IH}$                        | Single-ended Input High Voltage | 0.660                              | 0.710 | 0.850                              | V       | 2-13          |                      |
| $V_{CROSS(abs)}$                | Absolute Crossing Point         | 0.250                              | 0.350 | 0.550                              | V       | 2-13,<br>2-14 | 2,8                  |
| $V_{CROSS(rel)}$                | Relative Crossing Point         | $0.250 + 0.5 * (V_{Havg} - 0.700)$ | N/A   | $0.550 + 0.5 * (V_{Havg} - 0.700)$ | V       | 2-13,<br>2-14 | 3,8,9, 11            |
| $\Delta V_{CROSS}$              | Vcross variation                | N/A                                | N/A   | 0.140                              | V       | 2-13,<br>2-14 |                      |
| $V_{MAX}$ (Absolute Overshoot)  | Single-ended maximum voltage    | N/A                                | N/A   | 1.15                               | V       | 2-13          | 4                    |
| $V_{MIN}$ (Absolute Undershoot) | Single-ended minimum voltage    | -0.300                             | N/A   | N/A                                | V       | 2-13          | 5                    |
| $V_{RBM}$                       | Single-ended Ringback Margin    | 0.200                              | N/A   | N/A                                | V       | 2-13          | 6                    |
| $V_{TR}$                        | Single-ended Threshold Region   | $V_{CROSS} - 0.100$                | N/A   | $V_{CROSS} + 0.100$                | V       | 2-13          | 7                    |
| $I_{LI}$                        | Input Leakage Current           | N/A                                | N/A   | +/- 100                            | $\mu A$ |               | 10                   |

**Notes:**

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- Crossing Voltage is defined as the instantaneous voltage value when the rising edge of BCLK0 is equal to the falling edge of BCLK1.
- $V_{Havg}$  is the statistical average of the  $V_H$  measured by the oscilloscope.
- Overshoot is defined as the absolute value of the maximum voltage.
- Undershoot is defined as the absolute value of the minimum voltage.
- Ringback Margin is defined as the absolute voltage difference between the maximum Rising Edge Ringback and the maximum Falling Edge Ringback.
- Threshold Region is defined as a region entered around the crossing point voltage in which the differential receiver switches. It includes input threshold hysteresis.
- The crossing point must meet the absolute and relative crossing point specifications simultaneously.
- $V_{Havg}$  can be measured directly using "Vtop" on Agilent and "High" on Tektronix oscilloscopes.
- For  $V_{IN}$  between 0 V and  $V_H \Delta V_{CROSS}$  is defined as the total variation of all crossing voltages as defined in note 2.



## 2.12 Front Side Bus AC Specifications

The processor FSB timings specified in this section are defined at the processor core (pads). Therefore, proper simulation of the FSB is the only means to verify proper timing and signal quality.

See [Table 4-1](#) for the pin listing and [Table 5-1](#) for signal definitions. [Table 2-19](#) through [Table 2-24](#) list the AC specifications associated with the processor FSB.

All AGTL+ timings are referenced to GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END for both '0' and '1' logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the processor signal integrity models provided by Intel. AGTL+ layout guidelines are also available in the appropriate platform design guidelines.

**Note:** Care should be taken to read all notes associated with a particular timing parameter.

**Table 2-19. Front Side Bus Differential Clock AC Specifications**

| T# Parameter                               | Min     | Max     | Unit | Figure | Notes <sup>1</sup> |
|--------------------------------------------|---------|---------|------|--------|--------------------|
| FSB Clock Frequency                        | 265.247 | 266.745 | MHz  |        | 2                  |
| T1: BCLK[1:0] Period                       | 3.7489  | 3.7700  | ns   | 2-13   | 3                  |
| T2: BCLK[1:0] Period Stability             | N/A     | 150     | ps   |        | 4                  |
| T3: BCLK[1:0] Rise Time                    | 175     | 700     | ps   |        | 5                  |
| T4: BCLK[1:0] Fall Time                    | 175     | 700     | ps   |        | 5                  |
| Differential Rising and Falling Edge Rates | 0.6     | 4       | V/ns |        | 7                  |

**Notes:**

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- The processor core clock frequency is derived from BCLK. The bus clock to processor core clock ratio is determined during initialization as described in [Section 2.3](#). [Table 2-1](#) includes core frequency to FSB multipliers.
- The period specified here is the average period. A given period may vary from this specification as governed by the period stability specification (T2).
- In this context, period stability is defined as the worst case timing difference between successive crossover voltages. In other words, the largest absolute difference between adjacent clock periods must be less than the period stability.
- Rise and fall times are measured single ended between 245 mV and 455 mV of the clock swing.
- Measured from -200 mV to +200 mV. The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero.

**Table 2-20. Front Side Bus Common Clock AC Specifications**

| T# Parameter                         | Min   | Max  | Unit | Figure | Notes <sup>1, 2, 3</sup> |
|--------------------------------------|-------|------|------|--------|--------------------------|
| T10: Common Clock Output Valid Delay | 0.22  | 1.10 | ns   | 2-16   | 4                        |
| T11: Common Clock Input Setup Time   | 0.650 | N/A  | ns   | 2-16   | 5                        |
| T12: Common Clock Input Hold Time    | 0.150 | N/A  | ns   | 2-16   | 5                        |
| T13: RESET# Pulse Width              | 1     | 10   | ms   | 2-24   | 6, 7, 8                  |

**Notes:**

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- Not 100% tested. Specified by design characterization.
- All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (VCROSS) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced at nominal GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END at the processor core (pads).
- Valid delay timings for these signals are specified into the test circuit described in [Figure 2-11](#) and with GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END at  $0.67 \cdot V_{TT}$ .



5. Specification is for a minimum swing is specified into the test circuit described in Figure 2-11 and defined between  $AGTL + V_{IL\_MAX}$  to  $V_{IH\_MIN}$ . This assumes an edge rate of 2.0 V/ns to 3.0 V/ns.
6. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
7. This should be measured after  $V_{TT}$  and BCLK[1:0] become stable.
8. Maximum specification applies only while PWRGOOD is asserted.

Table 2-21. FSB Source Synchronous AC Specifications

| T# Parameter                                                           | Min                    | Max  | Unit | Figure     | Notes 1, 2, 3, 4 |
|------------------------------------------------------------------------|------------------------|------|------|------------|------------------|
| T20: Source Sync. Output Valid Delay (first data/address only)         | 0.00                   | 1.10 | ns   | 2-17, 2-18 | 5                |
| T21: $T_{VBD}$ Source Sync. Data Output Valid Before Data Strobe       | 0.270                  |      | ns   | 2-18       | 5,8              |
| T22: $T_{VAD}$ Source Sync. Data Output Valid After Data Strobe        | 0.270                  |      | ns   | 2-18       | 5,9              |
| T23: $T_{VBA}$ Source Sync. Address Output Valid Before Address Strobe | 0.660                  |      | ns   | 2-17       | 5,8              |
| T24: $T_{VAA}$ Source Sync. Address Output Valid After Address Strobe  | 0.660                  |      | ns   | 2-17       | 5,9              |
| T25: $T_{SUSS}$ Data Input Setup Time                                  | 0.190                  |      | ns   | 2-17 2-18  | 6                |
| T25: $T_{SUSS}$ Address Input Setup Time                               | 0.300                  |      | ns   | 2-17, 2-18 | 6                |
| T26: $T_{HSS}$ Data Input Hold Time                                    | 0.190                  |      | ns   | 2-17, 2-18 | 6                |
| T26: $T_{HSS}$ Address Input Hold Time                                 | 0.300                  |      | ns   | 2-17, 2-18 | 6                |
| T27: Source Synchronous Address Strobe Setup Time to BCLK[1:0]         | 3.5 -<br>(1.875 * n)   |      | ns   | 2-17       | 12, 14, 15       |
| T28: Source Synchronous Data Strobe Setup Time to BCLK[1:0]            | 4.15 -<br>(0.9375 * n) |      | ns   | 2-18       | 11,14            |
| T30: Data Strobe 'n' (DSTBN#) Output Valid Delay                       | 3.28                   | 4.38 | ns   | 2-18       | 13               |
| T31: Address Strobe Output Valid Delay                                 | 2.81                   | 3.91 | ns   | 2-17       |                  |

**Notes:**

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All source synchronous AC timings are referenced to their associated strobe at nominal GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced at nominal GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END at the processor core (pads).
4. Unless otherwise noted, these specifications apply to both data and address timings.
5. Valid delay timings for these signals are specified into the test circuit described in Figure 2-11 and with GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END at  $0.67 * V_{TT}$ .
6. Specification is for a minimum swing into the test circuit described in Figure 2-11 and defined between  $AGTL + V_{IL\_MAX}$  to  $V_{IH\_MIN}$ . This assumes an edge rate of 3.0 V/ns to 5.5 V/ns.
7. All source synchronous signals must meet the specified setup time to BCLK as well as the setup time to each respective strobe.
8. This specification represents the minimum time the data or address will be valid before its strobe. Refer to the appropriate platform design guidelines for more information on the definitions and use of these specifications.
9. This specification represents the minimum time the data or address will be valid after its strobe. Refer to the appropriate platform design guidelines for more information on the definitions and use of these specifications.
10. The rising edge of ADSTB# must come approximately 1/2 BCLK period after the falling edge of ADSTB#.
11. For this timing parameter, n = 1, 2, and 3 for the second, third, and last data strobes respectively.
12. The address strobe setup time is measured with respect to T2. Calculation of the setup time is as follows.:
  - a. If  $T27 > \text{BCLK period}$ , then the setup time calculated is positive. The value calculated indicates setup time before T1.
  - b. If  $T27 < \text{BCLK period}$ , then the setup time calculated is negative. The value calculated indicates setup time after T1. Refer to Figure 2-17.
13. This specification applies only to DSTBN[3:0]# and is measured to the second falling edge of the strobe.
14. This specification reflects a typical value, not a minimum or maximum.
15. For this timing parameter, n = 0 to 1.



**Table 2-22. Miscellaneous GTL+ AC Specifications**

| T# Parameter                                            | Min  | Max | Unit  | Figure | Notes<br>1, 2, 3, 4 |
|---------------------------------------------------------|------|-----|-------|--------|---------------------|
| T35: Asynchronous GTL+ input pulse width                | 30   |     | ns    |        | 5                   |
| T36: PWRGOOD assertion to RESET# de-assertion           | 1    | 10  | ms    | 2-24   |                     |
| T37: BCLK stable to PWRGOOD assertion                   | 10   |     | BCLKs | 2-24   | 6,12                |
| T38: PROCHOT# pulse width                               | 500  |     | μs    | 2-20   | 7                   |
| T39: THERMTRIP# assertion until V <sub>CC</sub> removed |      | 500 | ms    | 2-21   | 8                   |
| T40: FERR# valid delay from STPCLK# deassertion         | 0    | 5   | BCLKs | 2-25   |                     |
| T41: V <sub>CC</sub> stable to PWRGOOD assertion        | 0.05 | 500 | ms    | 2-24   | 10                  |
| T42: PWRGOOD rise time                                  |      | 20  | ns    |        | 11                  |
| T43: V <sub>CC_BOOT</sub> stable to VID / BSEL valid    | 10   |     | μs    | 2-24   | 9,10                |
| T44: VID / BSEL valid to V <sub>CC</sub> stable         | 100  |     | μs    | 2-24   | 10                  |
| T48: V <sub>TT</sub> stable to VID / BSEL valid         | 10   |     | μs    | 2-24   | 10                  |
| T49: V <sub>CCPLL</sub> stable to PWRGOOD assertion     | 1    |     | ms    | 2-24   | 10                  |

**Notes:**

- Unless otherwise noted, all specifications in this table apply to all processor frequencies.
- All AC timings for the Asynchronous GTL+ signals are referenced to the BCLK0 rising edge at Crossing Voltage (V<sub>CROSS</sub>). PWRGOOD is referenced to BCLK0 rising edge at 0.5 \* V<sub>TT</sub>.
- These signals may be driven asynchronously.
- Refer to [Section 7.2](#) for additional timing requirements for entering and leaving low power states.
- A minimum pulse width of 500 μs is recommended when FORCEPR# is asserted by the system.
- Refer to the PWRGOOD signal definition in [Section 5](#) for more details information on behavior of the signal.
- Length of assertion for PROCHOT# does not equal TCC activation time. Time is required after the assertion and before the deassertion of PROCHOT# for the processor to enable or disable the TCC.
- Intel recommends the V<sub>TT</sub> power supply also be removed upon assertion of THERMTRIP#.
- This specification requires that the VID and BSEL signals be sampled no earlier than 10 μs after V<sub>CC</sub> (at V<sub>CC\_BOOT</sub> voltage) and V<sub>TT</sub> are stable.
- Parameter must be measured after applicable voltage level is stable. "Stable" means that the power supply is in regulation as defined by the minimum and maximum DC/AC specifications for all components being powered by it.
- The maximum PWRGOOD rise time specification denotes the slowest allowable rise time for the processor. Measured between (0.3 \* V<sub>TT</sub>) and (0.7 \* V<sub>TT</sub>).
- See [Table 2-19](#) for BCLK specifications.

**Table 2-23. Front Side Bus AC Specifications (Reset Conditions)**

| T# Parameter                                                                  | Min | Max | Unit  | Figure | Notes |
|-------------------------------------------------------------------------------|-----|-----|-------|--------|-------|
| T45: Reset Configuration Signals (A[39:3]#, BR[1:0]#, INIT#, SMI#) Setup Time | 480 |     | μs    | 2-24   | 1     |
| T46: Reset Configuration Signals (A[39:3]#, INIT#, SMI#) Hold Time            | 2   | 20  | BCLKs | 2-24   | 2     |
| T47: Reset Configuration Signals BR[1:0]# Hold Time                           | 2   | 2   | BCLKs | 2-24   | 2     |

**Notes:**

- Before the clock that de-asserts RESET#
- After the clock that de-asserts RESET#.

**Table 2-24. TAP Signal Group AC Specifications (Sheet 1 of 2)**

| T# Parameter             | Min | Max | Unit | Figure | Notes<br>1, 2, 8 |
|--------------------------|-----|-----|------|--------|------------------|
| T55: TCK Period          | 30  |     | ns   | 2-12   | 3                |
| T56: TDI, TMS Setup Time | 7.5 |     | ns   | 2-19   | 4,7              |



Table 2-24. TAP Signal Group AC Specifications (Sheet 2 of 2)

| T# Parameter                   | Min | Max | Unit             | Figure | Notes<br>1, 2, 8 |
|--------------------------------|-----|-----|------------------|--------|------------------|
| T57: TDI, TMS Hold Time        | 7.5 |     | ns               | 2-19   | 4, 7             |
| T58: TDO Clock to Output Delay | 0   | 7.5 | ns               | 2-19   | 5                |
| T59: TRST# Assert Time         | 2   |     | T <sub>TCK</sub> | 2-20   | 6                |

**Notes:**

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. This specification is based on the capabilities of the ITP debug port, not on processor silicon.
4. Referenced to the rising edge of TCK.
5. Referenced to the falling edge of TCK.
6. TRST# must be held asserted for 2 TCK periods to be guaranteed that it is recognized by the processor.
7. Specification for a minimum swing defined between TAP  $V_{t-}$  to  $V_{t+}$ . This assumes a minimum edge rate of 0.5 V/ns.
8. It is recommended that TMS be asserted while TRST# is being deasserted.



**Table 2-25. VID Signal Group AC Specifications**

| T # Parameter                                           | Min | Max | Unit | Figure    | Notes <sup>1, 2</sup> |
|---------------------------------------------------------|-----|-----|------|-----------|-----------------------|
| T80: VID Step Time                                      | 5   |     | μs   | 2-27      |                       |
| T81: VID Dwell Time at 266.666 MHz FSB                  | 500 |     | μs   | 2-27      |                       |
| T82: VID Down Transition to Valid V <sub>CC</sub> (min) |     | 0   | μs   | 2-26,2-27 |                       |
| T83: VID Up Transition to Valid V <sub>CC</sub> (min)   |     | 50  | μs   | 2-26,2-27 |                       |
| T84: VID Down Transition to Valid V <sub>CC</sub> (max) |     | 50  | μs   | 2-26,2-27 |                       |
| T85: VID Up Transition to Valid V <sub>CC</sub> (max)   |     | 0   | μs   | 2-26,2-27 |                       |

**Notes:**

1. See *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0 Design Guidelines* for addition information.
2. Platform support for VID transitions is required for the processor to operate within specifications.

**Table 2-26. SMBus Signal Group AC Specifications**

| T# Parameter                                   | Min  | Max | Unit | Figure | Notes 1, 2 |
|------------------------------------------------|------|-----|------|--------|------------|
| T90: SM_CLK Frequency                          | 10   | 100 | KHz  |        |            |
| T91: SM_CLK Period                             | 10   | 100 | μs   |        |            |
| T92: SM_CLK High Time                          | 4.0  | N/A | μs   | 2-22   |            |
| T93: SM_CLK Low Time                           | 4.7  | N/A | μs   | 2-22   |            |
| T94: SMBus Rise Time                           | 0.02 | 1.0 | μs   | 2-22   | 3          |
| T95: SMBus Fall Time                           | 0.02 | 0.3 | μs   | 2-22   | 3          |
| T96: SMBus Output Valid Delay                  | 0.1  | 4.5 | μs   | 2-23   |            |
| T97: SMBus Input Setup Time                    | 250  | N/A | ns   | 2-22   |            |
| T98: SMBus Input Hold Time                     | 300  | N/A | ns   | 2-22   |            |
| T99: Bus Free Time                             | 4.7  | N/A | μs   | 2-22   | 4, 5       |
| T100: Hold Time after Repeated Start Condition | 4.0  | N/A | μs   | 2-22   |            |
| T101: Repeated Start Condition Setup Time      | 4.7  | N/A | μs   | 2-22   |            |
| T102: Stop Condition Setup Time                | 4.0  | N/A | μs   | 2-22   |            |

**Notes:**

1. These parameters are based on design characterization and are not tested.
2. All AC timings for the SMBus signals are referenced at V<sub>IL\_MAX</sub> or V<sub>IL\_MIN</sub> and measured at the processor pins. Refer to [Figure 2-23](#).
3. Rise time is measured from (V<sub>IL\_MAX</sub> - 0.15V) to (V<sub>IH\_MIN</sub> + 0.15V). Fall time is measured from (0.9 \* SM\_VCC) to (V<sub>IL\_MAX</sub> - 0.15V). DC parameters are specified in [Table 2-26](#).
4. Minimum time allowed between request cycles.
5. Following a write transaction, an internal write cycle time of 10ms must be allowed before starting the next transaction.



## 2.13 Processor AC Timing Waveforms

The following figures are used in conjunction with the AC timing tables, [Table 2-19](#) through [Table 2-25](#).

**Note:**

For [Figure 2-12](#) through [Figure 2-25](#), the following apply:

1. All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage ( $V_{CROSS}$ ) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced at nominal GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END at the processor core (pads).
2. All source synchronous AC timings for AGTL+ signals are referenced to their associated strobe (address or data) at nominal GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced at nominal GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END at the processor core (pads).
3. All AC timings for AGTL+ strobe signals are referenced to BCLK[1:0] at  $V_{CROSS}$ . All AGTL+ strobe signal timings are referenced at nominal GTLREF\_DATA\_MID, GTLREF\_DATA\_END, GTLREF\_ADD\_MID, and GTLREF\_ADD\_END at the processor core (pads).
4. All AC timings for the TAP signals are referenced to the TCK at  $0.5 * V_{TT}$  at the processor pins. All TAP signal timings (TMS, TDI, etc...) are referenced at  $0.5 * V_{TT}$  at the processor core (pads).
5. All CMOS signal timings are referenced at  $0.5 * V_{TT}$  at the processor pins.
6. All AC timings for the SMBus signals are referenced to the SM\_CLK at  $0.5 * SM\_VCC$  at the processor pins. All SMBus signal timings (SM\_DAT, SM\_CLK, etc.) are referenced at

The circuit used to test the AC specification is shown in [Figure 2-11](#).

Figure 2-11. Electrical Test Circuit

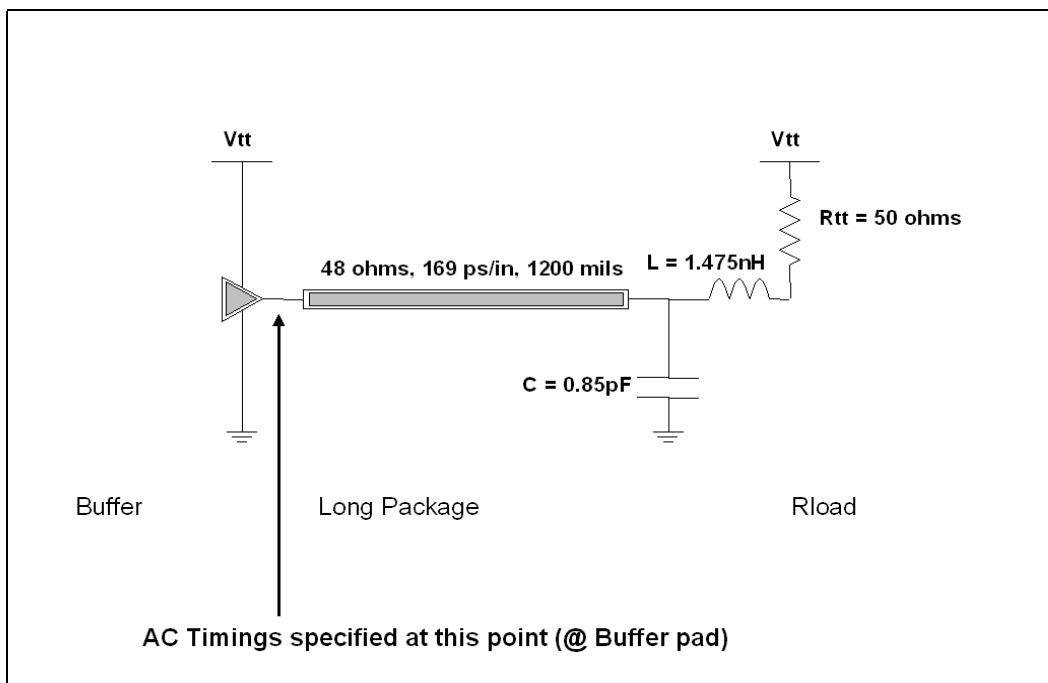


Figure 2-12. TCK Clock Waveform

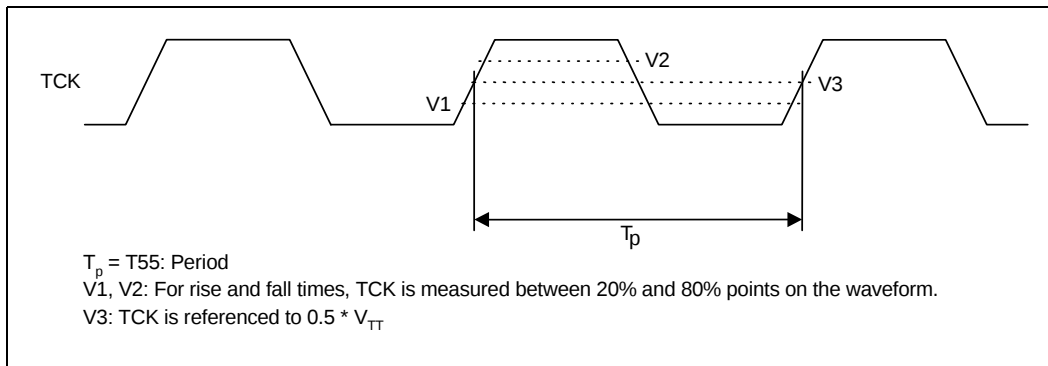




Figure 2-13. Differential Clock Waveform

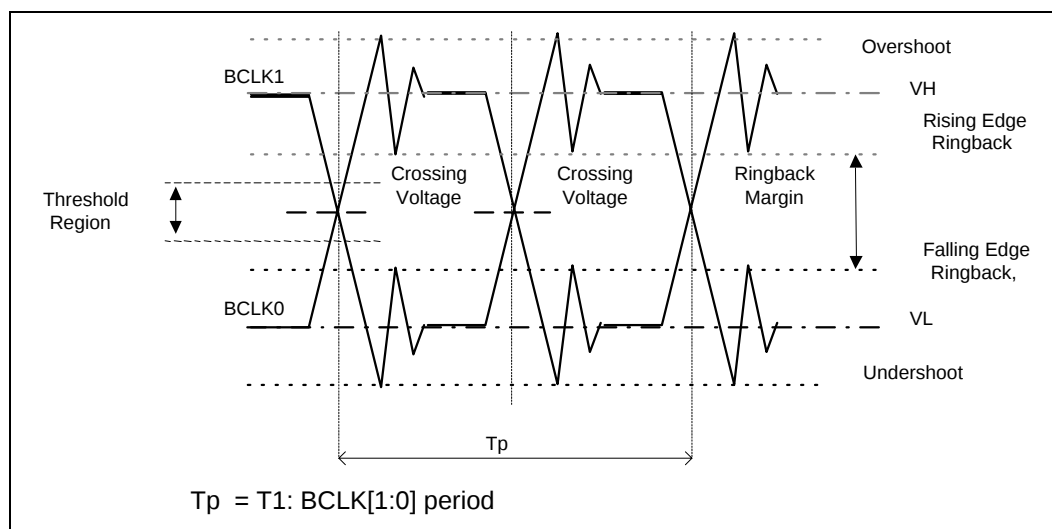


Figure 2-14. Differential Clock Crosspoint Specification

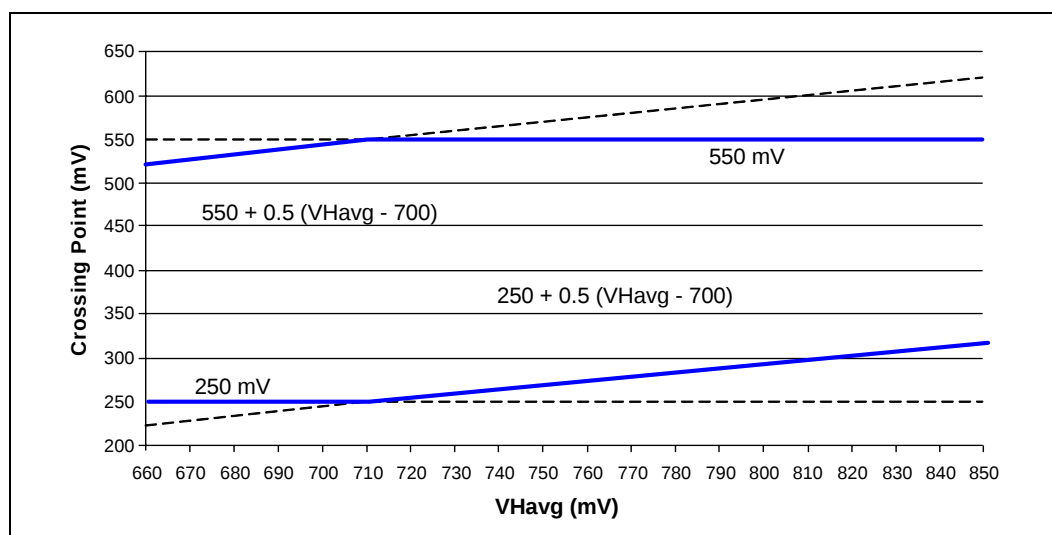
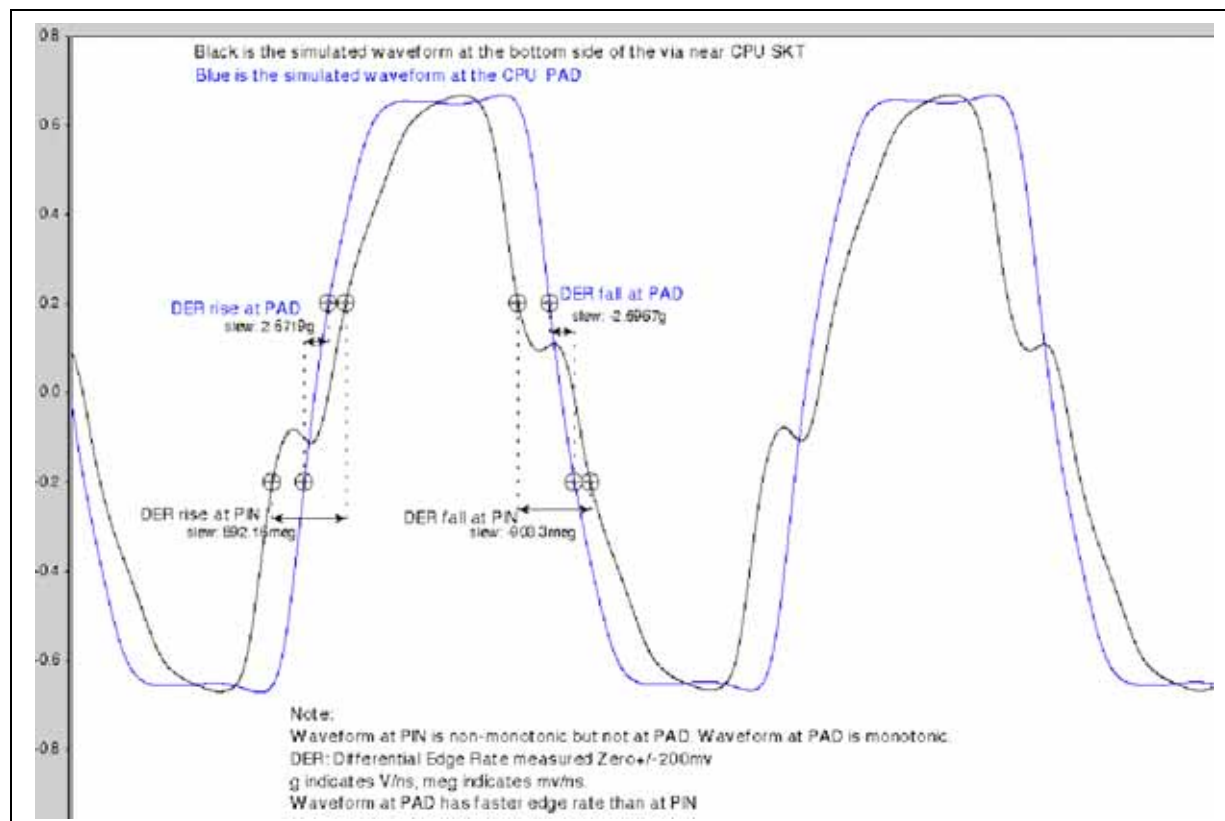


Figure 2-15. BCLK Waveform at Processor Pad and Pin


**Notes:**

1. Waveform at pin is non-monotonic. Waveform at pad is monotonic.
2. Differential Edge Rate (DER) measured zero +/- 200mv.
3. g indicates V/ns units and meg indicates mv/ns units.
4. Waveform at pad has faster edge rate than at pin.

Figure 2-16. FSB Common Clock Valid Delay Timing Waveform

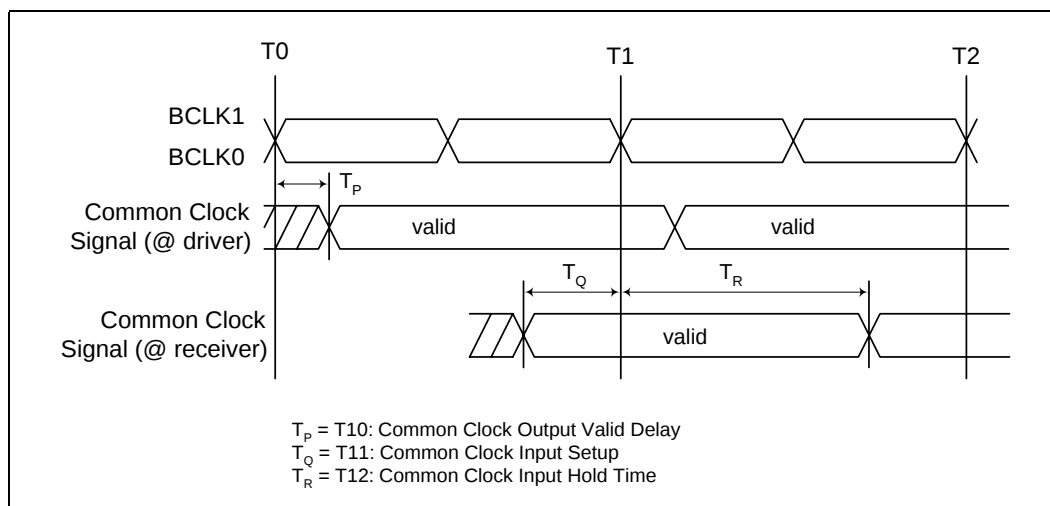




Figure 2-17. FSB Source Synchronous 2X (Address) Timing Waveform

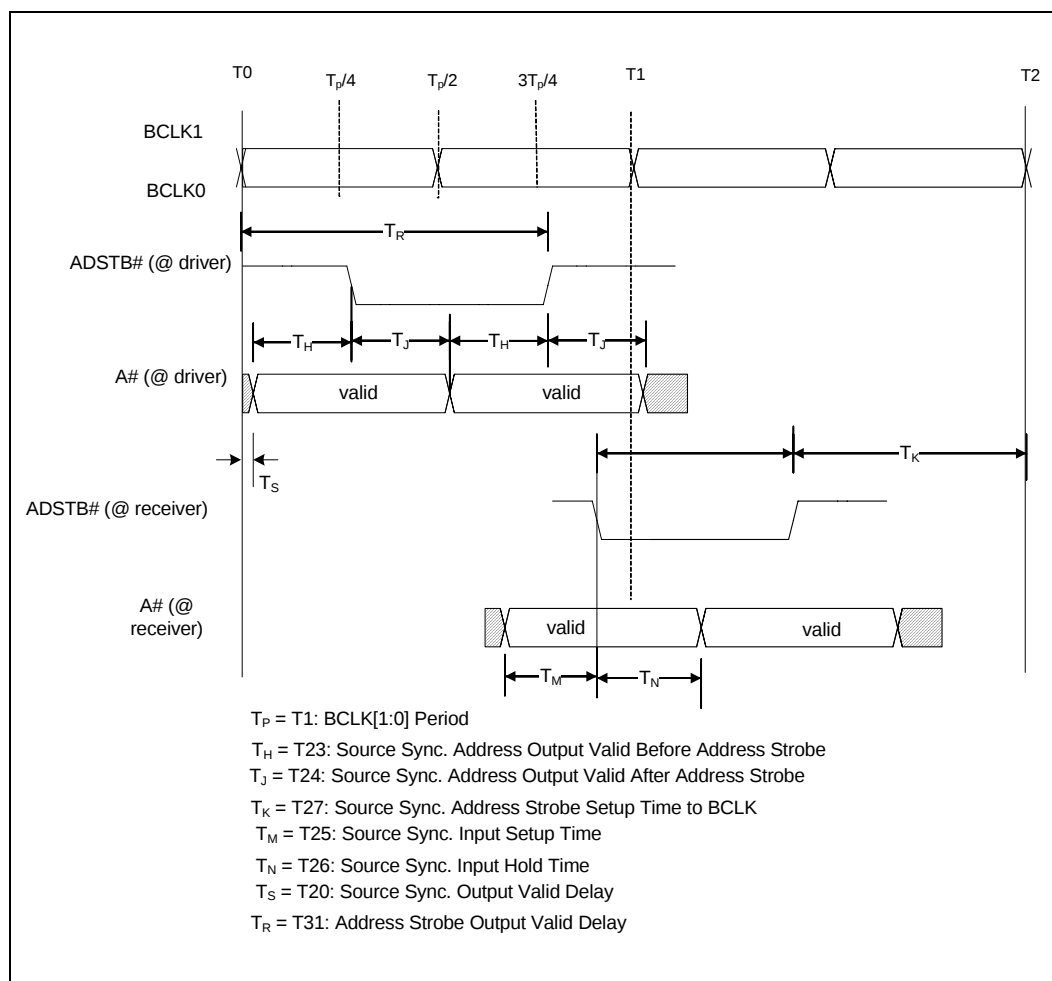


Figure 2-18. FSB Source Synchronous 4X (Data) Timing Waveform

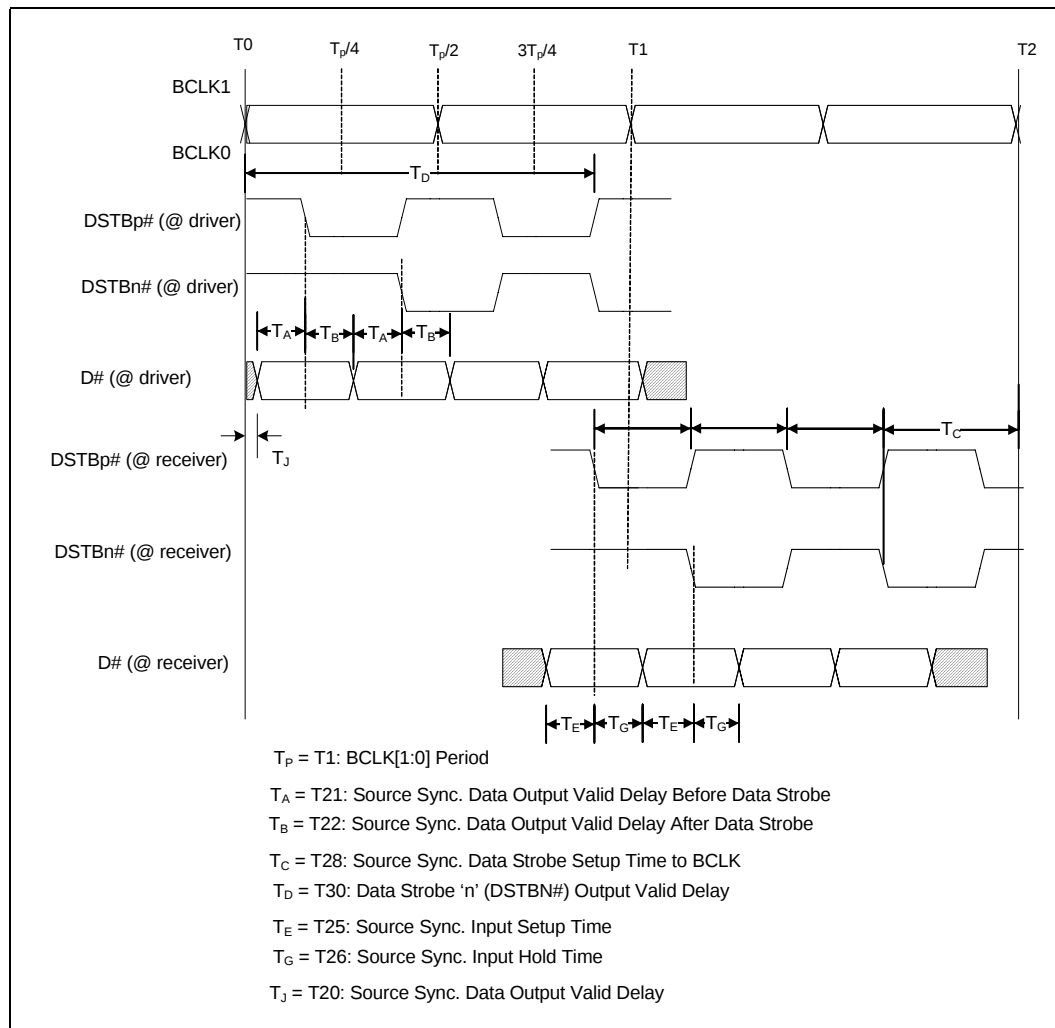
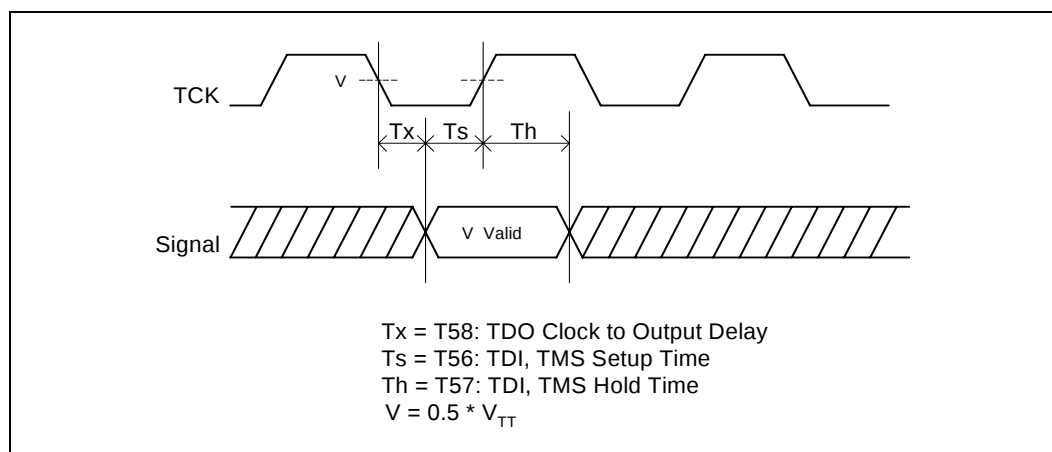


Figure 2-19. TAP Valid Delay Timing Waveform



**Note:** Please refer to Table 2-12 for TAP Signal Group DC specifications and Table 2-24 for TAP Signal Group AC specifications.

Figure 2-20. Test Reset (TRST#), Async GTL+ Input, and PROCHOT# Timing Waveform

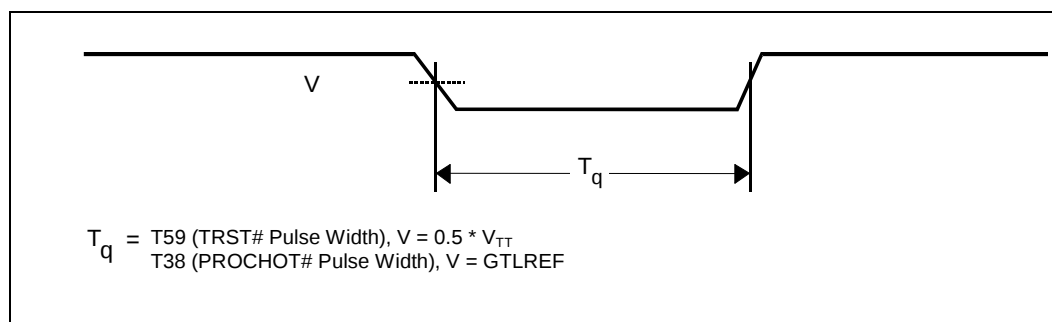


Figure 2-21. THERMTRIP# Power Down Sequence

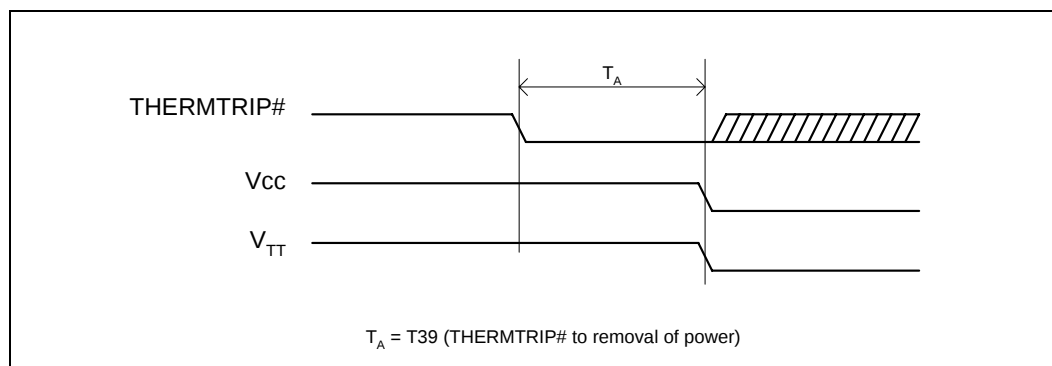


Figure 2-22. SMBus Timing Waveform

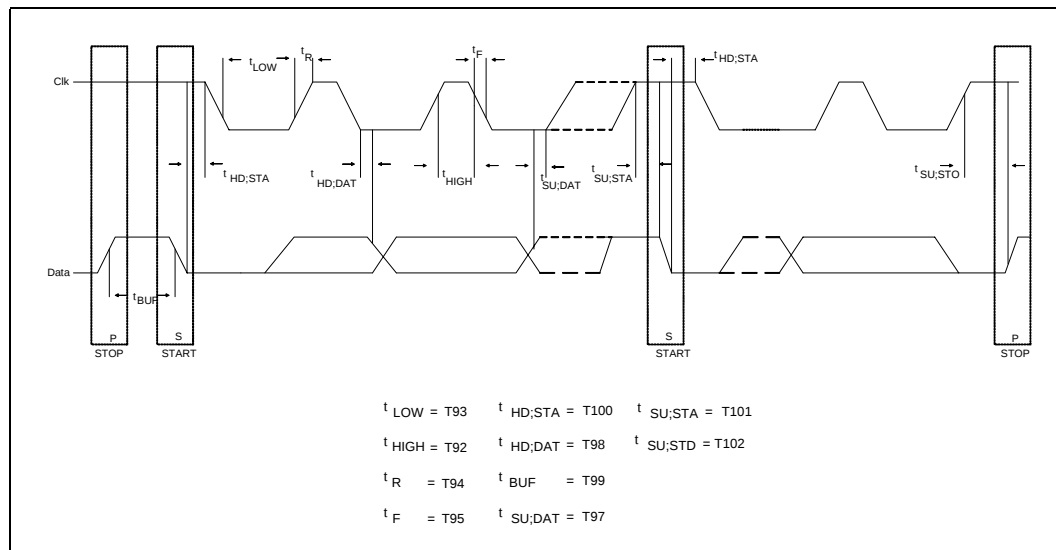


Figure 2-23. SMBus Valid Delay Timing Waveform

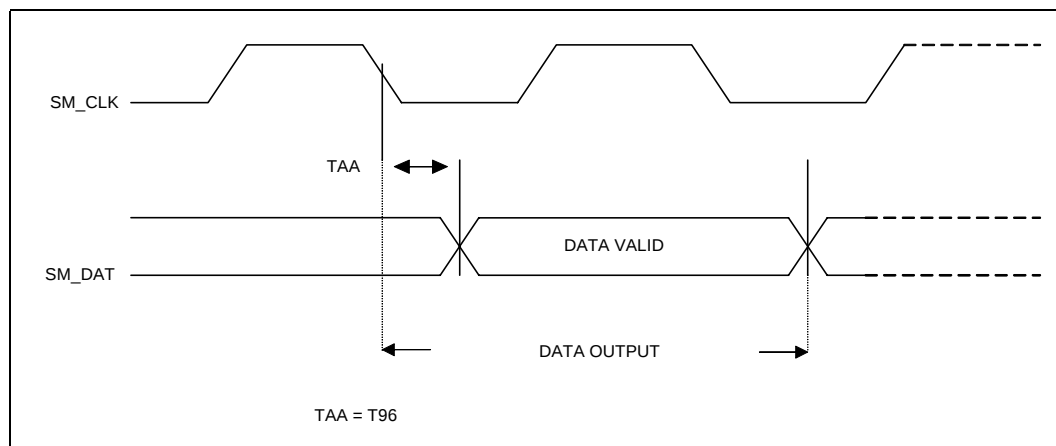




Figure 2-24. Voltage Sequence Timing Requirements

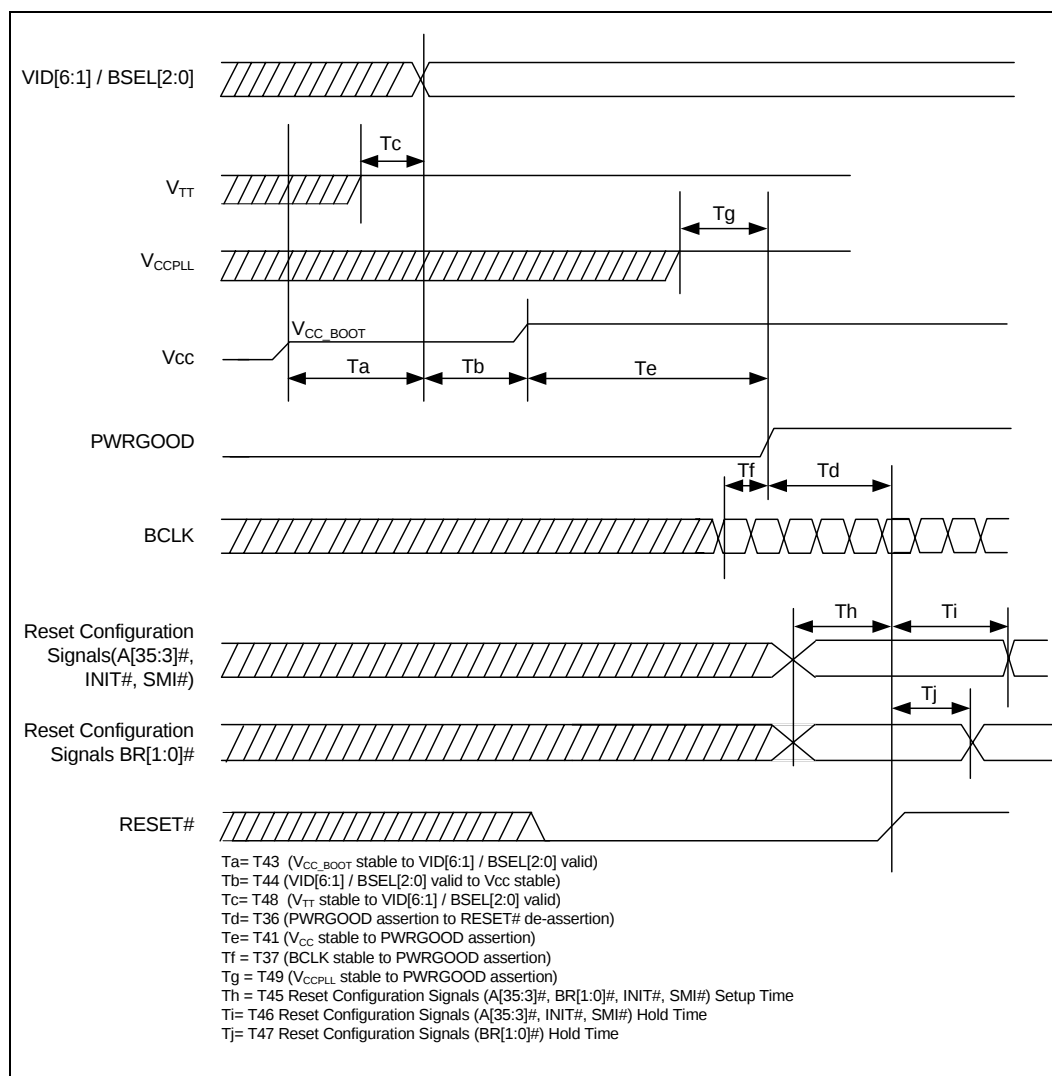
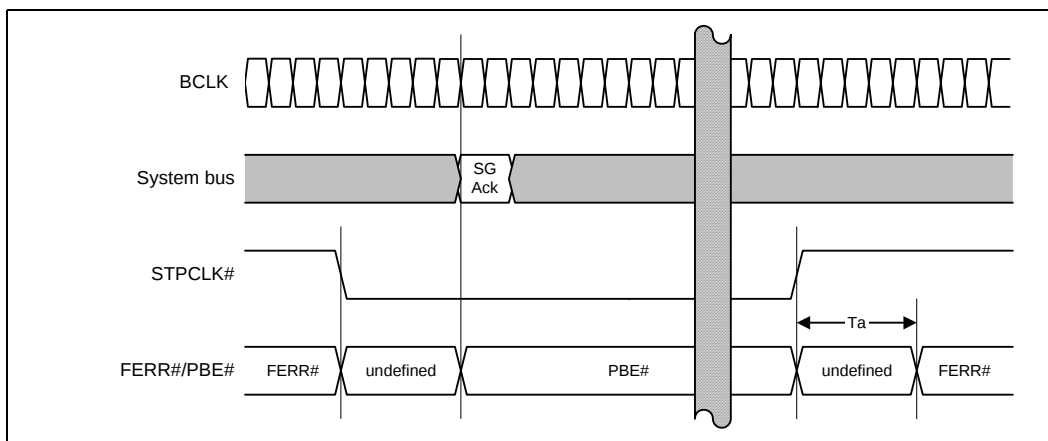


Figure 2-25. FERR# / PBE# Valid Delay Timing



**Notes:**

1.  $T_a = T40$  (FERR# Valid Delay from STPCLK# Deassertion).
2. FERR# / PBE# is undefined from STPCLK# assertion until the Stop-Grant acknowledge is driven on the FSB. FERR# / PBE# is also undefined for a period of  $T_a$  from STPCLK# deassertion. Inside these undefined regions, the PBE# signal is driven. FERR# is driven at all other times.

Figure 2-26. VID Step Timings

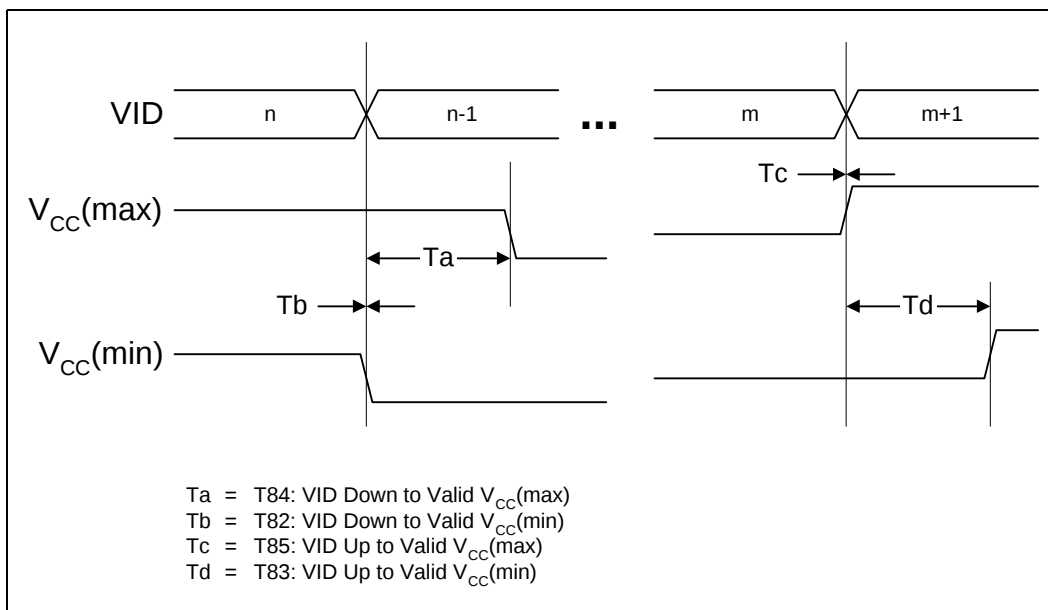
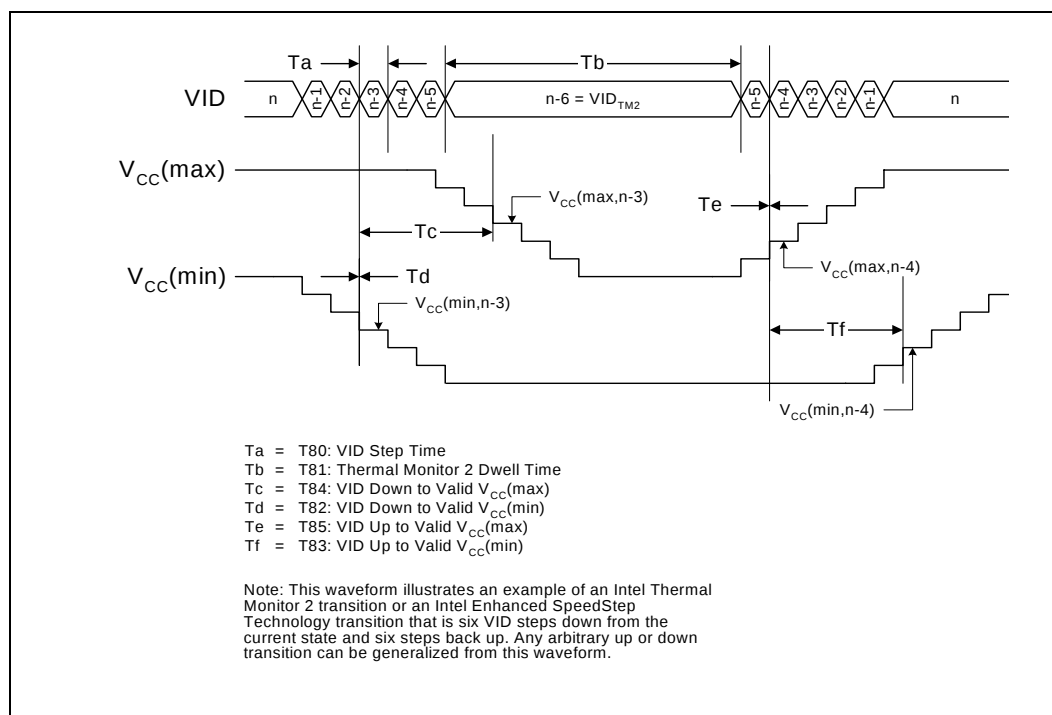




Figure 2-27. VID Step Times and Vcc Waveforms



§



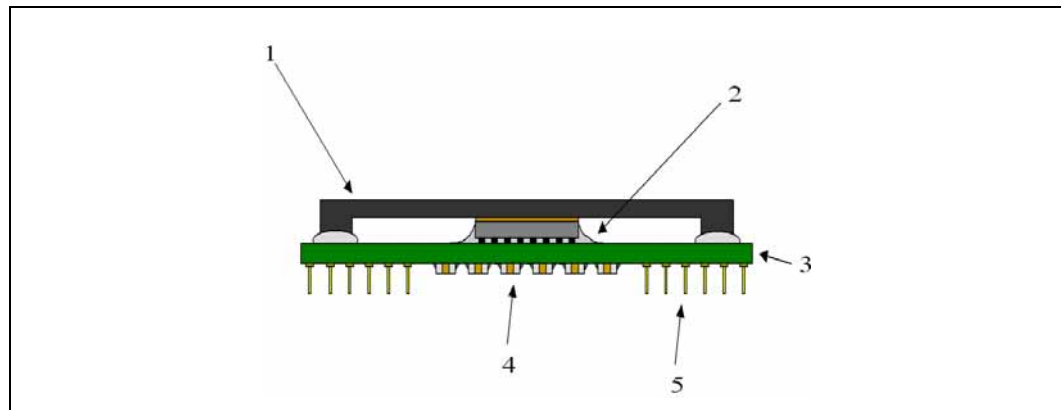
## 3 Mechanical Specifications

The Intel® Xeon® Processor 7200 Series and 7300 Series is packaged in a FC-mPGA6 package that interfaces with the motherboard via a mPGA604 socket. The package consists of two processor dies mounted on a substrate pin-carrier. An IHS is attached to the package substrate and die and serves as the mating surface for processor component thermal solutions, such as a heatsink. [Figure 3-1](#) shows a sketch of the processor package components and how they are assembled together. Refer to the *mPGA604 Socket Design Guidelines* for complete details on the mPGA604 socket.

The package components shown in [Figure 3-1](#) include the following:

1. IHS
2. Processor die
3. FC-mPGA6 package
4. Pin-side capacitors
5. Package pin

**Figure 3-1. Processor Package Assembly Sketch**



**Note:** [Figure 3-1](#) is not to scale and is for reference only. The mPGA604 socket is not shown.

### 3.1 Package Mechanical Drawing

The package mechanical drawings are shown in [Figure 3-2](#) and [Figure 3-3](#). The drawings include dimensions necessary to design a thermal solution for the processor. These dimensions include:

1. Package reference with tolerances (total height, length, width, etc.)
2. IHS parallelism and tilt
3. Pin dimensions
4. Top-side and back-side component keepout dimensions
5. Reference datums

All drawing dimension are in mm [in].

Figure 3-2.Processor Package Drawing (Sheet 1 of 2)

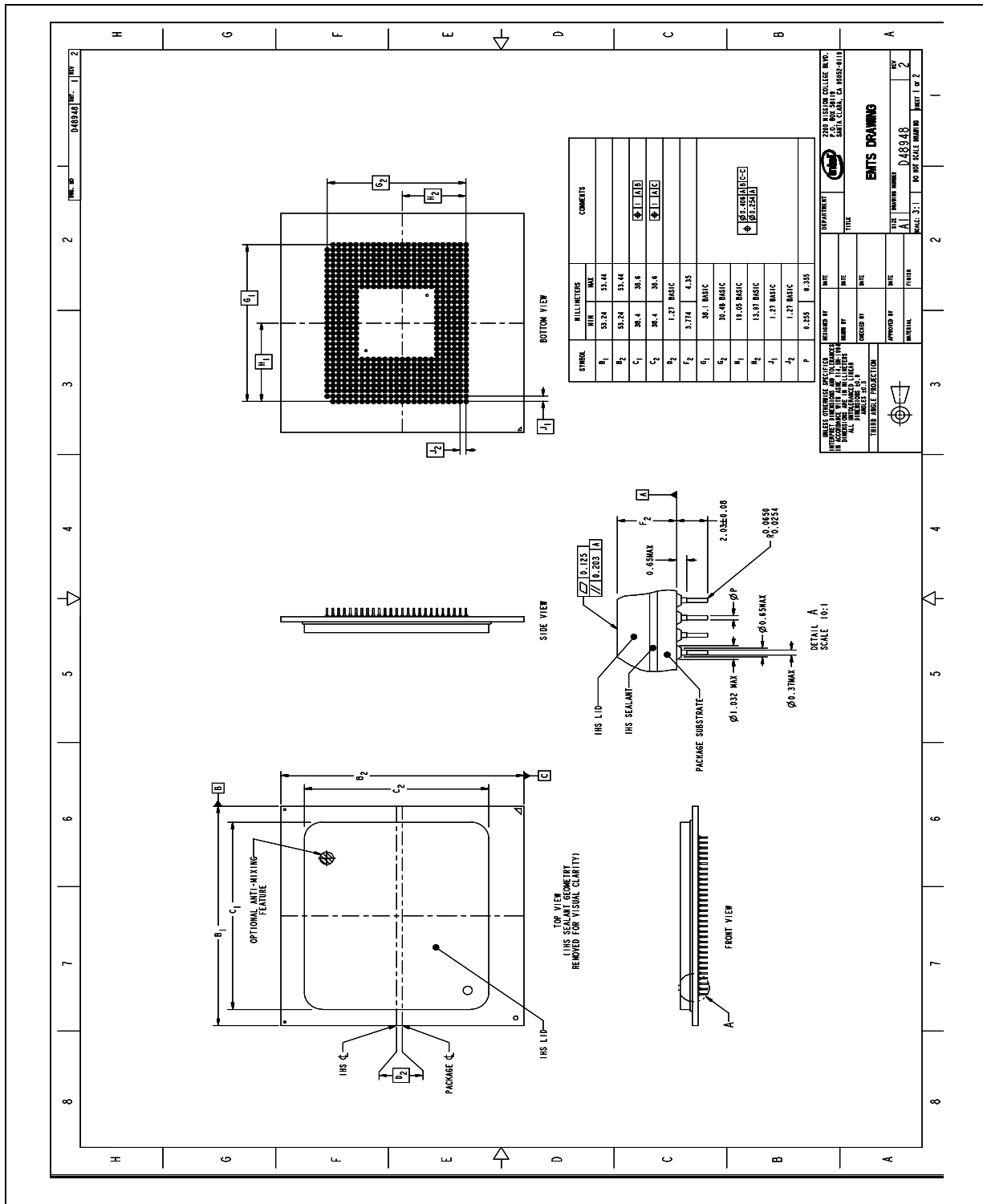
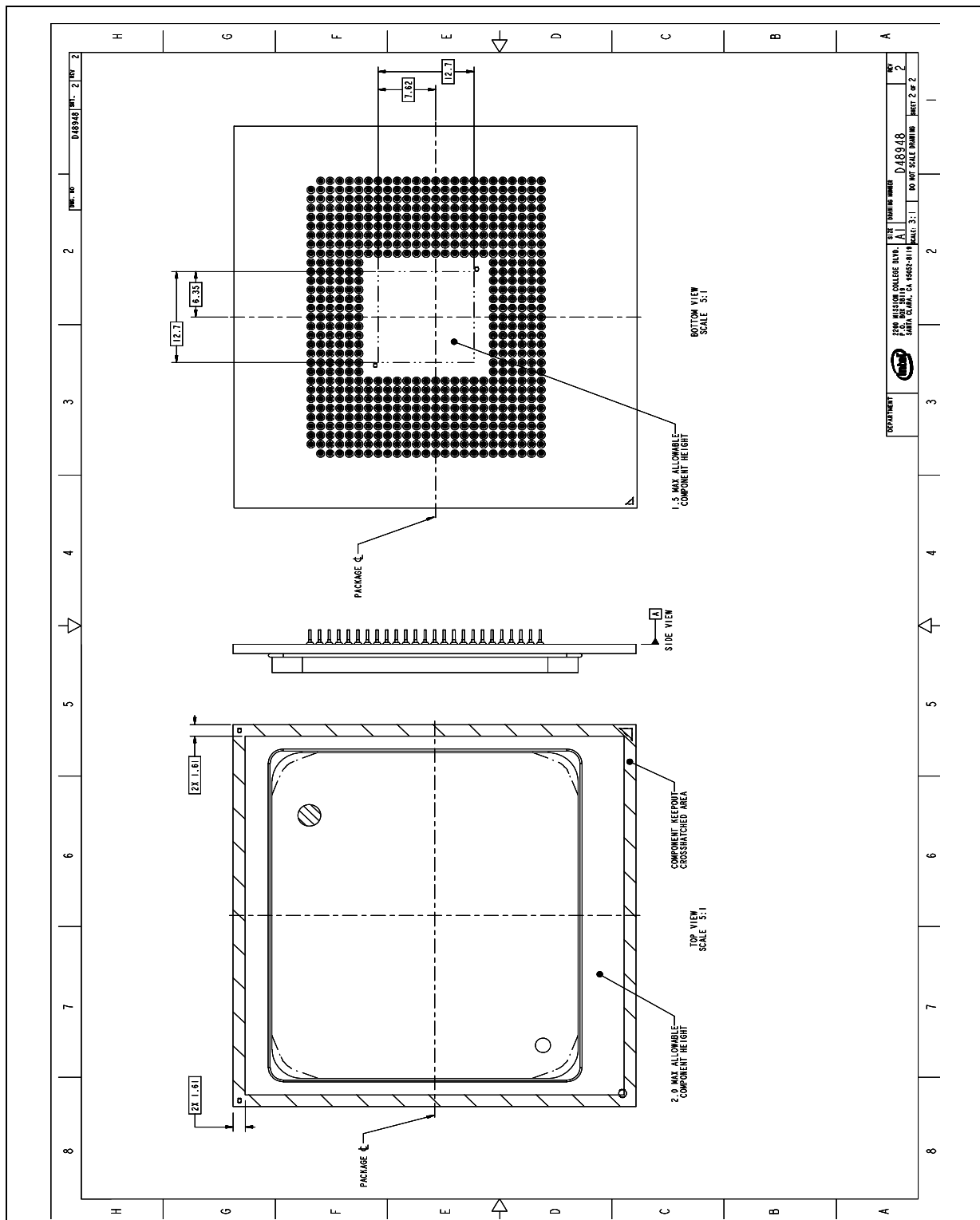


Figure 3-3.Processor Package Drawing (Sheet 2 of 2)





## 3.2 Processor Component Keepout Zones

The processor may contain components on the substrate that define component keepout zone requirements. A thermal and mechanical solution design must not intrude into the required keepout zones. Decoupling capacitors are typically mounted to either the topside or pin-side of the package substrate. See [Figure 3-4](#) and [Figure 3-5](#) for keepout zones.

61

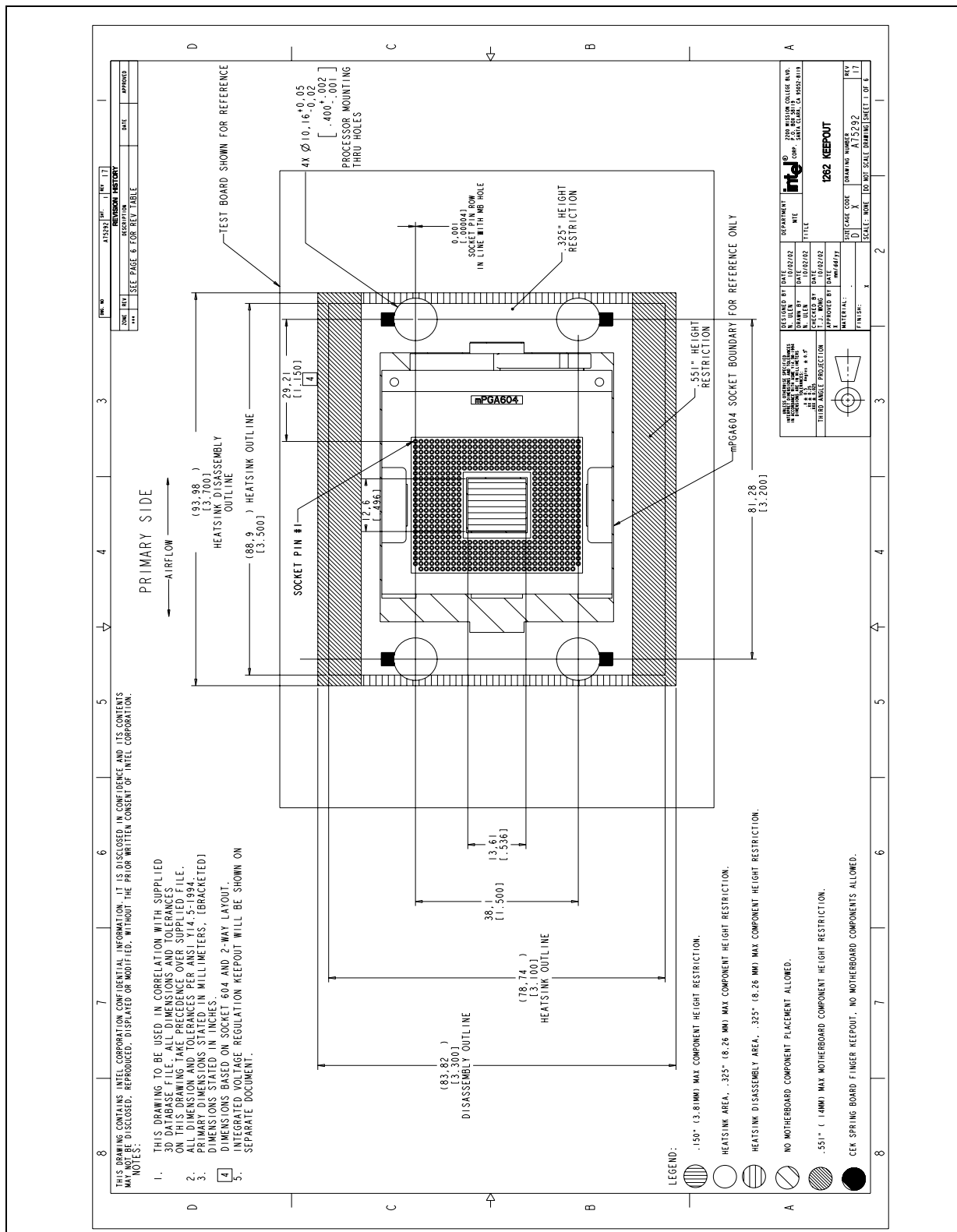
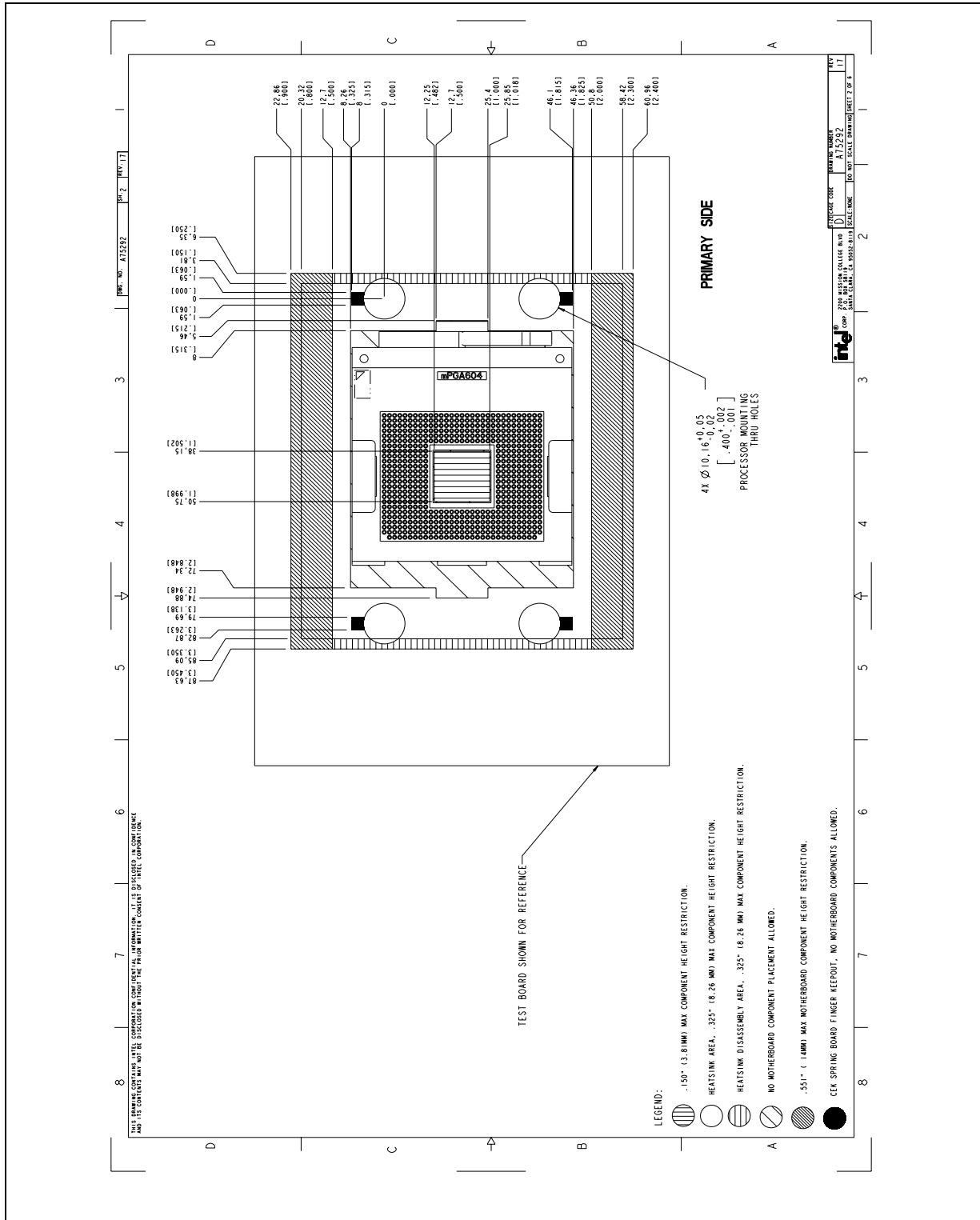


Figure 3-5.Top Side Board Keepout Zones (Part 2)



[illegible]

Figure 3-7.Board Mounting-Hole Keepout Zones

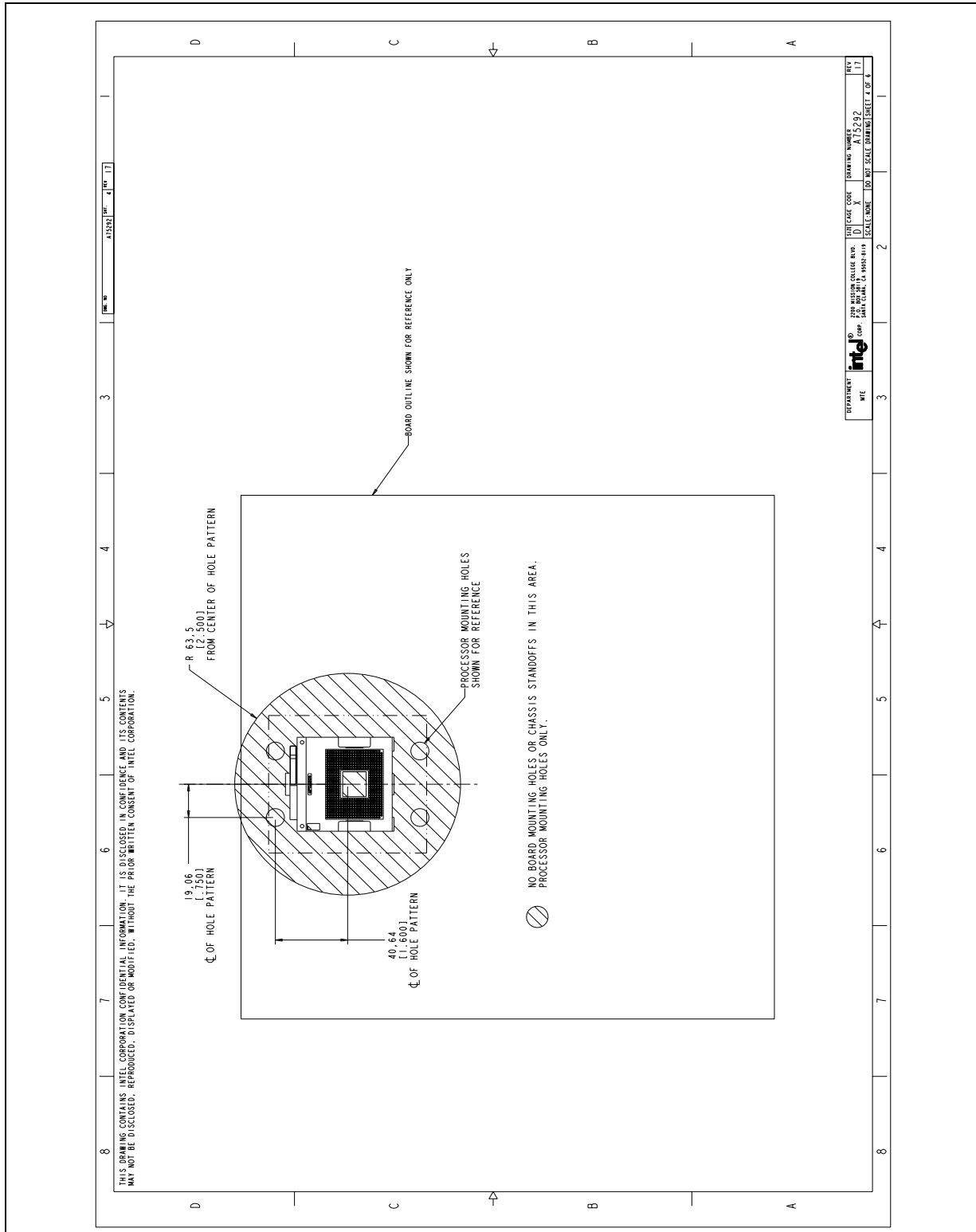
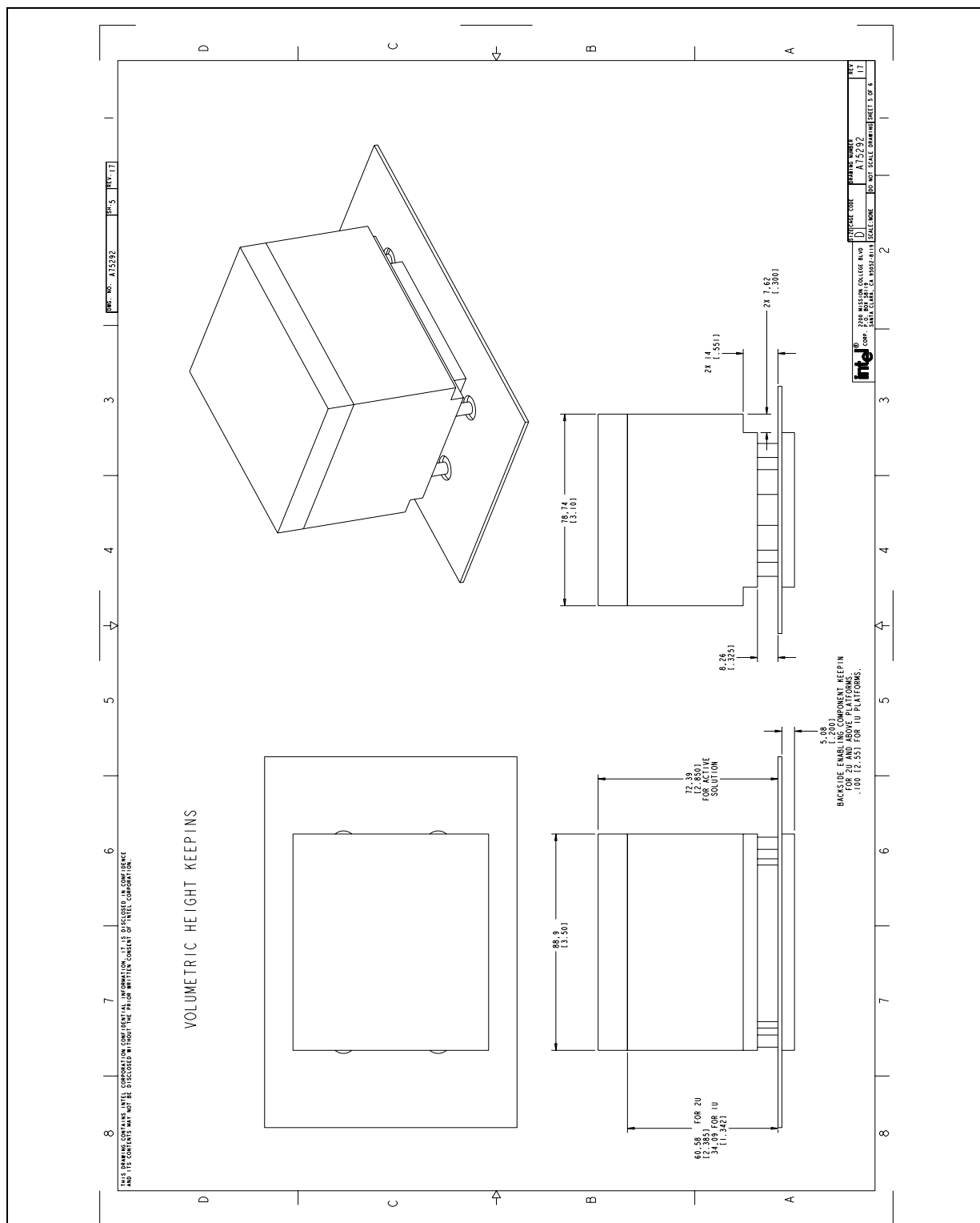


Figure 3-8. Volumetric Height Keep-Ins





### 3.3 Package Loading Specifications

Table 3-1 provides dynamic and static load specifications for the processor package. These mechanical load limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Also, any mechanical system or component testing should not exceed the maximum limits. The processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal and mechanical solutions. The minimum loading specification must be maintained by any thermal and mechanical solution.

**Table 3-1. Processor Loading Specifications**

| Parameter                | Minimum  | Maximum                                                    | Unit     | Notes         |
|--------------------------|----------|------------------------------------------------------------|----------|---------------|
| Static Compressive Load  | 44<br>10 | 222<br>50                                                  | N<br>lbf | 1, 2, 3, 4    |
|                          | 44<br>10 | 288<br>65                                                  | N<br>lbf | 1, 2, 3, 5    |
| Dynamic Compressive Load |          | 222 N + 0.45 kg * 100 G<br>50 lbf (static) + 1 lbf * 100 G | N<br>lbf | 1, 3, 4, 6, 7 |
|                          |          | 288 N + 0.45 kg * 100 G<br>65 lbf (static) + 1 lbf * 100 G | N<br>lbf | 1, 3, 5, 6, 7 |
| Transient                |          | 445<br>100                                                 | N<br>lbf | 1, 3, 8       |

**Notes:**

1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. This is the minimum and maximum static force that can be applied by the heatsink and retention solution to maintain the heatsink and processor interface.
3. These parameters are based on limited testing for design characterization. Loading limits are for the package only and do not include the limits of the processor socket.
4. This specification applies for thermal retention solutions that allow baseboard deflection.
5. This specification applies either for thermal retention solutions that prevent baseboard deflection or for the Intel enabled reference solution (CEK).
6. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
7. Experimentally validated test condition used a heatsink mass of 1 lbf (~0.45 kg) with 100 G acceleration measured at heatsink mass. The dynamic portion of this specification in the product application can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this validated dynamic load (1 lbf x 100 G = 100 lb).
8. Transient loading is defined as a 2 second duration peak load superimposed on the static load requirement, representative of loads experienced by the package during heatsink installation.



## 3.4 Package Handling Guidelines

Table 3-2 includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

**Table 3-2. Package Handling Guidelines**

| Parameter | Maximum Recommended | Notes |
|-----------|---------------------|-------|
| Shear     | 356 N [80 lbf]      | 1, 2  |
| Tensile   | 156 N [35 lbf]      | 3, 2  |
| Torque    | 8 N-m [70 lbf-in]   | 4, 2  |

**Notes:**

1. A shear load is defined as a load applied to the IHS in a direction parallel to the IHS top surface.
2. These guidelines are based on limited testing for design characterization.
3. A tensile load is defined as a pulling load applied to the IHS in the direction normal to the IHS surface.
4. A torque load is defined as a twisting load applied to the IHS in an axis of rotation normal to the IHS top surface.

## 3.5 Package Insertion Specifications

The Intel® Xeon® Processor 7200 Series and 7300 Series can be inserted into and removed from a mPGA604 socket 15 times. The socket should meet the mPGA604 requirements detailed in the *mPGA604 Socket Design Guidelines*.

## 3.6 Processor Mass Specifications

The typical mass of the Intel® Xeon® Processor 7200 Series and 7300 Series is 37.6 g (1.5oz). This mass [weight] includes all the components that are included in the package.

## 3.7 Processor Materials

Table 3-3 lists some of the package components and associated materials.

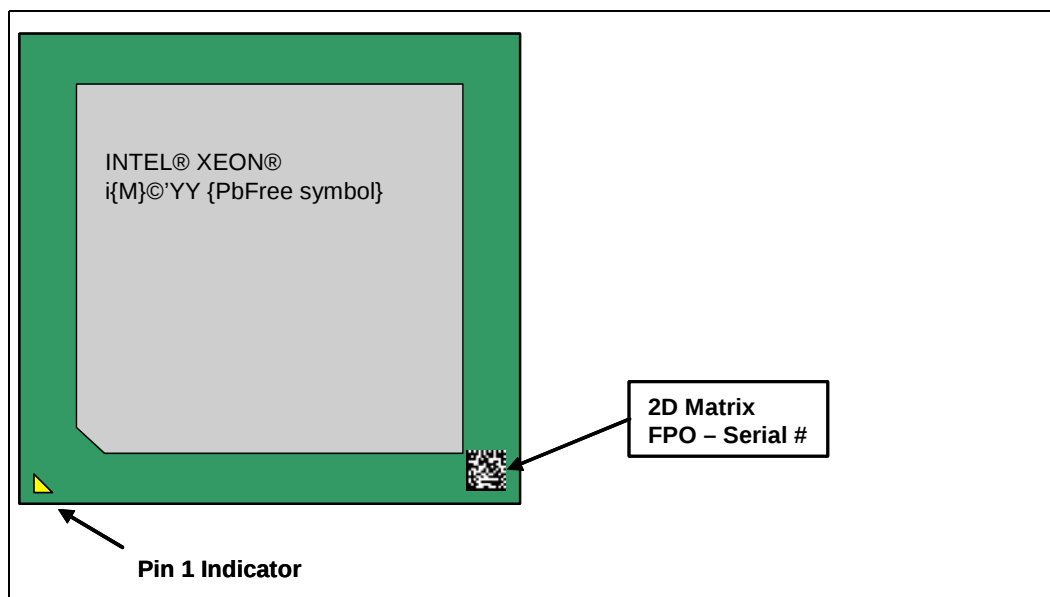
**Table 3-3. Processor Materials**

| Component                      | Material               |
|--------------------------------|------------------------|
| Integrated Heat Spreader (IHS) | Nickel Plated Copper   |
| Substrate                      | Fiber-Reinforced Resin |
| Substrate Pins                 | Gold Plated Copper     |

## 3.8 Processor Markings

Figure 3-9 shows the topside markings and Figure 3-10 shows the bottom-side markings on the processor. These diagrams are to aid in the identification of the Intel® Xeon® Processor 7200 Series and 7300 Series. Please note that the figures in this section are not to scale.

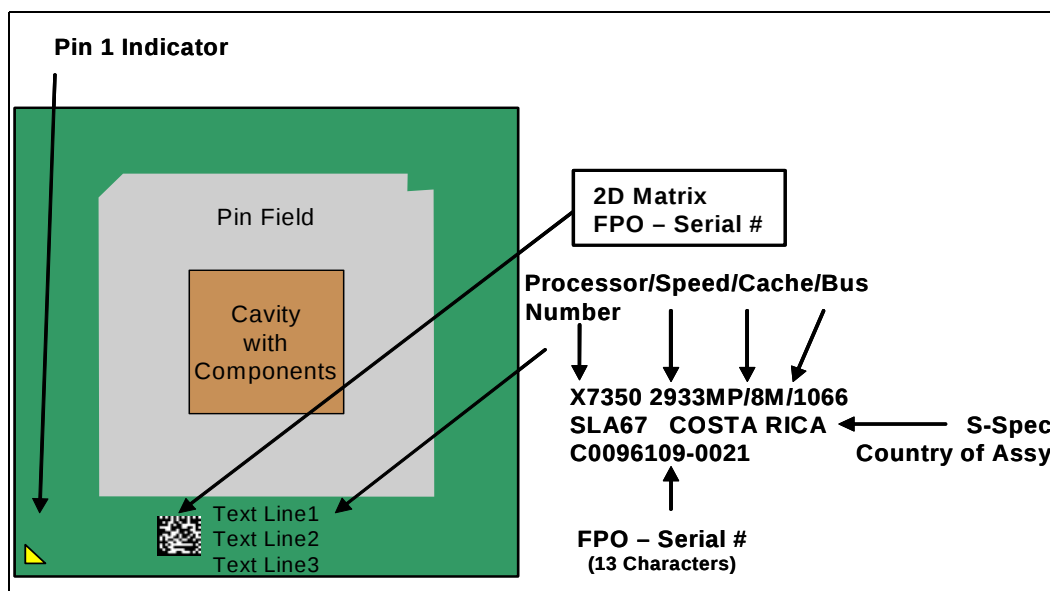
**Figure 3-9. Processor Topside Markings**



**Notes:**

1. Character size for laser markings is: 17 Point, height 1.27 mm (50 mils), width 0.81 mm (32 mils)
2. All characters will be in upper case.

**Figure 3-10. Processor Bottom-Side Markings**



**Notes:**

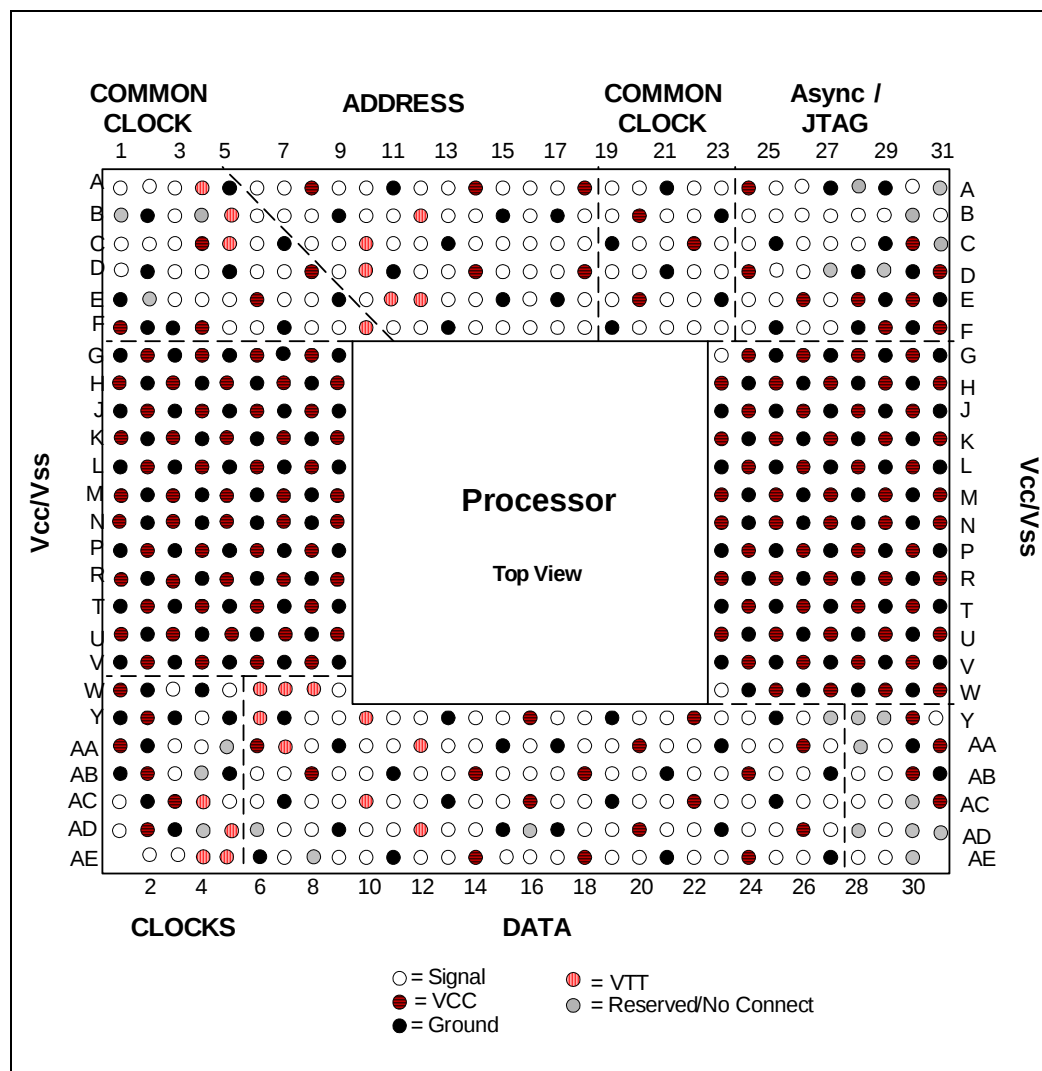
1. Character size for laser markings is: 21 Point, height 1.43 mm (56 mils), width 0.95 mm (37.5 mils)



### 3.9 Processor Pin-Out Coordinates

Figure 3-11 shows the top view of the processor pin coordinates. The coordinates are referred to throughout the document to identify processor pins.

Figure 3-11. Processor Pin-Out Coordinates, Top View







# 4 Pin Listing

## 4.1 Pin Assignments

Section 2.6 contains the front side bus signal groups for the Intel® Xeon® Processor 7200 Series and 7300 Series (see Table 2-4). This section provides a sorted pin lists in Table 4-1 and Table 4-2.

Table 4-1 is a listing of all processor pins ordered alphabetically by pin name. Table 4-2 is a listing of all processor pins ordered by pin number.

### 4.1.1 Pin Listing by Pin Name

**Table 4-1. Pin Listing by Pin Name (Sheet 1 of 16)**

| Pin Name | Pin No. | Signal Buffer Type | Direction    |
|----------|---------|--------------------|--------------|
| A3#      | A22     | Source Sync        | Input/Output |
| A4#      | A20     | Source Sync        | Input/Output |
| A5#      | B18     | Source Sync        | Input/Output |
| A6#      | C18     | Source Sync        | Input/Output |
| A7#      | A19     | Source Sync        | Input/Output |
| A8#      | C17     | Source Sync        | Input/Output |
| A9#      | D17     | Source Sync        | Input/Output |
| A10#     | A13     | Source Sync        | Input/Output |
| A11#     | B16     | Source Sync        | Input/Output |
| A12#     | B14     | Source Sync        | Input/Output |
| A13#     | B13     | Source Sync        | Input/Output |
| A14#     | A12     | Source Sync        | Input/Output |
| A15#     | C15     | Source Sync        | Input/Output |
| A16#     | C14     | Source Sync        | Input/Output |
| A17#     | D16     | Source Sync        | Input/Output |
| A18#     | D15     | Source Sync        | Input/Output |
| A19#     | F15     | Source Sync        | Input/Output |
| A20#     | A10     | Source Sync        | Input/Output |
| A21#     | B10     | Source Sync        | Input/Output |
| A22#     | B11     | Source Sync        | Input/Output |
| A23#     | C12     | Source Sync        | Input/Output |
| A24#     | E14     | Source Sync        | Input/Output |
| A25#     | D13     | Source Sync        | Input/Output |
| A26#     | A9      | Source Sync        | Input/Output |
| A27#     | B8      | Source Sync        | Input/Output |
| A28#     | E13     | Source Sync        | Input/Output |
| A29#     | D12     | Source Sync        | Input/Output |
| A30#     | C11     | Source Sync        | Input/Output |

**Table 4-1. Pin Listing by Pin Name (Sheet 2 of 16)**

| Pin Name | Pin No. | Signal Buffer Type | Direction    |
|----------|---------|--------------------|--------------|
| A31#     | B7      | Source Sync        | Input/Output |
| A32#     | A6      | Source Sync        | Input/Output |
| A33#     | A7      | Source Sync        | Input/Output |
| A34#     | C9      | Source Sync        | Input/Output |
| A35#     | C8      | Source Sync        | Input/Output |
| A36#     | F16     | Source Sync        | Input/Output |
| A37#     | F22     | Source Sync        | Input/Output |
| A38#     | B6      | Source Sync        | Input/Output |
| A39#     | C16     | Source Sync        | Input/Output |
| A20M#    | F27     | Async GTL+         | Input        |
| ADS#     | D19     | Common Clk         | Input/Output |
| ADSTB0#  | F17     | Source Sync        | Input/Output |
| ADSTB1#  | F14     | Source Sync        | Input/Output |
| AP0#     | E10     | Common Clk         | Input/Output |
| AP1#     | D9      | Common Clk         | Input/Output |
| BCLK0    | Y4      | FSB Clk            | Input        |
| BCLK1    | W5      | FSB Clk            | Input        |
| BINIT#   | F11     | Common Clk         | Input/Output |
| BNR#     | F20     | Common Clk         | Input/Output |
| BPM0#    | F6      | Common Clk         | Input/Output |
| BPM1#    | F8      | Common Clk         | Output       |
| BPM2#    | E7      | Common Clk         | Output       |
| BPM3#    | F5      | Common Clk         | Input/Output |
| BPM4#    | E8      | Common Clk         | Output       |
| BPM5#    | E4      | Common Clk         | Input/Output |
| BPMb0#   | AA4     | Common Clk         | Input/Output |
| BPMb1#   | AC1     | Common Clk         | Output       |
| BPMb2#   | AE2     | Common Clk         | Output       |



**Table 4-1. Pin Listing by Pin Name (Sheet 3 of 16)**

| Pin Name | Pin No. | Signal Buffer Type | Direction    |
|----------|---------|--------------------|--------------|
| BPMb3#   | AE3     | Common Clk         | Input/Output |
| BPRI#    | D23     | Common Clk         | Input        |
| BR0#     | D20     | Common Clk         | Input/Output |
| BR1#     | F12     | Common Clk         | Input/Output |
| BSEL0    | AA3     | Power/Other        | Output       |
| BSEL1    | AB3     | Power/Other        | Output       |
| BSEL2    | Y31     | Power/Other        | Output       |
| COMP0    | D25     | Power/Other        | Input        |
| COMP1    | E16     | Power/Other        | Input        |
| COMP2    | AE15    | Power/Other        | Input        |
| COMP3    | AE16    | Power/Other        | Input        |
| D0#      | Y26     | Source Sync        | Input/Output |
| D1#      | AA27    | Source Sync        | Input/Output |
| D2#      | Y24     | Source Sync        | Input/Output |
| D3#      | AA25    | Source Sync        | Input/Output |
| D4#      | AD27    | Source Sync        | Input/Output |
| D5#      | Y23     | Source Sync        | Input/Output |
| D6#      | AA24    | Source Sync        | Input/Output |
| D7#      | AB26    | Source Sync        | Input/Output |
| D8#      | AB25    | Source Sync        | Input/Output |
| D9#      | AB23    | Source Sync        | Input/Output |
| D10#     | AA22    | Source Sync        | Input/Output |
| D11#     | AA21    | Source Sync        | Input/Output |
| D12#     | AB20    | Source Sync        | Input/Output |
| D13#     | AB22    | Source Sync        | Input/Output |
| D14#     | AB19    | Source Sync        | Input/Output |
| D15#     | AA19    | Source Sync        | Input/Output |
| D16#     | AE26    | Source Sync        | Input/Output |
| D17#     | AC26    | Source Sync        | Input/Output |
| D18#     | AD25    | Source Sync        | Input/Output |
| D19#     | AE25    | Source Sync        | Input/Output |
| D20#     | AC24    | Source Sync        | Input/Output |
| D21#     | AD24    | Source Sync        | Input/Output |
| D22#     | AE23    | Source Sync        | Input/Output |
| D23#     | AC23    | Source Sync        | Input/Output |
| D24#     | AA18    | Source Sync        | Input/Output |
| D25#     | AC20    | Source Sync        | Input/Output |
| D26#     | AC21    | Source Sync        | Input/Output |
| D27#     | AE22    | Source Sync        | Input/Output |
| D28#     | AE20    | Source Sync        | Input/Output |

**Table 4-1. Pin Listing by Pin Name (Sheet 4 of 16)**

| Pin Name | Pin No. | Signal Buffer Type | Direction    |
|----------|---------|--------------------|--------------|
| D29#     | AD21    | Source Sync        | Input/Output |
| D30#     | AD19    | Source Sync        | Input/Output |
| D31#     | AB17    | Source Sync        | Input/Output |
| D32#     | AB16    | Source Sync        | Input/Output |
| D33#     | AA16    | Source Sync        | Input/Output |
| D34#     | AC17    | Source Sync        | Input/Output |
| D35#     | AE13    | Source Sync        | Input/Output |
| D36#     | AD18    | Source Sync        | Input/Output |
| D37#     | AB15    | Source Sync        | Input/Output |
| D38#     | AD13    | Source Sync        | Input/Output |
| D39#     | AD14    | Source Sync        | Input/Output |
| D40#     | AD11    | Source Sync        | Input/Output |
| D41#     | AC12    | Source Sync        | Input/Output |
| D42#     | AE10    | Source Sync        | Input/Output |
| D43#     | AC11    | Source Sync        | Input/Output |
| D44#     | AE9     | Source Sync        | Input/Output |
| D45#     | AD10    | Source Sync        | Input/Output |
| D46#     | AD8     | Source Sync        | Input/Output |
| D47#     | AC9     | Source Sync        | Input/Output |
| D48#     | AA13    | Source Sync        | Input/Output |
| D49#     | AA14    | Source Sync        | Input/Output |
| D50#     | AC14    | Source Sync        | Input/Output |
| D51#     | AB12    | Source Sync        | Input/Output |
| D52#     | AB13    | Source Sync        | Input/Output |
| D53#     | AA11    | Source Sync        | Input/Output |
| D54#     | AA10    | Source Sync        | Input/Output |
| D55#     | AB10    | Source Sync        | Input/Output |
| D56#     | AC8     | Source Sync        | Input/Output |
| D57#     | AD7     | Source Sync        | Input/Output |
| D58#     | AE7     | Source Sync        | Input/Output |
| D59#     | AC6     | Source Sync        | Input/Output |
| D60#     | AC5     | Source Sync        | Input/Output |
| D61#     | AA8     | Source Sync        | Input/Output |
| D62#     | Y9      | Source Sync        | Input/Output |
| D63#     | AB6     | Source Sync        | Input/Output |
| DBI0#    | AC27    | Source Sync        | Input/Output |
| DBI1#    | AD22    | Source Sync        | Input/Output |
| DBI2#    | AE12    | Source Sync        | Input/Output |
| DBI3#    | AB9     | Source Sync        | Input/Output |
| DBSY#    | F18     | Common Clk         | Input/Output |



Table 4-1. Pin Listing by Pin Name (Sheet 5 of 16)

| Pin Name       | Pin No. | Signal Buffer Type | Direction    |
|----------------|---------|--------------------|--------------|
| DEFER#         | C23     | Common Clk         | Input        |
| DP0#           | AC18    | Common Clk         | Input/Output |
| DP1#           | AE19    | Common Clk         | Input/Output |
| DP2#           | AC15    | Common Clk         | Input/Output |
| DP3#           | AE17    | Common Clk         | Input/Output |
| DRDY#          | E18     | Common Clk         | Input/Output |
| DSTBN0#        | Y21     | Source Sync        | Input/Output |
| DSTBN1#        | Y18     | Source Sync        | Input/Output |
| DSTBN2#        | Y15     | Source Sync        | Input/Output |
| DSTBN3#        | Y12     | Source Sync        | Input/Output |
| DSTBP0#        | Y20     | Source Sync        | Input/Output |
| DSTBP1#        | Y17     | Source Sync        | Input/Output |
| DSTBP2#        | Y14     | Source Sync        | Input/Output |
| DSTBP3#        | Y11     | Source Sync        | Input/Output |
| FERR#/PBE#     | E27     | Async GTL+         | Output       |
| FORCEPR#       | A15     | Async GTL+         | Input        |
| GTLREF_ADD_EN  | F9      | Power/Other        | Input        |
| GTLREF_ADD_MI  | F23     | Power/Other        | Input        |
| GTLREF_DATA_EN | W9      | Power/Other        | Input        |
| GTLREF_DATA_M  | W23     | Power/Other        | Input        |
| HIT#           | E22     | Common Clk         | Input/Output |
| HITM#          | A23     | Common Clk         | Input/Output |
| IERR#          | E5      | Async GTL+         | Output       |
| IGNNE#         | C26     | Async GTL+         | Input        |
| INIT#          | D6      | Async GTL+         | Input        |
| LINT0          | B24     | Async GTL+         | Input        |
| LINT1          | G23     | Async GTL+         | Input        |
| LL_IDO         | B31     | Power/Other        | Output       |
| LL_ID1         | B28     | Power/Other        | Output       |
| LOCK#          | A17     | Common Clk         | Input/Output |
| MCERR#         | D7      | Common Clk         | Input/Output |
| PECI           | C28     | Power/Other        | Input/Output |
| PROC_ID0       | A30     | Power/Other        | Output       |
| PROC_ID1       | B29     | Power/Other        | Output       |
| PROCHOT#       | B25     | Async GTL+         | Output       |
| PWRGOOD        | AB7     | Async GTL+         | Input        |
| REQ0#          | B19     | Source Sync        | Input/Output |
| REQ1#          | B21     | Source Sync        | Input/Output |

Table 4-1. Pin Listing by Pin Name (Sheet 6 of 16)

| Pin Name | Pin No. | Signal Buffer Type | Direction    |
|----------|---------|--------------------|--------------|
| REQ2#    | C21     | Source Sync        | Input/Output |
| REQ3#    | C20     | Source Sync        | Input/Output |
| REQ4#    | B22     | Source Sync        | Input/Output |
| Reserved | A28     |                    |              |
| Reserved | A31     |                    |              |
| Reserved | B1      |                    |              |
| Reserved | B4      |                    |              |
| Reserved | B30     |                    |              |
| Reserved | C31     |                    |              |
| Reserved | D27     |                    |              |
| Reserved | D29     |                    |              |
| Reserved | E2      |                    |              |
| Reserved | Y27     |                    |              |
| Reserved | Y28     |                    |              |
| Reserved | Y29     |                    |              |
| Reserved | AA5     |                    |              |
| Reserved | AA28    |                    |              |
| Reserved | AB4     |                    |              |
| Reserved | AC30    |                    |              |
| Reserved | AD4     |                    |              |
| Reserved | AD6     |                    |              |
| Reserved | AD16    |                    |              |
| Reserved | AD28    |                    |              |
| Reserved | AD30    |                    |              |
| Reserved | AD31    |                    |              |
| Reserved | AE8     |                    |              |
| Reserved | AE30    |                    |              |
| RESET#   | Y8      | Common Clk         | Input        |
| RS0#     | E21     | Common Clk         | Input        |
| RS1#     | D22     | Common Clk         | Input        |
| RS2#     | F21     | Common Clk         | Input        |
| RSP#     | C6      | Common Clk         | Input        |
| SKTOCC#  | A3      | Power/Other        | Output       |
| SM_CLK   | AC28    | SMBus              | Input        |
| SM_DAT   | AC29    | SMBus              | Input/Output |
| SM_EP_A0 | AA29    | SMBus              | Input        |
| SM_EP_A1 | AB29    | SMBus              | Input        |
| SM_EP_A2 | AB28    | SMBus              | Input        |
| SM_VCC   | AE28    | Power/Other        |              |
| SM_VCC   | AE29    | Power/Other        |              |



**Table 4-1. Pin Listing by Pin Name (Sheet 7 of 16)**

| Pin Name        | Pin No. | Signal Buffer Type | Direction |
|-----------------|---------|--------------------|-----------|
| SM_WP           | AD29    | SMBus              | Input     |
| SMI#            | C27     | Async GTL+         | Input     |
| STPCLK#         | D4      | Async GTL+         | Input     |
| TCK             | E24     | TAP                | Input     |
| TDI             | C24     | TAP                | Input     |
| TDO             | E25     | TAP                | Output    |
| TESTHI0         | A16     | Power/Other        | Input     |
| TESTHI1         | W3      | Power/Other        | Input     |
| TESTIN1         | D1      | Power/Other        | Input     |
| TESTIN2         | C2      | Power/Other        | Input     |
| THERMTRIP#      | F26     | Async GTL+         | Output    |
| TMS             | A25     | TAP                | Input     |
| TRDY#           | E19     | Common Clk         | Input     |
| TRST#           | F24     | TAP                | Input     |
| V <sub>CC</sub> | A8      | Power/Other        |           |
| V <sub>CC</sub> | A14     | Power/Other        |           |
| V <sub>CC</sub> | A18     | Power/Other        |           |
| V <sub>CC</sub> | A24     | Power/Other        |           |
| V <sub>CC</sub> | B20     | Power/Other        |           |
| V <sub>CC</sub> | C4      | Power/Other        |           |
| V <sub>CC</sub> | C22     | Power/Other        |           |
| V <sub>CC</sub> | C30     | Power/Other        |           |
| V <sub>CC</sub> | D8      | Power/Other        |           |
| V <sub>CC</sub> | D14     | Power/Other        |           |
| V <sub>CC</sub> | D18     | Power/Other        |           |
| V <sub>CC</sub> | D24     | Power/Other        |           |
| V <sub>CC</sub> | D31     | Power/Other        |           |
| V <sub>CC</sub> | E6      | Power/Other        |           |
| V <sub>CC</sub> | E20     | Power/Other        |           |
| V <sub>CC</sub> | E26     | Power/Other        |           |
| V <sub>CC</sub> | E28     | Power/Other        |           |
| V <sub>CC</sub> | E30     | Power/Other        |           |
| V <sub>CC</sub> | F1      | Power/Other        |           |
| V <sub>CC</sub> | F4      | Power/Other        |           |
| V <sub>CC</sub> | F29     | Power/Other        |           |
| V <sub>CC</sub> | F31     | Power/Other        |           |
| V <sub>CC</sub> | G2      | Power/Other        |           |
| V <sub>CC</sub> | G4      | Power/Other        |           |
| V <sub>CC</sub> | G6      | Power/Other        |           |
| V <sub>CC</sub> | G8      | Power/Other        |           |

**Table 4-1. Pin Listing by Pin Name (Sheet 8 of 16)**

| Pin Name        | Pin No. | Signal Buffer Type | Direction |
|-----------------|---------|--------------------|-----------|
| V <sub>CC</sub> | G24     | Power/Other        |           |
| V <sub>CC</sub> | G26     | Power/Other        |           |
| V <sub>CC</sub> | G28     | Power/Other        |           |
| V <sub>CC</sub> | G30     | Power/Other        |           |
| V <sub>CC</sub> | H1      | Power/Other        |           |
| V <sub>CC</sub> | H3      | Power/Other        |           |
| V <sub>CC</sub> | H5      | Power/Other        |           |
| V <sub>CC</sub> | H7      | Power/Other        |           |
| V <sub>CC</sub> | H9      | Power/Other        |           |
| V <sub>CC</sub> | H23     | Power/Other        |           |
| V <sub>CC</sub> | H25     | Power/Other        |           |
| V <sub>CC</sub> | H27     | Power/Other        |           |
| V <sub>CC</sub> | H29     | Power/Other        |           |
| V <sub>CC</sub> | H31     | Power/Other        |           |
| V <sub>CC</sub> | J2      | Power/Other        |           |
| V <sub>CC</sub> | J4      | Power/Other        |           |
| V <sub>CC</sub> | J6      | Power/Other        |           |
| V <sub>CC</sub> | J8      | Power/Other        |           |
| V <sub>CC</sub> | J24     | Power/Other        |           |
| V <sub>CC</sub> | J26     | Power/Other        |           |
| V <sub>CC</sub> | J28     | Power/Other        |           |
| V <sub>CC</sub> | J30     | Power/Other        |           |
| V <sub>CC</sub> | K1      | Power/Other        |           |
| V <sub>CC</sub> | K3      | Power/Other        |           |
| V <sub>CC</sub> | K5      | Power/Other        |           |
| V <sub>CC</sub> | K7      | Power/Other        |           |
| V <sub>CC</sub> | K9      | Power/Other        |           |
| V <sub>CC</sub> | K23     | Power/Other        |           |
| V <sub>CC</sub> | K25     | Power/Other        |           |
| V <sub>CC</sub> | K27     | Power/Other        |           |
| V <sub>CC</sub> | K29     | Power/Other        |           |
| V <sub>CC</sub> | K31     | Power/Other        |           |
| V <sub>CC</sub> | L2      | Power/Other        |           |
| V <sub>CC</sub> | L4      | Power/Other        |           |
| V <sub>CC</sub> | L6      | Power/Other        |           |
| V <sub>CC</sub> | L8      | Power/Other        |           |
| V <sub>CC</sub> | L24     | Power/Other        |           |
| V <sub>CC</sub> | L26     | Power/Other        |           |
| V <sub>CC</sub> | L28     | Power/Other        |           |
| V <sub>CC</sub> | L30     | Power/Other        |           |



Table 4-1. Pin Listing by Pin Name (Sheet 9 of 16)

| Pin Name        | Pin No. | Signal Buffer Type | Direction |
|-----------------|---------|--------------------|-----------|
| V <sub>CC</sub> | M1      | Power/Other        |           |
| V <sub>CC</sub> | M3      | Power/Other        |           |
| V <sub>CC</sub> | M5      | Power/Other        |           |
| V <sub>CC</sub> | M7      | Power/Other        |           |
| V <sub>CC</sub> | M9      | Power/Other        |           |
| V <sub>CC</sub> | M23     | Power/Other        |           |
| V <sub>CC</sub> | M25     | Power/Other        |           |
| V <sub>CC</sub> | M27     | Power/Other        |           |
| V <sub>CC</sub> | M29     | Power/Other        |           |
| V <sub>CC</sub> | M31     | Power/Other        |           |
| V <sub>CC</sub> | N1      | Power/Other        |           |
| V <sub>CC</sub> | N3      | Power/Other        |           |
| V <sub>CC</sub> | N5      | Power/Other        |           |
| V <sub>CC</sub> | N7      | Power/Other        |           |
| V <sub>CC</sub> | N9      | Power/Other        |           |
| V <sub>CC</sub> | N23     | Power/Other        |           |
| V <sub>CC</sub> | N25     | Power/Other        |           |
| V <sub>CC</sub> | N27     | Power/Other        |           |
| V <sub>CC</sub> | N29     | Power/Other        |           |
| V <sub>CC</sub> | N31     | Power/Other        |           |
| V <sub>CC</sub> | P2      | Power/Other        |           |
| V <sub>CC</sub> | P4      | Power/Other        |           |
| V <sub>CC</sub> | P6      | Power/Other        |           |
| V <sub>CC</sub> | P8      | Power/Other        |           |
| V <sub>CC</sub> | P24     | Power/Other        |           |
| V <sub>CC</sub> | P26     | Power/Other        |           |
| V <sub>CC</sub> | P28     | Power/Other        |           |
| V <sub>CC</sub> | P30     | Power/Other        |           |
| V <sub>CC</sub> | R1      | Power/Other        |           |
| V <sub>CC</sub> | R3      | Power/Other        |           |
| V <sub>CC</sub> | R5      | Power/Other        |           |
| V <sub>CC</sub> | R7      | Power/Other        |           |
| V <sub>CC</sub> | R9      | Power/Other        |           |
| V <sub>CC</sub> | R23     | Power/Other        |           |
| V <sub>CC</sub> | R25     | Power/Other        |           |
| V <sub>CC</sub> | R27     | Power/Other        |           |
| V <sub>CC</sub> | R29     | Power/Other        |           |
| V <sub>CC</sub> | R31     | Power/Other        |           |
| V <sub>CC</sub> | T2      | Power/Other        |           |
| V <sub>CC</sub> | T4      | Power/Other        |           |

Table 4-1. Pin Listing by Pin Name (Sheet 10 of 16)

| Pin Name        | Pin No. | Signal Buffer Type | Direction |
|-----------------|---------|--------------------|-----------|
| V <sub>CC</sub> | T6      | Power/Other        |           |
| V <sub>CC</sub> | T8      | Power/Other        |           |
| V <sub>CC</sub> | T24     | Power/Other        |           |
| V <sub>CC</sub> | T26     | Power/Other        |           |
| V <sub>CC</sub> | T28     | Power/Other        |           |
| V <sub>CC</sub> | T30     | Power/Other        |           |
| V <sub>CC</sub> | U1      | Power/Other        |           |
| V <sub>CC</sub> | U3      | Power/Other        |           |
| V <sub>CC</sub> | U5      | Power/Other        |           |
| V <sub>CC</sub> | U7      | Power/Other        |           |
| V <sub>CC</sub> | U9      | Power/Other        |           |
| V <sub>CC</sub> | U23     | Power/Other        |           |
| V <sub>CC</sub> | U25     | Power/Other        |           |
| V <sub>CC</sub> | U27     | Power/Other        |           |
| V <sub>CC</sub> | U29     | Power/Other        |           |
| V <sub>CC</sub> | U31     | Power/Other        |           |
| V <sub>CC</sub> | V2      | Power/Other        |           |
| V <sub>CC</sub> | V4      | Power/Other        |           |
| V <sub>CC</sub> | V6      | Power/Other        |           |
| V <sub>CC</sub> | V8      | Power/Other        |           |
| V <sub>CC</sub> | V24     | Power/Other        |           |
| V <sub>CC</sub> | V26     | Power/Other        |           |
| V <sub>CC</sub> | V28     | Power/Other        |           |
| V <sub>CC</sub> | V30     | Power/Other        |           |
| V <sub>CC</sub> | W1      | Power/Other        |           |
| V <sub>CC</sub> | W25     | Power/Other        |           |
| V <sub>CC</sub> | W27     | Power/Other        |           |
| V <sub>CC</sub> | W29     | Power/Other        |           |
| V <sub>CC</sub> | W31     | Power/Other        |           |
| V <sub>CC</sub> | Y2      | Power/Other        |           |
| V <sub>CC</sub> | Y16     | Power/Other        |           |
| V <sub>CC</sub> | Y22     | Power/Other        |           |
| V <sub>CC</sub> | Y30     | Power/Other        |           |
| V <sub>CC</sub> | AA1     | Power/Other        |           |
| V <sub>CC</sub> | AA6     | Power/Other        |           |
| V <sub>CC</sub> | AA20    | Power/Other        |           |
| V <sub>CC</sub> | AA26    | Power/Other        |           |
| V <sub>CC</sub> | AA31    | Power/Other        |           |
| V <sub>CC</sub> | AB2     | Power/Other        |           |
| V <sub>CC</sub> | AB8     | Power/Other        |           |



Table 4-1. Pin Listing by Pin Name (Sheet 11 of 16)

| Pin Name                | Pin No. | Signal Buffer Type | Direction |
|-------------------------|---------|--------------------|-----------|
| V <sub>CC</sub>         | AB14    | Power/Other        |           |
| V <sub>CC</sub>         | AB18    | Power/Other        |           |
| V <sub>CC</sub>         | AB24    | Power/Other        |           |
| V <sub>CC</sub>         | AB30    | Power/Other        |           |
| V <sub>CC</sub>         | AC3     | Power/Other        |           |
| V <sub>CC</sub>         | AC16    | Power/Other        |           |
| V <sub>CC</sub>         | AC22    | Power/Other        |           |
| V <sub>CC</sub>         | AC31    | Power/Other        |           |
| V <sub>CC</sub>         | AD2     | Power/Other        |           |
| V <sub>CC</sub>         | AD20    | Power/Other        |           |
| V <sub>CC</sub>         | AD26    | Power/Other        |           |
| V <sub>CC</sub>         | AE14    | Power/Other        |           |
| V <sub>CC</sub>         | AE18    | Power/Other        |           |
| V <sub>CC</sub>         | AE24    | Power/Other        |           |
| V <sub>CC</sub> PLL     | AD1     | Power/Other        | Input     |
| V <sub>CC</sub> _SENSE  | B27     | Power/Other        | Output    |
| V <sub>CC</sub> _SENSE2 | A26     | Power/Other        | Output    |
| VID1                    | E3      | Power/Other        | Output    |
| VID2                    | D3      | Power/Other        | Output    |
| VID3                    | C3      | Power/Other        | Output    |
| VID4                    | B3      | Power/Other        | Output    |
| VID5                    | A1      | Power/Other        | Output    |
| VID6                    | C1      | Power/Other        | Output    |
| V <sub>SS</sub>         | A5      | Power/Other        |           |
| V <sub>SS</sub>         | A11     | Power/Other        |           |
| V <sub>SS</sub>         | A21     | Power/Other        |           |
| V <sub>SS</sub>         | A27     | Power/Other        |           |
| V <sub>SS</sub>         | A29     | Power/Other        |           |
| V <sub>SS</sub>         | B2      | Power/Other        |           |
| V <sub>SS</sub>         | B9      | Power/Other        |           |
| V <sub>SS</sub>         | B15     | Power/Other        |           |
| V <sub>SS</sub>         | B17     | Power/Other        |           |
| V <sub>SS</sub>         | B23     | Power/Other        |           |
| V <sub>SS</sub>         | C7      | Power/Other        |           |
| V <sub>SS</sub>         | C13     | Power/Other        |           |
| V <sub>SS</sub>         | C19     | Power/Other        |           |
| V <sub>SS</sub>         | C25     | Power/Other        |           |
| V <sub>SS</sub>         | C29     | Power/Other        |           |
| V <sub>SS</sub>         | D2      | Power/Other        |           |
| V <sub>SS</sub>         | D5      | Power/Other        |           |

Table 4-1. Pin Listing by Pin Name (Sheet 12 of 16)

| Pin Name        | Pin No. | Signal Buffer Type | Direction |
|-----------------|---------|--------------------|-----------|
| V <sub>SS</sub> | D11     | Power/Other        |           |
| V <sub>SS</sub> | D21     | Power/Other        |           |
| V <sub>SS</sub> | D28     | Power/Other        |           |
| V <sub>SS</sub> | D30     | Power/Other        |           |
| V <sub>SS</sub> | E1      | Power/Other        |           |
| V <sub>SS</sub> | E9      | Power/Other        |           |
| V <sub>SS</sub> | E15     | Power/Other        |           |
| V <sub>SS</sub> | E17     | Power/Other        |           |
| V <sub>SS</sub> | E23     | Power/Other        |           |
| V <sub>SS</sub> | E29     | Power/Other        |           |
| V <sub>SS</sub> | E31     | Power/Other        |           |
| V <sub>SS</sub> | F2      | Power/Other        |           |
| V <sub>SS</sub> | F3      | Power/Other        |           |
| V <sub>SS</sub> | F7      | Power/Other        |           |
| V <sub>SS</sub> | F13     | Power/Other        |           |
| V <sub>SS</sub> | F19     | Power/Other        |           |
| V <sub>SS</sub> | F25     | Power/Other        |           |
| V <sub>SS</sub> | F28     | Power/Other        |           |
| V <sub>SS</sub> | F30     | Power/Other        |           |
| V <sub>SS</sub> | G1      | Power/Other        |           |
| V <sub>SS</sub> | G3      | Power/Other        |           |
| V <sub>SS</sub> | G5      | Power/Other        |           |
| V <sub>SS</sub> | G7      | Power/Other        |           |
| V <sub>SS</sub> | G9      | Power/Other        |           |
| V <sub>SS</sub> | G25     | Power/Other        |           |
| V <sub>SS</sub> | G27     | Power/Other        |           |
| V <sub>SS</sub> | G29     | Power/Other        |           |
| V <sub>SS</sub> | G31     | Power/Other        |           |
| V <sub>SS</sub> | H2      | Power/Other        |           |
| V <sub>SS</sub> | H4      | Power/Other        |           |
| V <sub>SS</sub> | H6      | Power/Other        |           |
| V <sub>SS</sub> | H8      | Power/Other        |           |
| V <sub>SS</sub> | H24     | Power/Other        |           |
| V <sub>SS</sub> | H26     | Power/Other        |           |
| V <sub>SS</sub> | H28     | Power/Other        |           |
| V <sub>SS</sub> | H30     | Power/Other        |           |
| V <sub>SS</sub> | J1      | Power/Other        |           |
| V <sub>SS</sub> | J3      | Power/Other        |           |
| V <sub>SS</sub> | J5      | Power/Other        |           |
| V <sub>SS</sub> | J7      | Power/Other        |           |



Table 4-1. Pin Listing by Pin Name (Sheet 13 of 16)

| Pin Name        | Pin No. | Signal Buffer Type | Direction |
|-----------------|---------|--------------------|-----------|
| V <sub>SS</sub> | J9      | Power/Other        |           |
| V <sub>SS</sub> | J23     | Power/Other        |           |
| V <sub>SS</sub> | J25     | Power/Other        |           |
| V <sub>SS</sub> | J27     | Power/Other        |           |
| V <sub>SS</sub> | J29     | Power/Other        |           |
| V <sub>SS</sub> | J31     | Power/Other        |           |
| V <sub>SS</sub> | K2      | Power/Other        |           |
| V <sub>SS</sub> | K4      | Power/Other        |           |
| V <sub>SS</sub> | K6      | Power/Other        |           |
| V <sub>SS</sub> | K8      | Power/Other        |           |
| V <sub>SS</sub> | K24     | Power/Other        |           |
| V <sub>SS</sub> | K26     | Power/Other        |           |
| V <sub>SS</sub> | K28     | Power/Other        |           |
| V <sub>SS</sub> | K30     | Power/Other        |           |
| V <sub>SS</sub> | L1      | Power/Other        |           |
| V <sub>SS</sub> | L3      | Power/Other        |           |
| V <sub>SS</sub> | L5      | Power/Other        |           |
| V <sub>SS</sub> | L7      | Power/Other        |           |
| V <sub>SS</sub> | L9      | Power/Other        |           |
| V <sub>SS</sub> | L23     | Power/Other        |           |
| V <sub>SS</sub> | L25     | Power/Other        |           |
| V <sub>SS</sub> | L27     | Power/Other        |           |
| V <sub>SS</sub> | L29     | Power/Other        |           |
| V <sub>SS</sub> | L31     | Power/Other        |           |
| V <sub>SS</sub> | M2      | Power/Other        |           |
| V <sub>SS</sub> | M4      | Power/Other        |           |
| V <sub>SS</sub> | M6      | Power/Other        |           |
| V <sub>SS</sub> | M8      | Power/Other        |           |
| V <sub>SS</sub> | M24     | Power/Other        |           |
| V <sub>SS</sub> | M26     | Power/Other        |           |
| V <sub>SS</sub> | M28     | Power/Other        |           |
| V <sub>SS</sub> | M30     | Power/Other        |           |
| V <sub>SS</sub> | N2      | Power/Other        |           |
| V <sub>SS</sub> | N4      | Power/Other        |           |
| V <sub>SS</sub> | N6      | Power/Other        |           |
| V <sub>SS</sub> | N8      | Power/Other        |           |
| V <sub>SS</sub> | N24     | Power/Other        |           |
| V <sub>SS</sub> | N26     | Power/Other        |           |
| V <sub>SS</sub> | N28     | Power/Other        |           |
| V <sub>SS</sub> | N30     | Power/Other        |           |

Table 4-1. Pin Listing by Pin Name (Sheet 14 of 16)

| Pin Name        | Pin No. | Signal Buffer Type | Direction |
|-----------------|---------|--------------------|-----------|
| V <sub>SS</sub> | P1      | Power/Other        |           |
| V <sub>SS</sub> | P3      | Power/Other        |           |
| V <sub>SS</sub> | P5      | Power/Other        |           |
| V <sub>SS</sub> | P7      | Power/Other        |           |
| V <sub>SS</sub> | P9      | Power/Other        |           |
| V <sub>SS</sub> | P23     | Power/Other        |           |
| V <sub>SS</sub> | P25     | Power/Other        |           |
| V <sub>SS</sub> | P27     | Power/Other        |           |
| V <sub>SS</sub> | P29     | Power/Other        |           |
| V <sub>SS</sub> | P31     | Power/Other        |           |
| V <sub>SS</sub> | R2      | Power/Other        |           |
| V <sub>SS</sub> | R4      | Power/Other        |           |
| V <sub>SS</sub> | R6      | Power/Other        |           |
| V <sub>SS</sub> | R8      | Power/Other        |           |
| V <sub>SS</sub> | R24     | Power/Other        |           |
| V <sub>SS</sub> | R26     | Power/Other        |           |
| V <sub>SS</sub> | R28     | Power/Other        |           |
| V <sub>SS</sub> | R30     | Power/Other        |           |
| V <sub>SS</sub> | T1      | Power/Other        |           |
| V <sub>SS</sub> | T3      | Power/Other        |           |
| V <sub>SS</sub> | T5      | Power/Other        |           |
| V <sub>SS</sub> | T7      | Power/Other        |           |
| V <sub>SS</sub> | T9      | Power/Other        |           |
| V <sub>SS</sub> | T23     | Power/Other        |           |
| V <sub>SS</sub> | T25     | Power/Other        |           |
| V <sub>SS</sub> | T27     | Power/Other        |           |
| V <sub>SS</sub> | T29     | Power/Other        |           |
| V <sub>SS</sub> | T31     | Power/Other        |           |
| V <sub>SS</sub> | U2      | Power/Other        |           |
| V <sub>SS</sub> | U4      | Power/Other        |           |
| V <sub>SS</sub> | U6      | Power/Other        |           |
| V <sub>SS</sub> | U8      | Power/Other        |           |
| V <sub>SS</sub> | U24     | Power/Other        |           |
| V <sub>SS</sub> | U26     | Power/Other        |           |
| V <sub>SS</sub> | U28     | Power/Other        |           |
| V <sub>SS</sub> | U30     | Power/Other        |           |
| V <sub>SS</sub> | V1      | Power/Other        |           |
| V <sub>SS</sub> | V3      | Power/Other        |           |
| V <sub>SS</sub> | V5      | Power/Other        |           |
| V <sub>SS</sub> | V7      | Power/Other        |           |



**Table 4-1. Pin Listing by Pin Name (Sheet 15 of 16)**

| Pin Name        | Pin No. | Signal Buffer Type | Direction |
|-----------------|---------|--------------------|-----------|
| V <sub>SS</sub> | V9      | Power/Other        |           |
| V <sub>SS</sub> | V23     | Power/Other        |           |
| V <sub>SS</sub> | V25     | Power/Other        |           |
| V <sub>SS</sub> | V27     | Power/Other        |           |
| V <sub>SS</sub> | V29     | Power/Other        |           |
| V <sub>SS</sub> | V31     | Power/Other        |           |
| V <sub>SS</sub> | W2      | Power/Other        |           |
| V <sub>SS</sub> | W4      | Power/Other        |           |
| V <sub>SS</sub> | W24     | Power/Other        |           |
| V <sub>SS</sub> | W26     | Power/Other        |           |
| V <sub>SS</sub> | W28     | Power/Other        |           |
| V <sub>SS</sub> | W30     | Power/Other        |           |
| V <sub>SS</sub> | Y1      | Power/Other        |           |
| V <sub>SS</sub> | Y3      | Power/Other        |           |
| V <sub>SS</sub> | Y5      | Power/Other        |           |
| V <sub>SS</sub> | Y7      | Power/Other        |           |
| V <sub>SS</sub> | Y13     | Power/Other        |           |
| V <sub>SS</sub> | Y19     | Power/Other        |           |
| V <sub>SS</sub> | Y25     | Power/Other        |           |
| V <sub>SS</sub> | AA2     | Power/Other        |           |
| V <sub>SS</sub> | AA9     | Power/Other        |           |
| V <sub>SS</sub> | AA15    | Power/Other        |           |
| V <sub>SS</sub> | AA17    | Power/Other        |           |
| V <sub>SS</sub> | AA23    | Power/Other        |           |
| V <sub>SS</sub> | AA30    | Power/Other        |           |
| V <sub>SS</sub> | AB1     | Power/Other        |           |
| V <sub>SS</sub> | AB5     | Power/Other        |           |
| V <sub>SS</sub> | AB11    | Power/Other        |           |
| V <sub>SS</sub> | AB21    | Power/Other        |           |
| V <sub>SS</sub> | AB27    | Power/Other        |           |
| V <sub>SS</sub> | AB31    | Power/Other        |           |
| V <sub>SS</sub> | AC2     | Power/Other        |           |
| V <sub>SS</sub> | AC7     | Power/Other        |           |
| V <sub>SS</sub> | AC13    | Power/Other        |           |
| V <sub>SS</sub> | AC19    | Power/Other        |           |
| V <sub>SS</sub> | AC25    | Power/Other        |           |

**Table 4-1. Pin Listing by Pin Name (Sheet 16 of 16)**

| Pin Name               | Pin No. | Signal Buffer Type | Direction |
|------------------------|---------|--------------------|-----------|
| V <sub>SS</sub>        | AD3     | Power/Other        |           |
| V <sub>SS</sub>        | AD9     | Power/Other        |           |
| V <sub>SS</sub>        | AD15    | Power/Other        |           |
| V <sub>SS</sub>        | AD17    | Power/Other        |           |
| V <sub>SS</sub>        | AD23    | Power/Other        |           |
| V <sub>SS</sub>        | AE6     | Power/Other        |           |
| V <sub>SS</sub>        | AE11    | Power/Other        |           |
| V <sub>SS</sub>        | AE21    | Power/Other        |           |
| V <sub>SS</sub>        | AE27    | Power/Other        |           |
| V <sub>SS_SENSE</sub>  | D26     | Power/Other        | Output    |
| V <sub>SS_SENSE2</sub> | B26     | Power/Other        | Output    |
| V <sub>TT</sub>        | A4      | Power/Other        |           |
| V <sub>TT</sub>        | B5      | Power/Other        |           |
| V <sub>TT</sub>        | B12     | Power/Other        |           |
| V <sub>TT</sub>        | C5      | Power/Other        |           |
| V <sub>TT</sub>        | C10     | Power/Other        |           |
| V <sub>TT</sub>        | D10     | Power/Other        |           |
| V <sub>TT</sub>        | E11     | Power/Other        |           |
| V <sub>TT</sub>        | E12     | Power/Other        |           |
| V <sub>TT</sub>        | F10     | Power/Other        |           |
| V <sub>TT</sub>        | W6      | Power/Other        |           |
| V <sub>TT</sub>        | W7      | Power/Other        |           |
| V <sub>TT</sub>        | W8      | Power/Other        |           |
| V <sub>TT</sub>        | Y6      | Power/Other        |           |
| V <sub>TT</sub>        | Y10     | Power/Other        |           |
| V <sub>TT</sub>        | AA7     | Power/Other        |           |
| V <sub>TT</sub>        | AA12    | Power/Other        |           |
| V <sub>TT</sub>        | AC4     | Power/Other        |           |
| V <sub>TT</sub>        | AC10    | Power/Other        |           |
| V <sub>TT</sub>        | AD5     | Power/Other        |           |
| V <sub>TT</sub>        | AD12    | Power/Other        |           |
| V <sub>TT</sub>        | AE4     | Power/Other        |           |
| V <sub>TT</sub>        | AE5     | Power/Other        |           |
| V <sub>TT_SEL</sub>    | A2      | Power/Other        | Output    |



## 4.1.2 Pin Listing by Pin Number

Table 4-2. Pin Listing by Pin Number (Sheet 1 of 14)

| Pin No. | Pin Name               | Signal Buffer Type | Direction    |
|---------|------------------------|--------------------|--------------|
| A1      | VID5                   | Power/Other        | Output       |
| A2      | VTT_SEL                | Power/Other        | Output       |
| A3      | SKTOCC#                | Power/Other        | Output       |
| A4      | V <sub>TT</sub>        | Power/Other        |              |
| A5      | V <sub>SS</sub>        | Power/Other        |              |
| A6      | A32#                   | Source Sync        | Input/Output |
| A7      | A33#                   | Source Sync        | Input/Output |
| A8      | V <sub>CC</sub>        | Power/Other        |              |
| A9      | A26#                   | Source Sync        | Input/Output |
| A10     | A20#                   | Source Sync        | Input/Output |
| A11     | V <sub>SS</sub>        | Power/Other        |              |
| A12     | A14#                   | Source Sync        | Input/Output |
| A13     | A10#                   | Source Sync        | Input/Output |
| A14     | V <sub>CC</sub>        | Power/Other        |              |
| A15     | FORCEPR#               | Async GTL+         | Input        |
| A16     | TESTH10                | Power/Other        | Input        |
| A17     | LOCK#                  | Common Clk         | Input/Output |
| A18     | V <sub>CC</sub>        | Power/Other        |              |
| A19     | A7#                    | Source Sync        | Input/Output |
| A20     | A4#                    | Source Sync        | Input/Output |
| A21     | V <sub>SS</sub>        | Power/Other        |              |
| A22     | A3#                    | Source Sync        | Input/Output |
| A23     | HITM#                  | Common Clk         | Input/Output |
| A24     | V <sub>CC</sub>        | Power/Other        |              |
| A25     | TMS                    | TAP                | Input        |
| A26     | V <sub>CC_SENSE2</sub> | Power/Other        | Output       |
| A27     | V <sub>SS</sub>        | Power/Other        |              |
| A28     | Reserved               |                    |              |
| A29     | V <sub>SS</sub>        | Power/Other        |              |
| A30     | PROC_ID0               | Power/Other        | Output       |
| A31     | Reserved               |                    |              |
| B1      | Reserved               |                    |              |
| B2      | V <sub>SS</sub>        | Power/Other        |              |
| B3      | VID4                   | Power/Other        | Output       |
| B4      | Reserved               |                    |              |
| B5      | V <sub>TT</sub>        | Power/Other        |              |
| B6      | A38#                   | Source Sync        | Input/Output |
| B7      | A31#                   | Source Sync        | Input/Output |
| B8      | A27#                   | Source Sync        | Input/Output |
| B9      | V <sub>SS</sub>        | Power/Other        |              |
| B10     | A21#                   | Source Sync        | Input/Output |
| B11     | A22#                   | Source Sync        | Input/Output |

Table 4-2. Pin Listing by Pin Number (Sheet 2 of 14)

| Pin No. | Pin Name               | Signal Buffer Type | Direction    |
|---------|------------------------|--------------------|--------------|
| B12     | V <sub>TT</sub>        | Power/Other        |              |
| B13     | A13#                   | Source Sync        | Input/Output |
| B14     | A12#                   | Source Sync        | Input/Output |
| B15     | V <sub>SS</sub>        | Power/Other        |              |
| B16     | A11#                   | Source Sync        | Input/Output |
| B17     | V <sub>SS</sub>        | Power/Other        |              |
| B18     | A5#                    | Source Sync        | Input/Output |
| B19     | REQ0#                  | Common Clk         | Input/Output |
| B20     | V <sub>CC</sub>        | Power/Other        |              |
| B21     | REQ1#                  | Common Clk         | Input/Output |
| B22     | REQ4#                  | Common Clk         | Input/Output |
| B23     | V <sub>SS</sub>        | Power/Other        |              |
| B24     | LINT0                  | Async GTL+         | Input        |
| B25     | PROCHOT#               | Async GTL+         | Output       |
| B26     | V <sub>SS_SENSE2</sub> | Power/Other        | Output       |
| B27     | V <sub>CC_SENSE</sub>  | Power/Other        | Output       |
| B31     | LL_ID0                 | Power/Other        | Output       |
| B29     | PROC_ID1               | Power/Other        | Output       |
| B30     | Reserved               |                    |              |
| B28     | LL_ID1                 | Power/Other        | Output       |
| C1      | VID6                   | Power/Other        | Output       |
| C2      | TESTIN2                | Power/Other        | Input        |
| C3      | VID3                   | Power/Other        | Output       |
| C4      | V <sub>CC</sub>        | Power/Other        |              |
| C5      | V <sub>TT</sub>        | Power/Other        |              |
| C6      | RSP#                   | Common Clk         | Input        |
| C7      | V <sub>SS</sub>        | Power/Other        |              |
| C8      | A35#                   | Source Sync        | Input/Output |
| C9      | A34#                   | Source Sync        | Input/Output |
| C10     | V <sub>TT</sub>        | Power/Other        |              |
| C11     | A30#                   | Source Sync        | Input/Output |
| C12     | A23#                   | Source Sync        | Input/Output |
| C13     | V <sub>SS</sub>        | Power/Other        |              |
| C14     | A16#                   | Source Sync        | Input/Output |
| C15     | A15#                   | Source Sync        | Input/Output |
| C16     | A39#                   | Source Sync        | Input/Output |
| C17     | A8#                    | Source Sync        | Input/Output |
| C18     | A6#                    | Source Sync        | Input/Output |
| C19     | V <sub>SS</sub>        | Power/Other        |              |
| C20     | REQ3#                  | Common Clk         | Input/Output |
| C21     | REQ2#                  | Common Clk         | Input/Output |
| C22     | V <sub>CC</sub>        | Power/Other        |              |



**Table 4-2. Pin Listing by Pin Number (Sheet 3 of 14)**

| Pin No. | Pin Name              | Signal Buffer Type | Direction    |
|---------|-----------------------|--------------------|--------------|
| C23     | DEFER#                | Common Clk         | Input        |
| C24     | TDI                   | TAP                | Input        |
| C25     | V <sub>SS</sub>       | Power/Other        | Input        |
| C26     | IGNNE#                | Async GTL+         | Input        |
| C27     | SMI#                  | Async GTL+         | Input        |
| C28     | PECI                  | Power/Other        | Input/Output |
| C29     | V <sub>SS</sub>       | Power/Other        |              |
| C30     | V <sub>CC</sub>       | Power/Other        |              |
| C31     | Reserved              |                    |              |
| D1      | TESTIN1               | Power/Other        | Input        |
| D2      | V <sub>SS</sub>       | Power/Other        |              |
| D3      | VID2                  | Power/Other        | Output       |
| D4      | STPCLK#               | Async GTL+         | Input        |
| D5      | V <sub>SS</sub>       | Power/Other        |              |
| D6      | INIT#                 | Async GTL+         | Input        |
| D7      | MCERR#                | Common Clk         | Input/Output |
| D8      | V <sub>CC</sub>       | Power/Other        |              |
| D9      | AP1#                  | Common Clk         | Input/Output |
| D10     | V <sub>TT</sub>       | Power/Other        |              |
| D11     | V <sub>SS</sub>       | Power/Other        |              |
| D12     | A29#                  | Source Sync        | Input/Output |
| D13     | A25#                  | Source Sync        | Input/Output |
| D14     | V <sub>CC</sub>       | Power/Other        |              |
| D15     | A18#                  | Source Sync        | Input/Output |
| D16     | A17#                  | Source Sync        | Input/Output |
| D17     | A9#                   | Source Sync        | Input/Output |
| D18     | V <sub>CC</sub>       | Power/Other        |              |
| D19     | ADS#                  | Common Clk         | Input/Output |
| D20     | BR0#                  | Common Clk         | Input/Output |
| D21     | V <sub>SS</sub>       | Power/Other        |              |
| D22     | RS1#                  | Common Clk         | Input        |
| D23     | BPRI#                 | Common Clk         | Input        |
| D24     | V <sub>CC</sub>       | Power/Other        |              |
| D25     | COMP0                 | Power/Other        | Input        |
| D26     | V <sub>SS_SENSE</sub> | Power/Other        | Output       |
| D27     | Reserved              |                    |              |
| D28     | V <sub>SS</sub>       | Power/Other        |              |
| D29     | Reserved              |                    |              |
| D30     | V <sub>SS</sub>       | Power/Other        |              |
| D31     | V <sub>CC</sub>       | Power/Other        |              |
| E1      | V <sub>SS</sub>       | Power/Other        |              |
| E2      | Reserved              |                    |              |
| E3      | VID1                  | Power/Other        | Output       |
| E4      | BPM5#                 | Common Clk         | Input/Output |

**Table 4-2. Pin Listing by Pin Number (Sheet 4 of 14)**

| Pin No. | Pin Name        | Signal Buffer Type | Direction    |
|---------|-----------------|--------------------|--------------|
| E5      | IERR#           | Async GTL+         | Output       |
| E6      | V <sub>CC</sub> | Power/Other        |              |
| E7      | BPM2#           | Common Clk         | Input/Output |
| E8      | BPM4#           | Common Clk         | Input/Output |
| E9      | V <sub>SS</sub> | Power/Other        |              |
| E10     | AP0#            | Common Clk         | Input/Output |
| E11     | V <sub>TT</sub> | Power/Other        |              |
| E12     | V <sub>TT</sub> | Power/Other        |              |
| E13     | A28#            | Source Sync        | Input/Output |
| E14     | A24#            | Source Sync        | Input/Output |
| E15     | V <sub>SS</sub> | Power/Other        |              |
| E16     | COMP1           | Power/Other        | Input        |
| E17     | V <sub>SS</sub> | Power/Other        |              |
| E18     | DRDY#           | Common Clk         | Input/Output |
| E19     | TRDY#           | Common Clk         | Input        |
| E20     | V <sub>CC</sub> | Power/Other        |              |
| E21     | RS0#            | Common Clk         | Input        |
| E22     | HIT#            | Common Clk         | Input/Output |
| E23     | V <sub>SS</sub> | Power/Other        |              |
| E24     | TCK             | TAP                | Input        |
| E25     | TDO             | TAP                | Output       |
| E26     | V <sub>CC</sub> | Power/Other        |              |
| E27     | FERR#/PBE#      | Async GTL+         | Output       |
| E28     | V <sub>CC</sub> | Power/Other        |              |
| E29     | V <sub>SS</sub> | Power/Other        |              |
| E30     | V <sub>CC</sub> | Power/Other        |              |
| E31     | V <sub>SS</sub> | Power/Other        |              |
| F1      | V <sub>CC</sub> | Power/Other        |              |
| F2      | V <sub>SS</sub> | Power/Other        |              |
| F3      | V <sub>SS</sub> | Power/Other        |              |
| F4      | V <sub>CC</sub> | Power/Other        |              |
| F5      | BPM3#           | Common Clk         | Input/Output |
| F6      | BPM0#           | Common Clk         | Input/Output |
| F7      | V <sub>SS</sub> | Power/Other        |              |
| F8      | BPM1#           | Common Clk         | Input/Output |
| F9      | GTLREF_ADD_END  | Power/Other        | Input        |
| F10     | V <sub>TT</sub> | Power/Other        |              |
| F11     | BINIT#          | Common Clk         | Input/Output |
| F12     | BR1#            | Common Clk         | Input/Output |
| F13     | V <sub>SS</sub> | Power/Other        |              |
| F14     | ADSTB1#         | Source Sync        | Input/Output |
| F15     | A19#            | Source Sync        | Input/Output |
| F16     | A36#            | Source Sync        | Input/Output |
| F17     | ADSTB0#         | Source Sync        | Input/Output |



Table 4-2. Pin Listing by Pin Number (Sheet 5 of 14)

| Pin No. | Pin Name        | Signal Buffer Type | Direction    |
|---------|-----------------|--------------------|--------------|
| F18     | DBSY#           | Common Clk         | Input/Output |
| F19     | V <sub>SS</sub> | Power/Other        |              |
| F20     | BNR#            | Common Clk         | Input/Output |
| F21     | RS2#            | Common Clk         | Input        |
| F22     | A37#            | Source Sync        | Input/Output |
| F23     | GTLREF_ADD_MID  | Power/Other        | Input        |
| F24     | TRST#           | TAP                | Input        |
| F25     | V <sub>SS</sub> | Power/Other        |              |
| F26     | THERMTRIP#      | Async GTL+         | Output       |
| F27     | A20M#           | Async GTL+         | Input        |
| F28     | V <sub>SS</sub> | Power/Other        |              |
| F29     | V <sub>CC</sub> | Power/Other        |              |
| F30     | V <sub>SS</sub> | Power/Other        |              |
| F31     | V <sub>CC</sub> | Power/Other        |              |
| G1      | V <sub>SS</sub> | Power/Other        |              |
| G2      | V <sub>CC</sub> | Power/Other        |              |
| G3      | V <sub>SS</sub> | Power/Other        |              |
| G4      | V <sub>CC</sub> | Power/Other        |              |
| G5      | V <sub>SS</sub> | Power/Other        |              |
| G6      | V <sub>CC</sub> | Power/Other        |              |
| G7      | V <sub>SS</sub> | Power/Other        |              |
| G8      | V <sub>CC</sub> | Power/Other        |              |
| G9      | V <sub>SS</sub> | Power/Other        |              |
| G23     | LINT1           | Async GTL+         | Input        |
| G24     | V <sub>CC</sub> | Power/Other        |              |
| G25     | V <sub>SS</sub> | Power/Other        |              |
| G26     | V <sub>CC</sub> | Power/Other        |              |
| G27     | V <sub>SS</sub> | Power/Other        |              |
| G28     | V <sub>CC</sub> | Power/Other        |              |
| G29     | V <sub>SS</sub> | Power/Other        |              |
| G30     | V <sub>CC</sub> | Power/Other        |              |
| G31     | V <sub>SS</sub> | Power/Other        |              |
| H1      | V <sub>CC</sub> | Power/Other        |              |
| H2      | V <sub>SS</sub> | Power/Other        |              |
| H3      | V <sub>CC</sub> | Power/Other        |              |
| H4      | V <sub>SS</sub> | Power/Other        |              |
| H5      | V <sub>CC</sub> | Power/Other        |              |
| H6      | V <sub>SS</sub> | Power/Other        |              |
| H7      | V <sub>CC</sub> | Power/Other        |              |
| H8      | V <sub>SS</sub> | Power/Other        |              |
| H9      | V <sub>CC</sub> | Power/Other        |              |
| H23     | V <sub>CC</sub> | Power/Other        |              |
| H24     | V <sub>SS</sub> | Power/Other        |              |
| H25     | V <sub>CC</sub> | Power/Other        |              |

Table 4-2. Pin Listing by Pin Number (Sheet 6 of 14)

| Pin No. | Pin Name        | Signal Buffer Type | Direction |
|---------|-----------------|--------------------|-----------|
| H26     | V <sub>SS</sub> | Power/Other        |           |
| H27     | V <sub>CC</sub> | Power/Other        |           |
| H28     | V <sub>SS</sub> | Power/Other        |           |
| H29     | V <sub>CC</sub> | Power/Other        |           |
| H30     | V <sub>SS</sub> | Power/Other        |           |
| H31     | V <sub>CC</sub> | Power/Other        |           |
| J1      | V <sub>SS</sub> | Power/Other        |           |
| J2      | V <sub>CC</sub> | Power/Other        |           |
| J3      | V <sub>SS</sub> | Power/Other        |           |
| J4      | V <sub>CC</sub> | Power/Other        |           |
| J5      | V <sub>SS</sub> | Power/Other        |           |
| J6      | V <sub>CC</sub> | Power/Other        |           |
| J7      | V <sub>SS</sub> | Power/Other        |           |
| J8      | V <sub>CC</sub> | Power/Other        |           |
| J9      | V <sub>SS</sub> | Power/Other        |           |
| J23     | V <sub>SS</sub> | Power/Other        |           |
| J24     | V <sub>CC</sub> | Power/Other        |           |
| J25     | V <sub>SS</sub> | Power/Other        |           |
| J26     | V <sub>CC</sub> | Power/Other        |           |
| J27     | V <sub>SS</sub> | Power/Other        |           |
| J28     | V <sub>CC</sub> | Power/Other        |           |
| J29     | V <sub>SS</sub> | Power/Other        |           |
| J30     | V <sub>CC</sub> | Power/Other        |           |
| J31     | V <sub>SS</sub> | Power/Other        |           |
| K1      | V <sub>CC</sub> | Power/Other        |           |
| K2      | V <sub>SS</sub> | Power/Other        |           |
| K3      | V <sub>CC</sub> | Power/Other        |           |
| K4      | V <sub>SS</sub> | Power/Other        |           |
| K5      | V <sub>CC</sub> | Power/Other        |           |
| K6      | V <sub>SS</sub> | Power/Other        |           |
| K7      | V <sub>CC</sub> | Power/Other        |           |
| K8      | V <sub>SS</sub> | Power/Other        |           |
| K9      | V <sub>CC</sub> | Power/Other        |           |
| K23     | V <sub>CC</sub> | Power/Other        |           |
| K24     | V <sub>SS</sub> | Power/Other        |           |
| K25     | V <sub>CC</sub> | Power/Other        |           |
| K26     | V <sub>SS</sub> | Power/Other        |           |
| K27     | V <sub>CC</sub> | Power/Other        |           |
| K28     | V <sub>SS</sub> | Power/Other        |           |
| K29     | V <sub>CC</sub> | Power/Other        |           |
| K30     | V <sub>SS</sub> | Power/Other        |           |
| K31     | V <sub>CC</sub> | Power/Other        |           |
| L1      | V <sub>SS</sub> | Power/Other        |           |
| L2      | V <sub>CC</sub> | Power/Other        |           |



Table 4-2. Pin Listing by Pin Number (Sheet 7 of 14)

| Pin No. | Pin Name        | Signal Buffer Type | Direction |
|---------|-----------------|--------------------|-----------|
| L3      | V <sub>SS</sub> | Power/Other        |           |
| L4      | V <sub>CC</sub> | Power/Other        |           |
| L5      | V <sub>SS</sub> | Power/Other        |           |
| L6      | V <sub>CC</sub> | Power/Other        |           |
| L7      | V <sub>SS</sub> | Power/Other        |           |
| L8      | V <sub>CC</sub> | Power/Other        |           |
| L9      | V <sub>SS</sub> | Power/Other        |           |
| L23     | V <sub>SS</sub> | Power/Other        |           |
| L24     | V <sub>CC</sub> | Power/Other        |           |
| L25     | V <sub>SS</sub> | Power/Other        |           |
| L26     | V <sub>CC</sub> | Power/Other        |           |
| L27     | V <sub>SS</sub> | Power/Other        |           |
| L28     | V <sub>CC</sub> | Power/Other        |           |
| L29     | V <sub>SS</sub> | Power/Other        |           |
| L30     | V <sub>CC</sub> | Power/Other        |           |
| L31     | V <sub>SS</sub> | Power/Other        |           |
| M1      | V <sub>CC</sub> | Power/Other        |           |
| M2      | V <sub>SS</sub> | Power/Other        |           |
| M3      | V <sub>CC</sub> | Power/Other        |           |
| M4      | V <sub>SS</sub> | Power/Other        |           |
| M5      | V <sub>CC</sub> | Power/Other        |           |
| M6      | V <sub>SS</sub> | Power/Other        |           |
| M7      | V <sub>CC</sub> | Power/Other        |           |
| M8      | V <sub>SS</sub> | Power/Other        |           |
| M9      | V <sub>CC</sub> | Power/Other        |           |
| M23     | V <sub>CC</sub> | Power/Other        |           |
| M24     | V <sub>SS</sub> | Power/Other        |           |
| M25     | V <sub>CC</sub> | Power/Other        |           |
| M26     | V <sub>SS</sub> | Power/Other        |           |
| M27     | V <sub>CC</sub> | Power/Other        |           |
| M28     | V <sub>SS</sub> | Power/Other        |           |
| M29     | V <sub>CC</sub> | Power/Other        |           |
| M30     | V <sub>SS</sub> | Power/Other        |           |
| M31     | V <sub>CC</sub> | Power/Other        |           |
| N1      | V <sub>CC</sub> | Power/Other        |           |
| N2      | V <sub>SS</sub> | Power/Other        |           |
| N3      | V <sub>CC</sub> | Power/Other        |           |
| N4      | V <sub>SS</sub> | Power/Other        |           |
| N5      | V <sub>CC</sub> | Power/Other        |           |
| N6      | V <sub>SS</sub> | Power/Other        |           |
| N7      | V <sub>CC</sub> | Power/Other        |           |
| N8      | V <sub>SS</sub> | Power/Other        |           |
| N9      | V <sub>CC</sub> | Power/Other        |           |
| N23     | V <sub>CC</sub> | Power/Other        |           |

Table 4-2. Pin Listing by Pin Number (Sheet 8 of 14)

| Pin No. | Pin Name        | Signal Buffer Type | Direction |
|---------|-----------------|--------------------|-----------|
| N24     | V <sub>SS</sub> | Power/Other        |           |
| N25     | V <sub>CC</sub> | Power/Other        |           |
| N26     | V <sub>SS</sub> | Power/Other        |           |
| N27     | V <sub>CC</sub> | Power/Other        |           |
| N28     | V <sub>SS</sub> | Power/Other        |           |
| N29     | V <sub>CC</sub> | Power/Other        |           |
| N30     | V <sub>SS</sub> | Power/Other        |           |
| N31     | V <sub>CC</sub> | Power/Other        |           |
| P1      | V <sub>SS</sub> | Power/Other        |           |
| P2      | V <sub>CC</sub> | Power/Other        |           |
| P3      | V <sub>SS</sub> | Power/Other        |           |
| P4      | V <sub>CC</sub> | Power/Other        |           |
| P5      | V <sub>SS</sub> | Power/Other        |           |
| P6      | V <sub>CC</sub> | Power/Other        |           |
| P7      | V <sub>SS</sub> | Power/Other        |           |
| P8      | V <sub>CC</sub> | Power/Other        |           |
| P9      | V <sub>SS</sub> | Power/Other        |           |
| P23     | V <sub>SS</sub> | Power/Other        |           |
| P24     | V <sub>CC</sub> | Power/Other        |           |
| P25     | V <sub>SS</sub> | Power/Other        |           |
| P26     | V <sub>CC</sub> | Power/Other        |           |
| P27     | V <sub>SS</sub> | Power/Other        |           |
| P28     | V <sub>CC</sub> | Power/Other        |           |
| P29     | V <sub>SS</sub> | Power/Other        |           |
| P30     | V <sub>CC</sub> | Power/Other        |           |
| P31     | V <sub>SS</sub> | Power/Other        |           |
| R1      | V <sub>CC</sub> | Power/Other        |           |
| R2      | V <sub>SS</sub> | Power/Other        |           |
| R3      | V <sub>CC</sub> | Power/Other        |           |
| R4      | V <sub>SS</sub> | Power/Other        |           |
| R5      | V <sub>CC</sub> | Power/Other        |           |
| R6      | V <sub>SS</sub> | Power/Other        |           |
| R7      | V <sub>CC</sub> | Power/Other        |           |
| R8      | V <sub>SS</sub> | Power/Other        |           |
| R9      | V <sub>CC</sub> | Power/Other        |           |
| R23     | V <sub>CC</sub> | Power/Other        |           |
| R24     | V <sub>SS</sub> | Power/Other        |           |
| R25     | V <sub>CC</sub> | Power/Other        |           |
| R26     | V <sub>SS</sub> | Power/Other        |           |
| R27     | V <sub>CC</sub> | Power/Other        |           |
| R28     | V <sub>SS</sub> | Power/Other        |           |
| R29     | V <sub>CC</sub> | Power/Other        |           |
| R30     | V <sub>SS</sub> | Power/Other        |           |
| R31     | V <sub>CC</sub> | Power/Other        |           |



Table 4-2. Pin Listing by Pin Number (Sheet 9 of 14)

| Pin No. | Pin Name        | Signal Buffer Type | Direction |
|---------|-----------------|--------------------|-----------|
| T1      | V <sub>SS</sub> | Power/Other        |           |
| T2      | V <sub>CC</sub> | Power/Other        |           |
| T3      | V <sub>SS</sub> | Power/Other        |           |
| T4      | V <sub>CC</sub> | Power/Other        |           |
| T5      | V <sub>SS</sub> | Power/Other        |           |
| T6      | V <sub>CC</sub> | Power/Other        |           |
| T7      | V <sub>SS</sub> | Power/Other        |           |
| T8      | V <sub>CC</sub> | Power/Other        |           |
| T9      | V <sub>SS</sub> | Power/Other        |           |
| T23     | V <sub>SS</sub> | Power/Other        |           |
| T24     | V <sub>CC</sub> | Power/Other        |           |
| T25     | V <sub>SS</sub> | Power/Other        |           |
| T26     | V <sub>CC</sub> | Power/Other        |           |
| T27     | V <sub>SS</sub> | Power/Other        |           |
| T28     | V <sub>CC</sub> | Power/Other        |           |
| T29     | V <sub>SS</sub> | Power/Other        |           |
| T30     | V <sub>CC</sub> | Power/Other        |           |
| T31     | V <sub>SS</sub> | Power/Other        |           |
| U1      | V <sub>CC</sub> | Power/Other        |           |
| U2      | V <sub>SS</sub> | Power/Other        |           |
| U3      | V <sub>CC</sub> | Power/Other        |           |
| U4      | V <sub>SS</sub> | Power/Other        |           |
| U5      | V <sub>CC</sub> | Power/Other        |           |
| U6      | V <sub>SS</sub> | Power/Other        |           |
| U7      | V <sub>CC</sub> | Power/Other        |           |
| U8      | V <sub>SS</sub> | Power/Other        |           |
| U9      | V <sub>CC</sub> | Power/Other        |           |
| U23     | V <sub>CC</sub> | Power/Other        |           |
| U24     | V <sub>SS</sub> | Power/Other        |           |
| U25     | V <sub>CC</sub> | Power/Other        |           |
| U26     | V <sub>SS</sub> | Power/Other        |           |
| U27     | V <sub>CC</sub> | Power/Other        |           |
| U28     | V <sub>SS</sub> | Power/Other        |           |
| U29     | V <sub>CC</sub> | Power/Other        |           |
| U30     | V <sub>SS</sub> | Power/Other        |           |
| U31     | V <sub>CC</sub> | Power/Other        |           |
| V1      | V <sub>SS</sub> | Power/Other        |           |
| V2      | V <sub>CC</sub> | Power/Other        |           |
| V3      | V <sub>SS</sub> | Power/Other        |           |
| V4      | V <sub>CC</sub> | Power/Other        |           |
| V5      | V <sub>SS</sub> | Power/Other        |           |
| V6      | V <sub>CC</sub> | Power/Other        |           |
| V7      | V <sub>SS</sub> | Power/Other        |           |
| V8      | V <sub>CC</sub> | Power/Other        |           |

Table 4-2. Pin Listing by Pin Number (Sheet 10 of 14)

| Pin No. | Pin Name        | Signal Buffer Type | Direction    |
|---------|-----------------|--------------------|--------------|
| V9      | V <sub>SS</sub> | Power/Other        |              |
| V23     | V <sub>SS</sub> | Power/Other        |              |
| V24     | V <sub>CC</sub> | Power/Other        |              |
| V25     | V <sub>SS</sub> | Power/Other        |              |
| V26     | V <sub>CC</sub> | Power/Other        |              |
| V27     | V <sub>SS</sub> | Power/Other        |              |
| V28     | V <sub>CC</sub> | Power/Other        |              |
| V29     | V <sub>SS</sub> | Power/Other        |              |
| V30     | V <sub>CC</sub> | Power/Other        |              |
| V31     | V <sub>SS</sub> | Power/Other        |              |
| W1      | V <sub>CC</sub> | Power/Other        |              |
| W2      | V <sub>SS</sub> | Power/Other        |              |
| W3      | TESTH11         | Power/Other        | Input        |
| W4      | V <sub>SS</sub> | Power/Other        |              |
| W5      | BCLK1           | FSB Clk            | Input        |
| W6      | V <sub>TT</sub> | Power/Other        |              |
| W7      | V <sub>TT</sub> | Power/Other        |              |
| W8      | V <sub>TT</sub> | Power/Other        |              |
| W9      | GTLREF_DATA_END | Power/Other        | Input        |
| W23     | GTLREF_DATA_MID | Power/Other        | Input        |
| W24     | V <sub>SS</sub> | Power/Other        |              |
| W25     | V <sub>CC</sub> | Power/Other        |              |
| W26     | V <sub>SS</sub> | Power/Other        |              |
| W27     | V <sub>CC</sub> | Power/Other        |              |
| W28     | V <sub>SS</sub> | Power/Other        |              |
| W29     | V <sub>CC</sub> | Power/Other        |              |
| W30     | V <sub>SS</sub> | Power/Other        |              |
| W31     | V <sub>CC</sub> | Power/Other        |              |
| Y1      | V <sub>SS</sub> | Power/Other        |              |
| Y2      | V <sub>CC</sub> | Power/Other        |              |
| Y3      | V <sub>SS</sub> | Power/Other        |              |
| Y4      | BCLK0           | FSB Clk            | Input        |
| Y5      | V <sub>SS</sub> | Power/Other        |              |
| Y6      | V <sub>TT</sub> | Power/Other        |              |
| Y7      | V <sub>SS</sub> | Power/Other        |              |
| Y8      | RESET#          | Common Clk         | Input        |
| Y9      | D62#            | Source Sync        | Input/Output |
| Y10     | V <sub>TT</sub> | Power/Other        |              |
| Y11     | DSTBP3#         | Source Sync        | Input/Output |
| Y12     | DSTBN3#         | Source Sync        | Input/Output |
| Y13     | V <sub>SS</sub> | Power/Other        |              |
| Y14     | DSTBP2#         | Source Sync        | Input/Output |
| Y15     | DSTBN2#         | Source Sync        | Input/Output |
| Y16     | V <sub>CC</sub> | Power/Other        |              |



**Table 4-2. Pin Listing by Pin Number (Sheet 11 of 14)**

| Pin No. | Pin Name        | Signal Buffer Type | Direction    |
|---------|-----------------|--------------------|--------------|
| Y17     | DSTBP1#         | Source Sync        | Input/Output |
| Y18     | DSTBN1#         | Source Sync        | Input/Output |
| Y19     | V <sub>SS</sub> | Power/Other        |              |
| Y20     | DSTBP0#         | Source Sync        | Input/Output |
| Y21     | DSTBN0#         | Source Sync        | Input/Output |
| Y22     | V <sub>CC</sub> | Power/Other        |              |
| Y23     | D5#             | Source Sync        | Input/Output |
| Y24     | D2#             | Source Sync        | Input/Output |
| Y25     | V <sub>SS</sub> | Power/Other        |              |
| Y26     | D0#             | Source Sync        | Input/Output |
| Y27     | Reserved        |                    |              |
| Y28     | Reserved        |                    |              |
| Y29     | Reserved        |                    |              |
| Y30     | V <sub>CC</sub> | Power/Other        |              |
| Y31     | BSEL2           | Power/Other        | Output       |
| AA1     | V <sub>CC</sub> | Power/Other        |              |
| AA2     | V <sub>SS</sub> | Power/Other        |              |
| AA3     | BSEL0           | Power/Other        | Output       |
| AA4     | BPMb0#          | Common Clk         | Input/Output |
| AA5     | Reserved        |                    |              |
| AA6     | V <sub>CC</sub> | Power/Other        |              |
| AA7     | V <sub>TT</sub> | Power/Other        |              |
| AA8     | D61#            | Source Sync        | Input/Output |
| AA9     | V <sub>SS</sub> | Power/Other        |              |
| AA10    | D54#            | Source Sync        | Input/Output |
| AA11    | D53#            | Source Sync        | Input/Output |
| AA12    | V <sub>TT</sub> | Power/Other        |              |
| AA13    | D48#            | Source Sync        | Input/Output |
| AA14    | D49#            | Source Sync        | Input/Output |
| AA15    | V <sub>SS</sub> | Power/Other        |              |
| AA16    | D33#            | Source Sync        | Input/Output |
| AA17    | V <sub>SS</sub> | Power/Other        |              |
| AA18    | D24#            | Source Sync        | Input/Output |
| AA19    | D15#            | Source Sync        | Input/Output |
| AA20    | V <sub>CC</sub> | Power/Other        |              |
| AA21    | D11#            | Source Sync        | Input/Output |
| AA22    | D10#            | Source Sync        | Input/Output |
| AA23    | V <sub>SS</sub> | Power/Other        |              |
| AA24    | D6#             | Source Sync        | Input/Output |
| AA25    | D3#             | Source Sync        | Input/Output |
| AA26    | V <sub>CC</sub> | Power/Other        |              |
| AA27    | D1#             | Source Sync        | Input/Output |
| AA28    | Reserved        |                    |              |
| AA29    | SM_EP_A0        | SMBus              | Input        |

**Table 4-2. Pin Listing by Pin Number (Sheet 12 of 14)**

| Pin No. | Pin Name        | Signal Buffer Type | Direction    |
|---------|-----------------|--------------------|--------------|
| AA30    | V <sub>SS</sub> | Power/Other        |              |
| AA31    | V <sub>CC</sub> | Power/Other        |              |
| AB1     | V <sub>SS</sub> | Power/Other        |              |
| AB2     | V <sub>CC</sub> | Power/Other        |              |
| AB3     | BSEL1           | Power/Other        | Output       |
| AB4     | Reserved        |                    |              |
| AB5     | V <sub>SS</sub> | Power/Other        |              |
| AB6     | D63#            | Source Sync        | Input/Output |
| AB7     | PWRGOOD         | Async GTL+         | Input        |
| AB8     | V <sub>CC</sub> | Power/Other        |              |
| AB9     | DBI3#           | Source Sync        | Input/Output |
| AB10    | D55#            | Source Sync        | Input/Output |
| AB11    | V <sub>SS</sub> | Power/Other        |              |
| AB12    | D51#            | Source Sync        | Input/Output |
| AB13    | D52#            | Source Sync        | Input/Output |
| AB14    | V <sub>CC</sub> | Power/Other        |              |
| AB15    | D37#            | Source Sync        | Input/Output |
| AB16    | D32#            | Source Sync        | Input/Output |
| AB17    | D31#            | Source Sync        | Input/Output |
| AB18    | V <sub>CC</sub> | Power/Other        |              |
| AB19    | D14#            | Source Sync        | Input/Output |
| AB20    | D12#            | Source Sync        | Input/Output |
| AB21    | V <sub>SS</sub> | Power/Other        |              |
| AB22    | D13#            | Source Sync        | Input/Output |
| AB23    | D9#             | Source Sync        | Input/Output |
| AB24    | V <sub>CC</sub> | Power/Other        |              |
| AB25    | D8#             | Source Sync        | Input/Output |
| AB26    | D7#             | Source Sync        | Input/Output |
| AB27    | V <sub>SS</sub> | Power/Other        |              |
| AB28    | SM_EP_A2        | SMBus              | Input        |
| AB29    | SM_EP_A1        | SMBus              | Input        |
| AB30    | V <sub>CC</sub> | Power/Other        |              |
| AB31    | V <sub>SS</sub> | Power/Other        |              |
| AC1     | BPMb1#          | Common Clk         | Output       |
| AC2     | V <sub>SS</sub> | Power/Other        |              |
| AC3     | V <sub>CC</sub> | Power/Other        |              |
| AC4     | V <sub>TT</sub> | Power/Other        |              |
| AC5     | D60#            | Source Sync        | Input/Output |
| AC6     | D59#            | Source Sync        | Input/Output |
| AC7     | V <sub>SS</sub> | Power/Other        |              |
| AC8     | D56#            | Source Sync        | Input/Output |
| AC9     | D47#            | Source Sync        | Input/Output |
| AC10    | V <sub>TT</sub> | Power/Other        |              |
| AC11    | D43#            | Source Sync        | Input/Output |



Table 4-2. Pin Listing by Pin Number (Sheet 13 of 14)

| Pin No. | Pin Name           | Signal Buffer Type | Direction    |
|---------|--------------------|--------------------|--------------|
| AC12    | D41#               | Source Sync        | Input/Output |
| AC13    | V <sub>SS</sub>    | Power/Other        |              |
| AC14    | D50#               | Source Sync        | Input/Output |
| AC15    | DP2#               | Common Clk         | Input/Output |
| AC16    | V <sub>CC</sub>    | Power/Other        |              |
| AC17    | D34#               | Source Sync        | Input/Output |
| AC18    | DP0#               | Common Clk         | Input/Output |
| AC19    | V <sub>SS</sub>    | Power/Other        |              |
| AC20    | D25#               | Source Sync        | Input/Output |
| AC21    | D26#               | Source Sync        | Input/Output |
| AC22    | V <sub>CC</sub>    | Power/Other        |              |
| AC23    | D23#               | Source Sync        | Input/Output |
| AC24    | D20#               | Source Sync        | Input/Output |
| AC25    | V <sub>SS</sub>    | Power/Other        |              |
| AC26    | D17#               | Source Sync        | Input/Output |
| AC27    | DBI0#              | Source Sync        | Input/Output |
| AC28    | SM_CLK             | SMBus              | Input        |
| AC29    | SM_DAT             | SMBus              | Output       |
| AC30    | Reserved           |                    |              |
| AC31    | V <sub>CC</sub>    | Power/Other        |              |
| AD1     | V <sub>CCPLL</sub> | Power/Other        | Input        |
| AD2     | V <sub>CC</sub>    | Power/Other        |              |
| AD3     | V <sub>SS</sub>    | Power/Other        |              |
| AD4     | Reserved           |                    |              |
| AD5     | V <sub>TT</sub>    | Power/Other        |              |
| AD6     | Reserved           |                    |              |
| AD7     | D57#               | Source Sync        | Input/Output |
| AD8     | D46#               | Source Sync        | Input/Output |
| AD9     | V <sub>SS</sub>    | Power/Other        |              |
| AD10    | D45#               | Source Sync        | Input/Output |
| AD11    | D40#               | Source Sync        | Input/Output |
| AD12    | V <sub>TT</sub>    | Power/Other        |              |
| AD13    | D38#               | Source Sync        | Input/Output |
| AD14    | D39#               | Source Sync        | Input/Output |
| AD15    | V <sub>SS</sub>    | Power/Other        |              |
| AD16    | Reserved           |                    |              |
| AD17    | V <sub>SS</sub>    | Power/Other        |              |
| AD18    | D36#               | Source Sync        | Input/Output |
| AD19    | D30#               | Source Sync        | Input/Output |
| AD20    | V <sub>CC</sub>    | Power/Other        |              |

Table 4-2. Pin Listing by Pin Number (Sheet 14 of 14)

| Pin No. | Pin Name        | Signal Buffer Type | Direction    |
|---------|-----------------|--------------------|--------------|
| AD21    | D29#            | Source Sync        | Input/Output |
| AD22    | DBI1#           | Source Sync        | Input/Output |
| AD23    | V <sub>SS</sub> | Power/Other        |              |
| AD24    | D21#            | Source Sync        | Input/Output |
| AD25    | D18#            | Source Sync        | Input/Output |
| AD26    | V <sub>CC</sub> | Power/Other        |              |
| AD27    | D4#             | Source Sync        | Input/Output |
| AD28    | Reserved        |                    |              |
| AD29    | SM_WP           | SMBus              | Input        |
| AD30    | Reserved        |                    |              |
| AD31    | Reserved        |                    |              |
| AE2     | BPMb2#          | Common Clk         | Output       |
| AE3     | BPMb3#          | Common Clk         | Input/Output |
| AE4     | V <sub>TT</sub> | Power/Other        |              |
| AE5     | V <sub>TT</sub> | Power/Other        |              |
| AE6     | V <sub>SS</sub> | Power/Other        | Input        |
| AE7     | D58#            | Source Sync        | Input/Output |
| AE8     | Reserved        |                    |              |
| AE9     | D44#            | Source Sync        | Input/Output |
| AE10    | D42#            | Source Sync        | Input/Output |
| AE11    | V <sub>SS</sub> | Power/Other        |              |
| AE12    | DBI2#           | Source Sync        | Input/Output |
| AE13    | D35#            | Source Sync        | Input/Output |
| AE14    | V <sub>CC</sub> | Power/Other        |              |
| AE15    | COMP2           | Power/Other        | Input        |
| AE16    | COMP3           | Power/Other        | Input        |
| AE17    | DP3#            | Common Clk         | Input/Output |
| AE18    | V <sub>CC</sub> | Power/Other        |              |
| AE19    | DP1#            | Common Clk         | Input/Output |
| AE20    | D28#            | Source Sync        | Input/Output |
| AE21    | V <sub>SS</sub> | Power/Other        |              |
| AE22    | D27#            | Source Sync        | Input/Output |
| AE23    | D22#            | Source Sync        | Input/Output |
| AE24    | V <sub>CC</sub> | Power/Other        |              |
| AE25    | D19#            | Source Sync        | Input/Output |
| AE26    | D16#            | Source Sync        | Input/Output |
| AE27    | V <sub>SS</sub> | Power/Other        |              |
| AE28    | SM_VCC          | Power/Other        |              |
| AE29    | SM_VCC          | Power/Other        |              |
| AE30    | Reserved        |                    |              |





## 5 Signal Definitions

### 5.1 Signal Definitions.

Table 5-1. Signal Definitions (Sheet 1 of 8)

| Name                        | Type               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Notes           |                    |                             |           |                  |         |          |      |      |           |      |      |  |
|-----------------------------|--------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|--------------------|-----------------------------|-----------|------------------|---------|----------|------|------|-----------|------|------|--|
| A[39:3]#                    | I/O                | <p>A[39:3]# (Address) define a 2<sup>40</sup>-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Intel® Xeon® Processor 7200 Series and 7300 Series FSB. A[39:3]# are protected by parity signals AP[1:0]#. A[39:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#.</p> <p>On the active-to-inactive transition of RESET#, the processors sample a subset of the A[39:3]# pins to determine their power-on configuration. See <a href="#">Section 7.1</a>.</p>                                                                                                                                                         |                 |                    |                             |           |                  |         |          |      |      |           |      |      |  |
| A20M#                       | I                  | <p>If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1 MB boundary. Assertion of A20M# is only supported in real mode.</p> <p>A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O write bus transaction.</p>                                                                                                                                                                                                                                                                                                    |                 |                    |                             |           |                  |         |          |      |      |           |      |      |  |
| ADS#                        | I/O                | <p>ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[39:3]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must be connected to the appropriate pins on all Intel® Xeon® Processor 7200 Series and 7300 Series FSB agents.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                |                 |                    |                             |           |                  |         |          |      |      |           |      |      |  |
| ADSTB[1:0]#                 | I/O                | <p>Address strobes are used to latch A[39:3]# and REQ[4:0]# on their rising and falling edge. Strobes are associated with signals as shown below.</p> <table><thead><tr><th>Signals</th><th>Associated Strobes</th></tr></thead><tbody><tr><td>REQ[4:0],<br/>A[37:36,16:3]#</td><td>ADSTB0#</td></tr><tr><td>A[39:38, 35:17]#</td><td>ADSTB1#</td></tr></tbody></table>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Signals         | Associated Strobes | REQ[4:0],<br>A[37:36,16:3]# | ADSTB0#   | A[39:38, 35:17]# | ADSTB1# |          |      |      |           |      |      |  |
| Signals                     | Associated Strobes |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                 |                    |                             |           |                  |         |          |      |      |           |      |      |  |
| REQ[4:0],<br>A[37:36,16:3]# | ADSTB0#            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                 |                    |                             |           |                  |         |          |      |      |           |      |      |  |
| A[39:38, 35:17]#            | ADSTB1#            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                 |                    |                             |           |                  |         |          |      |      |           |      |      |  |
| AP[1:0]#                    | I/O                | <p>AP[1:0]# (Address Parity) are driven by the requestor one common clock after ADS#, A[39:3]#, REQ[4:0]# are driven. A correct parity signal is electrically high if an even number of covered signals are electrically low and electrically low if an odd number of covered signals are electrically low. This allows parity to be electrically high when all the covered signals are electrically high. AP[1:0]# should connect the appropriate pins of all Intel® Xeon® Processor 7200 Series and 7300 Series FSB agents. The following table defines the coverage for these signals.</p> <table><thead><tr><th>Request Signals</th><th>Subphase 1</th><th>Subphase 2</th></tr></thead><tbody><tr><td>A[39:24]#</td><td>AP0#</td><td>AP1#</td></tr><tr><td>A[23:3]#</td><td>AP1#</td><td>AP0#</td></tr><tr><td>REQ[4:0]#</td><td>AP1#</td><td>AP0#</td></tr></tbody></table> | Request Signals | Subphase 1         | Subphase 2                  | A[39:24]# | AP0#             | AP1#    | A[23:3]# | AP1# | AP0# | REQ[4:0]# | AP1# | AP0# |  |
| Request Signals             | Subphase 1         | Subphase 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                 |                    |                             |           |                  |         |          |      |      |           |      |      |  |
| A[39:24]#                   | AP0#               | AP1#                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                 |                    |                             |           |                  |         |          |      |      |           |      |      |  |
| A[23:3]#                    | AP1#               | AP0#                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                 |                    |                             |           |                  |         |          |      |      |           |      |      |  |
| REQ[4:0]#                   | AP1#               | AP0#                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                 |                    |                             |           |                  |         |          |      |      |           |      |      |  |
| BCLK[1:0]                   | I                  | <p>The differential bus clock pair BCLK[1:0] (Bus Clock) determines the FSB frequency. All processor FSB agents must receive these signals to drive their outputs and latch their inputs.</p> <p>All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V<sub>CROSS</sub>.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                 |                    |                             |           |                  |         |          |      |      |           |      |      |  |



Table 5-1. Signal Definitions (Sheet 2 of 8)

| Name                                          | Type                        | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Notes |
|-----------------------------------------------|-----------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| BINIT#                                        | I/O                         | <p>BINIT# (Bus Initialization) may be observed and driven by all processor FSB agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation.</p> <p>If BINIT# observation is enabled during power-on configuration (see <a href="#">Section 7.1</a>) and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their I/O Queue (IOQ) and transaction tracking state machines upon observation of BINIT# assertion. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the FSB and attempt completion of their bus queue and IOQ entries.</p> <p>If BINIT# observation is disabled during power-on configuration, a priority agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.</p> |       |
| BNR#                                          | I/O                         | <p>BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.</p> <p>Since multiple agents might need to request a bus stall at the same time, BNR# is a wired-OR signal which must connect the appropriate pins of all processor FSB agents. In order to avoid wired-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                  |       |
| BPM5#<br>BPM4#<br>BPM3#<br>BPM[2:1]#<br>BPM0# | I/O<br>O<br>I/O<br>O<br>I/O | <p>BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all FSB agents.</p> <p>BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness.</p> <p>BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processors.</p> <p>BPM[5:4]# must be bussed to all bus agents. Please refer to the appropriate platform design guidelines for more detailed information.</p>                                                                                                                                                                                                                                                           |       |
| BPMb3#<br>BPMb[2:1]#<br>BPMb0#                | I/O<br>O<br>I/O             | <p>BPMb[3:0]# (Breakpoint Monitor) are a second set of breakpoint and performance monitor signals. They are additional outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPMb[3:0]# should connect the appropriate pins of all FSB agents.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |       |
| BPRI#                                         | I                           | <p>BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor FSB. It must connect the appropriate pins of all processor FSB agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |       |
| BR[1:0]#                                      | I/O                         | <p>The BR[1:0]# signals are sampled on the active-to-inactive transition of RESET#. The signal which the agent samples asserted determines its agent ID. BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. These signals do not have on-die termination and must be terminated.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |       |
| BSEL[2:0]                                     | O                           | <p>The BCLK[1:0] frequency select signals BSEL[2:0] are used to select the processor input clock frequency. <a href="#">Table 2-2</a> defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processors, chipset, and clock synthesizer. All FSB agents must operate at the same frequency. For more information about these signals, including termination recommendations, refer to the appropriate platform design guideline.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |       |
| COMP[3:0]                                     | I                           | <p>COMP[3:0] must be terminated to VSS on the baseboard using precision resistors. These inputs configure the AGTL+ drivers of the processor. Refer to the appropriate platform design guidelines for implementation details.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |       |



Table 5-1. Signal Definitions (Sheet 3 of 8)

| Name       | Type             | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Notes      |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
|------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------------|-------|-----------|-------|------------|------------|------------|-------|------------|---|---|------------|---|---|--|
| D[63:0] #  | I/O              | <p>D[63:0] # (Data) are the data signals. These signals provide a 64-bit data path between the processor FSB agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.</p> <p>D[63:0] # are quad-pumped signals, and will thus be driven four times in a common clock period. D[63:0] # are latched off the falling edge of both DSTBP[3:0] # and DSTBN[3:0] #. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to strobes and DBI#.</p> <table><tr><th>Data Group</th><th>DSTBN # / DSTBP#</th><th>DBI #</th></tr><tr><td>D[15:0] #</td><td>0</td><td>0</td></tr><tr><td>D[31:16] #</td><td>1</td><td>1</td></tr><tr><td>D[47:32] #</td><td>2</td><td>2</td></tr><tr><td>D[63:48] #</td><td>3</td><td>3</td></tr></table> <p>Furthermore, the DBI# signals determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.</p> | Data Group | DSTBN # / DSTBP# | DBI # | D[15:0] # | 0     | 0          | D[31:16] # | 1          | 1     | D[47:32] # | 2 | 2 | D[63:48] # | 3 | 3 |  |
| Data Group | DSTBN # / DSTBP# | DBI #                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| D[15:0] #  | 0                | 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| D[31:16] # | 1                | 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| D[47:32] # | 2                | 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| D[63:48] # | 3                | 3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| DBI[3:0] # | I/O              | <p>DBI[3:0] # (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0] # signals. The DBI[3:0] # signals are activated when the data on the data bus is inverted. If more than half the data bits, within, within a 16-bit group, would have been asserted electronically low, the bus agent may invert the data bus signals for that particular sub-phase for that 16-bit group.</p> <p><b>DBI[3:0] Assignment to Data Bus</b></p> <table><tr><th>Bus Signal</th><th>Data Bus Signals</th></tr><tr><td>DBI0#</td><td>D[15:0] #</td></tr><tr><td>DBI1#</td><td>D[31:16] #</td></tr><tr><td>DBI2#</td><td>D[47:32] #</td></tr><tr><td>DBI3#</td><td>D[63:48] #</td></tr></table>                                                                                                                                                                                                                                                                                                                                                                                                                                            | Bus Signal | Data Bus Signals | DBI0# | D[15:0] # | DBI1# | D[31:16] # | DBI2#      | D[47:32] # | DBI3# | D[63:48] # |   |   |            |   |   |  |
| Bus Signal | Data Bus Signals |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| DBI0#      | D[15:0] #        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| DBI1#      | D[31:16] #       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| DBI2#      | D[47:32] #       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| DBI3#      | D[63:48] #       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| DBSY#      | I/O              | <p>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor FSB to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor FSB agents.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| DEFER#     | I                | <p>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all processor FSB agents.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| DP[3:0] #  | I/O              | <p>DP[3:0] # (Data Parity) provide parity protection for the D[63:0] # signals. They are driven by the agent responsible for driving D[63:0] #, and must connect the appropriate pins of all processor FSB agents.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |
| DRDY#      | I/O              | <p>DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor FSB agents.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |            |                  |       |           |       |            |            |            |       |            |   |   |            |   |   |  |



Table 5-1. Signal Definitions (Sheet 4 of 8)

| Name                               | Type               | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Notes   |                    |                 |         |                  |         |                  |         |                  |         |  |
|------------------------------------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|--------------------|-----------------|---------|------------------|---------|------------------|---------|------------------|---------|--|
| DSTBN[3:0]#                        | I/O                | <div>Data strobe used to latch in D[63:0]#.</div> <table><thead><tr><th>Signals</th><th>Associated Strobes</th></tr></thead><tbody><tr><td>D[15:0]#, DBI0#</td><td>DSTBN0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBN1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBN3#</td></tr></tbody></table>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Signals | Associated Strobes | D[15:0]#, DBI0# | DSTBN0# | D[31:16]#, DBI1# | DSTBN1# | D[47:32]#, DBI2# | DSTBN2# | D[63:48]#, DBI3# | DSTBN3# |  |
| Signals                            | Associated Strobes |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| D[15:0]#, DBI0#                    | DSTBN0#            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| D[31:16]#, DBI1#                   | DSTBN1#            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| D[47:32]#, DBI2#                   | DSTBN2#            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| D[63:48]#, DBI3#                   | DSTBN3#            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| DSTBP[3:0]#                        | I/O                | <div>Data strobe used to latch in D[63:0]#.</div> <table><thead><tr><th>Signals</th><th>Associated Strobes</th></tr></thead><tbody><tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#</td></tr></tbody></table>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Signals | Associated Strobes | D[15:0]#, DBI0# | DSTBP0# | D[31:16]#, DBI1# | DSTBP1# | D[47:32]#, DBI2# | DSTBP2# | D[63:48]#, DBI3# | DSTBP3# |  |
| Signals                            | Associated Strobes |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| D[15:0]#, DBI0#                    | DSTBP0#            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| D[31:16]#, DBI1#                   | DSTBP1#            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| D[47:32]#, DBI2#                   | DSTBP2#            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| D[63:48]#, DBI3#                   | DSTBP3#            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| FERR#/PBE#                         | O                  | FERR#/PBE# (floating-point error/pending break event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. For additional information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to Vol. 3 of the <i>IA_32 Intel® Architecture Software Developer's Manual</i> and the <i>AP-485 Intel® Processor Identification and the CPUID Instruction</i> application note. |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| FORCEPR#                           | I                  | The FORCEPR# (force power reduction) input can be used by the platform to cause the Intel® Xeon® Processor 7200 Series and 7300 Series to activate the Thermal Control Circuit (TCC).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| GTLREF_ADD_MID<br>GTLREF_ADD_END   | I                  | GTLREF_ADD determines the signal reference level for AGTL+ address and common clock input pins. GTLREF_ADD is used by the AGTL+ receivers to determine if a signal is a logical 0 or a logical 1. Please refer to <a href="#">Table 2-17</a> and the appropriate platform design guidelines for additional details.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| GTLREF_DATA_MID<br>GTLREF_DATA_END | I                  | GTLREF_DATA determines the signal reference level for AGTL+ data input pins. GTLREF_DATA is used by the AGTL+ receivers to determine if a signal is a logical 0 or a logical 1. Please refer to <a href="#">Table 2-17</a> and the appropriate platform design guidelines for additional details.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| HIT#<br>HITM#                      | I/O<br>I/O         | HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |         |                    |                 |         |                  |         |                  |         |                  |         |  |
| IERR#                              | O                  | IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#.<br><br>This signal does not have on-die termination.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |         |                    |                 |         |                  |         |                  |         |                  |         |  |



Table 5-1. Signal Definitions (Sheet 5 of 8)

| Name         | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Notes |
|--------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| IGNNE#       | I    | IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid along with the TRDY# assertion of the corresponding I/O write bus transaction.                                                                                                                                                                                               |       |
| INIT#        | I    | INIT# (Initialization), when asserted, resets integer registers inside all processors without affecting their internal caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor FSB agents.                                                                                                                                                                                                                                                                                                                                                                       |       |
| LINT[1:0]    | I    | LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all FSB agents. When the APIC functionality is disabled, the LINT0/INTR signal becomes INTR, a maskable interrupt request signal, and LINT1/NMI becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium® processor. Both signals are asynchronous. These signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.                                                                                                                                                                  |       |
| LL_ID[1:0]   | O    | The LL_ID[1:0] signals are used to select the correct loadline slope for the processor. These signals are not connected to the processor die. A logic 0 is pulled to ground and a logic 1 is a no-connect on the Intel® Xeon® Processor 7200 Series and 7300 Series package.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |       |
| LOCK#        | I/O  | LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor FSB agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor FSB, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor FSB throughout the bus locked operation and ensure the atomicity of lock.                                                                                                                                                                                                                                         |       |
| MCERR#       | I/O  | MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor FSB agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: <ul style="list-style-type: none"> <li>• Enabled or disabled.</li> <li>• Asserted, if configured, for internal errors along with IERR#.</li> <li>• Asserted, if configured, by the request initiator of a bus transaction after it observes an error.</li> <li>• Asserted by any bus agent when it observes an error in a bus transaction.</li> </ul> For more details regarding machine check architecture, refer to the <i>Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3: System Programming Guide</i> . |       |
| PECI         | I/O  | PECI is a proprietary one-wire bus interface that provides a communication channel between Intel processor and chipset components to external thermal monitoring devices. See <a href="#">Section 6.3, "Platform Environment Control Interface (PECI)"</a> for more on the Peci interface.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |       |
| PROC_ID[1:0] | O    | PROC_ID signals are used to identify which processor is installed. <ul style="list-style-type: none"> <li>00: Intel® Xeon® Processor 7400 Series</li> <li>01: Intel® Xeon® Processor 7200 Series and 7300 Series</li> <li>10: Reserved</li> <li>11: Reserved</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |       |
| PROCHOT#     | O    | PROCHOT# (Processor Hot) will go active when the processor's temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the Thermal Control Circuit (TCC) has been activated, if enabled. The TCC will remain active until shortly after the processor deasserts PROCHOT#. See <a href="#">Section 6.2.5</a> for more details.                                                                                                                                                                                                                                                                                                                                                                                                                     |       |



Table 5-1. Signal Definitions (Sheet 6 of 8)

| Name         | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Notes |
|--------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| PWRGOOD      | I    | <p>PWRGOOD (Power Good) is an input. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. <a href="#">Figure 2-24</a> illustrates the relationship of PWRGOOD to the RESET# signal. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in <a href="#">Table 2-16</a>, and be followed by a 1-10 ms RESET# pulse.</p> <p>The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.</p> |       |
| REQ[4:0]#    | I/O  | REQ[4:0]# (Request Command) must connect the appropriate pins of all processor FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[1:0]#. Refer to the AP[1:0]# signal description for details on parity checking of these signals.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |       |
| RESET#       | I    | <p>Asserting the RESET# signal resets all processors to known states and invalidates their internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least 1 ms after VCC and BCLK have reached their proper specifications. On observing active RESET#, all FSB agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted.</p> <p>A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the <a href="#">Section 7.1</a>.</p> <p>This signal does not have on-die termination and must be terminated on the system board.</p>                                                                                                                                                                                                                                                             |       |
| RS[2:0]#     | I    | RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor FSB agents.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |       |
| RSP#         | I    | <p>RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor FSB agents.</p> <p>A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |       |
| SKTOCC#      | O    | SKTOCC# (Socket occupied) will be pulled to ground by the processor to indicate that the processor is present. There is no connection to the processor silicon for this signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |       |
| SM_CLK       | I/O  | The SM_CLK (SMBus Clock) signal is an input clock to the system management logic which is required for operation of the system management features of the Intel® Xeon® Processor 7200 Series and 7300 Series. This clock is driven by the SMBus controller and is asynchronous to other clocks in the processor. The processor includes a 10 kΩ pull-up resistor to SM_VCC for this signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |       |
| SM_DAT       | I/O  | The SM_DAT (SMBus Data) signal is the data signal for the SMBus. This signal provides the single-bit mechanism for transferring data between SMBus devices. The processor includes a 10 kΩ pull-up resistor to SM_VCC for this signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |       |
| SM_EP_A[2:0] | I    | The SM_EP_A (EEPROM Select Address) pins are decoded on the SMBus in conjunction with the upper address bits in order to maintain unique addresses on the SMBus in a system with multiple processors. To set an SM_EP_A line high, a pull-up resistor should be used that is no larger than 1 kΩ. The processor includes a 10 kΩ pull-down resistor to V <sub>SS</sub> for each of these signals.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |       |
| SM_VCC       | I    | SM_VCC provides power to the SMBus components on the Intel® Xeon® Processor 7200 Series and 7300 Series package.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |       |
| SM_WP        | I    | WP (Write Protect) can be used to write protect the Scratch EEPROM. The Scratch EEPROM is write-protected when this input is pulled high to SM_VCC. The processor includes a 10 kΩ pull-down resistor to V <sub>SS</sub> for this signal.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |       |



Table 5-1. Signal Definitions (Sheet 7 of 8)

| Name                    | Type   | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Notes |
|-------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| SMI#                    | I      | SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler.<br>If SMI# is asserted during the deassertion of RESET# the processor will tri-state its outputs. See <a href="#">Section 7.1</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |       |
| STPCLK#                 | I      | STPCLK# (Stop Clock), when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the FSB and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |       |
| TCK                     | I      | TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |       |
| TDI                     | I      | TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |       |
| TDO                     | O      | TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |       |
| TESTHI[1:0]             | I      | TESTHI[1:0] must be connected to a $V_{TT}$ power source through a resistor for proper processor operation. Refer to <a href="#">Section 2.5</a> for TESTHI grouping restrictions.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |       |
| TESTIN1<br>TESTIN2      | I<br>I | TESTIN1 must be connected to a VTT power source through a resistor as well as to the TESTIN2 pin of the same socket for proper processor operation.<br>TESTIN2 must be connected to a VTT power source through a resistor as well as to the TESTIN1 pin of the same socket for proper processor operation.<br>Refer to <a href="#">Section 2.5</a> for TESTIN restrictions.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |       |
| THERMTRIP#              | O      | Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a temperature beyond which permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage ( $V_{CC}$ ) must be removed following the assertion of THERMTRIP#. See <a href="#">Figure 2-21</a> and <a href="#">Table 2-22</a> for the appropriate power down sequence and timing requirements. Intel also recommends the removal of $V_{TT}$ when THERMTRIP# is asserted.<br>Driving of the THERMTRIP# signals is enabled within 10 $\mu$ s of the assertion of PWRGOOD and is disabled on de-assertion of PWRGOOD. Once activated, THERMTRIP# remains latched until PWRGOOD is de-asserted. While the de-assertion of the PWRGOOD signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted within 10 $\mu$ s of the assertion of PWRGOOD. |       |
| TMS                     | I      | TMS (Test Mode Select) is a JTAG specification support signal used by debug tools. See the <i>XDP: Debug Port Design Guide for Intel® 7300 Chipset Platforms</i> for further information.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |       |
| TRDY#                   | I      | TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all FSB agents.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |       |
| TRST#                   | I      | TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |       |
| $V_{CCPLL}$             | I      | The Intel® Xeon® Processor 7200 Series and 7300 Series implement an on-die PLL filter solution. The $V_{CCPLL}$ input is used as a PLL supply voltage.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |       |
| VCC_SENSE<br>VCC_SENSE2 | O      | VCC_SENSE and VCC_SENSE2 provides an isolated, low impedance connection to the processor core power and ground. These signals should be used to provide feedback to the voltage regulator signals, which ensure the output voltage (that is, processor voltage) remains within specification. Please see the applicable platform design guide for implementation details.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |       |



Table 5-1. Signal Definitions (Sheet 8 of 8)

| Name                    | Type | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Notes |
|-------------------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| VID[6:1]                | O    | VID[6:1] (Voltage ID) pins are used to support automatic selection of power supply voltages ( $V_{CC}$ ). These are CMOS signals that are driven by the processor and must be pulled up through a resistor. Conversely, the voltage regulator output must be disabled prior to the voltage supply for these pins becomes invalid. The VID pins are needed to support processor voltage specification variations. See <a href="#">Table 2-3</a> for definitions of these pins. The VR must supply the voltage that is requested by these pins, or disable itself. |       |
| VSS_SENSE<br>VSS_SENSE2 | O    | VSS_SENSE and VSS_SENSE2 provides an isolated, low impedance connection to the processor core power and ground. These signals should be used to provide feedback to the voltage regulator signals, which ensure the output voltage (that is, processor voltage) remains within specification. Please see the applicable platform design guide for implementation details.                                                                                                                                                                                        |       |
| VTT                     | P    | The FSB termination voltage input pins. Refer to <a href="#">Table 2-9</a> for further details.                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |       |
| VTT_SEL                 | O    | The VTT_SEL signal is used to select the correct $V_{TT}$ voltage level for the processor. VTT_SEL is a no-connect on the Intel® Xeon® Processor 7200 Series and 7300 Series package.                                                                                                                                                                                                                                                                                                                                                                            |       |

§



## 6 Thermal Specifications

---

### 6.1 Package Thermal Specifications

The Intel® Xeon® Processor 7200 Series and 7300 Series requires a thermal solution to maintain temperatures within its operating limits. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor integrated heat spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

This section provides data necessary for developing a complete thermal solution. For more information on designing a component level thermal solution, refer to the *Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series Thermal / Mechanical Design Guide*.

#### 6.1.1 Thermal Specifications

To allow the optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum case temperature (TCASE) specifications as defined by the applicable thermal profile (see [Table 6-1](#) and [Figure 6-1](#) for Quad-Core Intel® Xeon® Processor E7300 Series, [Table 6-3](#) and [Figure 6-2](#) for Quad-Core Intel® Xeon® X7350 Processor, [Table 6-5](#) and [Figure 6-3](#) for Quad-Core Intel® Xeon® L7345 Processor, [Table 6-7](#) and [Figure 6-4](#) for Dual-Core Intel® Xeon® Processor 7200 Series). Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, please refer to the *Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series Thermal / Mechanical Design Guide*.

The Intel® Xeon® Processor 7200 Series and 7300 Series implement a methodology for managing processor temperatures which is intended to support acoustic noise reduction through fan speed control and to assure processor reliability. Selection of the appropriate fan speed is based on the relative temperature data reported by the processor's Platform Environment Control Interface (PECI) bus as described in [Section 6.3](#). The temperature reported over PECI is always a negative value and represents a delta below the onset of thermal control circuit (TCC) activation, as indicated by PROCHOT# (see [Section 6.2](#), Processor Thermal Features). Systems that implement fan speed control should be designed to use this data. Systems that do not alter the fan speed also need to guarantee the case temperature meets the thermal profile specifications.

The Quad-Core Intel® Xeon® Processor E7300 Series (see [Figure 6-1](#); [Table 6-2](#)), Quad-Core Intel® Xeon® L7345 Processor (see [Figure 6-3](#); [Table 6-6](#)) and Dual-Core Intel® Xeon® Processor 7200 Series (see [Figure 6-4](#); [Table 6-8](#)) supports a single Thermal Profile. The Thermal Profile is indicative of a constrained thermal environment (Ex: 1U form factor). Because of the reduced cooling capability represented by this solution, the probability of TCC activation and performance loss is increased.



Additionally, utilization of a thermal solution that does not meet the Thermal Profile will violate the thermal specifications and may result in permanent damage to the processor. Refer to the *Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series Thermal / Mechanical Design Guide* for details on system thermal solution design, thermal profiles and environmental considerations.

For the Quad-Core Intel® Xeon® X7350 Processor, Intel has developed a thermal profile which must be met to ensure adherence to Intel reliability requirements. The Thermal Profile (see [Figure 6-2](#); [Table 6-4](#)) is representative of a volumetrically unconstrained thermal solution (that is, industry enabled 2U heatsink). In this scenario, it is expected that the Thermal Control Circuit (TCC) would only be activated for very brief periods of time when running the most power intensive applications. Intel has developed the thermal profile to allow customers to choose the thermal solution and environmental parameters that best suit their platform implementation. Refer to the *Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series Thermal / Mechanical Design Guide* for details on system thermal solution design, thermal profiles and environmental considerations.

The upper point of the thermal profile consists of the Thermal Design Power (TDP) and the associated  $T_{CASE}$  value. It should be noted that the upper point associated with Quad-Core Intel® Xeon® X7350 Processor Thermal Profile ( $x = TDP$  and  $y = T_{CASE\_MAX}$  P @ TDP) represents a thermal solution design point. In actuality the processor case temperature will not reach this value due to TCC activation (see [Figure 6-2](#) for Quad-Core Intel® Xeon® X7350 Processor).

Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the Thermal Design Power (TDP) instead of the maximum processor power consumption. The Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. For more details on this feature, refer to [Section 6.2](#). To ensure maximum flexibility for future requirements, systems should be designed to the Flexible Motherboard (FMB) guidelines, even if a processor with lower power dissipation is currently planned. **Thermal Monitor and Thermal Monitor 2 feature must be enabled for the processor to remain within its specifications.**

**Table 6-1. Quad-Core Intel® Xeon® E7300 Processor Thermal Specifications**

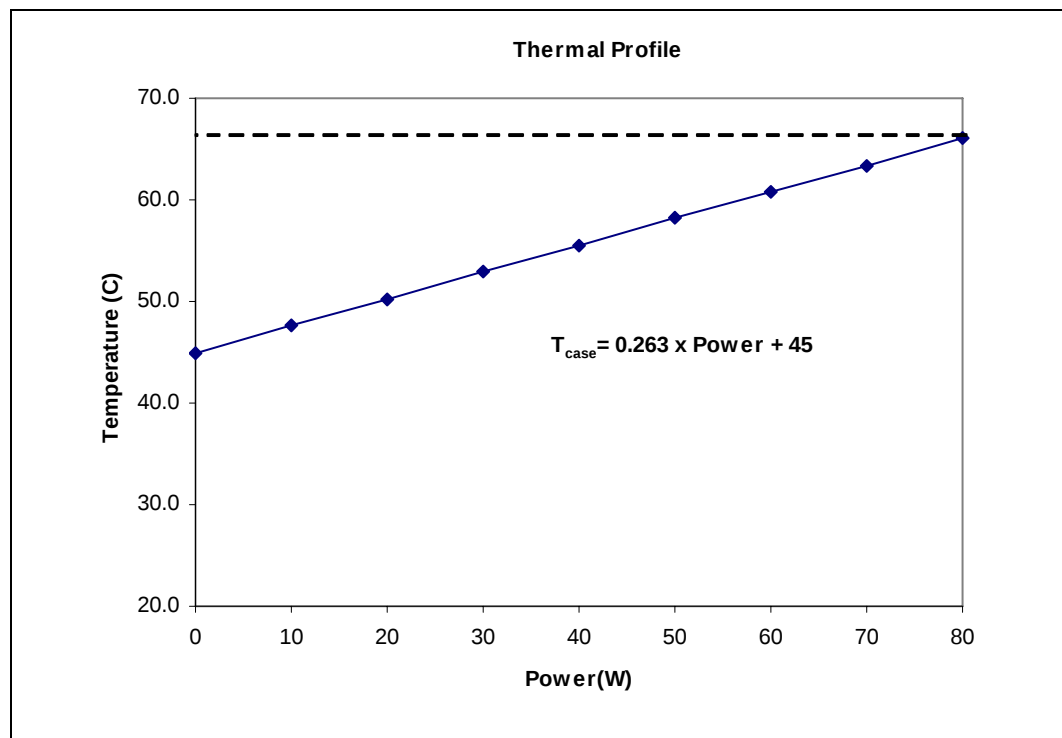
| Core Frequency | Thermal Design Power (W) | Minimum $T_{CASE}$ (°C) | Maximum $T_{CASE}$ (°C)                                      | Notes            |
|----------------|--------------------------|-------------------------|--------------------------------------------------------------|------------------|
| Launch to FMB  | 80                       | 5                       | See <a href="#">Figure 6-1</a> ; <a href="#">Table 6-2</a> ; | 1, 2, 3, 4, 5, 6 |

**Notes:**

1. These values are specified at  $V_{CC\_MAX}$  for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static  $V_{CC}$  and  $I_{CC}$  combination wherein  $V_{CC}$  exceeds  $V_{CC\_MAX}$  at specified  $I_{CC}$ . Please refer to the loadline specifications in [Section 2](#).
2. Maximum Power is the highest power the processor will dissipate, regardless of its VID. Maximum Power is measured at maximum  $T_{CASE}$ .
3. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum  $T_{CASE}$ .
4. These specifications are based on pre-silicon estimates and simulations. These specifications will be updated with characterized data from silicon measurements in a future release of this document.
5. Power specifications are defined at all VID's found in [Table 2-3](#). The Quad-Core Intel® Xeon® E7300 Processor may be shipped under multiple VID's for each frequency.
6. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.



Figure 6-1. Quad-Core Intel® Xeon® E7300 Processor Thermal Profile

**Notes:**

1. Please refer to [Table 6-2](#) for discrete points that constitute the thermal profile.
2. Implementation of Thermal Profile should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet processor Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss. (See [Section 6.2](#) for details on TCC activation).
3. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum  $T_{\text{CASE}}$ .
4. These specifications are based pre-silicon estimates and simulations. These specifications will be updated with characterized data from silicon measurements in a future release of this document.
5. Power specifications are defined at all VIDs found in [Table 2-3](#). The Quad-Core Intel® Xeon® E7300 Processor may be shipped under multiple VIDs for each frequency.
6. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Table 6-2. Quad-Core Intel® Xeon® E7300 Processor Thermal Profile Table

| Power (W) | $T_{\text{CASE\_MAX}}$ (°C) |
|-----------|-----------------------------|
| 0         | 45.0                        |
| 10        | 47.6                        |
| 20        | 50.3                        |
| 30        | 52.9                        |
| 40        | 55.5                        |
| 50        | 58.2                        |
| 60        | 60.8                        |
| 70        | 63.4                        |
| 80        | 66.0                        |



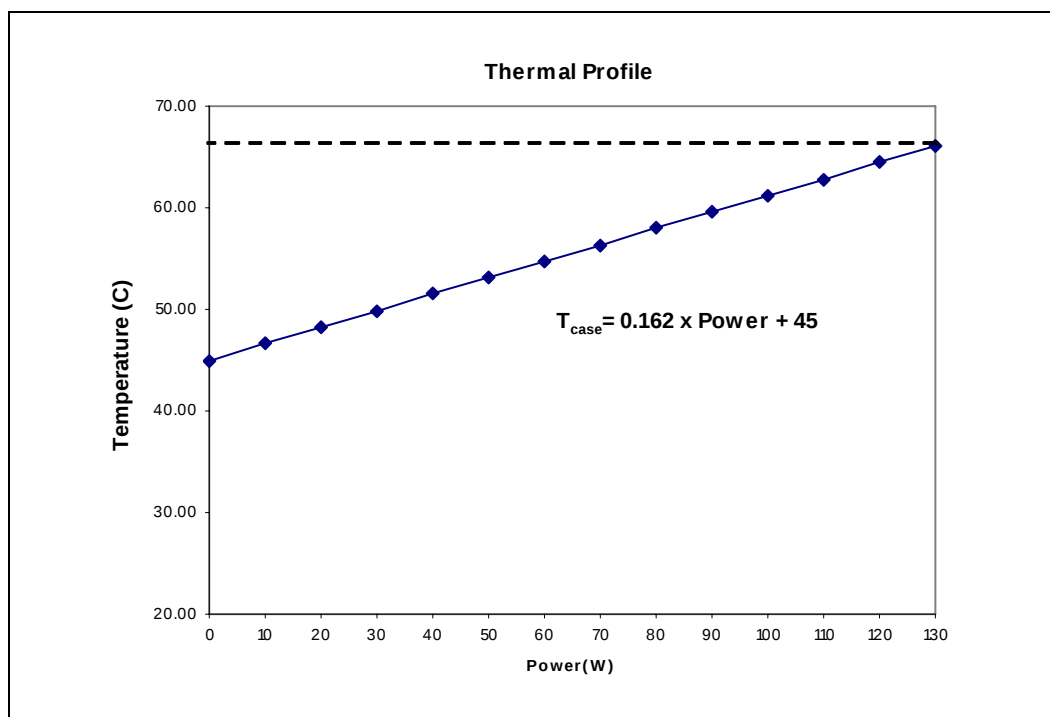
**Table 6-3. Quad-Core Intel® Xeon® X7350 Processor Thermal Specifications**

| Core Frequency | Thermal Design Power (W) | Minimum TCASE (°C) | Maximum TCASE (°C)         | Notes            |
|----------------|--------------------------|--------------------|----------------------------|------------------|
| Launch to FMB  | 130                      | 5                  | See Figure 6-2; Table 6-4; | 1, 2, 3, 4, 5, 6 |

**Notes:**

1. These values are specified at  $V_{CC\_MAX}$  for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static  $V_{CC}$  and  $I_{CC}$  combination wherein  $V_{CC}$  exceeds  $V_{CC\_MAX}$  at specified  $I_{CC}$ . Please refer to the loadline specifications in [Section 2](#).
2. Maximum Power is the highest power the processor will dissipate, regardless of its VID. Maximum Power is measured at maximum  $T_{CASE}$ .
3. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum  $T_{CASE}$ .
4. These specifications are based pre-silicon estimates and simulations. These specifications will be updated with characterized data from silicon measurements in a future release of this document.
5. Power specifications are defined at all VIDs found in [Table 2-3](#). The Intel® Xeon® X7350 Processor may be shipped under multiple VIDs for each frequency.
6. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

**Figure 6-2. Quad-Core Intel® Xeon® X7350 Processor Thermal Profile**



**Notes:**

1. Thermal Profile is representative of a volumetrically unconstrained platform. Please refer to [Table 6-4](#) for discrete points that constitute the thermal profile.
2. Implementation of Thermal Profile should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet processor Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss. (See [Section 6.2](#) for details on TCC activation).
3. Refer to the *Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series Thermal / Mechanical Design Guide* for system and environmental implementation details.

**Table 6-4. Quad-Core Intel® Xeon® X7350 Processor Thermal Profile Table**

| Power (W) | T <sub>CASE_MAX</sub> (°C) |
|-----------|----------------------------|
| 0         | 45.0                       |
| 10        | 46.6                       |
| 20        | 48.2                       |
| 30        | 49.9                       |
| 40        | 51.5                       |
| 50        | 53.1                       |
| 60        | 54.7                       |
| 70        | 56.3                       |
| 80        | 58.0                       |
| 90        | 59.6                       |
| 100       | 61.2                       |
| 110       | 62.8                       |
| 120       | 64.4                       |
| 130       | 66.0                       |

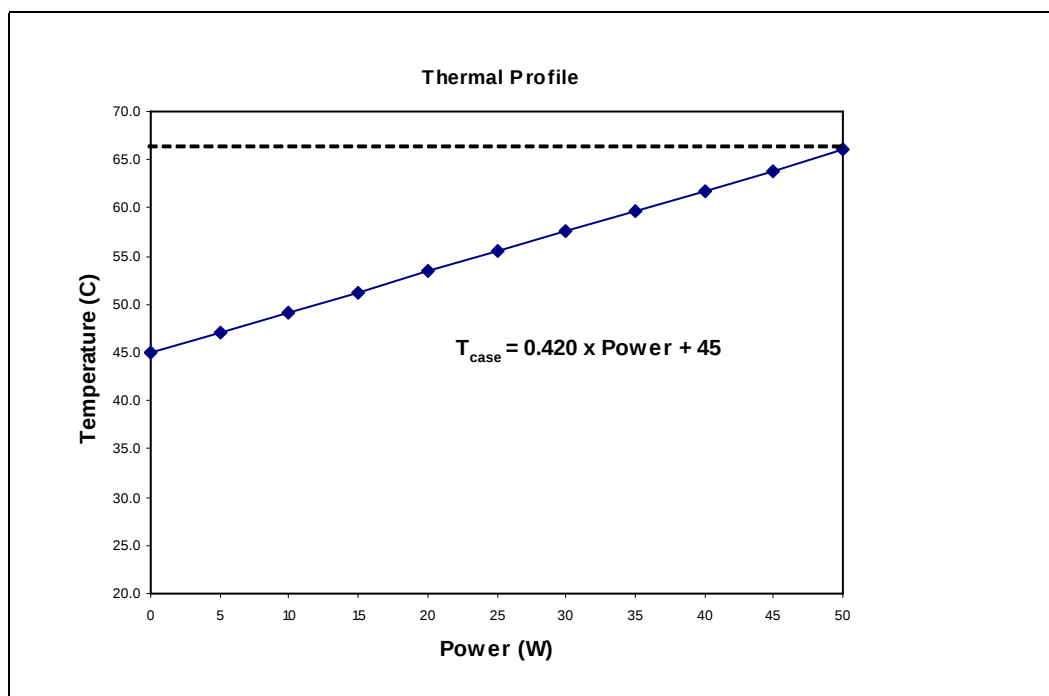
**Table 6-5. Quad-Core Intel® Xeon® L7345 Processor Thermal Specifications**

| Core Frequency | Thermal Design Power (W) | Minimum T <sub>CASE</sub> (°C) | Maximum T <sub>CASE</sub> (°C) | Notes            |
|----------------|--------------------------|--------------------------------|--------------------------------|------------------|
| Launch to FMB  | 50                       | 5                              | See Figure 6-3; Table 6-6      | 1, 2, 3, 4, 5, 6 |

**Notes:**

1. These values are specified at V<sub>CC\_MAX</sub> for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static V<sub>CC</sub> and I<sub>CC</sub> combination wherein V<sub>CC</sub> exceeds V<sub>CC\_MAX</sub> at specified I<sub>CC</sub>. Please refer to the loadline specifications in [Section 2](#).
2. Maximum Power is the highest power the processor will dissipate, regardless of its VID. Maximum Power is measured at maximum T<sub>CASE</sub>.
3. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T<sub>CASE</sub>.
4. These specifications are based on initial silicon characterization. These specifications may be further updated as more characterization data becomes available.
5. Power specifications are defined at all VIDs found in [Table 2-3](#). The Quad-Core Intel® Xeon® L7345 Processor may be shipped under multiple VIDs for each frequency.
6. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

Figure 6-3. Quad-Core Intel® Xeon® L7345 Processor Thermal Profile



**Notes:**

1. Please refer to [Table 6-6](#) for discrete points that constitute the thermal profile.
2. Refer to the *Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series Thermal / Mechanical Design Guide* for system and environmental implementation details.

Table 6-6. Quad-Core Intel® Xeon® L7345 Processor Thermal Profile

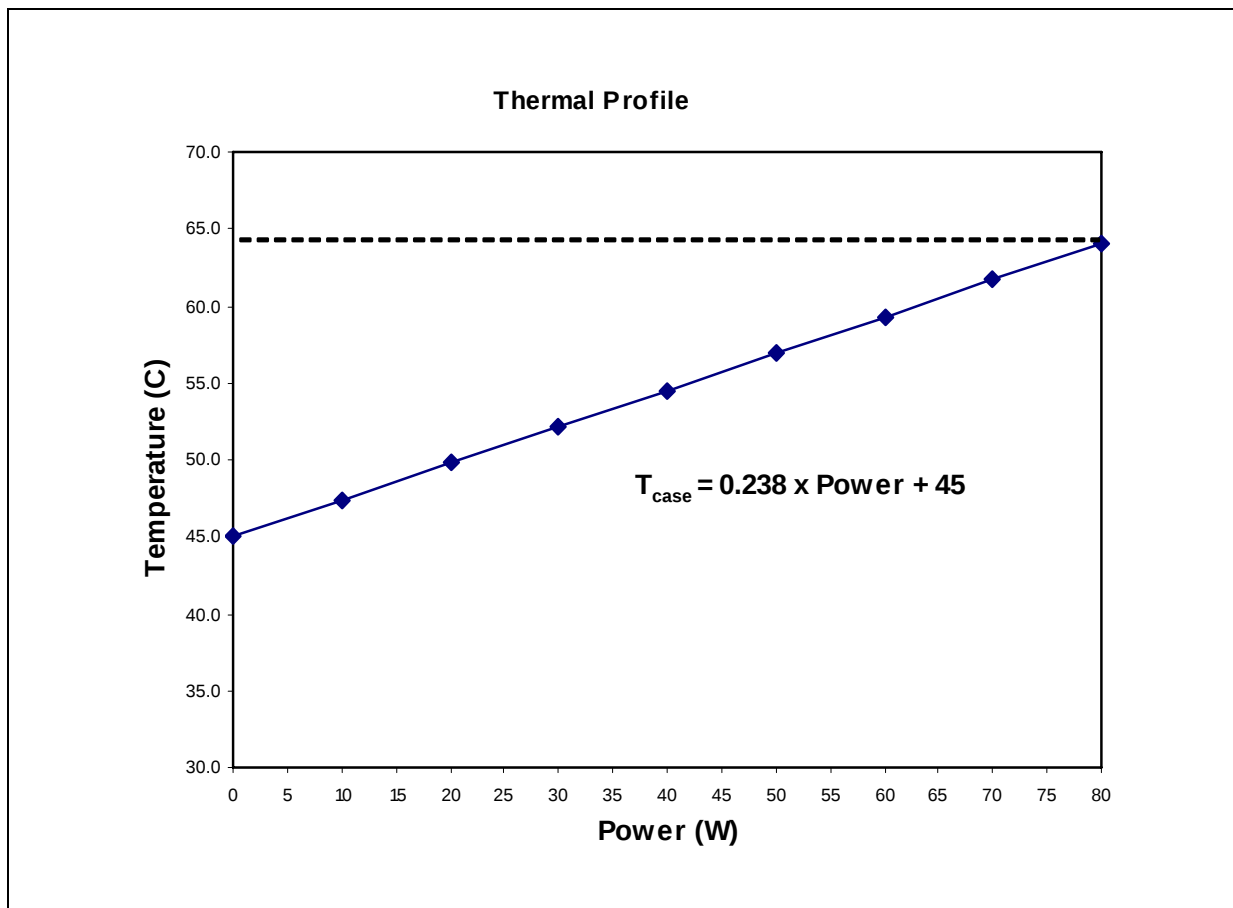
| Power (W) | T <sub>CASE_MAX</sub> (°C) |
|-----------|----------------------------|
| 0         | 45.0                       |
| 5         | 47.1                       |
| 10        | 49.2                       |
| 15        | 51.3                       |
| 20        | 53.4                       |
| 25        | 55.5                       |
| 30        | 57.6                       |
| 35        | 59.7                       |
| 40        | 61.8                       |
| 45        | 63.9                       |
| 50        | 66.0                       |

**Table 6-7. Dual-Core Intel® Xeon® Processor 7200 Series Thermal Specifications**

| Core Frequency | Thermal Design Power (W) | Minimum TCASE (°C) | Maximum TCASE (°C)         | Notes            |
|----------------|--------------------------|--------------------|----------------------------|------------------|
| Launch to FMB  | 80                       | 5                  | See Figure 6-4; Table 6-8; | 1, 2, 3, 4, 5, 6 |

**Notes:**

1. These values are specified at  $V_{CC\_MAX}$  for all processor frequencies. Systems must be designed to ensure the processor is not to be subjected to any static  $V_{CC}$  and  $I_{CC}$  combination wherein  $V_{CC}$  exceeds  $V_{CC\_MAX}$  at specified  $I_{CC}$ . Please refer to the loadline specifications in [Section 2](#).
2. Maximum Power is the highest power the processor will dissipate, regardless of its VID. Maximum Power is measured at maximum  $T_{CASE}$ .
3. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum  $T_{CASE}$ .
4. These specifications are based pre-silicon estimates and simulations. These specifications will be updated with characterized data from silicon measurements in a future release of this document.
5. Power specifications are defined at all VIDs found in [Table 2-3](#). The Dual-Core Intel® Xeon® Processor 7200 Series may be shipped under multiple VIDs for each frequency.
6. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

**Figure 6-4. Dual-Core Intel® Xeon® Processor 7200 Series Thermal Profile****Notes:**

1. Please refer to [Table 6-8](#) for discrete points that constitute the thermal profile.
2. Implementation of Thermal Profile should result in virtually no TCC activation. Furthermore, utilization of thermal solutions that do not meet processor Thermal Profile will result in increased probability of TCC activation and may incur measurable performance loss. (See [Section 6.2](#) for details on TCC activation).



3. Thermal Design Power (TDP) should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum  $T_{CASE}$ .
4. These specifications are based pre-silicon estimates and simulations. These specifications will be updated with characterized data from silicon measurements in a future release of this document.
5. Power specifications are defined at all VIDs found in [Table 2-3](#). The Dual-Core Intel® Xeon® Processor 7200 Series may be shipped under multiple VIDs for each frequency.
6. FMB, or Flexible Motherboard, guidelines provide a design target for meeting all planned processor frequency requirements.

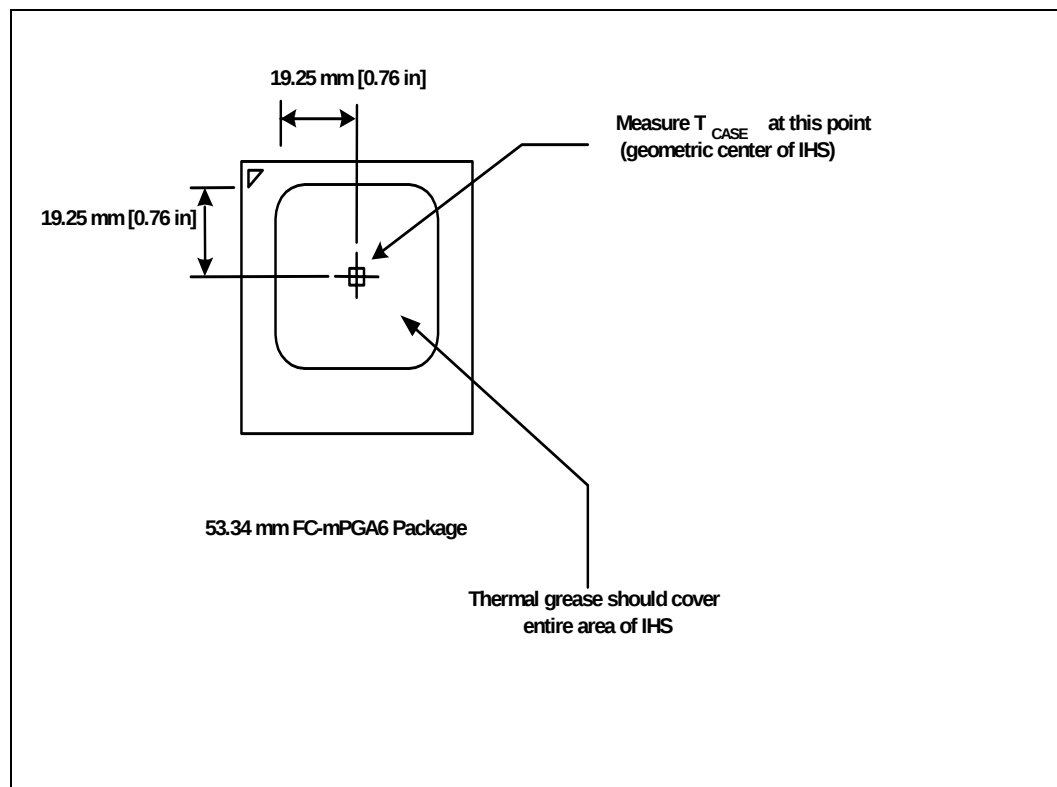
**Table 6-8. Dual-Core Intel® Xeon® Processor 7200 Series Thermal Profile**

| Power (W) | $T_{CASE\_MAX}$ (°C) |
|-----------|----------------------|
| 0         | 45.0                 |
| 10        | 47.4                 |
| 20        | 49.8                 |
| 30        | 52.1                 |
| 40        | 54.5                 |
| 50        | 56.9                 |
| 60        | 59.3                 |
| 70        | 61.7                 |
| 80        | 64.0                 |

### 6.1.2 Thermal Metrology

The minimum and maximum case temperatures ( $T_{CASE}$ ) are specified in [Table 6-2](#), through [Table 6-8](#), and are measured at the geometric top center of the processor integrated heat spreader (IHS). [Figure 6-5](#) illustrates the location where  $T_{CASE}$  temperature measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the *Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series Thermal / Mechanical Design Guide*.

**Figure 6-5. Case Temperature ( $T_{CASE}$ ) Measurement Location**



**Note:** Figure is not to scale and is for reference only.

## 6.2 Processor Thermal Features

### 6.2.1 Thermal Monitor Features

The Intel® Xeon® Processor 7200 Series and 7300 Series provide two thermal monitor features, Thermal Monitor (TM1) and Enhanced Thermal Monitor (TM2). The TM1 and TM2 must both be enabled in BIOS for the processor to be operating within specifications. When both are enabled, TM2 will be activated first and TM1 will be added if TM2 is not effective.

### 6.2.2 Thermal Monitor

The Thermal Monitor (TM1) feature helps control the processor temperature by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption as needed by modulating (starting and stopping) the internal processor core clocks. The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the TM1 is enabled, and a high temperature situation exists (that is, TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30 - 50%). Cycle times are processor

speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With thermal solutions designed to each of the Intel® Xeon® Processor 7200 Series and 7300 Series Thermal Profile it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. A thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously. Refer to the *Dual-Core Intel® Xeon® Processor 7200 Series and Quad-Core Intel® Xeon® Processor 7300 Series Thermal / Mechanical Design Guide* for information on designing a thermal solution.

The duty cycle for the TCC, when activated by the TM1, is factory configured and cannot be modified. The TM1 does not require any additional hardware, software drivers, or interrupt handling routines.

### 6.2.3 Thermal Monitor 2

The Intel® Xeon® Processor 7200 Series and 7300 Series adds supports for an Enhanced Thermal Monitor capability known as Thermal Monitor 2 (TM2). This mechanism provides an efficient means for limiting the processor temperature by reducing the power consumption within the processor. The Thermal Monitor or Enhanced Thermal Monitor must be enabled for the processor to be operating within specifications. TM2 requires support for dynamic VID transitions in the platform.

**Note:** Not all Intel® Xeon® Processor 7200 Series and 7300 Series are capable of supporting TM2.

When Thermal Monitor 2 is enabled, and a high temperature situation is detected, the Thermal Control Circuit (TCC) will be activated for all processor cores. The TCC causes the processor to adjust its operating frequency (via the bus multiplier) and input voltage (via the VID signals). This combination of reduced frequency and VID results in a reduction to the processor power consumption.

A processor enabled for Thermal Monitor 2 includes two operating points, each consisting of a specific operating frequency and voltage, which is identical for both processor dies. The first operating point represents the normal operating condition for the processor. Under this condition, the core-frequency-to-system-bus multiplier utilized by the processor is that contained in the CLOCK\_FLEX\_MAX MSR and the VID that is specified in [Table 2-3](#).

The second operating point consists of both a lower operating frequency and voltage. The lowest operating frequency is determined by the lowest supported bus ratio (1/6 for the Intel® Xeon® Processor 7200 Series and 7300 Series). When the TCC is activated, the processor automatically transitions to the new frequency. This transition occurs rapidly, on the order of 5  $\mu$ s. During the frequency transition, the processor is unable to service any bus requests, and consequently, all bus traffic is blocked. Edge-triggered interrupts will be latched and kept pending until the processor resumes operation at the new frequency.

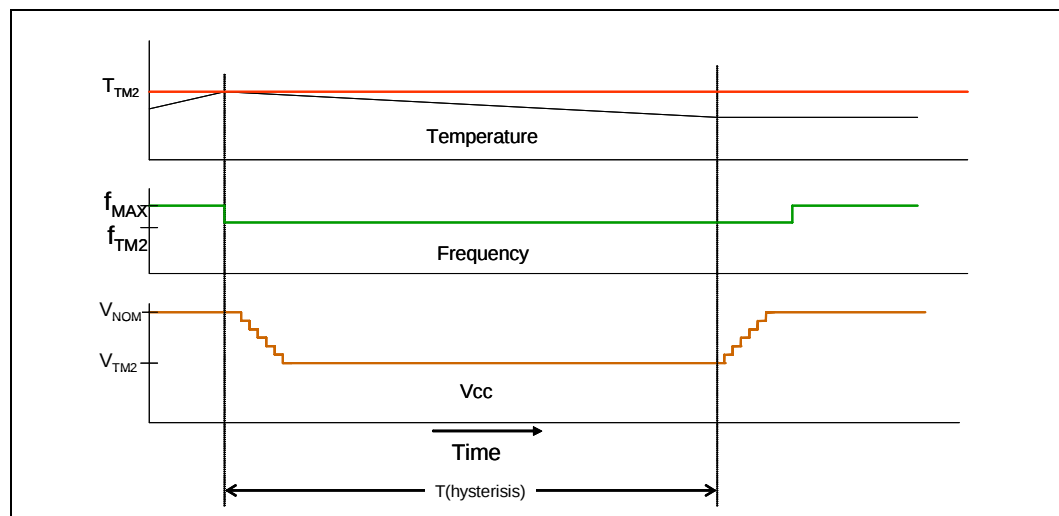
Once the new operating frequency is engaged, the processor will transition to the new core operating voltage by issuing a new VID code to the voltage regulator. The voltage regulator must support dynamic VID steps in order to support Thermal Monitor 2. During the voltage change, it will be necessary to transition through multiple VID codes



to reach the target operating voltage. Each step will be one VID table entry (see [Table 2-3](#)). The processor continues to execute instructions during the voltage transition. Operation at the lower voltage reduces the power consumption of the processor.

A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the operating frequency and voltage transition back to the normal system operating point. Transition of the VID code will occur first, in order to ensure proper operation once the processor reaches its normal operating frequency. Refer to [Figure 6-6](#) for an illustration of this ordering.

**Figure 6-6. Thermal Monitor 2 Frequency and Voltage Ordering**



The PROCHOT# signal is asserted when a high temperature situation is detected, regardless of whether Thermal Monitor or Thermal Monitor 2 is enabled.

#### 6.2.4 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as “On-Demand” mode and is distinct from the Thermal Monitor and Thermal Monitor 2 features. On-Demand mode is intended as a means to reduce system level power consumption. Systems utilizing the Intel® Xeon® Processor 7200 Series and 7300 Series must not rely on software usage of this mechanism to limit the processor temperature. If bit 4 of the IA32\_CLOCK\_MODULATION MSR is set to a ‘1’, the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same IA32\_CLOCK\_MODULATION MSR. In On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used in conjunction with the Thermal Monitor; however, if the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

### 6.2.5 PROCHOT# Signal

An external signal, PROCHOT# (processor hot) is asserted when the temperature of either processor die has reached its factory configured trip point. If Thermal Monitor is enabled (note that Thermal Monitor must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manual*.

PROCHOT# is designed to assert at or a few degrees higher than maximum  $T_{CASE}$  (as specified by Thermal Profile) when dissipating TDP power, and cannot be interpreted as an indication of processor case temperature. This temperature delta accounts for processor package, lifetime and manufacturing variations and attempts to ensure the Thermal Control Circuit is not activated below maximum  $T_{CASE}$  when dissipating TDP power. There is no defined or fixed correlation between the PROCHOT# trip temperature, or the case temperature. Thermal solutions must be designed to the processor specifications and cannot be adjusted based on experimental measurements of  $T_{CASE}$ , or PROCHOT#.

### 6.2.6 FORCEPR# Signal

The FORCEPR# (force power reduction) input can be used by the platform to cause the Intel® Xeon® Processor 7200 Series and 7300 Series to activate the TCC. If the Thermal Monitor is enabled, the TCC will be activated upon the assertion of the FORCEPR# signal. Assertion of the FORCEPR# signal will activate TCC for all processor cores. The TCC will remain active until the system deasserts FORCEPR#. FORCEPR# is an asynchronous input. FORCEPR# can be used to thermally protect other system components. To use the VR as an example, when FORCEPR# is asserted, the TCC circuit in the processor will activate, reducing the current consumption of the processor and the corresponding temperature of the VR.

It should be noted that assertion of FORCEPR# does not automatically assert PROCHOT#. As mentioned previously, the PROCHOT# signal is asserted when a high temperature situation is detected. A minimum pulse width of 500  $\mu$ s is recommended when FORCEPR# is asserted by the system. Sustained activation of the FORCEPR# signal may cause noticeable platform performance degradation.

### 6.2.7 THERMTRIP# Signal

Regardless of whether or not Thermal Monitor or Thermal Monitor 2 is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when either die has reached an elevated temperature (refer to the THERMTRIP# definition in [Table 5-1](#)). At this point, the FSB signal THERMTRIP# will go active and stay active as described in [Table 5-1](#). THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. If THERMTRIP# is asserted, processor core voltage ( $V_{CC}$ ) must be removed within the time frame defined in [Table 2-22](#) and [Figure 2-21](#). Intel also recommends the removal of  $V_{TT}$ .

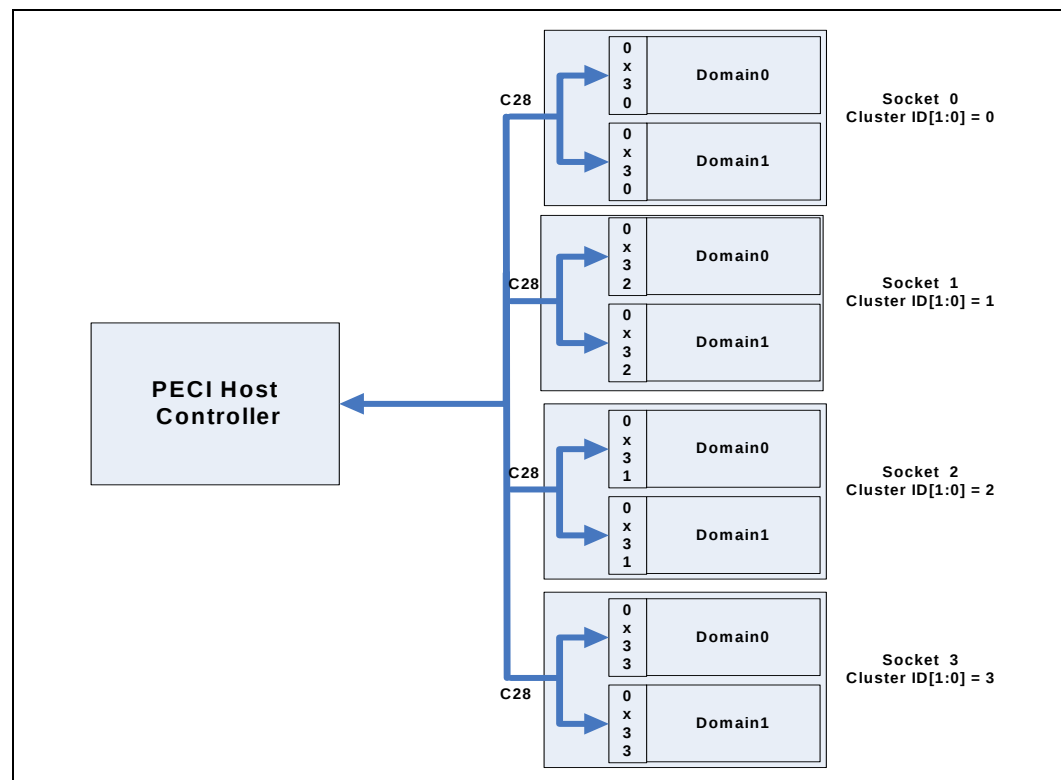


## 6.3 Platform Environment Control Interface (PECI)

### 6.3.1 Introduction

PECI offers an interface for thermal monitoring of Intel processor and chipset components. It uses a single wire, thus alleviating routing congestion issues. [Figure 6-7](#) shows an example of the PECI topology in a system with Intel® Xeon® Processor 7200 Series and 7300 Series. PECI uses CRC checking on the host side to ensure reliable transfers between the host and client devices. Also, data transfer speeds across the PECI interface are negotiable within a wide range (2 Kbps to 2 Mbps). The PECI interface on Intel® Xeon® Processor 7200 Series and 7300 Series is disabled by default and must be enabled through BIOS.

**Figure 6-7. PECI Topology**

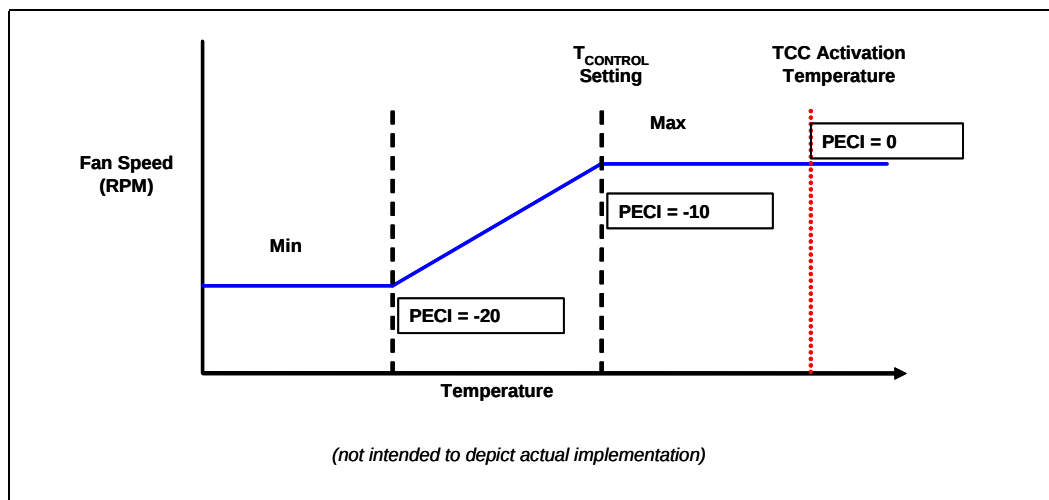


**Note:** The power-on configuration (POC) settings of third party chipsets may produce different PECI addresses than those shown in [Figure 6-7](#). Thermal designers should consult their third party chipset designers for the correct PECI addresses.

#### 6.3.1.1 $T_{\text{CONTROL}}$ and Tcc Activation on PECI-Based Systems

Fan speed control solutions based on PECI utilize a  $T_{\text{CONTROL}}$  value stored in the processor IA32\_TEMPERATURE\_TARGET MSR. This MSR uses the same offset temperature format as PECI, though it contains no sign bit. Thermal management devices should infer the  $T_{\text{CONTROL}}$  value as negative. Thermal management algorithms should utilize the relative temperature value delivered over PECI in conjunction with the MSR value to control or optimize fan speeds. [Figure 6-8](#) shows a conceptual fan control diagram using PECI temperatures.

Figure 6-8. Conceptual Fan Control Diagram For a PECI-Based Platform



### 6.3.1.2 Processor Thermal Data Sample Rate and Filtering

The DTS (Digital Thermal Sensors) provide an improved capability to monitor device hot spots, which inherently leads to more varying temperature readings over short time intervals. The DTS sample interval range can be modified, and a data filtering algorithm can be activated to help moderate this. The DTS sample interval range is 82  $\mu$ s (default) to 20 ms (max). This value can be set in BIOS.

To reduce the sample rate requirements on PECI and improve thermal data stability vs. time the processor DTS also implements an averaging algorithm that filters the incoming data. This is an alpha-beta filter with coefficients of 0.5, and is expressed mathematically as:  $\text{Current\_filtered\_temp} = (\text{Previous\_filtered\_temp} / 2) + (\text{new\_sensor\_temp} / 2)$ . This filtering algorithm is fixed and cannot be changed. It is on by default and can be turned off in BIOS.

Host controllers should utilize the min/max sample times to determine the appropriate sample rate based on the controller's fan control algorithm and targeted response rate. The key items to take into account when settling on a fan control algorithm are the DTS sample rate, whether the temperature filter is enabled, how often the PECI host will poll the processor for temperature data, and the rate at which fan speed is changed. Depending on the designer's specific requirements the DTS sample rate and alpha-beta filter may have no effect on the fan control algorithm.

## 6.3.2 PECI Specifications

### 6.3.2.1 PECI Device Address

The Intel® Xeon® Processor 7200 Series and 7300 Series obtains its PECI address based on the processor APIC ID[4:2] at power on. APIC ID[4:3] is also known as Cluster ID[1:0] and APIC ID[2] is also known as Agent ID[1]. Cluster ID[1:0] is set by the chipset driven power-on configuration (POC) signals A[12:11]#. Table 6-9 shows how the Agent ID is generated for each of the die based on the BREQ# signals asserted during power on for the Intel® Xeon® Processor 7200 Series and 7300 Series.

**Table 6-9. BREQ# signal assertion during power on**

| BREQ0#       | BREQ1#       | AgentID[1:0] Die 0                                 | AgentID[1:0] Die 1 |
|--------------|--------------|----------------------------------------------------|--------------------|
| Asserted     | Not asserted | 00                                                 | 01                 |
| Asserted     | Asserted     | 10                                                 | 11                 |
| Not asserted | Asserted     | This combination is not supported by the processor |                    |
| Not asserted | Not asserted |                                                    |                    |

Table 6-10 shows how the PECl address is assigned to each of the processors based on the ClusterID[1:0] and AgentID[1] setting at power on.

**Table 6-10. PECl Address assigned to processor**

| Cluster ID[1] / APIC ID[4] | ClusterID[0] / APIC ID[3] | AgentID[1] / APIC ID[2] | PECl Address |
|----------------------------|---------------------------|-------------------------|--------------|
| 0                          | 0                         | 0                       | 0x30         |
| 0                          | 0                         | 1                       | 0x31         |
| 0                          | 1                         | 0                       | 0x32         |
| 0                          | 1                         | 1                       | 0x33         |
| 1                          | 0                         | 0                       | 0x31         |
| 1                          | 0                         | 1                       | 0x30         |
| 1                          | 1                         | 0                       | 0x33         |
| 1                          | 1                         | 1                       | 0x32         |

The Intel® 7300 Chipset chipset assigns Agent ID, Cluster ID as listed below. When the Intel® Xeon® Processor 7200 Series and 7300 Series is used in conjunction with the Intel® 7300 Chipset, the following PECl device addresses are generated as shown below:

FSB0 {Cluster ID[1:0], Agent ID[1]} = 000; PECl address 0x30

FSB1 {Cluster ID[1:0], Agent ID[1]} = 010; PECl address 0x32

FSB2 {Cluster ID[1:0], Agent ID[1]} = 100; PECl address 0x31

FSB3 {Cluster ID[1:0], Agent ID[1]} = 110; PECl address 0x33

The power-on-configuration (POC) settings of third-party chipsets may produce different PECl addresses than those shown above. Thermal designers should consult their third party chipset designers for the correct PECl addresses.

Please note that each address also supports two domains (Domain 0 and Domain 1).

### 6.3.2.2 PECl Fault Handling Requirements

PECl is largely a fault tolerant interface, including noise immunity and error checking improvements over other comparable industry standard interfaces. The PECl client is as reliable as the device that it is embedded in, and thus given operating conditions that fall under the specification, the PECl will always respond to requests and the protocol itself can be relied upon to detect any transmission failures. There are, however, certain scenarios where the PECl is known to be unresponsive.



Prior to a power on RESET# and during RESET# assertion, PECI is not guaranteed to provide reliable thermal data. System designs should implement a default power-on condition that ensures proper processor operation during the time frame when reliable data is not available via PECI.

To protect platforms from potential operational or safety issues due to an abnormal condition on PECI, the Host controller should take action to protect the system from possible damaging states. If the Host controller cannot complete a valid PECI transactions of GetTemp0() with a given PECI device over 3 consecutive failed transactions or a one second max specified interval, then it should take appropriate actions to protect the corresponding device and/or other system components from overheating. The host controller may also implement an alert to software in the event of a critical or continuous fault condition.

### 6.3.2.3 PECI GetTemp0() and GetTemp1() Error Code Support

The error codes supported for the processor GetTemp0() and GetTemp1() commands are listed in [Table 6-11](#) below:

**Table 6-11. GetTemp0() and GetTemp1() Error Codes**

| Error Code | Description                                                                                                                         |
|------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 0x8000     | General sensor error                                                                                                                |
| 0x8002     | Sensor is operational, but has detected a temperature below its operational range (underflow), currently 30°C absolute temperature. |

§



# 7 Features

## 7.1 Power-On Configuration Options

Several configuration options can be configured by hardware. The Intel® Xeon® Processor 7200 Series and 7300 Series sample its hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifics on these options, please refer to [Table 7-1](#).

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor, for reset purposes, the processor does not distinguish between a “warm” reset (PWRGOOD signal remains asserted) and a “power-on” reset.

**Table 7-1. Power-On Configuration Option pins**

| Configuration Option              | Pin Name  | Notes |
|-----------------------------------|-----------|-------|
| Execute BIST (Built-In Self Test) | A3#       | 1,2   |
| Disable MCERR# observation        | A9#       | 1,2   |
| Disable BINIT# observation        | A10#      | 1,2   |
| Cluster ID / APIC ID[4:3]         | A[12:11]# | 1,2   |
| Disable dynamic bus parking       | A25#      | 1,2   |
| Symmetric agent arbitration ID    | BR[1:0]#  | 1,2   |
| Output tri state                  | SMI#      | 1,2,3 |

**Notes:**

1. Asserting this signal during RESET# will select the corresponding option.
2. Address pins not identified in this table as configuration options should not be asserted during RESET#.
3. Requires de-assertion of PWRGOOD.

Disabling of any of the cores within the Intel® Xeon® Processor 7200 Series and 7300 Series must be handled by configuring the EXT\_CONFIG Model Specific Register (MSR). This MSR will allow for the disabling of a single core per die within the Intel® Xeon® Processor 7200 Series and 7300 Series package..

## 7.2 Clock Control and Low Power States

The Intel® Xeon® Processor 7200 Series and 7300 Series supports the Extended HALT state (also referred to as C1E) in addition to the HALT state and Stop-Grant state to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See [Figure 7-1](#) for a visual representation of the processor low power states. The Extended HALT state is a lower power state than the HALT state or Stop Grant state.

**The Extended HALT state must be enabled via the BIOS for the processor to remain within its specifications.** For processors that are already running at the lowest bus to core frequency ratio for its nominal operating point, the processor will transition to the HALT state instead of the Extended HALT state.

The Stop Grant state requires chipset and BIOS support on multiprocessor systems. In a multiprocessor system, all the STPCLK# signals are bussed together, thus all processors are affected in unison. When the STPCLK# signal is asserted, the processor enters the Stop Grant state, issuing a Stop Grant Special Bus Cycle (SBC) for each



processor. The chipset needs to account for a variable number of processors asserting the Stop Grant SBC on the bus before allowing the processor to be transitioned into one of the lower processor power states.

### 7.2.1 Normal State

This is the normal operating state for the processor.

### 7.2.2 HALT or Extended HALT State

The Extended HALT state (C1E) is enabled via the BIOS. **The Extended HALT state must be enabled for the processor to remain within its specifications.** The Extended HALT state requires support for dynamic VID transitions in the platform.

#### 7.2.2.1 HALT State

HALT is a low power state entered when the processor has executed the HALT or MWAIT instruction. When one of the processor cores executes the HALT or MWAIT instruction, that processor core is halted; however, the other processor cores continue normal operation. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, LINT[1:0] (NMI, INTR), or an interrupt delivered over the front side bus. RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the HALT state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume III: System Programming Guide* for more information.

The system can generate a STPCLK# while the processor is in the HALT state. When the system deasserts STPCLK#, the processor will return execution to the HALT state.

While in HALT state, the processor will process front side bus snoops and interrupts.

#### 7.2.2.2 Extended HALT State

Extended HALT state is a low power state entered when all processor cores have executed the HALT or MWAIT instructions and Extended HALT state has been enabled via the BIOS. When one of the processor cores executes the HALT instruction, that processor core is halted; however, the other processor cores continue normal operation. The Extended HALT state is a lower power state than the HALT state or Stop Grant state. The Extended HALT state must be enabled for the processor to remain within its specifications.

**Note:** Not all Intel® Xeon® Processor 7200 Series and 7300 Series are capable of supporting Extended HALT State. More detail on which processor frequencies will support this feature will be provided in future releases of the *Intel® Xeon® Processor 7200, 7300 Series Specification Update* when available.

The processor will automatically transition to a lower core frequency and voltage operating point before entering the Extended HALT state. Note that the processor FSB frequency is not altered; only the internal core frequency is changed. When entering the low power state, the processor will first switch to the lower bus to core frequency ratio and then transition to the lower voltage (VID).

While in the Extended HALT state, the processor will process bus snoops.



Table 7-2. Extended HALT Maximum Power

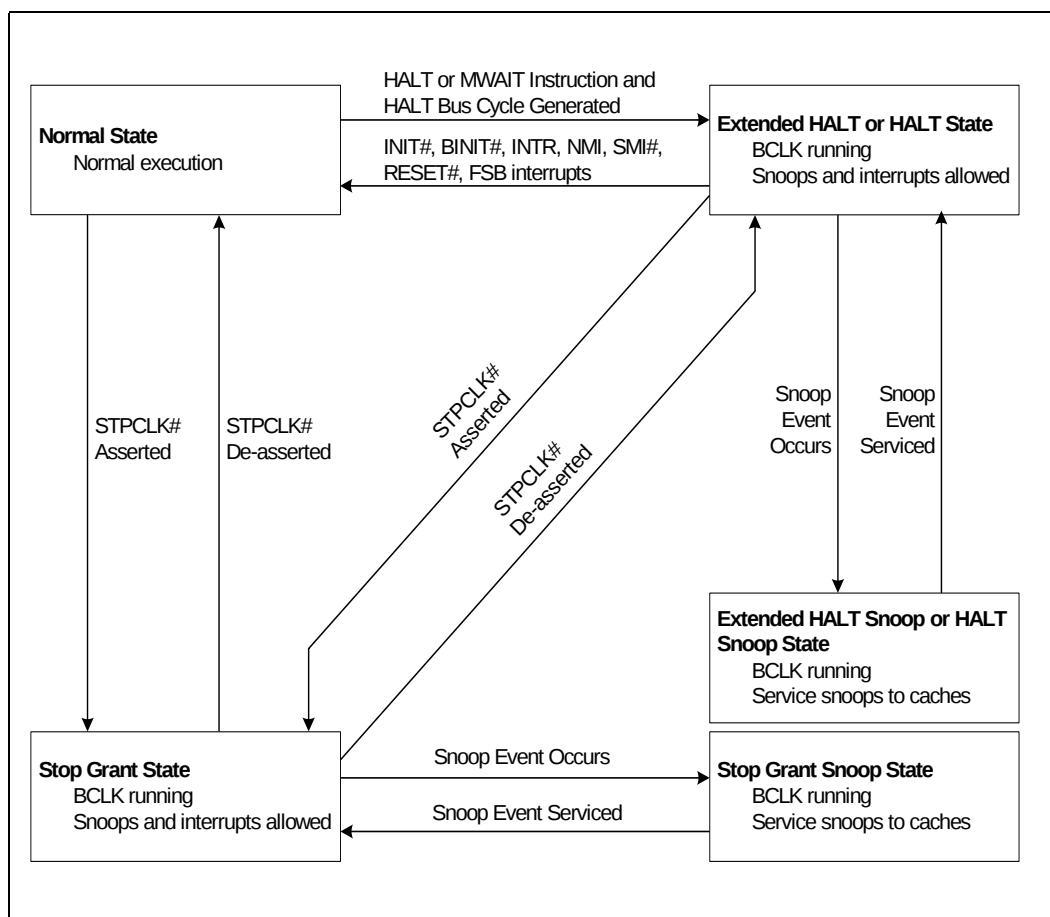
| Symbol                                                            | Parameter                 | Min | Typ | Max | Unit | Notes |
|-------------------------------------------------------------------|---------------------------|-----|-----|-----|------|-------|
| P <sub>EXTENDED HALT Quad-Core Intel® Xeon® E7300 Processor</sub> | Extended HALT State Power |     |     | 34  | W    | 2,3   |
| P <sub>EXTENDED HALT Quad-Core Intel® Xeon® X7350 Processor</sub> | Extended HALT State Power |     |     | 50  | W    | 2     |
| P <sub>EXTENDED HALT Quad-Core Intel® Xeon® L7345 Processor</sub> | Extended HALT State Power |     |     | 24  | W    | 1     |

**Notes:**

1. The specification is at T<sub>CASE</sub> = 50°C and nominal V<sub>CC</sub>. The VID setting represents the maximum expected VID while running in HALT state.
2. This specification is characterized by design.
3. Processors running in the lowest bus ratio will enter the HALT state when the processor has executed the HALT and MWAIT instruction since the processor is already in the lowest core frequency and voltage operating point.

The processor exits the Extended HALT state when a break event occurs. When the processor exits the Extended HALT state, it will first transition the VID to the original value and then change the bus to core frequency ratio back to the original value.

Figure 7-1. Stop Clock State Machine



### 7.2.3 Stop-Grant State

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor issued Stop Grant Acknowledge special bus cycle. Once the STPCLK# pin has been asserted, it may only be deasserted once the processor is in the Stop Grant state. All processor cores will enter the Stop-Grant state once the STPCLK# pin is asserted. Additionally, all processor cores must be in the Stop Grant state before the deassertion of STPCLK#.

Since the AGTL+ signal pins receive power from the front side bus, these pins should not be driven (allowing the level to return to  $V_{TT}$ ) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the front side bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from the Stop Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the deassertion of the STPCLK# signal.

A transition to the Grant Snoop state will occur when the processor detects a snoop on the front side bus (see [Section 7.2.4.1](#)).



While in the Stop-Grant state, SMI#, INIT#, BINIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process snoops on the front side bus and it will latch interrupts delivered on the front side bus.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# will be asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear will still cause assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state.

## 7.2.4 Extended HALT Snoop or HALT Snoop State, Stop Grant Snoop State

The Extended HALT Snoop state is used in conjunction with the Extended HALT state. If the Extended HALT state is not enabled in the BIOS, the default Snoop state entered will be the HALT Snoop state. Refer to the sections below for details on HALT Snoop state, Stop Grant Snoop state and Extended HALT Snoop state.

### 7.2.4.1 HALT Snoop State, Stop Grant Snoop State

The processor will respond to snoop or interrupt transactions on the front side bus while in Stop-Grant state or in HALT state. During a snoop or interrupt transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the front side bus has been serviced (whether by the processor or another agent on the front side bus) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the processor will return to the Stop-Grant state or HALT state, as appropriate.

### 7.2.4.2 Extended HALT Snoop State

The Extended HALT Snoop state is the default Snoop state when the Extended HALT state is enabled via the BIOS. The processor will remain in the lower bus to core frequency ratio and VID operating point of the Extended HALT state.

While in the Extended HALT Snoop state, snoops and interrupt transactions are handled the same way as in the HALT Snoop state. After the snoop is serviced or the interrupt is latched, the processor will return to the Extended HALT state.

## 7.3 Enhanced Intel SpeedStep® Technology

The Intel® Xeon® Processor 7200 Series and 7300 Series support Enhanced Intel SpeedStep® Technology. This technology enables the processor to switch between multiple frequency and voltage points, which results in platform power savings. Enhanced Intel SpeedStep Technology requires support for dynamic VID transitions in the platform. Switching between voltage/frequency states is software controlled.

**Note:** Not all Intel® Xeon® Processor 7200 Series and 7300 Series may be capable of supporting Enhanced Intel SpeedStep Technology. More details on which processor frequencies will support this feature will be provided in future releases of the *Intel® Xeon® Processor 7200, 7300 Series Specification Update* when available.

Enhanced Intel SpeedStep Technology creates processor performance states (P-states) or voltage/frequency operating points. P-states are lower power capability states within the Normal state as shown in [Figure 7-1](#). Enhanced Intel SpeedStep Technology enables real-time dynamic switching between frequency and voltage points. It alters the performance of the processor by changing the bus to core frequency ratio and voltage. This allows the processor to run at different core frequencies and voltages to best serve the performance and power requirements of the processor and system. The Intel® Xeon® Processor 7200 Series and 7300 Series have hardware logic that coordinates the requested voltage (VID) between the processor cores. The highest voltage requested from the four processor cores is selected for that processor package. Note that the front side bus is not altered; only the internal core frequency is changed. In order to run at reduced power consumption, the voltage is altered in step with the bus ratio.

The following are key features of Enhanced Intel SpeedStep Technology:

- Multiple voltage/frequency operating points provide optimal performance at reduced power consumption.
- Voltage/frequency selection is software controlled by writing to processor MSR's (Model Specific Registers), thus eliminating chipset dependency.
  - If the target frequency is higher than the current frequency,  $V_{CC}$  is incremented in steps (+12.5 mV) by placing a new value on the VID signals and the processor shifts to the new frequency. Note that the top frequency for the processor can not be exceeded.
  - If the target frequency is lower than the current frequency, the processor shifts to the new frequency and  $V_{CC}$  is then decremented in steps (-12.5 mV) by changing the target VID through the VID signals.

## 7.4 System Management Bus (SMBus) Interface

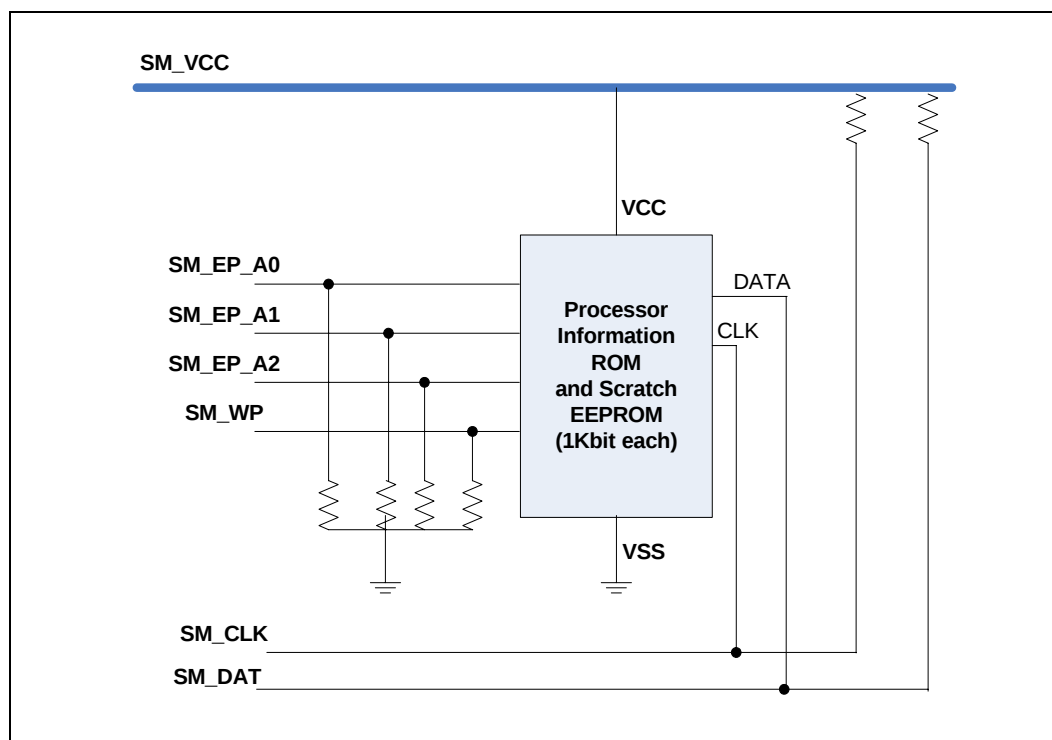
The Intel® Xeon® Processor 7200 Series and 7300 Series package includes an SMBus interface which allows access to a memory component with two sections (referred to as the Processor Information ROM and the Scratch EEPROM). These devices and their features are described below.

**Note:** The SMBus on-package thermal sensor has been removed and is no longer used. Refer to [Section 6.3](#) for details about the new digital thermometer and PECI interface.

The processor SMBus implementation uses the clock and data signals of the *System Management Bus (SMBus) Specification*. It does not implement the SMBSUS# signal.

For platforms which do not implement any of the SMBus features found on the processor, all of the SMBus connections, except SM\_VCC, to the socket pins may be left unconnected (SM\_CLK, SM\_DAT, SM\_EP\_A[2:0], SM\_WP).

Figure 7-2. Logical Schematic of SMBus Circuitry



**Note:** Actual implementation may vary. This figure is provided to offer a general understanding of the architecture. All SMBus pull-up and pull-down resistors are 10 k $\Omega$  and located on the processor.

### 7.4.1 SMBus Device Addressing

Of the addresses broadcast across the SMBus, the memory component claims those of the form "1010XXXZb". The "XXX" bits are defined by pull-up and pull-down resistors on the system baseboard. These address pins are pulled down weakly (10 k $\Omega$ ) on the processor substrate to ensure that the memory components are in a known state in systems which do not support the SMBus (or only support a partial implementation). The "Z" bit is the read/write bit for the serial bus transaction.

Note that addresses of the form "0000XXXXb" are Reserved and should not be generated by an SMBus master. The system designer must also ensure that their particular implementation does not add excessive capacitance to the address inputs. Excess capacitance at the address inputs may cause address recognition problems. Refer to the appropriate platform design guide document.

Figure 7-2 shows a logical diagram of the pin connections. Table 7-3 describe the address pin connections and how they affect the addressing of the devices.

**Table 7-3. Memory Device SMBus Addressing**

| Address (Hex) | Upper Address <sup>1</sup> | Device Select     |                   |                   | R/W   |
|---------------|----------------------------|-------------------|-------------------|-------------------|-------|
|               | bits 7-4                   | SM_EP_A2<br>bit 3 | SM_EP_A1<br>bit 2 | SM_EP_A0<br>bit 1 | bit 0 |
| A0h/A1h       | 1010                       | 0                 | 0                 | 0                 | X     |
| A2h/A3h       | 1010                       | 0                 | 0                 | 1                 | X     |
| A4h/A5h       | 1010                       | 0                 | 1                 | 0                 | X     |
| A6h/A7h       | 1010                       | 0                 | 1                 | 1                 | X     |
| A8h/A9h       | 1010                       | 1                 | 0                 | 0                 | X     |
| AAh/ABh       | 1010                       | 1                 | 0                 | 1                 | X     |
| ACh/ADh       | 1010                       | 1                 | 1                 | 0                 | X     |
| A Eh/AFh      | 1010                       | 1                 | 1                 | 1                 | X     |

**Note:**

1. This addressing scheme will support up to 8 processors on a single SMBus.

## 7.4.2 PIROM and Scratch EEPROM Supported SMBus Transactions

The Processor Information ROM (PIROM) responds to two SMBus packet types: Read Byte and Write Byte. However, since the PIROM is write-protected, it will acknowledge a Write Byte command but ignore the data. The Scratch EEPROM responds to Read Byte and Write Byte commands. [Table 7-4](#) diagrams the Read Byte command. [Table 7-5](#) diagrams the Write Byte command. Following a write cycle to the scratch ROM, software must allow a minimum of 10 ms before accessing either ROM of the processor.

In the tables, 'S' represents the SMBus start bit, 'P' represents a stop bit, 'R' represents a read bit, 'W' represents a write bit, 'A' represents an acknowledge (ACK), and '///' represents a negative acknowledge (NACK). The shaded bits are transmitted by the Processor Information ROM or Scratch EEPROM, and the bits that aren't shaded are transmitted by the SMBus host controller. In the tables, the data addresses indicate 8 bits. The SMBus host controller should transmit 8 bits with the most significant bit indicating which section of the EEPROM is to be addressed: the Processor Information ROM (MSB = 0) or the Scratch EEPROM (MSB = 1).

**Table 7-4. Read Byte SMBus Packet**

| S | Slave Address | Write | A | Command Code | A | S | Slave Address | Read | A | Data   | /// | P |
|---|---------------|-------|---|--------------|---|---|---------------|------|---|--------|-----|---|
| 1 | 7-bits        | 1     | 1 | 8-bits       | 1 | 1 | 7-bits        | 1    | 1 | 8-bits | 1   | 1 |

**Table 7-5. Write Byte SMBus Packet**

| S | Slave Address | Write | A | Command Code | A | Data   | A | P |
|---|---------------|-------|---|--------------|---|--------|---|---|
| 1 | 7-bits        | 1     | 1 | 8-bits       | 1 | 8-bits | 1 | 1 |



### 7.4.3 Processor Information ROM (PIROM)

The lower half (128 bytes) of the SMBus memory component is an electrically programmed read-only memory with information about the processor. This information is permanently write-protected. [Table 7-6](#) shows the data fields and [Section 7.4.3](#) provides the formats of the data fields included in the Processor Information ROM (PIROM).

The PIROM consists of the following sections:

- Header
- Processor Data
- Processor Core Data
- Cache Data
- Package Data
- Part Number Data
- Thermal Reference Data
- Feature Data
- Other Data

**Table 7-6. Processor Information ROM Data Sections (Sheet 1 of 3)**

| Offset / Section            | # of Bits | Function                       | Notes                            |
|-----------------------------|-----------|--------------------------------|----------------------------------|
| <b>Header:</b>              |           |                                |                                  |
| 00h                         | 8         | Data Format Revision           | Two 4-bit hex digits             |
| 01 - 02h                    | 16        | PIROM Size                     | Size in bytes (MSB first)        |
| 03h                         | 8         | Processor Data Address         | Byte pointer, 00h if not present |
| 04h                         | 8         | Processor Core Data Address    | Byte pointer, 00h if not present |
| 05h                         | 8         | L3 Cache Data Address          | Byte pointer, 00h if not present |
| 06h                         | 8         | Package Data Address           | Byte pointer, 00h if not present |
| 07h                         | 8         | Part Number Data Address       | Byte pointer, 00h if not present |
| 08h                         | 8         | Thermal Reference Data Address | Byte pointer, 00h if not present |
| 09h                         | 8         | Feature Data Address           | Byte pointer, 00h if not present |
| 0Ah                         | 8         | Other Data Address             | Byte pointer, 00h if not present |
| 0B - 0Ch                    | 16        | Reserved                       | Reserved                         |
| 0Dh                         | 8         | Checksum                       | 1 byte checksum                  |
| <b>Processor Data:</b>      |           |                                |                                  |
| 0E - 13h                    | 48        | S-spec Number                  | Six 8-bit ASCII characters       |
| 14h                         | 6         | Reserved                       | Reserved (most significant bits) |
|                             | 2         | Sample/Production              | 00b = Sample, 01b = Production   |
| 15h                         | 8         | Checksum                       | 1 byte checksum                  |
| <b>Processor Core Data:</b> |           |                                |                                  |
| 16 - 19h                    | 2         | Reserved                       | Reserved for future use          |
|                             | 8         | Extended Family                | From CPUID                       |
|                             | 4         | Extended Model                 | From CPUID                       |



Table 7-6. Processor Information ROM Data Sections (Sheet 2 of 3)

| Offset / Section          | # of Bits | Function                           | Notes                                               |
|---------------------------|-----------|------------------------------------|-----------------------------------------------------|
|                           | 2         | Reserved                           | Reserved for future use                             |
|                           | 2         | Processor Core Type                | From CPUID                                          |
|                           | 4         | Processor Core Family              | From CPUID                                          |
|                           | 4         | Processor Core Model               | From CPUID                                          |
|                           | 4         | Processor Core Stepping            | From CPUID                                          |
|                           | 2         | Reserved                           | Reserved for future use                             |
| 1A - 1Bh                  | 16        | Front Side Bus Speed               | 16-bit binary number (in MHz)                       |
| 1Ch                       | 2<br>6    | Multiprocessor Support<br>Reserved | 00b = UP,01b = DP,10b = RSVD,11b = MP<br>Reserved   |
| 1D - 1Eh                  | 16        | Maximum Core Frequency             | 16-bit binary number (in MHz)                       |
| 1F - 20h                  | 16        | Maximum Core VID                   | Maximum $V_{CC}$ requested by VID outputs in mV     |
| 21 - 22h                  | 16        | Minimum Core Voltage               | Minimum processor DC $V_{CC}$ in mV                 |
| 23h                       | 8         | $T_{CASE}$ Maximum                 | Maximum case temperature spec in °C                 |
| 24h                       | 8         | Checksum                           | 1 byte checksum                                     |
| <b>Cache Data:</b>        |           |                                    |                                                     |
| 25 - 26h                  | 16        | Reserved                           | Reserved for future use                             |
| 27 - 28h                  | 16        | L2 Cache Size                      | 16-bit binary number (in KB)                        |
| 29 - 2Ah                  | 16        | L3 Cache Size                      | 16-bit binary number (in KB)                        |
| 2B - 2Ch                  | 16        | Maximum Cache CVID                 | Maximum $V_{CACHE}$ requested by CVID outputs in mV |
| 2D - 2Eh                  | 16        | Minimum Cache Voltage              | Minimum processor DC $V_{CACHE}$ in mV              |
| 2F - 30h                  | 16        | Reserved                           | Reserved                                            |
| 31h                       | 8         | Checksum                           | 1 byte checksum                                     |
| <b>Package Data:</b>      |           |                                    |                                                     |
| 32 - 35h                  | 32        | Package Revision                   | Four 8-bit ASCII characters                         |
| 36h                       | 8         | Reserved                           | Reserved for future use                             |
| 37h                       | 8         | Checksum                           | 1 byte checksum                                     |
| <b>Part Number Data:</b>  |           |                                    |                                                     |
| 38 - 3Eh                  | 56        | Processor Part Number              | Seven 8-bit ASCII characters                        |
| 3F - 4Ch                  | 112       | Reserved                           | Reserved                                            |
| 4D - 54h                  | 64        | Processor Electronic Signature     | 64-bit identification number                        |
| 55 - 6Eh                  | 208       | Reserved                           | Reserved                                            |
| 6Fh                       | 8         | Checksum                           | 1 byte checksum                                     |
| <b>Thermal Ref. Data:</b> |           |                                    |                                                     |
| 70h                       | 8         | Reserved                           | Reserved                                            |
| 71 - 72h                  | 16        | Reserved                           | Reserved                                            |
| 73h                       | 8         | Checksum                           | 1 byte checksum                                     |
| <b>Feature Data:</b>      |           |                                    |                                                     |
| 74 - 77h                  | 32        | Processor Core Feature Flags       | From CPUID function 1, EDX contents                 |



Table 7-6. Processor Information ROM Data Sections (Sheet 3 of 3)

| Offset / Section | # of Bits | Function                              | Notes                                                                                                                                                                                                                                                     |
|------------------|-----------|---------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 78h              | 8         | Processor Feature Flags               | [7] = Multi-Core<br>[6] = Serial Signature<br>[5] = Electronic Signature Present<br>[4] = Thermal Sense Device Present<br>[3] = Reserved<br>[2] = OEM EEPROM Present<br>[1] = Core VID Present<br>[0] = L3 Cache Present                                  |
| 79h              | 8         | Processor Thread and Core Information | [7:2] = Number of cores<br>[1:0] = Number of threads per core                                                                                                                                                                                             |
| 7Ah              | 8         | Additional Processor Feature Flags    | [7] = Reserved<br>[6] = Intel® Cache Safe Technology<br>[5] = Extended Halt State (C1E)<br>[4] = Intel® Virtualization Technology<br>[3] = Execute Disable<br>[2] = Intel® 64<br>[1] = Thermal Monitor TM2<br>[0] = Enhanced Intel® SpeedStep® Technology |
| 7B-7Ch           | 16        | Thermal Adjustment Factors (Pending)  | [15:8] = Measurement Correction Factor<br>[7:0] = Temperature Target                                                                                                                                                                                      |
| 7D-7Eh           | 16        | Reserved                              | Reserved                                                                                                                                                                                                                                                  |
| 7Fh              | 8         | Checksum                              | 1 byte checksum                                                                                                                                                                                                                                           |

Details on each of these sections are described below.

**Note:** Reserved fields or bits SHOULD be programmed to zeros. However, OEMs should not rely on this model.

#### 7.4.3.1 Header

To maintain backward compatibility, the Header defines the starting address for each subsequent section of the PIROM. Software should check for the offset before reading data from a particular section of the ROM.

**Example:** Code looking for the cache data of a processor would read offset 05h to find a value of 25h. 25h is the first address within the 'Cache Data' section of the PIROM.

##### 7.4.3.1.1 DFR: Data Format Revision

This location identifies the data format revision of the PIROM data structure. Writes to this register have no effect.

| Offset: 00h |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 7:0         | <b>Data Format Revision</b><br>The data format revision is used whenever fields within the PIROM are redefined. The initial definition will begin at a value of 1. If a field, or bit assignment within a field, is changed such that software needs to discern between the old and new definition, then the data format revision field will be incremented.<br><br>00h: Reserved<br>01h: Initial definition<br>02h: Second revision<br>03h: Third revision<br>04h: Fourth revision ( <i>Defined by this document</i> )<br>05h-FFh: Reserved |



#### 7.4.3.1.2 PISIZE: PIROM Size

This location identifies the PIROM size. Writes to this register have no effect.

| Offset: 01h-02h |                                                                                                                                                                                                                                 |
|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit             | Description                                                                                                                                                                                                                     |
| 15:0            | <b>PIROM Size</b><br>The PIROM size provides the size of the device in hex bytes. The MSB is at location 01h, the LSB is at location 02h.<br><br>0000h - 007Fh: Reserved<br>0080h: 128 byte PIROM size<br>0081- FFFFh: Reserved |

#### 7.4.3.1.3 PDA: Processor Data Address

This location provides the offset to the Processor Data Section. Writes to this register have no effect.

| Offset: 03h |                                                                                                                                                                                                                     |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                                                                                                                         |
| 7:0         | <b>Processor Data Address</b><br>Byte pointer to the Processor Data section<br><br>00h: Processor Data section not present<br>01h - 0Dh: Reserved<br>0Eh: Processor Data section pointer value<br>0Fh-FFh: Reserved |

#### 7.4.3.1.4 PCDA: Processor Core Data Address

This location provides the offset to the Processor Core Data Section. Writes to this register have no effect.

| Offset: 04h |                                                                                                                                                                                                                                    |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                                                                                                                                        |
| 7:0         | <b>Processor Core Data Address</b><br>Byte pointer to the Processor Data section<br><br>00h: Processor Core Data section not present<br>01h - 15h: Reserved<br>16h: Processor Core Data section pointer value<br>17h-FFh: Reserved |

#### 7.4.3.1.5 L3CDA: L3 Cache Data Address

This location provides the offset to the L3 Cache Data Section. Writes to this register have no effect.

| Offset: 05h |                                                                                                                                                                                                                 |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                                                                                                                     |
| 7:0         | <b>L3 Cache Data Address</b><br>Byte pointer to the L3 Cache Data section<br><br>00h: L3 Cache Data section not present<br>01h - 24h: Reserved<br>25h: L3 Cache Data section pointer value<br>26h-FFh: Reserved |



#### 7.4.3.1.6 PDA: Package Data Address

This location provides the offset to the Package Data Section. Writes to this register have no effect.

| <b>Offset: 06h</b> |                                                                                                                                                                                                             |
|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                | Description                                                                                                                                                                                                 |
| 7:0                | <b>Package Data Address</b><br>Byte pointer to the Package Data section<br><br>00h: Package Data section not present<br>01h - 31h: Reserved<br>32h: Package Data section pointer value<br>33h-FFh: Reserved |

#### 7.4.3.1.7 PNDA: Part Number Data Address

This location provides the offset to the Part Number Data Section. Writes to this register have no effect.

| <b>Offset: 07h</b> |                                                                                                                                                                                                                             |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                | Description                                                                                                                                                                                                                 |
| 7:0                | <b>Part Number Data Address</b><br>Byte pointer to the Part Number Data section<br><br>00h: Part Number Data section not present<br>01h - 37h: Reserved<br>38h: Part Number Data section pointer value<br>39h-FFh: Reserved |

#### 7.4.3.1.8 TRDA: Thermal Reference Data Address

This location provides the offset to the Thermal Reference Data Section. Writes to this register have no effect.

| <b>Offset: 08h</b> |                                                                                                                                                                                                                                                     |
|--------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit                | Description                                                                                                                                                                                                                                         |
| 7:0                | <b>Thermal Reference Data Address</b><br>Byte pointer to the Thermal Reference Data section<br><br>00h: Thermal Reference Data section not present<br>01h - 6Fh: Reserved<br>70h: Thermal Reference Data section pointer value<br>71h-FFh: Reserved |

#### 7.4.3.1.9 FDA: Feature Data Address

This location provides the offset to the Feature Data Section. Writes to this register have no effect.

| Offset: 09h |                                                                                                                                                                                                             |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                                                                                                                 |
| 7:0         | <b>Feature Data Address</b><br>Byte pointer to the Feature Data section<br><br>00h: Feature Data section not present<br>01h - 73h: Reserved<br>74h: Feature Data section pointer value<br>75h-FFh: Reserved |

#### 7.4.3.1.10 ODA: Other Data Address

This location provides the offset to the Other Data Section. Writes to this register have no effect.

| Offset: 0Ah |                                                                                                                                                                                                      |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                                                                                                          |
| 7:0         | <b>Other Data Address</b><br>Byte pointer to the Other Data section<br><br>00h: Other Data section not present<br>01h - 7Dh: Reserved<br>7Eh: Other Data section pointer value<br>7Fh- FFh: Reserved |

#### 7.4.3.1.11 RES1: Reserved 1

This locations are reserved. Writes to this register have no effect.

| Offset: 0Bh-0Ch |                                              |
|-----------------|----------------------------------------------|
| Bit             | Description                                  |
| 15:0            | <b>RESERVED</b><br><br>0000h-FFFFh: Reserved |

#### 7.4.3.1.12 HCKS: Header Checksum

This location provides the checksum of the Header Section. Writes to this register have no effect.

| Offset: 0Dh |                                                                                                                                                   |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                                                       |
| 7:0         | <b>Header Checksum</b><br>One Byte Checksum of the Header Section<br><br>00h- FFh: See <a href="#">Section 7.4.4</a> for calculation of the value |



### 7.4.3.2 Processor Data

This section contains two pieces of data:

- The S-spec of the part in ASCII format
- (1) 2-bit field to declare if the part is a pre-production sample or a production unit

#### 7.4.3.2.1 SNUM: S-Spec Number

This location provides the S-Spec number of the processor. The S-spec field is six ASCII characters wide and is programmed with the same S-spec value as marked on the processor. If the value is less than six characters in length, leading spaces (20h) are programmed in this field. Writes to this register have no effect.

**Example:** A processor with a S-Spec mark of SLA67 contains the following in field 0E-13h: 20h, 53h, 4Ch, 41h, 36h, 37h. This data consists of one blank at 0Eh followed by the ASCII codes for SLA67 in locations 0F - 13h.

| Offset: 0Eh-13h |                                                                            |
|-----------------|----------------------------------------------------------------------------|
| Bit             | Description                                                                |
| 7:0             | <b>Character 6</b><br>S-SPEC character or 20h<br>00h-0FFh: ASCII character |
| 15:8            | <b>Character 5</b><br>S-SPEC character<br>00h-0FFh: ASCII character        |
| 23:16           | <b>Character 4</b><br>S-SPEC character<br>00h-0FFh: ASCII character        |
| 31:24           | <b>Character 3</b><br>S-SPEC character<br>00h-0FFh: ASCII character        |
| 39:32           | <b>Character 2</b><br>S-SPEC character<br>00h-0FFh: ASCII character        |
| 47:40           | <b>Character 1</b><br>S-SPEC character<br>00h-0FFh: ASCII character        |



#### 7.4.3.2.2 SAMPROD: Sample / Production

This location contains the sample/production field, which is a two-bit field and is LSB aligned. All S-spec material will use a value of 01b. All other values are reserved. Writes to this register have no effect.

**Example:** A processor with an Sxxxx mark (production unit) will use 01h at offset 14h.

| Offset: 14h |                                                                                                                         |
|-------------|-------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                             |
| 7:2         | <b>RESERVED</b><br>000000b-111111b: Reserved                                                                            |
| 1:0         | <b>Sample / Production</b><br>Sample or Production indicator<br><br>00b: Sample<br>01b: Production<br>10b-11b: Reserved |

#### 7.4.3.2.3 PDCKS: Processor Data Checksum

This location provides the checksum of the Processor Data Section. Writes to this register have no effect.

| Offset: 15h |                                                                                                                                                                      |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                                                                          |
| 7:0         | <b>Processor Data Checksum</b><br>One Byte Checksum of the of Processor Data Section<br><br>00h- FFh: See <a href="#">Section 7.4.4</a> for calculation of the value |

#### 7.4.3.3 Processor Core Data

This section contains core silicon-related data.

##### 7.4.3.3.1 CPUID: CPUID

This location contains the CPUID, Processor Type, Family, Model and Stepping. The CPUID field is a copy of the results in EAX[27:0] from Function 1 of the CPUID instruction. The MSB is at location 16h, the LSB is at location 19h. Writes to this register have no effect.

**Note:** The field is not aligned on a byte boundary since the first two bits of the offset are reserved. Thus, the data must be shifted left by two in order to obtain the same results.

**Example:** The CPUID of a G-0 stepping Intel® Xeon® Processor 7200 Series and 7300 Series is 06FBh. The value programmed into the PIROM is 00001BECh.

**Note:** The first two bits of the PIROM are reserved, as highlighted in the example below.

|                           |      |      |      |                      |
|---------------------------|------|------|------|----------------------|
| CPUID instruction results | 0000 | 0110 | 1111 | 1011 (06F9h)         |
| PIROM content             | 0001 | 1011 | 1110 | 11 <b>00</b> (1BECh) |



| Offset: 16h-19h |                                                        |
|-----------------|--------------------------------------------------------|
| Bit             | Description                                            |
| 31:30           | <b>Reserved</b><br>00b-11b: Reserved                   |
| 29:21           | <b>Extended Family</b><br>00h-0Fh: Extended Family     |
| 21:18           | <b>Extended Model</b><br>0h-Fh: Extended Model         |
| 17:16           | <b>Reserved</b><br>00b-11b: Reserved                   |
| 15:14           | <b>Processor Type</b><br>00b-11b: Processor Type       |
| 13:10           | <b>Processor Family</b><br>0h-Fh: Processor Family     |
| 9:6             | <b>Processor Model</b><br>0h-Fh: Processor Model       |
| 5:2             | <b>Processor Stepping</b><br>0h-Fh: Processor Stepping |
| 1:0             | <b>Reserved</b><br>00b-11b: Reserved                   |

#### 7.4.3.3.2 FSB: Front Side Bus Speed

This location contains the front side bus frequency information. Systems may need to read this offset to decide if all installed processors support the same front side bus speed. Because the FSB is described as a 4X data bus, the frequency given in this field is 1066 MTS. The data provided is the speed, rounded to a whole number, and reflected in hex. Writes to this register have no effect.

**Example:** The Intel® Xeon® Processor 7200 Series and 7300 Series supports a 1066 MTS front side bus. Therefore, offset 1A - 1Bh has a value of 042Ah.

| Offset: 1Ah-1Bh |                                                 |
|-----------------|-------------------------------------------------|
| Bit             | Description                                     |
| 15:0            | <b>Front Side Bus Speed</b><br>0000h-FFFFh: MHz |

#### 7.4.3.3.3 MPSUP: Multiprocessor Support

This location contains 2 bits for representing the supported number of physical processors on the bus. These two bits are MSB aligned where 00b equates to single-processor operation, 01b is a dual-processor operation, and 11b represents multi-processor operation. The Intel® Xeon® Processor 7200 Series and 7300 Series is an MP processor. The remaining six bits in this field are reserved for the future use. Writes to this register have no effect.

**Example:** An MP processor will use C0h at offset 1Ch.

| Offset: 1Ch |                                                                                                               |
|-------------|---------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                   |
| 7:6         | <b>Multiprocessor Support</b><br>UP, DP or MP indicator<br><br>00b: UP<br>01b: DP<br>10b: Reserved<br>11b: MP |
| 5:0         | <b>RESERVED</b><br><br>000000b-111111b: Reserved                                                              |

#### 7.4.3.3.4 MCF: Maximum Core Frequency

This location contains the maximum core frequency for the processor. Format of this field is in MHz, rounded to a whole number, and encoded in hex format. Writes to this register have no effect.

**Example:** A 2.666 GHz processor will have a value of 0A6Ah, which equates to 2666 decimal.

| Offset: 1Dh-1Eh |                                                       |
|-----------------|-------------------------------------------------------|
| Bit             | Description                                           |
| 15:0            | <b>Maximum Core Frequency</b><br><br>0000h-FFFFh: MHz |

#### 7.4.3.3.5 MAXVID: Maximum Core VID

This location contains the maximum Core VID (Voltage Identification) voltage that may be requested via the VID pins. This field, rounded to the next thousandth, is in mV and is reflected in hex. Writes to this register have no effect.

**Example:** A voltage of 1.350 V maximum core VID would contain 0546h (1350 decimal) in Offset 1F - 20h.

| Offset: 1Fh-20h |                                                |
|-----------------|------------------------------------------------|
| Bit             | Description                                    |
| 15:0            | <b>Maximum Core VID</b><br><br>0000h-FFFFh: mV |



#### 7.4.3.3.6 MINV: Minimum Core Voltage

This location contains the minimum Processor Core voltage. This field, rounded to the next thousandth, is in mV and is reflected in hex. The minimum  $V_{CC}$  reflected in this field is the minimum allowable voltage assuming the FMB maximum current draw. Writes to this register have no effect.

**Note:** The minimum core voltage value in offset 21 - 22h is a single value that assumes the FMB maximum current draw. Refer to [Table 2-10](#) and [Table 2-11](#) for the minimum core voltage specifications based on actual real-time current draw.

**Example:** A voltage of 1.000 V minimum core voltage would contain 03E8h (1000 decimal) in Offset 21 - 22h.

| Offset: 21h-22h |                                                |
|-----------------|------------------------------------------------|
| Bit             | Description                                    |
| 15:0            | <b>Minimum Core Voltage</b><br>0000h-FFFFh: mV |

#### 7.4.3.3.7 TCASE: $T_{CASE}$ Maximum

This location provides the maximum  $T_{CASE}$  for the processor. The field reflects temperature in degrees Celsius in hex format. This data can be found in [Section 6](#). The thermal specifications are specified at the case Integrated Heat Spreader (IHS). Writes to this register have no effect.

**Example:** A temperature of 66C would contain 42h (66 decimal) in Offset 23h.

| Offset: 23h |                                                                  |
|-------------|------------------------------------------------------------------|
| Bit         | Description                                                      |
| 7:0         | <b><math>T_{CASE}</math> Maximum</b><br>00h-FFh: Degrees Celsius |

#### 7.4.3.3.8 PCCKS: Processor Core Data Checksum

This location provides the checksum of the Processor Core Data Section. Writes to this register have no effect.

| Offset: 24h |                                                                                                                                                                         |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                                                                             |
| 7:0         | <b>Processor Core Data Checksum</b><br>One Byte Checksum of the Processor Core Data Section<br>00h- FFh: See <a href="#">Section 7.4.4</a> for calculation of the value |

#### 7.4.3.4 Cache Data

This section contains cache-related data.



#### 7.4.3.4.1 RES3: Reserved 3

These locations are reserved. Writes to this register have no effect.

| Offset: 25h-26h |                                            |
|-----------------|--------------------------------------------|
| Bit             | Description                                |
| 15:0            | <b>RESERVED 3</b><br>0000h-FFFFh: Reserved |

#### 7.4.3.4.2 L2SIZE: L2 Cache Size

This location contains the size of the level two cache in kilobytes. Writes to this register have no effect.

**Example:** The Intel® Xeon® Processor 7200 Series and 7300 Series has a 2x4MB (8192 KB) L2 cache total. Thus, offset 27 - 28h would contain 2000h.

| Offset: 27h-28h |                                         |
|-----------------|-----------------------------------------|
| Bit             | Description                             |
| 15:0            | <b>L2 Cache Size</b><br>0000h-FFFFh: KB |

#### 7.4.3.4.3 L3SIZE: L3 Cache Size

This location contains the size of the level three cache in kilobytes. Writes to this register have no effect.

**Example:** The Intel® Xeon® Processor 7200 Series and 7300 Series has no L3 cache. Thus, offset 29 - 2Ah will contain 0000h (0 decimal).

| Offset: 29h-2Ah |                                         |
|-----------------|-----------------------------------------|
| Bit             | Description                             |
| 15:0            | <b>L3 Cache Size</b><br>0000h-FFFFh: KB |

#### 7.4.3.4.4 MAXCVID: Maximum Cache VID

This location contains the maximum Cache VID (Voltage Identification) voltage that may be requested via the CVID pins. This field, rounded to the next thousandth, is in mV and is reflected in hex. Writes to this register have no effect.

**Example:** The Intel® Xeon® Processor 7200 Series and 7300 Series does not utilize a Cache VID. Offset 2B - 2Ch will contain 0000h (0 decimal).

| Offset: 2Bh-2Ch |                                             |
|-----------------|---------------------------------------------|
| Bit             | Description                                 |
| 15:0            | <b>Maximum Cache VID</b><br>0000h-FFFFh: mV |



#### 7.4.3.4.5 MINV: Minimum Cache Voltage

This location contains the minimum Cache voltage. This field, rounded to the next thousandth, is in mV and is reflected in hex. The minimum  $V_{\text{CACHE}}$  reflected in this field is the minimum allowable voltage assuming the FMB maximum current draw for two processors. Writes to this register have no effect.

**Example:** The Intel® Xeon® Processor 7200 Series and 7300 Series does not utilize a Cache VID. Offset 2D - 2Eh will contain 0000h (0 decimal).

| Offset: 2Dh-2Eh |                                                 |
|-----------------|-------------------------------------------------|
| Bit             | Description                                     |
| 15:0            | <b>Minimum Cache Voltage</b><br>0000h-FFFFh: mV |

#### 7.4.3.4.6 RES4: Reserved 4

These locations are reserved. Writes to this register have no effect.

| Offset: 2Fh-30h |                                            |
|-----------------|--------------------------------------------|
| Bit             | Description                                |
| 15:0            | <b>RESERVED 4</b><br>0000h-FFFFh: Reserved |

#### 7.4.3.4.7 CDCKS: Cache Data Checksum

This location provides the checksum of the Cache Data Section. Writes to this register have no effect.

| Offset: 31h |                                                                                                                                                       |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                                                           |
| 7:0         | <b>Cache Data Checksum</b><br>One Byte Checksum of the Cache Data Section<br>00h- FFh: See <a href="#">Section 7.4.4</a> for calculation of the value |

#### 7.4.3.5 Package Data

This section provides package revision information.

##### 7.4.3.5.1 PREV: Package Revision

This location tracks the highest level package revision. It is provided in ASCII format of four characters (8 bits x 4 characters = 32 bits). The package is documented as 1.0, 2.0, etc. If this only consumes three ASCII characters, a leading space is provided in the data field.

**Example:** The Intel® Xeon® Processor 7200 Series and 7300 Series utilizes the first revision of the FC-mPGA6 package. Thus, at offset 32-35h, the data is a space followed by 1.0. In hex, this would be 20h, 31h, 2Eh, 30h.

| Offset: 32h-35h |                                                                           |
|-----------------|---------------------------------------------------------------------------|
| Bit             | Description                                                               |
| 7:0             | <b>Character 4</b><br>ASCII character or 20h<br>00h-0FFh: ASCII character |
| 15:8            | <b>Character 3</b><br>ASCII character<br>00h-0FFh: ASCII character        |
| 23:16           | <b>Character 2</b><br>ASCII character<br>00h-0FFh: ASCII character        |
| 31:24           | <b>Character 1</b><br>ASCII character<br>00h-0FFh: ASCII character        |

#### 7.4.3.5.2 RES5: Reserved 5

This location is reserved. Writes to this register have no effect.

| Offset: 36h |                                        |
|-------------|----------------------------------------|
| Bit         | Description                            |
| 7:0         | <b>RESERVED 5</b><br>00h-FFh: Reserved |

#### 7.4.3.5.3 PDCKS: Package Data Checksum

This location provides the checksum of the Package Data Section. Writes to this register have no effect.

| Offset: 37h |                                                                                                                                                           |
|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                                                               |
| 7:0         | <b>Package Data Checksum</b><br>One Byte Checksum of the Package Data Section<br>00h- FFh: See <a href="#">Section 7.4.4</a> for calculation of the value |

#### 7.4.3.6 Part Number Data

This section provides traceability. There are 208 available bytes in this section for future use.

##### 7.4.3.6.1 PPN: Processor Part Number

This location contains seven ASCII characters reflecting the Intel part number for the processor. This information is typically marked on the outside of the processor. If the part number is less than 7 characters, a leading space is inserted into the value. The part number should match the information found in the marking specification found in [Section 3](#). Writes to this register have no effect.

**Example:** A processor with a part number of 80565KH will have the following at offset 38 - 3Eh: 38h, 30h, 35h, 36h, 35h, 4Bh, 48h.



| Offset: 38h-3Eh |                                                                           |
|-----------------|---------------------------------------------------------------------------|
| Bit             | Description                                                               |
| 7:0             | <b>Character 7</b><br>ASCII character or 20h<br>00h-0FFh: ASCII character |
| 15:8            | <b>Character 6</b><br>ASCII character or 20h<br>00h-0FFh: ASCII character |
| 23:16           | <b>Character 5</b><br>ASCII character or 20h<br>00h-0FFh: ASCII character |
| 31:24           | <b>Character 4</b><br>ASCII character<br>00h-0FFh: ASCII character        |
| 39:32           | <b>Character 3</b><br>ASCII character<br>00h-0FFh: ASCII character        |
| 47:40           | <b>Character 2</b><br>ASCII character<br>00h-0FFh: ASCII character        |
| 4F:48           | <b>Character 1</b><br>ASCII character<br>00h-0FFh: ASCII character        |

#### 7.4.3.6.2 RES6: Reserved 6

This location is reserved. Writes to this register have no effect.

| Offset: 3Fh-4Ch |                   |
|-----------------|-------------------|
| Bit             | Description       |
| 111:0           | <b>RESERVED 6</b> |

#### 7.4.3.6.3 Processor Serial/Electronic Signature

This location contains a 64-bit identification number. The value in this field is either a serial signature or an electronic signature. Bits 5 & 6 of the Processor Feature Flags (Offset 78h) indicates which signature is present. Intel does not guarantee that each processor will have a unique value in this field. Writes to this register have no effect.

| Offset: 4Dh=54h |                                                                                           |
|-----------------|-------------------------------------------------------------------------------------------|
| Bit             | Description                                                                               |
| 63:0            | <b>Processor Serial/Electronic Signature</b><br>00000000h-FFFFFFFFh: Electronic Signature |



#### 7.4.3.6.4 RES7: Reserved 7

This location is reserved. Writes to this register have no effect.

| Offset: 55h-6Eh |             |
|-----------------|-------------|
| Bit             | Description |
| 207:0           | RESERVED 7  |

#### 7.4.3.6.5 PNDCKS: Part Number Data Checksum

This location provides the checksum of the Part Number Data Section. Writes to this register have no effect.

| Offset: 6F |                                                                                                                                                                  |
|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit        | Description                                                                                                                                                      |
| 7:0        | <b>Part Number Data Checksum</b><br>One Byte Checksum of the Part Number Section<br><br>00h- FFh: See <a href="#">Section 7.4.4</a> for calculation of the value |

#### 7.4.3.7 Thermal Reference Data

This section is reserved for future use.

##### 7.4.3.7.1 RES8: Reserved 8

This location is reserved. Writes to this register have no effect.

| Offset: 70h |             |
|-------------|-------------|
| Bit         | Description |
| 7:0         | RESERVED 8  |

##### 7.4.3.7.2 RES9: Reserved 9

This location is reserved. Writes to this register have no effect.

| Offset: 71h-72h |             |
|-----------------|-------------|
| Bit             | Description |
| 15:0            | RESERVED 9  |

##### 7.4.3.7.3 TRDCKS: Thermal Reference Data Checksum

This location provides the checksum of the Thermal Reference Data Section. Writes to this register have no effect.

| Offset: 73h |                                                                                                                                                                              |
|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Bit         | Description                                                                                                                                                                  |
| 7:0         | <b>Thermal Reference Data Checksum</b><br>One Byte Checksum of the Thermal Reference Section<br><br>00h- FFh: See <a href="#">Section 7.4.4</a> for calculation of the value |



### 7.4.3.8 Feature Data

This section provides information on key features that the platform may need to understand without powering on the processor.

#### 7.4.3.8.1 Processor Core Feature Flags

This location contains a copy of results in EDX[31:0] from Function 1 of the CPUID instruction. These details provide instruction and feature support by product family. A decode of these bits is found in the *AP-485 Intel® Processor Identification and CPUID Instruction* application note. Writes to this register have no effect.

**Example:** A value of BFEFBFFh can be found at offset 74 - 77h.

| Offset: 74h-77h |                                                            |
|-----------------|------------------------------------------------------------|
| Bit             | Description                                                |
| 31:0            | Processor Core Feature Flags<br>0000h-FFFFh: Feature Flags |

#### 7.4.3.8.2 Processor Feature Flags

This location contains additional feature information from the processor. Writes to this register have no effect.

**Note:** Bit 5 and Bit 6 are mutually exclusive (only one bit will be set).

| Offset: 78h |                                                                                   |
|-------------|-----------------------------------------------------------------------------------|
| Bit         | Description                                                                       |
| 7           | Multi-Core (set if the processor is a multi core processor)                       |
| 6           | Serial signature (set if there is a serial signature at offset 4D - 54h)          |
| 5           | Electronic signature present (set if there is a electronic signature at 4D - 54h) |
| 4           | Thermal Sense Device present (set if an SMBus thermal sensor on package)          |
| 3           | Reserved                                                                          |
| 2           | OEM EEPROM present (set if there is a scratch ROM at offset 80 - FFh)             |
| 1           | Core VID present (set if there is a VID provided by the processor)                |
| 0           | L3 Cache present (set if there is a level 3 cache on the processor)               |

Bits are set when a feature is present, and cleared when they are not.

**Example:** A value of A6h can be found at offset 78h.

#### 7.4.3.8.3 Processor Thread and Core Information

This location contains information regarding the number of cores and threads on the processor. Writes to this register have no effect.

**Example:** The Intel® Xeon® Processor 7200 Series and 7300 Series has two or four cores and one thread per core.



| Offset: 79h |                            |
|-------------|----------------------------|
| Bit         | Description                |
| 7:2         | Number of cores            |
| 1:0         | Number of threads per core |

#### 7.4.3.8.4 Additional Processor Feature Flags

This location contains additional feature information for the processor. This field is defined as follows: Writes to this register have no effect.

| Offset: 7Ah |                                       |
|-------------|---------------------------------------|
| Bit         | Description                           |
| 7           | Reserved                              |
| 6           | Intel® Cache Safe Technology          |
| 5           | Extended Halt State (C1E)             |
| 4           | Intel® Virtualization Technology      |
| 3           | Execute Disable                       |
| 2           | Intel® 64                             |
| 1           | Thermal Monitor 2                     |
| 0           | Enhanced Intel Speed Step® Technology |

Bits are set when a feature is present, and cleared when they are not.

#### 7.4.3.8.5 Thermal Adjustment Factors

This location contains information on thermal adjustment factors for the processor. This field and its details are pending and will be updated in a future revision. Writes to this register have no effect.

| Offset: 7Bh-7Ch |                               |
|-----------------|-------------------------------|
| Bit             | Description                   |
| 15:8            | Measurement Correction Factor |
| 7:0             | Temperature Target            |

#### 7.4.3.9 Other Data

These locations are reserved. Writes to this register have no effect.

| Offset: 7Dh-7Eh |             |
|-----------------|-------------|
| Bit             | Description |
| 15:0            | RESERVED    |

#### 7.4.3.9.1 FDCKS: Feature Data Checksum

This location provides the checksum of the Feature Data Section. Writes to this register have no effect.



|                    |                                                                                                                                                               |
|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Offset:</b> 7Fh |                                                                                                                                                               |
| <b>Bit</b>         | <b>Description</b>                                                                                                                                            |
| 7:0                | <b>Feature Data Checksum</b><br>One Byte Checksum of the Feature Data Section<br><br>00h- FFh: See <a href="#">Section 7.4.4</a> for calculation of the value |

## 7.4.4 Checksums

The PIROM includes multiple checksums. [Table 7-7](#) includes the checksum values for each section defined in the 128 byte ROM.

**Table 7-7. 128 Byte ROM Checksum Values**

| Section             | Checksum Address |
|---------------------|------------------|
| Header              | 0Dh              |
| Processor Data      | 15h              |
| Processor Core Data | 24h              |
| Cache Data          | 31h              |
| Package Data        | 37h              |
| Part Number Data    | 6Fh              |
| Thermal Ref. Data   | 73h              |
| Feature Data        | 7Fh              |

Checksums are automatically calculated and programmed by Intel. The first step in calculating the checksum is to add each byte from the field to the next subsequent byte. This result is then negated to provide the checksum.

**Example:** For a byte string of AA445Ch, the resulting checksum will be B6h.

AA = 10101010      44 = 01000100      5C = 0101100

AA + 44 + 5C = 01001010

Negate the sum: 10110101 + 1 = **101101 (B6h)**

## 7.4.5 Scratch EEPROM

Also available in the memory component on the processor SMBus is an EEPROM which may be used for other data at the system or processor vendor's discretion. The data in this EEPROM, once programmed, can be write-protected by asserting the active-high SM\_WP signal. This signal has a weak pull-down (10 kΩ) to allow the EEPROM to be programmed in systems with no implementation of this signal. The Scratch EEPROM resides in the upper half of the memory component (addresses 80 - FFh). The lower half comprises the Processor Information ROM (addresses 00 - 7Fh), which is permanently write-protected by Intel.





## 8 Boxed Processor Specifications

---

### 8.1 Introduction

The Intel® Xeon® Processor 7200 Series and 7300 Series is also offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from baseboards and standard components. The boxed processor will not be supplied with a cooling solution. Future revisions may have solutions that differ from those discussed here.

### 8.2 Thermal Specifications

Please see [Chapter 6](#) for the the cooling requirements of the boxed processor.

#### 8.2.1 Boxed Processor Cooling Requirements

A suitable heatsink is required to properly cool the boxed processor. However, meeting the processor's temperature specifications is also a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specification is found in [Section 6.1.1](#) of this document.





## 9 Debug Tools Specifications

---

### 9.1 Debug Port System Requirements

The Intel® Xeon® Processor 7200 Series and 7300 Series debug port is the command and control interface for the In-Target Probe (ITP) debugger. The ITP enables run-time control of the processors for system debug. The debug port, which is connected to the FSB, is a combination of the system JTAG and execution signals. There are several mechanical, electrical and functional constraints on the debug port that must be followed. The mechanical constraint requires the debug port connector to be installed in the system with adequate physical clearance. Electrical constraints exist due to the mixed high and low speed signals of the debug port for the processor. While the JTAG signals operate at a maximum of 75 MHz, the execution signals operate at the common clock FSB frequency. The functional constraint requires the debug port to use the JTAG system via a handshake and multiplexing scheme.

In general, the information in this chapter may be used as a basis for including all run-control tools in Intel® Xeon® Processor 7200 Series and 7300 Series-based systems designs including tools from vendors other than Intel.

**Note:** The debug port and JTAG signal chain must be designed into the processor board to utilize the XDP for debug purposes except for interposer solutions.

### 9.2 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging Intel® Xeon® Processor 7200 Series and 7300 Series systems. Tektronix and Agilent should be contacted to obtain specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Intel® Xeon® Processor 7200 Series and 7300 Series-based multiprocessor systems, the LAI is critical in providing the ability to probe and capture FSB signals. There are two sets of considerations to keep in mind when designing a Intel® Xeon® Processor 7200 Series and 7300 Series-based system that can make use of an LAI: mechanical and electrical.

#### 9.2.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI plugs into the socket, while the processor plugs into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. In some cases, it is known that some of the electrolytic capacitors fall inside of the keepout volume for the LAI. In this case, it is necessary to move these capacitors to the backside of the board before using the LAI. Additionally, note that it is possible that the keepout volume reserved for the LAI may include different requirements from the space normally occupied by the heatsink. If this is the case, the logic analyzer vendor will provide either a cooling solution as part of the LAI or additional hardware to mount the existing cooling solution.



### 9.2.2 Electrical Considerations

The LAI will also affect the electrical performance of the FSB, therefore it is critical to obtain electrical load models from each of the logic analyzer vendors to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

§