FAIRCHILD

August 2014

FDMC7696

N-Channel PowerTrench® MOSFET

30 V, 12 A, 11.5 mΩ

Features

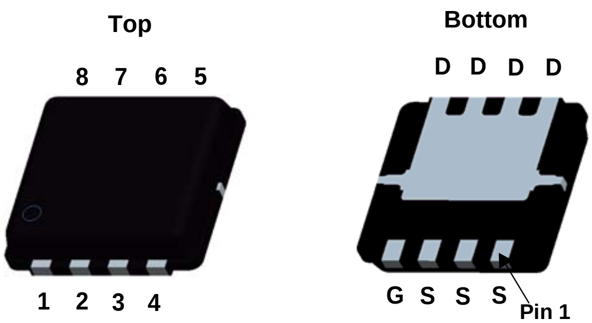
- Max $r_{DS(on)}$ = 11.5 mΩ at V_{GS} = 10 V, I_D = 12 A
- Max $r_{DS(on)}$ = 14.5 mΩ at V_{GS} = 4.5 V, I_D = 10 A
- High performance technology for extremely low $r_{DS(on)}$
- Termination is Lead-free and RoHS Compliant

General Description

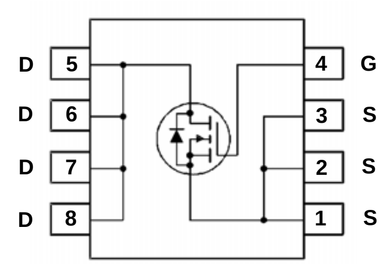
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance.This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Applications

- DC/DC Buck Converters
- Notebook battery power management
- Load Switch in Notebook



MLP 3.3x3.3



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	±20	V
I_D	Drain Current -Continuous (Package limited) T_C = 25°C	20	A
	-Continuous (Silicon limited) T_C = 25°C	38	
	-Continuous T_A = 25°C (Note 1a)	12	
	-Pulsed	50	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	21	mJ
P_D	Power Dissipation T_C = 25°C	25	W
	Power Dissipation T_A = 25°C (Note 1a)	2.4	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

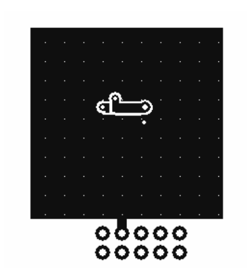
Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7696	FDMC7696	MLP 3.3x3.3	13 ”	12 mm	3000 units

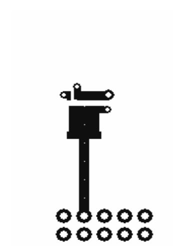
Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30			V
BV_{DSST}	Drain to Source Breakdown Voltage Transient	V_{GS} = 0 V, Transient=100 ns	33			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		14		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.2	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 12 A		8.5	11.5	mΩ
		V_{GS} = 4.5 V, I_D = 10 A		11.5	14.5	
		V_{GS} = 10 V, I_D = 12 A, T_J = 125 °C		11.6	15.7	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 12 A		45		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz		1075	1430	pF
C_{oss}	Output Capacitance			380	505	pF
C_{rss}	Reverse Transfer Capacitance			40	55	pF
R_g	Gate Resistance		0.2	1.0	2.0	Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 12 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		9	18	ns
t_r	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			19	33	ns
t_f	Fall Time			2	10	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 15 V, I_D = 12 A		16	22	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 5 V		8	11	nC
Q_{gs}	Gate to Source Charge			3.2		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.8		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.9 A (Note 2)		0.75	1.2	V
		V_{GS} = 0 V, I_S = 12 A (Note 2)		0.84	1.2	
t_{rr}	Reverse Recovery Time	I_F = 12 A, di/dt = 100 A/μs		25	40	ns
Q_{rr}	Reverse Recovery Charge			9	18	nC

Notes:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 21 mJ is based on starting T_J = 25 °C, L = 0.3 mH, I_{AS} = 12 A, V_{DD} = 27 V, V_{GS} = 10 V.
4. As an N-ch device, the negative Vgs rating is for low duty cycle pulse ocurrence only. No continuous rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

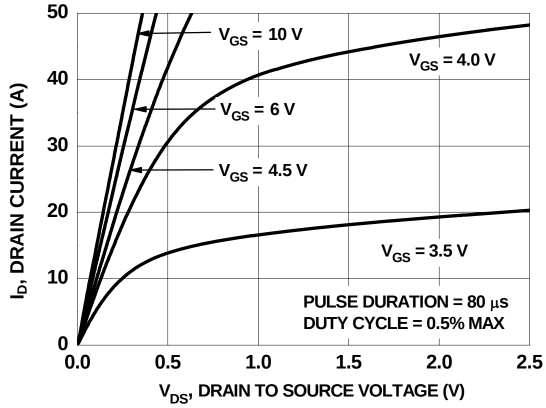


Figure 1. On Region Characteristics

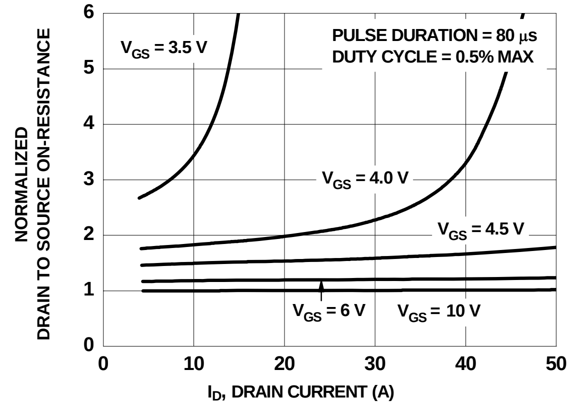


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

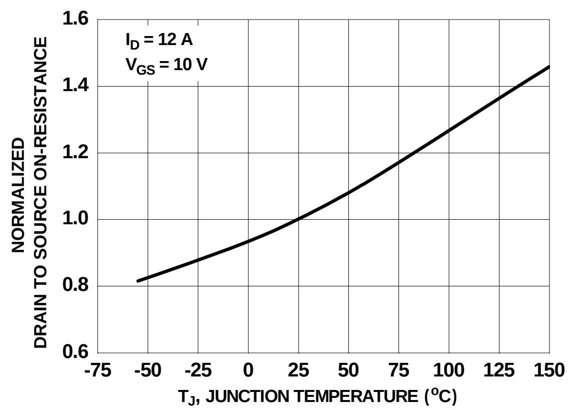


Figure 3. Normalized On Resistance vs Junction Temperature

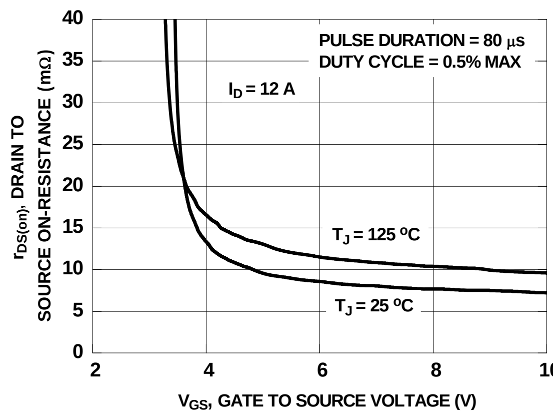


Figure 4. On-Resistance vs Gate to Source Voltage

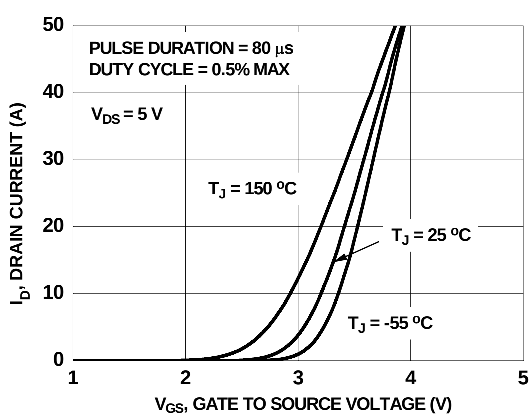


Figure 5. Transfer Characteristics

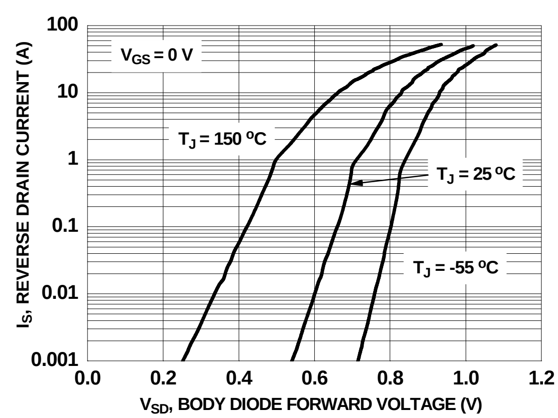


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

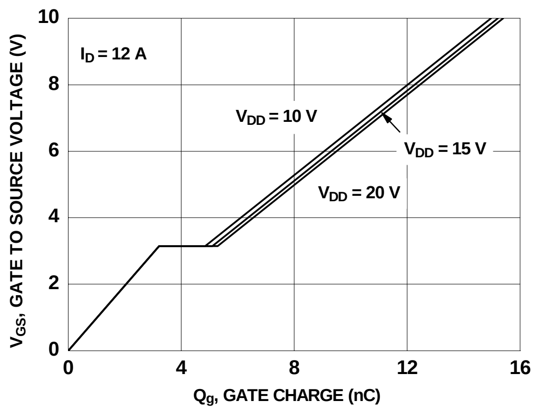


Figure 7. Gate Charge Characteristics

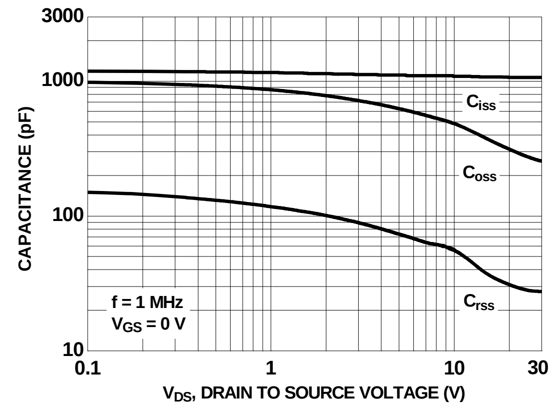


Figure 8. Capacitance vs Drain to Source Voltage

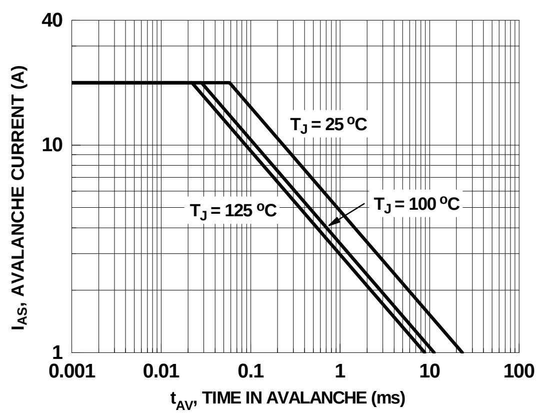


Figure 9. Unclamped Inductive Switching Capability

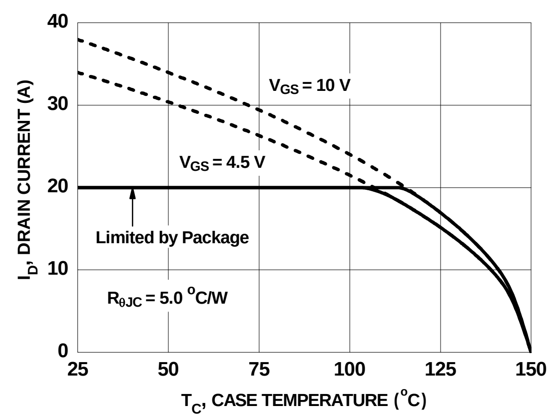


Figure 10. Maximum Continuous Drain Current vs Case Temperature

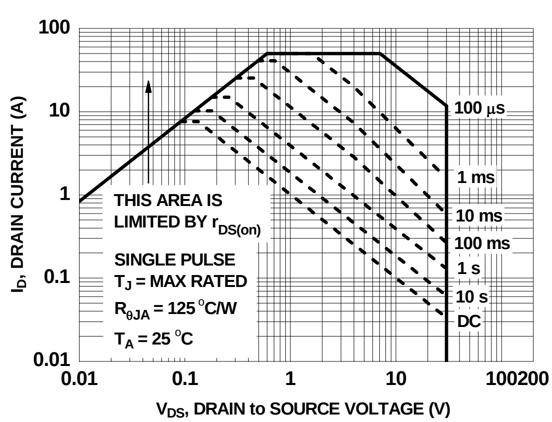


Figure 11. Forward Bias Safe Operating Area

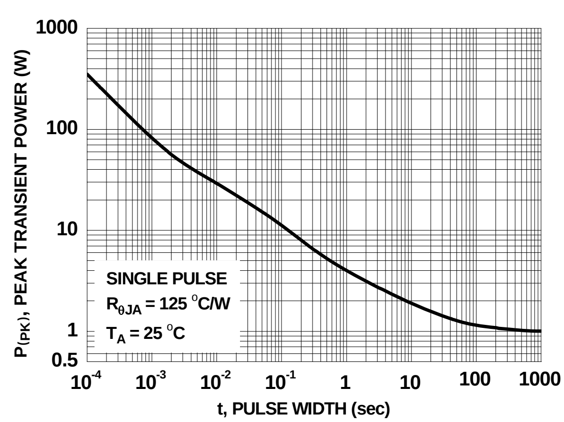


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

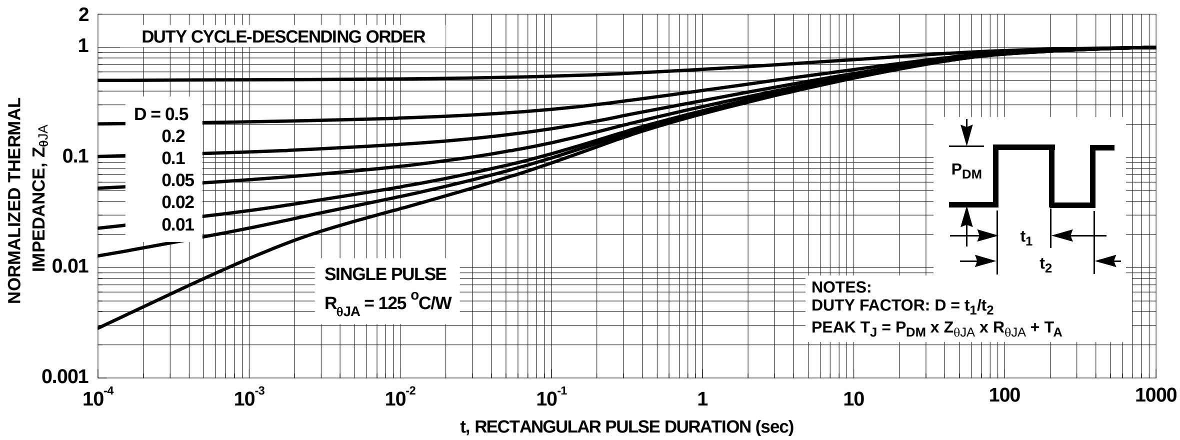
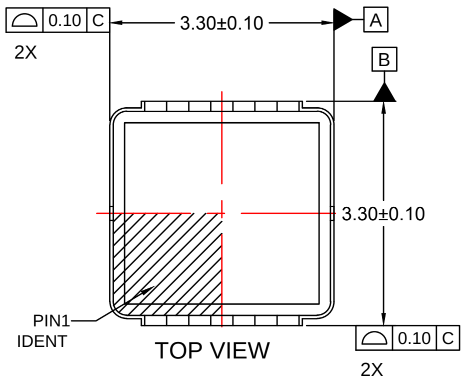
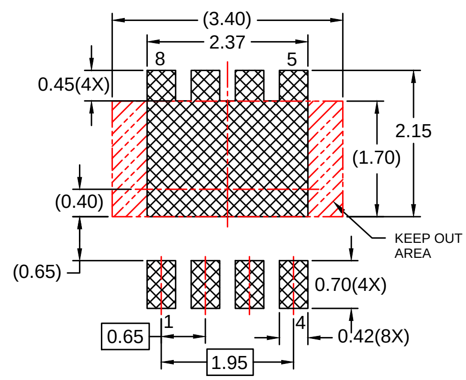


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

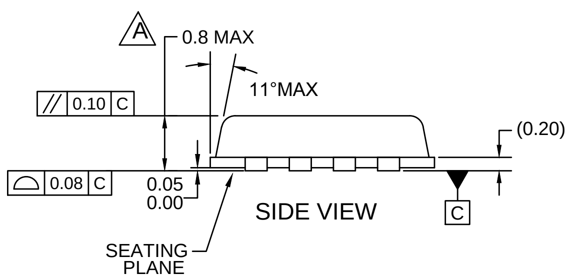
Dimensional Outline and Pad Layout



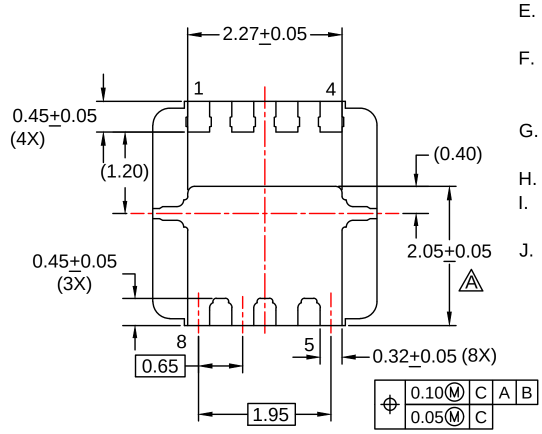
TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. EXCEPT AS NOTED, PACKAGE CONFORMS TO JEDEC REGISTRATION MO-240 VARIATION BA..

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY

E. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS.

F. FLANGE DIMENSIONS INCLUDE INTERTERMINAL FLASH OR PROTRUSION. INTERTERMINAL FLASH OR PROTRUSION SHALL NOT EXCEED 0.25MM PER SIDE.

G. IT IS RECOMMENDED TO HAVE NO TRACES OR VIA WITHIN THE KEEP OUT AREA.

H. DRAWING FILENAME: MKT-MLP08Trev3.

I. GENERAL RADII FOR ALL CORNERS SHALL BE 0.20MM MAX.

J. FAIRCHILD SEMICONDUCTOR.

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SuperSOT™-6
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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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