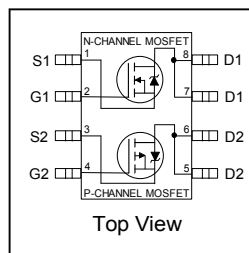


Features

- Advanced Planar Technology
- Ultra Low On-Resistance
- Logic Level Gate Drive
- Dual N and P Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- 150°C Operating Temperature
- Lead-Free, RoHS Compliant
- Automotive Qualified *

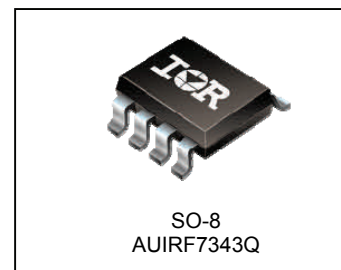


	N-CH	P-CH
V_{DS}	55V	-55V
$R_{DS(on)}$ typ.	0.043Ω	0.095Ω
max.	0.050Ω	0.105Ω
I_D	4.7A	-3.4A

Description

Specifically designed for Automotive applications, these HEXFET® Power MOSFET's in a Dual SO-8 package utilize the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of these Automotive qualified HEXFET Power MOSFET's are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

The efficient SO-8 package provides enhanced thermal characteristics and dual MOSFET die capability making it ideal in a variety of power applications. This dual, surface mount SO-8 can dramatically reduce board space and is also available in Tape & Reel.



G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF7343Q	SO-8	Tape and Reel	4000	AUIRF7343QTR

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.		Units
		N-Channel	P-Channel	
V _{DS}	Drain-Source Voltage	55	-55	V
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	4.7	-3.4	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	3.8	-2.7	
I _{DM}	Pulsed Drain Current ①	38	-27	
P _D @T _A = 25°C	Maximum Power Dissipation ⑤	2.0		W
P _D @T _A = 70°C	Maximum Power Dissipation ⑤	1.3		
E _{AS}	Single Pulse Avalanche Energy (Thermally Limited) ③	72	114	mJ
I _{AR}	Avalanche Current	4.7	-3.4	A
E _{AR}	Repetitive Avalanche Energy	0.20		mJ
V _{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	-5.0	V/ns
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑤	—	62.5	°C/W

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*Qualification standards can be found at www.infineon.com

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
		P-Ch	-55	—	—		$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.059	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
		P-Ch	—	0.054	—		Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	N-Ch	—	0.043	0.050	Ω	$V_{GS} = 10V, I_D = 4.7A$ ④
			—	0.056	0.065		$V_{GS} = 4.5V, I_D = 3.8A$ ④
		P-Ch	—	0.095	0.105		$V_{GS} = -10V, I_D = -3.4A$ ⑤
			—	0.150	0.170		$V_{GS} = -4.5V, I_D = -2.7A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		P-Ch	-1.0	—	—		$V_{DS} = V_{GS}, I_D = -250\mu A$
gfs	Forward Trans conductance	N-Ch	7.9	—	—	S	$V_{DS} = 10V, I_D = 4.5A$ ④
		P-Ch	3.3	—	—		$V_{DS} = -10V, I_D = -3.1A$ ④
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	2.0	μA	$V_{DS} = 55V, V_{GS} = 0V$
		P-Ch	—	—	-2.0		$V_{DS} = -55V, V_{GS} = 0V$
		N-Ch	—	—	25		$V_{DS} = 55V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
		P-Ch	—	—	-25		$V_{DS} = -55V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	± 100	nA	$V_{GS} = \pm 20V$
	Gate-to-Source Reverse Leakage	N-P	—	—	± 100		$V_{GS} = \pm 20V$

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

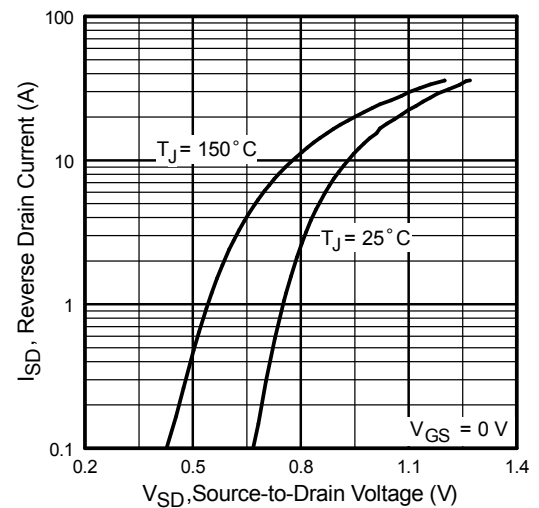
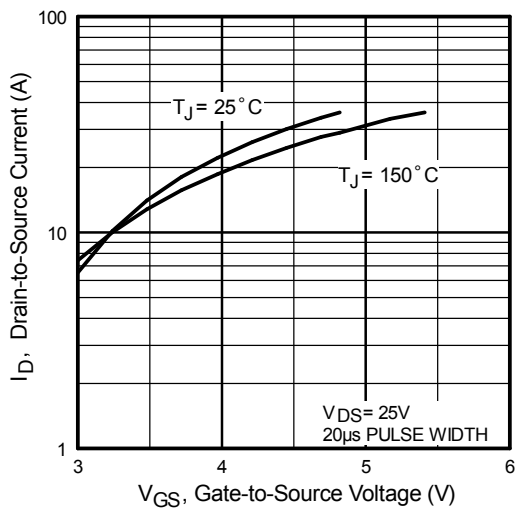
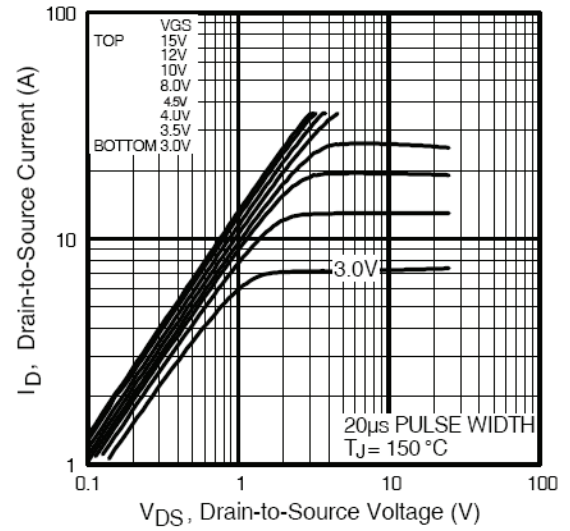
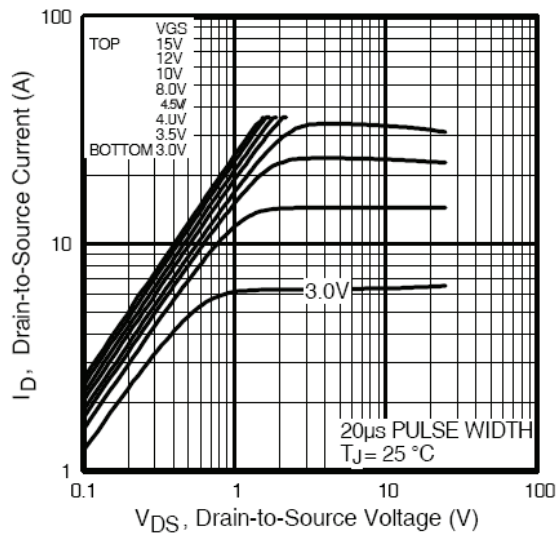
Q_g	Total Gate Charge	N-Ch	—	24	36	nC	N-Channel $I_D = 4.5A, V_{DS} = 44V, V_{GS} = 10V$ ④
		P-Ch	—	26	38		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	2.3	3.4	nC	P-Channel $I_D = -3.1A, V_{DS} = -44V, V_{GS} = -10V$
		P-Ch	—	3.0	4.5		
Q_{gd}	Gate-to-Drain Charge	N-Ch	—	7.0	10	nC	P-Channel $I_D = -3.1A, V_{DS} = -44V, V_{GS} = -10V$
		P-Ch	—	8.4	13		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	8.3	12	ns	N-Channel $V_{DD} = 28V, I_D = 1.0A, R_G = 6.0\Omega, R_D = 28\Omega$ ④
		P-Ch	—	14	22		
t_r	Rise Time	N-Ch	—	3.2	4.8	ns	P-Channel $V_{DD} = -28V, I_D = -1.0A, R_G = 6.0\Omega, R_D = 28\Omega$ ④
		P-Ch	—	10	15		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	32	48	ns	P-Channel $V_{DD} = -28V, I_D = -1.0A, R_G = 6.0\Omega, R_D = 28\Omega$ ④
		P-Ch	—	43	64		
t_f	Fall Time	N-Ch	—	13	20	ns	P-Channel $V_{DD} = -28V, I_D = -1.0A, R_G = 6.0\Omega, R_D = 28\Omega$ ④
		P-Ch	—	22	32		
C_{iss}	Input Capacitance	N-Ch	—	740	—	pF	N-Channel $V_{GS} = 0V, V_{DS} = 25V, f = 1.0\text{MHz}$
		P-Ch	—	690	—		
C_{oss}	Output Capacitance	N-Ch	—	190	—	pF	P-Channel $V_{GS} = 0V, V_{DS} = -25V, f = 1.0\text{MHz}$
		P-Ch	—	210	—		
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	71	—	pF	P-Channel $V_{GS} = 0V, V_{DS} = -25V, f = 1.0\text{MHz}$
		P-Ch	—	86	—		

Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	2.0	A	
		P-Ch	—	—	-2.0		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	38	A	
		P-Ch	—	—	-27		
V_{SD}	Diode Forward Voltage	N-Ch	—	0.70	1.2	V	$T_J = 25^\circ\text{C}, I_S = 2.0A, V_{GS} = 0V$ ④
		P-Ch	—	-0.80	-1.2		$T_J = 25^\circ\text{C}, I_S = -2.0A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	N-Ch	—	60	90	ns	N-Channel $T_J = 25^\circ\text{C}, I_F = 2.0A, di/dt = 100A/\mu s$
		P-Ch	—	54	80		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	120	170	nC	P-Channel $T_J = 25^\circ\text{C}, I_F = -2.0A, di/dt = 100A/\mu s$ ④
		P-Ch	—	85	130		

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 22)
- ② N-Channel $I_{SD} \leq 4.7A, di/dt \leq 220A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$.
P-Channel $I_{SD} \leq -3.4A, di/dt \leq -150A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
- ③ N-Channel Starting $T_J = 25^\circ\text{C}, L = 6.5\text{mH}, R_G = 25\Omega, I_{AS} = 4.7A$.
P-Channel Starting $T_J = 25^\circ\text{C}, L = 20\text{mH}, R_G = 25\Omega, I_{AS} = -3.4A$.
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Surface mounted on FR-4 board, $t \leq 10\text{sec}$.



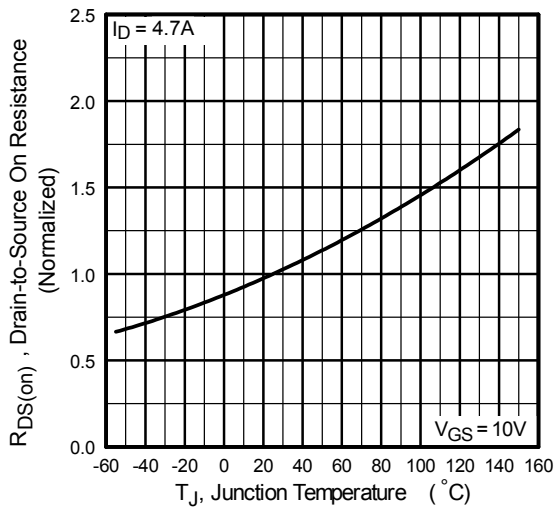


Fig 5. Normalized On-Resistance Vs. Temperature

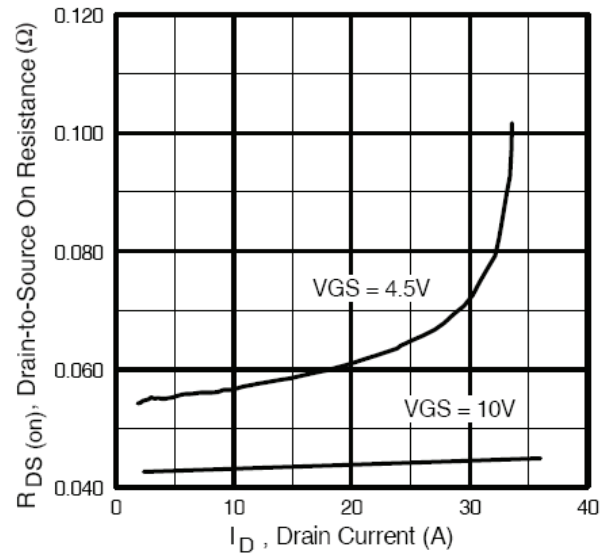


Fig 6. Typical On-Resistance Vs. Drain Current

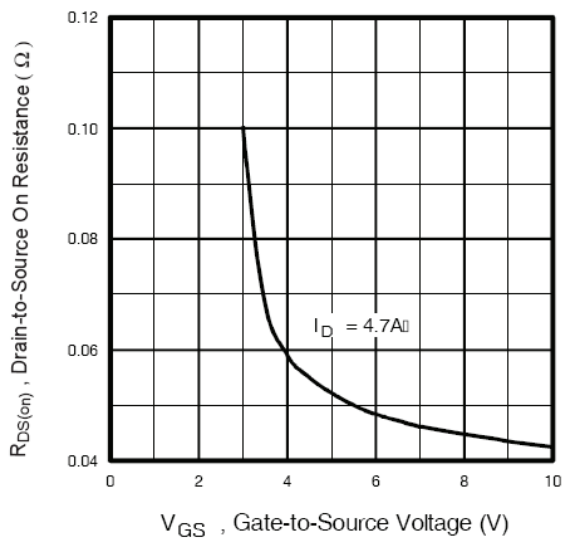


Fig. 7 Typical On-Resistance Vs. Gate Voltage

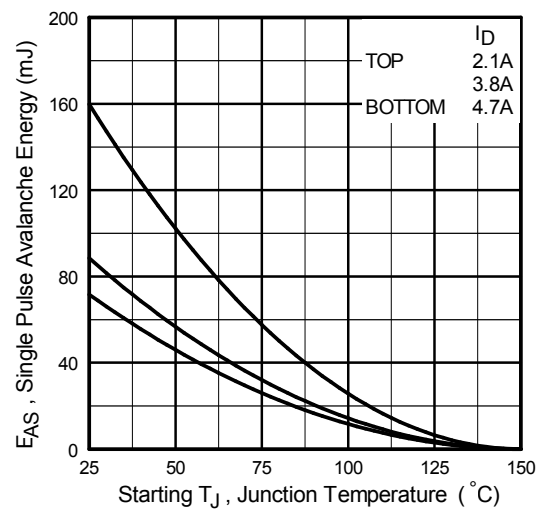


Fig 8. Maximum Avalanche Energy Vs. Drain Current

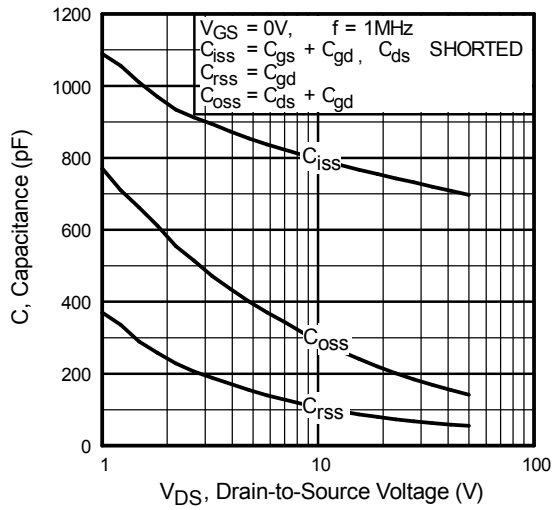


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

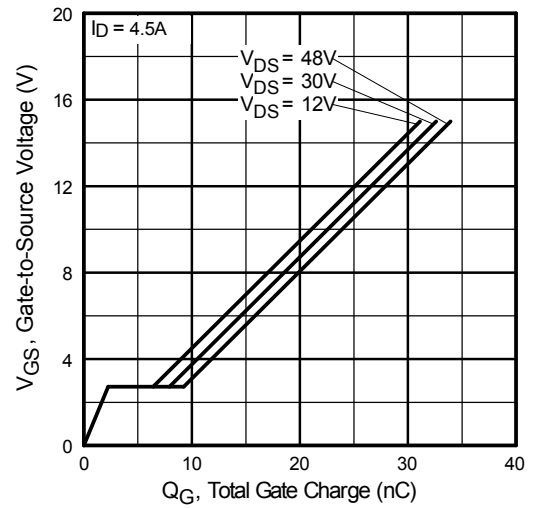


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

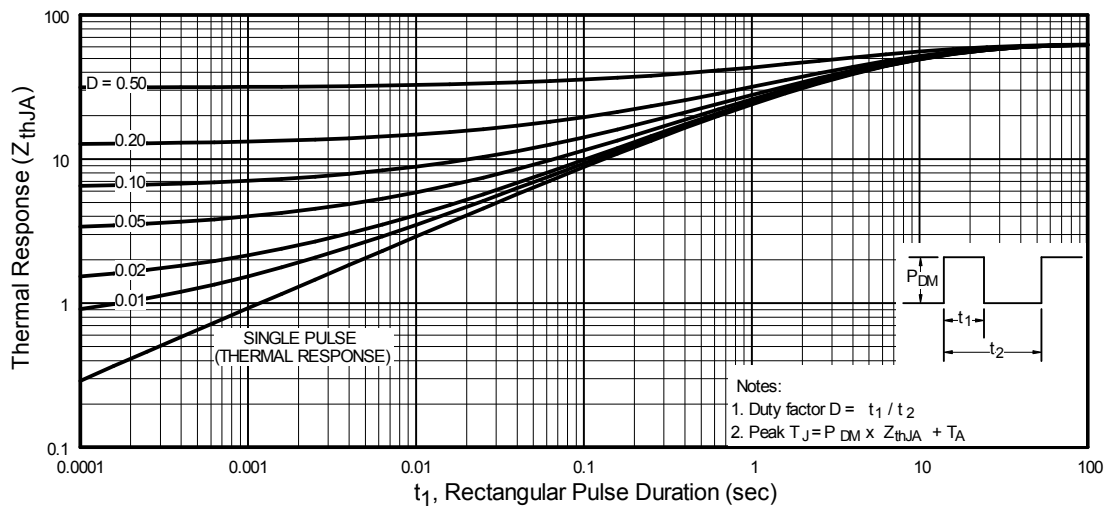


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

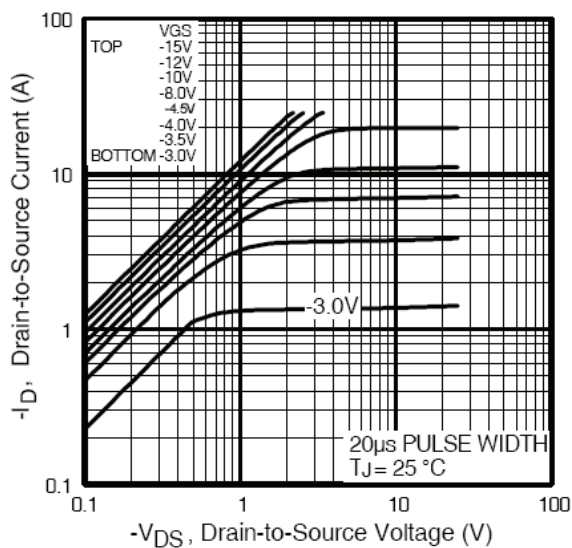


Fig. 12 Typical Output Characteristics

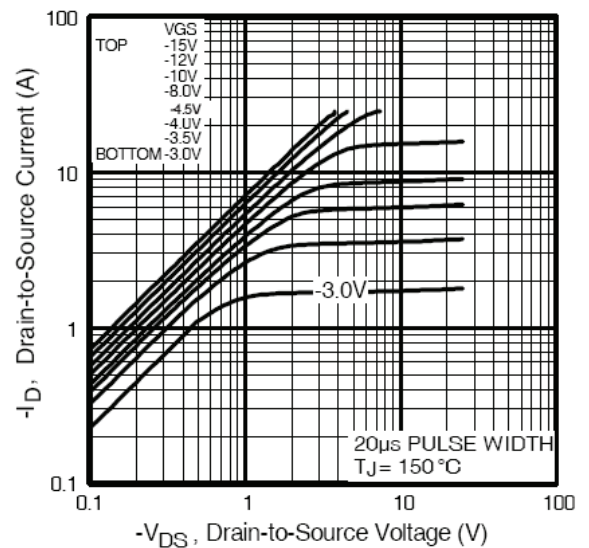


Fig. 13 Typical Output Characteristics

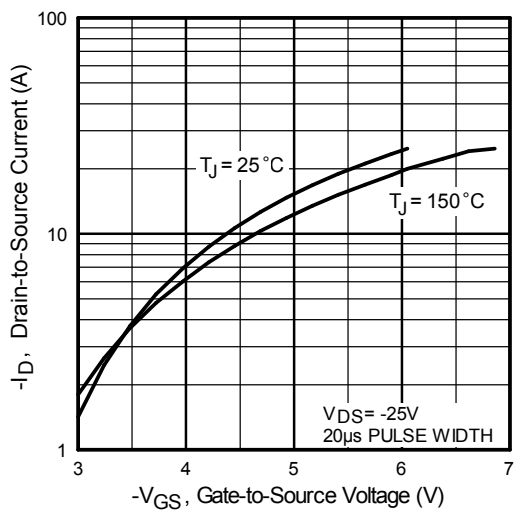


Fig. 14 Typical Transfer Characteristics

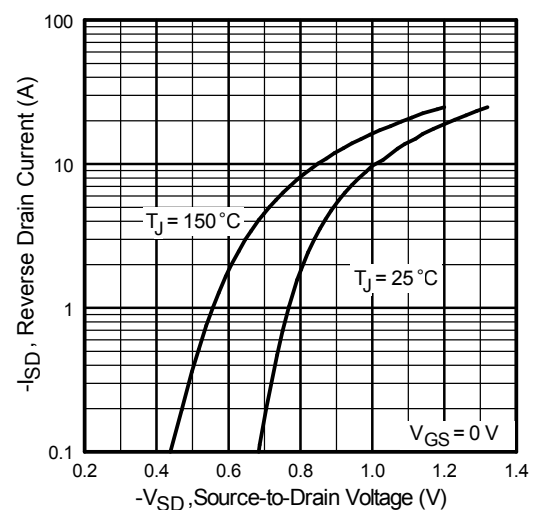


Fig. 15 Typical Source-Drain Diode Forward Voltage

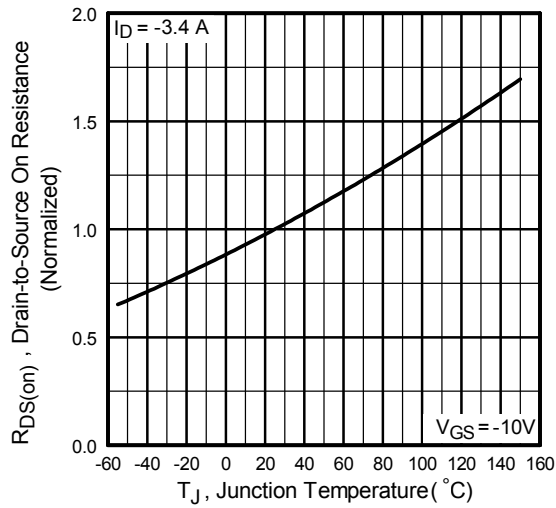


Fig 16. Normalized On-Resistance Vs. Temperature

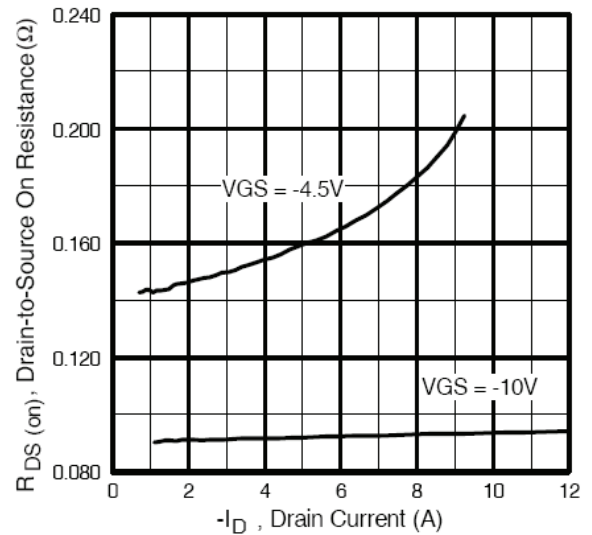


Fig 17. Typical On-Resistance Vs. Drain Current

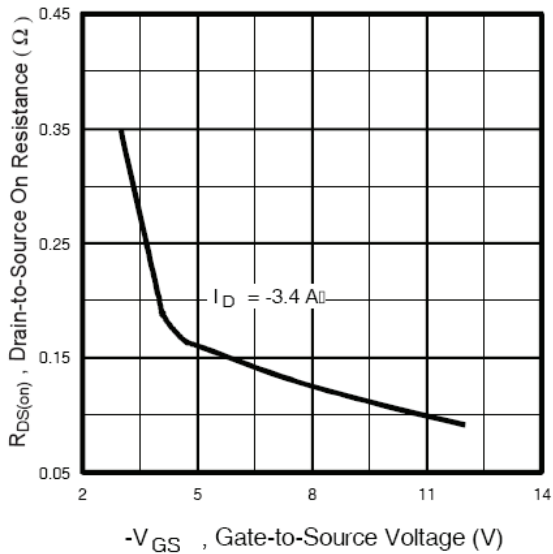


Fig. 18 Typical On-Resistance Vs. Gate Voltage

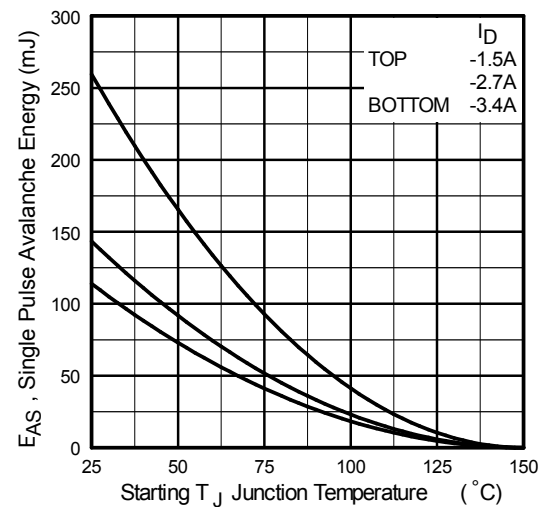


Fig 19. Maximum Avalanche Energy Vs. Drain Current

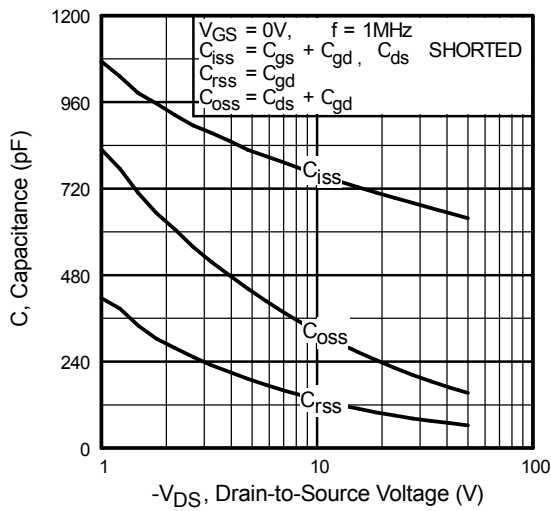


Fig 20. Typical Capacitance Vs. Drain-to-Source Voltage

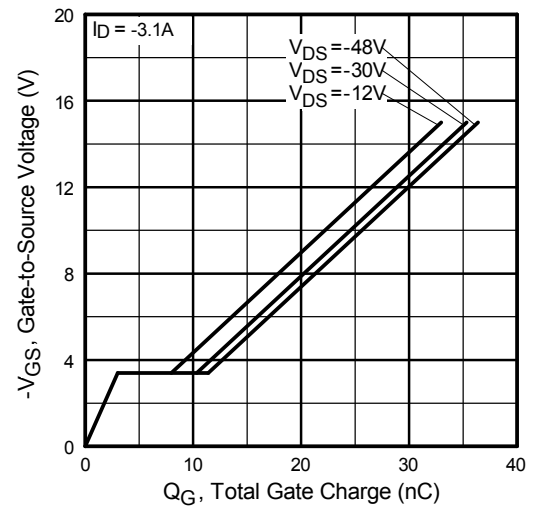


Fig 21. Typical Gate Charge Vs. Gate-to-Source Voltage

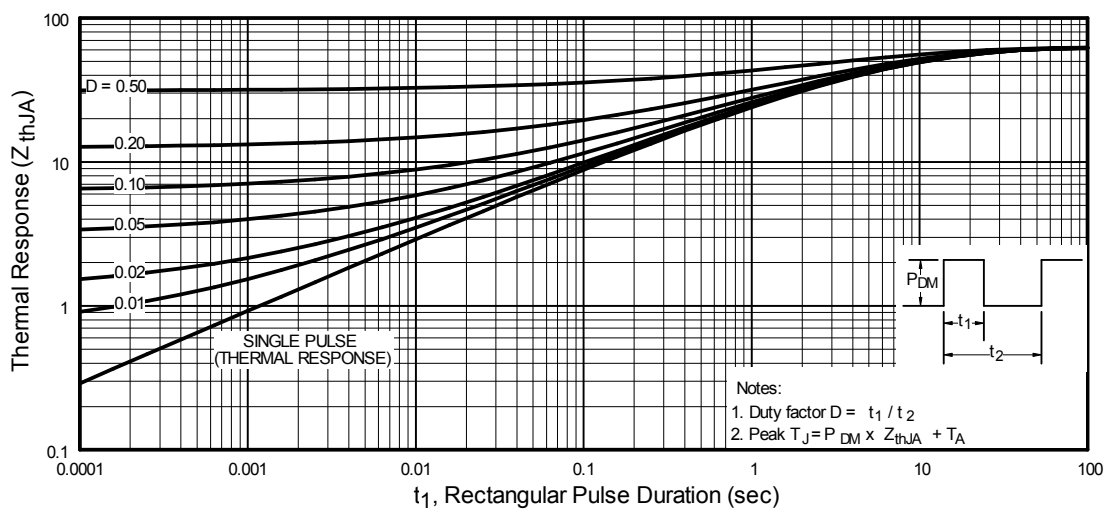
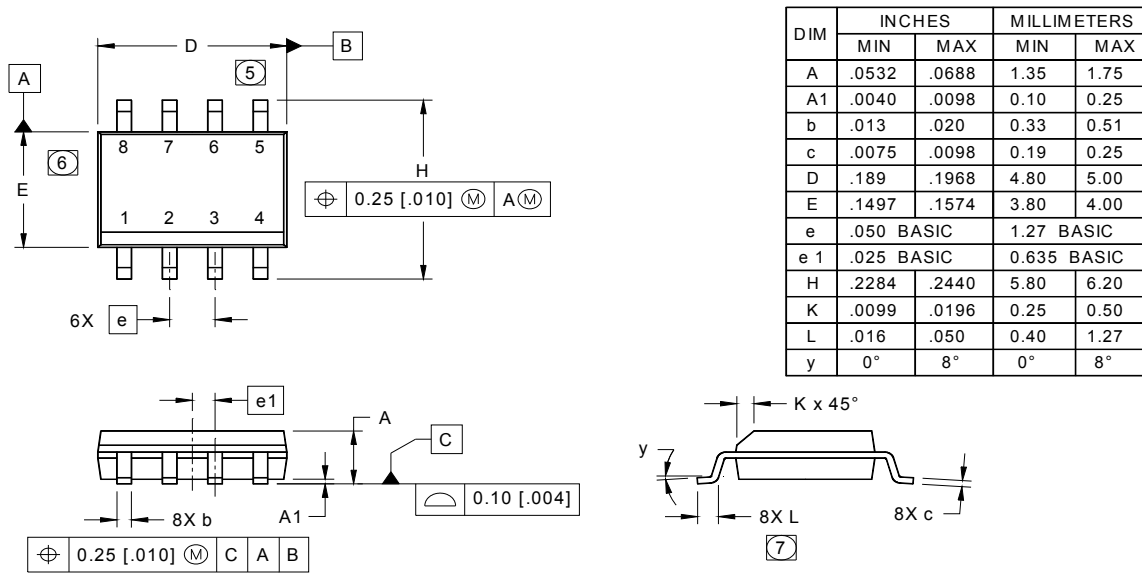
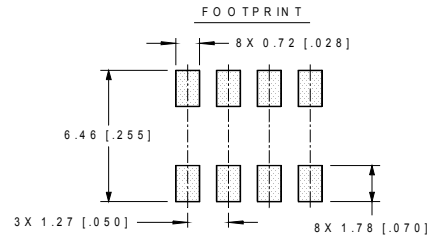


Fig 22. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

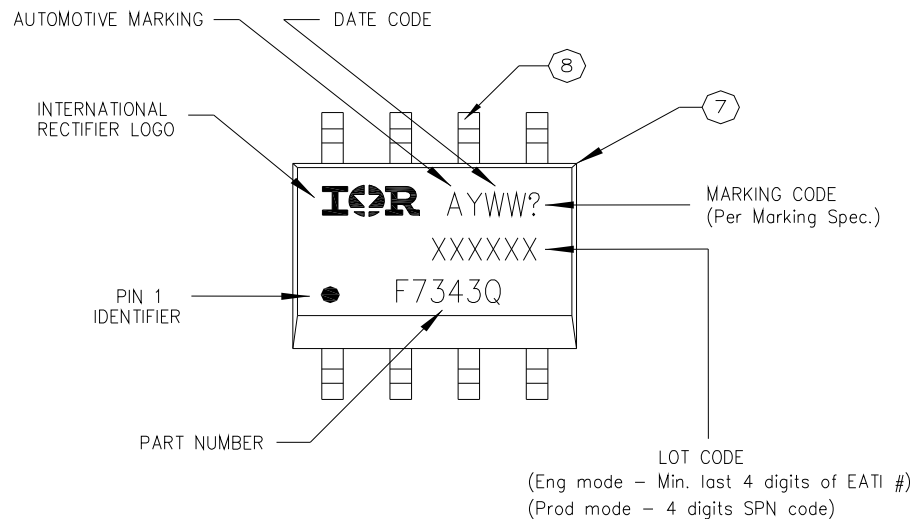
SO-8 Package Outline (Dimensions are shown in millimeters (inches))

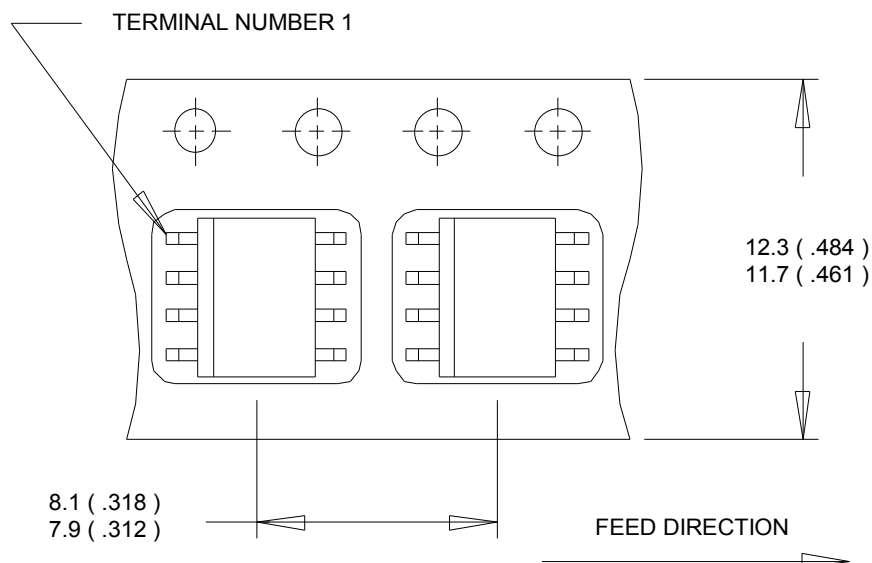


- NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M -1994.
 2. CONTROLLING DIMENSION: MILLIMETER
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
 5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
 6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
 7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

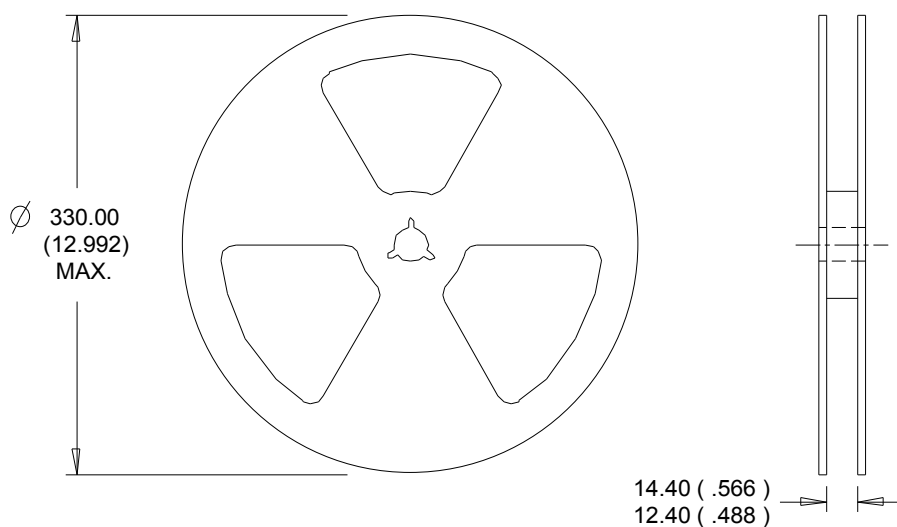


SO-8 Part Marking Information



SO-8 Tape and Reel (Dimensions are shown in millimeters (inches))

NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SO-8	MSL1
ESD	Machine Model	Class M2 (+/- 200V) [†] AEC-Q101-002	
	Human Body Model	Class H1A (+/- 500V) [†] AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
3/10/2014	- Added "Logic Level Gate Drive" bullet in the features section on page 1 - Updated data sheet with new IR corporate template
9/30/2015	- Updated datasheet with corporate template - Corrected ordering table on page 1.

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