

SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

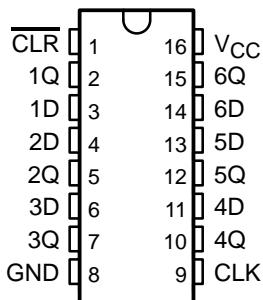
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- 'ALS174 and 'AS174 Contain Six Flip-Flops With Single-Rail Outputs
- 'ALS175 and 'AS175B Contain Four Flip-Flops With Double-Rail Outputs
- Buffered Clock and Direct-Clear Inputs
- Applications Include:
 - Buffer/Storage Registers
 - Shift Registers
 - Pattern Generators
- Fully Buffered Outputs for Maximum Isolation From External Disturbances ('AS Only)

SN54ALS174 . . . J OR W PACKAGE

SN54AS174 . . . J PACKAGE

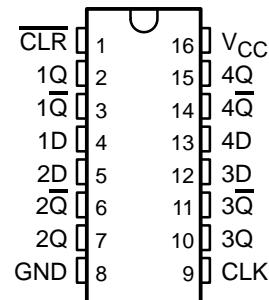
SN74ALS174, SN74AS174 . . . D, N, OR NS PACKAGE
(TOP VIEW)



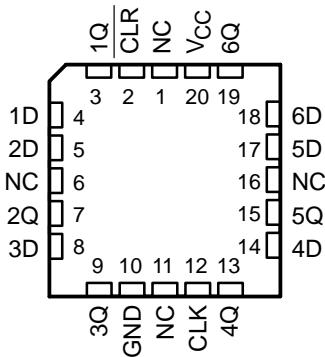
SN54ALS175 . . . J OR W PACKAGE

SN54AS175B . . . J PACKAGE

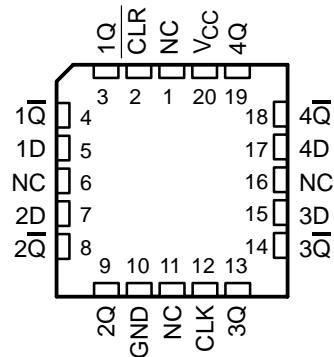
SN74ALS175, SN74AS175B . . . D, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS174, SN54AS174 . . . FK PACKAGE
(TOP VIEW)



SN54ALS175 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct-clear (CLR) input. The 'ALS175 and 'AS175B feature complementary outputs from each flip-flop.

Information at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock (CLK) input is at either the high or low level, the D-input signal has no effect at the output.

These circuits are fully compatible for use with most TTL circuits.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

**SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B
SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR**

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ORDERING INFORMATION

TA	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP - N	Tube	SN74ALS174N	SN74ALS174N
			SN74AS174N	SN74AS174N
			SN74ALS175N	SN74ALS175N
			SN74AS175BN	SN74AS175BN
	SOIC - D	Tube	SN74ALS174D	ALS174
		Tape and reel	SN74ALS174DR	
		Tube	SN74AS174D	AS174
		Tape and reel	SN74AS174DR	
		Tube	SN74ALS175D	ALS175
		Tape and reel	SN74ALS175DR	
		Tube	SN74AS175BD	AS175B
		Tape and reel	SN74AS175BDR	
	SOP - NS	Tape and reel	SN74ALS174NSR	ALS174
			SN74AS174NSR	74AS174
			SN74ALS175NSR	ALS175
			SN74AS175BNSR	74AS175B
-55°C to 125°C	CDIP - J	Tube	SNJ54ALS174J	SNJ54ALS174J
			SNJ54AS174J	SNJ54AS174J
			SNJ54ALS175J	SNJ54ALS175J
			SNJ54AS175BJ	SNJ54AS175BJ
	CFP - W	Tube	SNJ54ALS174W	SNJ54ALS174W
			SNJ54ALS175W	SNJ54ALS175W
	LCCC - FK	Tube	SNJ54ALS174FK	SNJ54ALS174FK
			SNJ54AS174FK [‡]	SNJ54AS174FK
			SNJ54ALS175FK	SNJ54ALS175FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

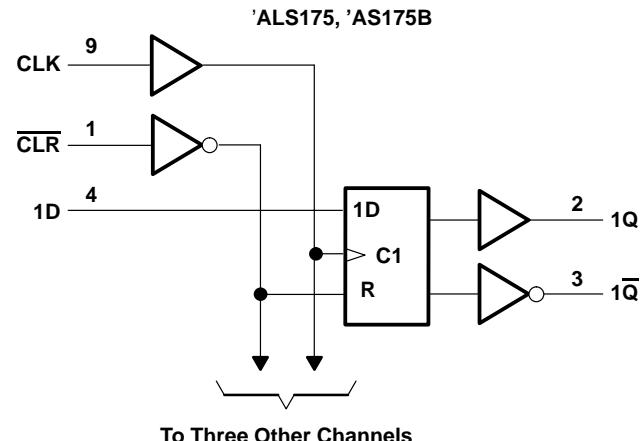
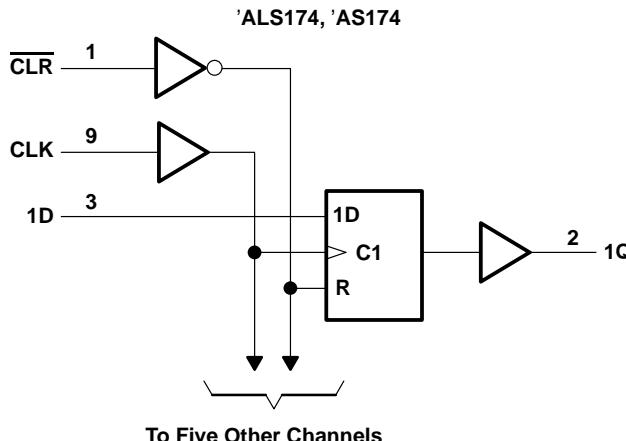
[‡] This orderable is not recommended for new designs.

**FUNCTION TABLE
(each flip-flop)**

INPUTS			OUTPUTS	
CLR	CLK	D	Q	\bar{Q} [§]
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\bar{Q}_0

[§] 'ALS175 and 'AS175B only

logic diagrams (positive logic)



Pin numbers shown are for the D, J, N, NS, and W packages.

absolute maximum ratings over operating free-air temperature range, SN54/74ALS174,
SN54/74ALS175 (unless otherwise noted)[†]

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JEDEC 51-7.

recommended operating conditions (see Note 2)

		SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2			2		V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-0.4			-0.4	mA
I _{OL}	Low-level output current			4			8	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B
SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS174 SN54ALS175			SN74ALS174 SN74ALS175			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.5			-1.5		V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} -2			V _{CC} -2			V
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 4 mA	0.25	0.4	0.25	0.4		V
		I _{OL} = 8 mA			0.35	0.5		
I _I	V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1		mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V		20			20		μA
I _{IL}	All others	V _{CC} = 5.5 V, CLK	-0.1		-0.1			mA
	CLK		-0.15					
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V	-20	-112	-30	-112			mA
I _{CC}	'ALS174	V _{CC} = 5.5 V, See Note 3	11	19	11	19		mA
	'ALS175		8	14	9	14		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.
NOTE 3: I_{CC} is measured with D inputs and CLR grounded, and CLK at 4.5 V.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			SN54ALS174 SN54ALS175		SN74ALS174 SN74ALS175		UNIT
			MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency			40		50	MHz
t _w	Pulse duration	CLR low	15		10		ns
		CLK high	12.5		10		
		CLK low	12.5		10		
t _{su}	Setup time before CLK↑	Data	15		10		ns
		CLR inactive	8		6		
t _h	Hold time, data after CLK↑		0		0		ns

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§		UNIT	
			SN54ALS174 SN54ALS175			
			MIN	MAX		
f _{max}			40	50	MHz	
t _{PLH}	CLR	Any Q (or \bar{Q} , 'ALS175)	3	20	ns	
t _{PHL}		Any Q (or \bar{Q} , 'ALS175)	5	30		
t _{PLH}	CLK	Any Q (or \bar{Q} , 'ALS175)	3	20	ns	
t _{PHL}		Any Q (or \bar{Q} , 'ALS175)	5	24		

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range, SN54/74AS174,
SN54/74AS175B (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Package thermal impedance, θ_{JA} (see Note 1):	
D package	73°C/W
N package	67°C/W
NS package	64°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		SN54AS174 SN54AS175B			SN74AS174 SN74AS175B			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{OH}	High-level output current			-2			-2	mA
I _{OL}	Low-level output current			20			20	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS174 SN54AS175B			SN74AS174 SN74AS175B			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V	
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V	
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 20\text{ mA}$		0.35	0.5		0.35	0.5	V	
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1			0.1	mA	
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20			20	μA	
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-0.5			-0.5	mA	
$I_O\$$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-30	-112	-30	-112			mA	
I_{CC}	'AS174			30	45		30	45	mA
	'AS175B	$V_{CC} = 5.5\text{ V}$, See Note 4		22.5	34		22.5	34	

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

§ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .
NOTE 4: I_{CC} is measured with D inputs, CLR, and CLK grounded.

**SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B
SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR**

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

				SN54AS174 SN54AS175B	SN74AS174 SN74AS175B	UNIT
		MIN	MAX	MIN	MAX	
f_{clock}^*	Clock frequency		100		100	MHz
t_w^*	Pulse duration	CLR low	5.5	5		ns
		CLK high	4	4		
		CLK low 'AS174	6	6		
		CLK low 'AS175B	5	5		
t_{su}^*	Setup time before CLK↑	Data	'AS174	4	4	ns
			'AS175B	3	3	
		CLR inactive		6	6	
t_h^*	Hold time, data after CLK↑		1	1		ns

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data, but is not production tested.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}^{\dagger}$				UNIT	
			SN54AS174		SN74AS174			
			MIN	MAX	MIN	MAX		
f_{max}^*			100		100		MHz	
t_{PLH}	CLR	Any Q	5	15	5	14	ns	
t_{PLH}	CLK	Any Q	3.5	9.5	3.5	8	ns	
t_{PHL}			4.5	11.5	4.5	10		

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data, but is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

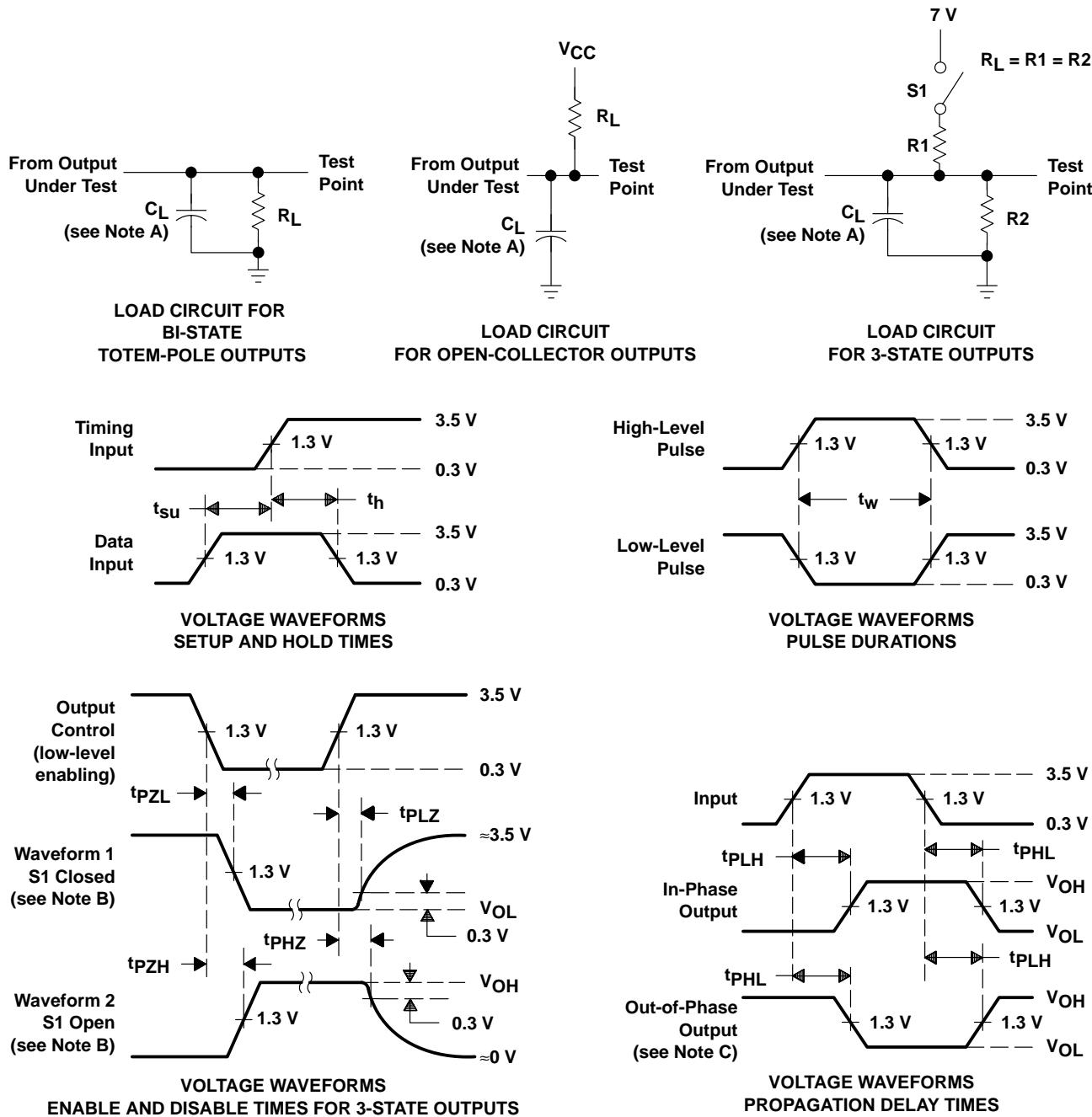
switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$ $C_L = 50 \text{ pF},$ $R_L = 500 \Omega,$ $T_A = \text{MIN to MAX}^{\dagger}$				UNIT	
			SN54AS175B		SN74AS175B			
			MIN	MAX	MIN	MAX		
f_{max}^*			100		100		MHz	
t_{PLH}	CLR	Any Q or \bar{Q}	4	10	4	9	ns	
t_{PHL}			4.5	15	4.5	13		
t_{PLH}	CLK	Any Q or \bar{Q}	3	8.5	3	7.5	ns	
t_{PHL}			3	11	3	10		

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data, but is not production tested.

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

PARAMETER MEASUREMENT INFORMATION
 SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



NOTES:

- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- When measuring propagation delay items of 3-state outputs, switch S1 is open.
- All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_f = t_r = 2$ ns, duty cycle = 50%.
- The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9553701Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9553701Q2A SNJ54AS 175BFK	Samples
5962-9553701QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9553701QE A SNJ54AS175BJ	Samples
83019012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	83019012A SNJ54ALS 174FK	Samples
8301901EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8301901EA SNJ54ALS174J	Samples
8301901FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8301901FA SNJ54ALS174W	Samples
83019022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	83019022A SNJ54ALS 175FK	Samples
8301902EA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8301902EA SNJ54ALS175J	Samples
8301902FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8301902FA SNJ54ALS175W	Samples
JM38510/37201B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 37201B2A	Samples
JM38510/37201BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 37201BEA	Samples
JM38510/37202B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 37202B2A	Samples
JM38510/37202BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 37202BEA	Samples
M38510/37201B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 37201B2A	Samples
M38510/37201BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 37201BEA	Samples
M38510/37202B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	JM38510/ 37202B2A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
M38510/37202BEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 37202BEA	Samples
SN54ALS174J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54ALS174J	Samples
SN54ALS175J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54ALS175J	Samples
SN74ALS174D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS174	Samples
SN74ALS174DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS174	Samples
SN74ALS174DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS174	Samples
SN74ALS174DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS174	Samples
SN74ALS174N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS174N	Samples
SN74ALS174N3	OBsolete	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74ALS174NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS174	Samples
SN74ALS175D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS175	Samples
SN74ALS175DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS175	Samples
SN74ALS175DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS175	Samples
SN74ALS175N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS175N	Samples
SN74ALS175NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS175N	Samples
SN74ALS175NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS175	Samples
SN74AS174D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	AS174	Samples
SN74AS174N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS174N	Samples
SN74AS174NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS174	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AS175BD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	AS175B	Samples
SN74AS175BN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS175BN	Samples
SN74AS175BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS175B	Samples
SNJ54ALS174FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	83019012A SNJ54ALS 174FK	Samples
SNJ54ALS174J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8301901EA SNJ54ALS174J	Samples
SNJ54ALS174W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8301901FA SNJ54ALS174W	Samples
SNJ54ALS175FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	83019022A SNJ54ALS 175FK	Samples
SNJ54ALS175J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8301902EA SNJ54ALS175J	Samples
SNJ54ALS175W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	8301902FA SNJ54ALS175W	Samples
SNJ54AS174FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54AS 174FK	Samples
SNJ54AS174J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ54AS174J	Samples
SNJ54AS175BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9553701Q2A SNJ54AS 175BFK	Samples
SNJ54AS175BJ	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9553701QE A SNJ54AS175BJ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54ALS174, SN54ALS175, SN54AS174, SN54AS175B, SN74ALS174, SN74ALS175, SN74AS174, SN74AS175B :

- Catalog: [SN74ALS174](#), [SN74ALS175](#), [SN74AS174](#), [SN74AS175B](#)
- Military: [SN54ALS174](#), [SN54ALS175](#), [SN54AS174](#), [SN54AS175B](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



www.ti.com

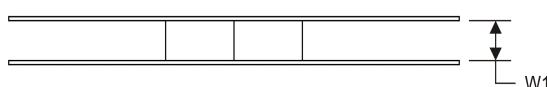
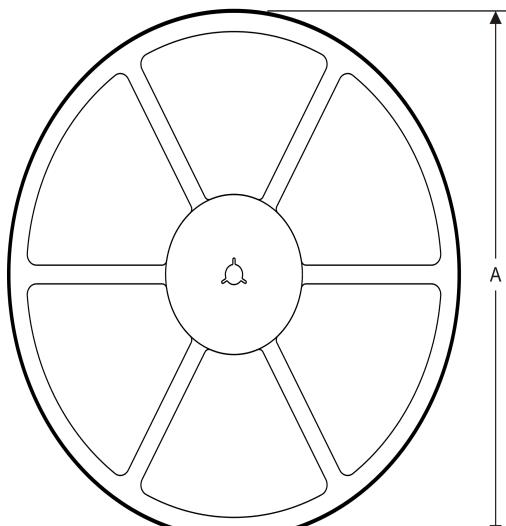
PACKAGE OPTION ADDENDUM

10-Jun-2014

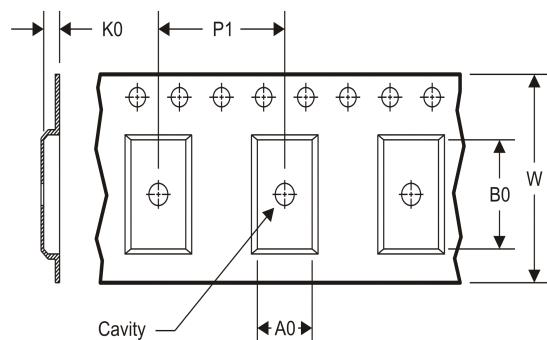
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS174DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74ALS174NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74ALS175DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74ALS175NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AS174NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AS175BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

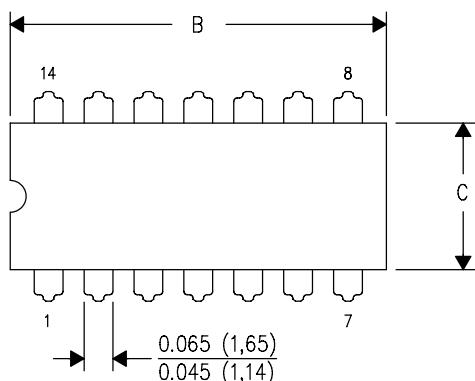

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS174DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74ALS174NSR	SO	NS	16	2000	367.0	367.0	38.0
SN74ALS175DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74ALS175NSR	SO	NS	16	2000	367.0	367.0	38.0
SN74AS174NSR	SO	NS	16	2000	367.0	367.0	38.0
SN74AS175BNSR	SO	NS	16	2000	367.0	367.0	38.0

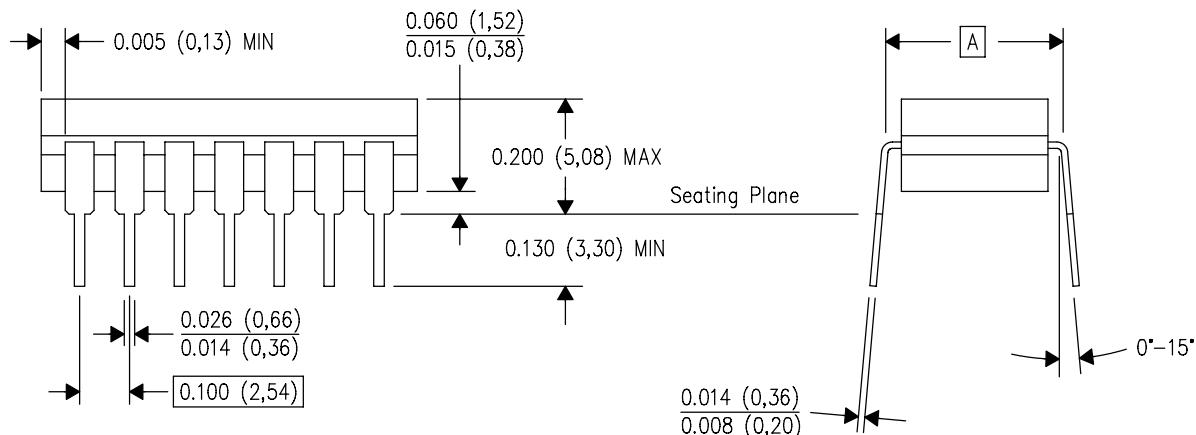
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

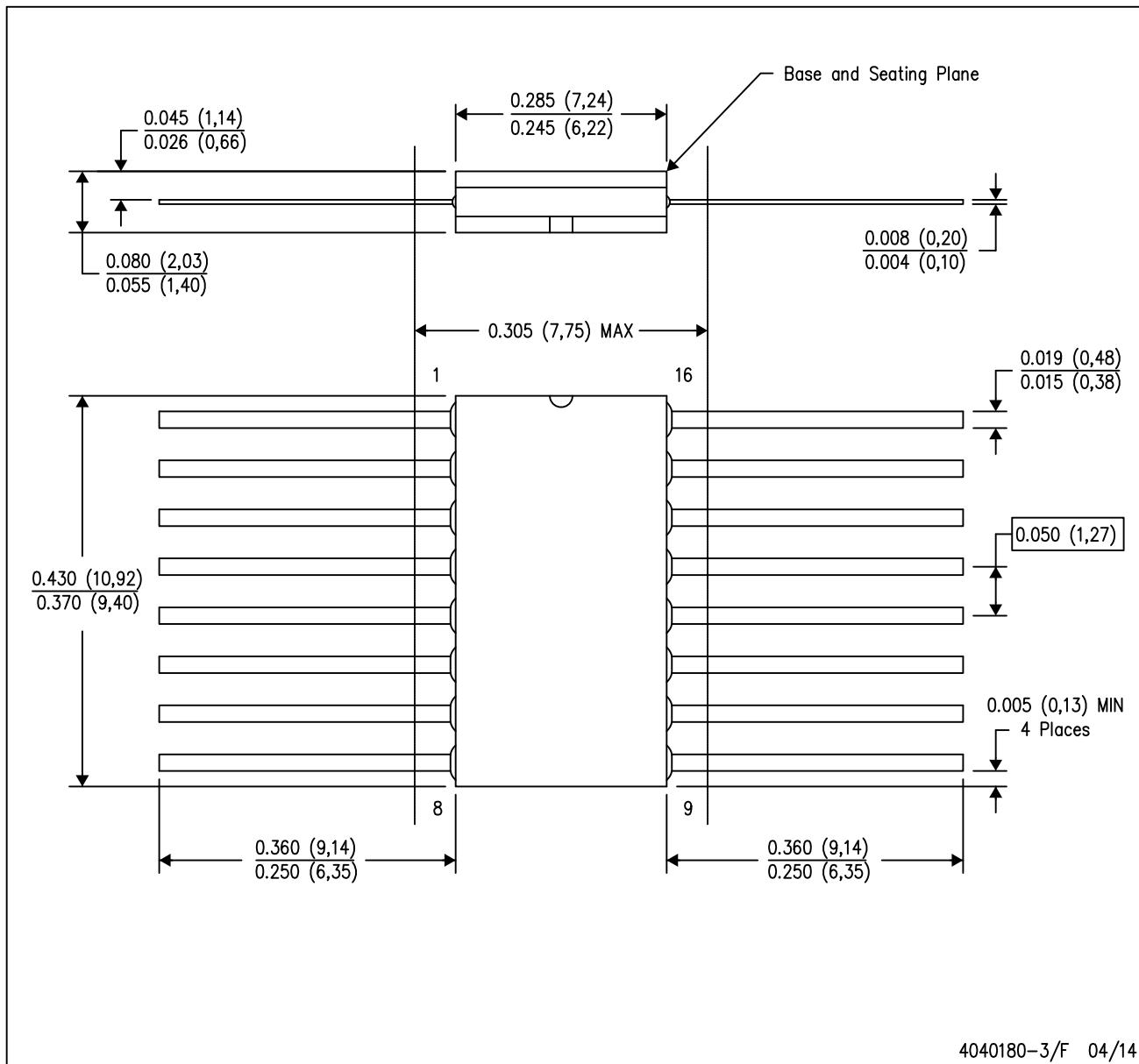


4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/F 04/14

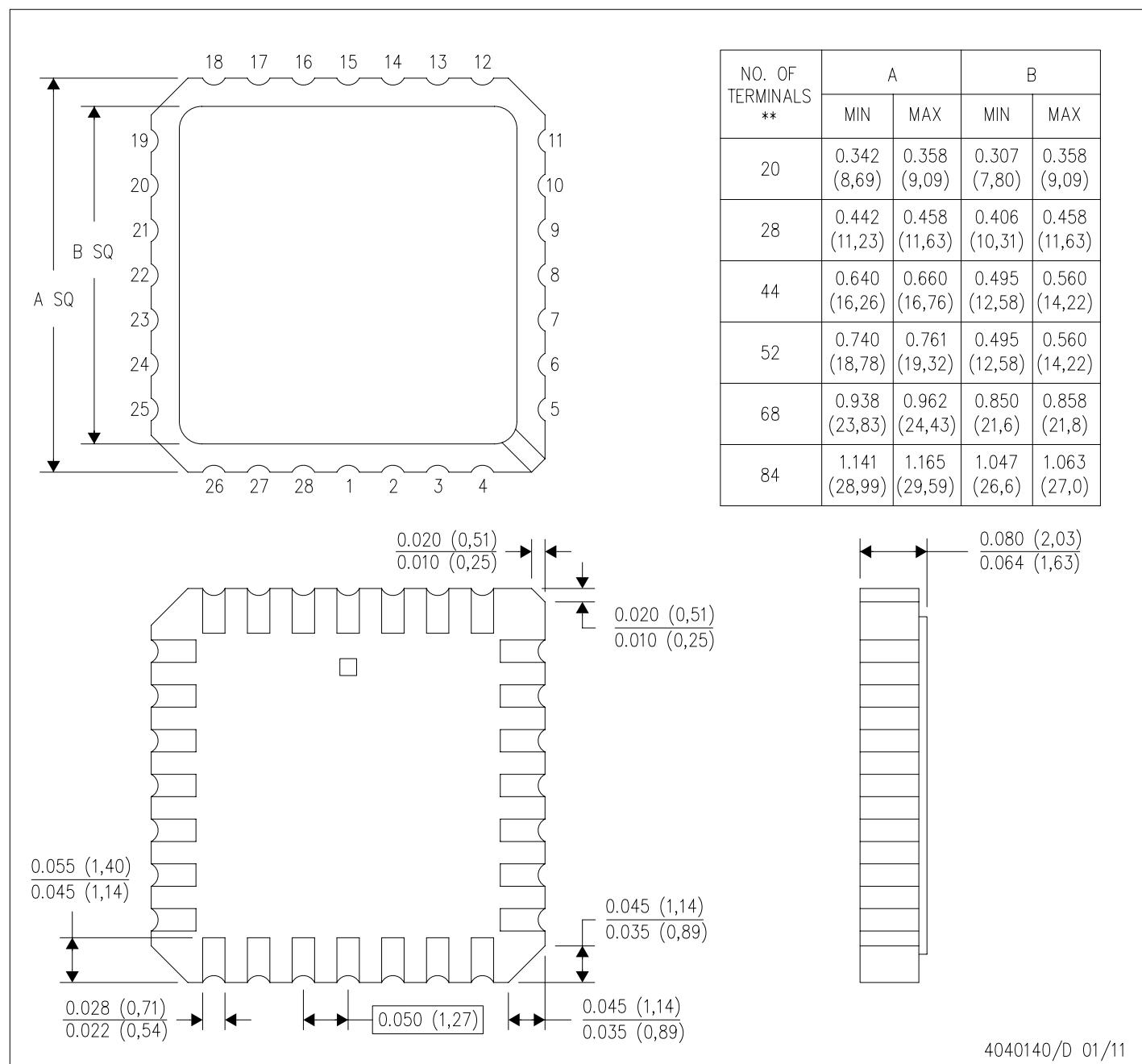
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL-STD 1835 GDFP2-F16

FK (S-CQCC-N**)

28 TERMINAL SHOWN

LEADLESS CERAMIC CHIP CARRIER



NOTES:

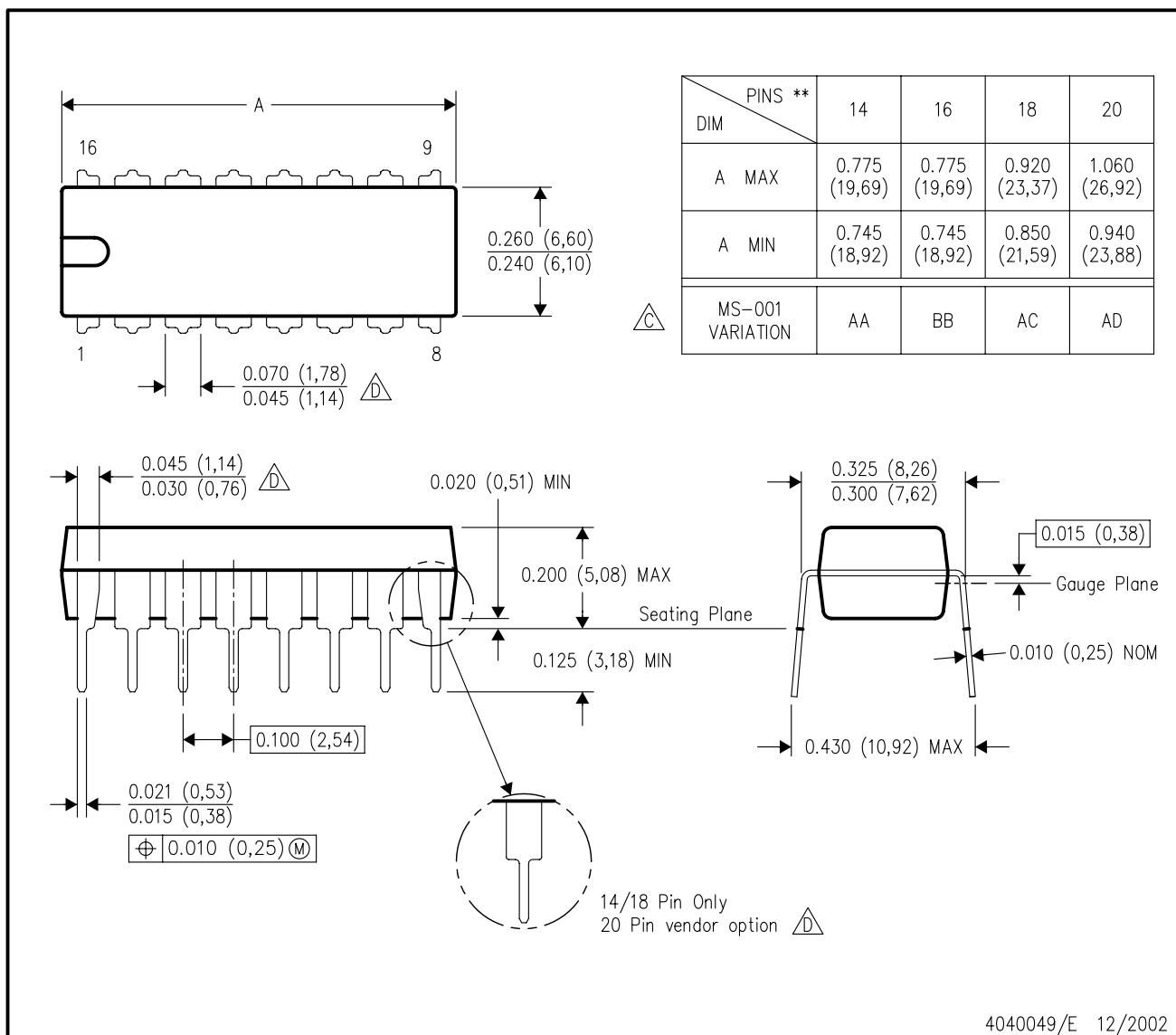
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004

4040140/D 01/11

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



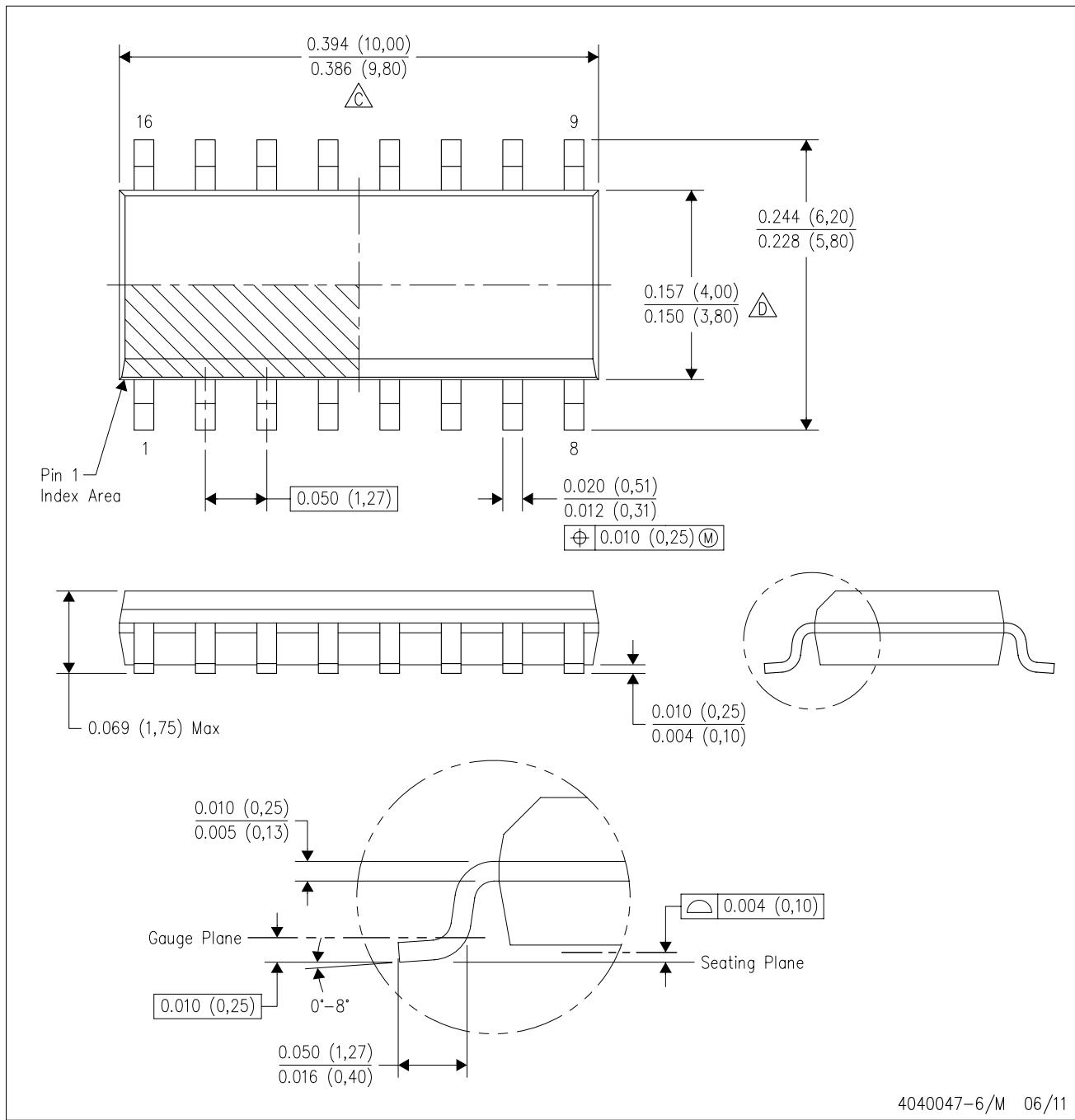
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

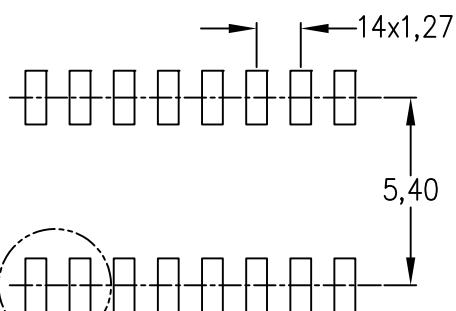
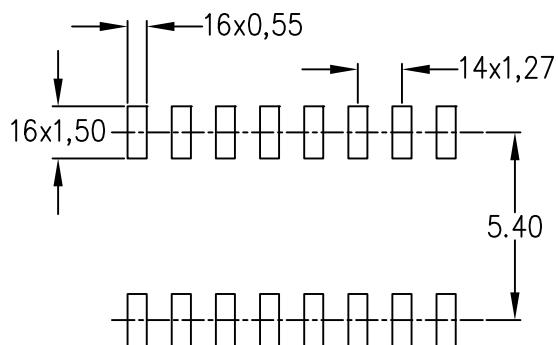
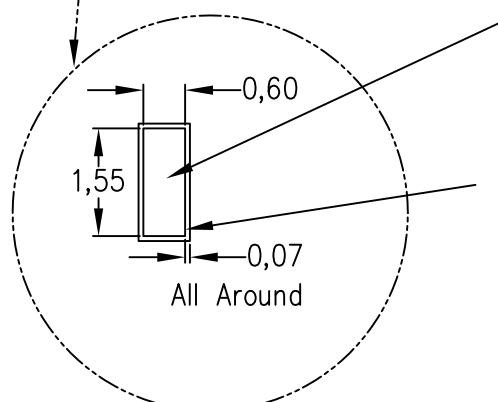
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

4211283-4/E 08/12

NOTES:

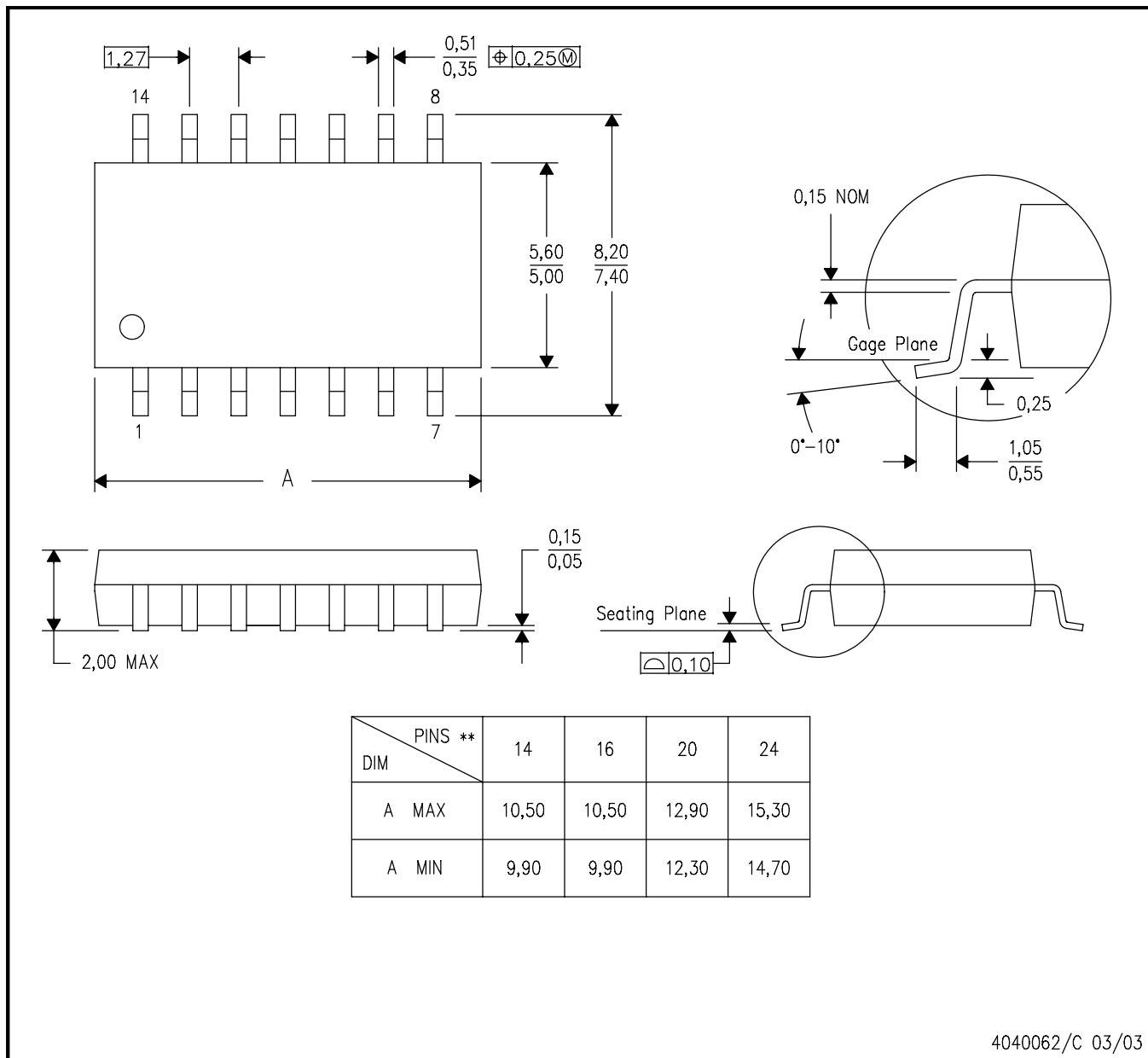
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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