



# PCAL6524

Ultra low-voltage translating 24-bit Fm+ I<sup>2</sup>C-bus/SMBus I/O expander with Agile I/O features, interrupt output and reset

Rev. 1 — 24 November 2016

Product data sheet

## 1. General description

The PCAL6524 is a 24-bit general purpose I/O expander that provides remote I/O expansion for most microcontroller families via the Fast-mode Plus (Fm+) I<sup>2</sup>C-bus interface. The ultra low-voltage interface allows for direct connection to a microcontroller operating down to 0.8 V.

NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in battery-powered mobile applications for interfacing to sensors, push buttons, keypad, etc. In addition to providing a flexible set of GPIOs, it simplifies interconnection of a processor running at one voltage level down to 0.8 V to I/O devices operating at a different voltage level 1.65 V to 5.5 V. The PCAL6524 has built-in level shifting feature that makes these devices extremely flexible in mixed power supply systems where communication between incompatible I/O voltages is required, allowing seamless communications with next-generation low voltage microprocessors and microcontrollers on the interface side (SDA/SCL) and peripherals at a higher voltage on the port side.

There are two supply voltages for PCAL6524:  $V_{DD(I2C-bus)}$  and  $V_{DD(P)}$ .  $V_{DD(I2C-bus)}$  provides the supply voltage for the interface at the master side (for example, a microcontroller) and the  $V_{DD(P)}$  provides the supply for core circuits and Port P. The bidirectional voltage level translation in the PCAL6524 is provided through  $V_{DD(I2C-bus)}$ .  $V_{DD(I2C-bus)}$  should be connected to the  $V_{DD}$  of the external SCL/SDA lines. This indicates the  $V_{DD}$  level of the I<sup>2</sup>C-bus to the PCAL6524, while the voltage level on Port P of the PCAL6524 is determined by the  $V_{DD(P)}$ .

The PCAL6524 fully meets the Fm+ I<sup>2</sup>C-bus specification at speeds to 1 MHz and implements Agile I/O, which are additional features specifically designed to enhance the I/O. These additional features are: programmable output drive strength, latchable inputs, programmable pull-up/pull-down resistors, maskable interrupt, interrupt status register, programmable open-drain or push-pull outputs.

Additional Agile I/O Plus features include I<sup>2</sup>C software reset and device ID. Interrupts can be specified by level or edge, and can be cleared individually without disturbing the other interrupt events. Also, switch debounce hardware is implemented.

At power-on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register, saving external logic gates. Programmable pull-up and pull-down resistors eliminate the need for discrete components.



The power-on reset puts the registers in their default state and initializes the I<sup>2</sup>C-bus/SMBus state machine. The  $\overline{\text{RESET}}$  pin causes the same reset/initialization to occur without depowering the part. The system master can also accomplish a reset via an I<sup>2</sup>C command and initialize all registers to their default state.

The PCAL6524 open-drain interrupt ( $\overline{\text{INT}}$ ) output is activated when any input state differs from its corresponding Input Port register state. As well, the  $\overline{\text{INT}}$  output can be specified to activate on input pin edges. There are a large number of interrupt mask functions available to maximize flexibility.

$\overline{\text{INT}}$  can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without communication via the I<sup>2</sup>C-bus. Thus, the PCAL6524 can remain a simple slave device. The input latch feature holds or latches the input pin state and keeps the logic values that created the interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

The device Port P outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

One hardware pin (ADDR) can be used to program and vary the fixed I<sup>2</sup>C-bus address and allow up to four devices to share the same I<sup>2</sup>C-bus or SMBus.

## 2. Features and benefits

- I<sup>2</sup>C-bus to parallel port expander
- 1 MHz Fast-mode Plus I<sup>2</sup>C-bus
- Operating power supply voltage range of 0.8 V to 3.6 V on the I<sup>2</sup>C-bus side
- Allows bidirectional voltage-level translation and GPIO expansion between 0.8 V to 3.6 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V, 5.5 V Port P
- Low standby current consumption: 2.0  $\mu\text{A}$  typical at 3.3 V  $V_{\text{DD(P)}}$
- Schmitt trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - ◆  $V_{\text{hys}} = 0.05 \text{ V}$  (typical) at 0.8 V
  - ◆  $V_{\text{hys}} = 0.18 \text{ V}$  (typical) at 1.8 V
  - ◆  $V_{\text{hys}} = 0.33 \text{ V}$  (typical) at 3.3 V
- 5.5 V tolerant I/O ports and 3.6 V tolerant I<sup>2</sup>C-bus pins
- Active LOW reset input ( $\overline{\text{RESET}}$ )
- Open-drain active LOW interrupt output ( $\overline{\text{INT}}$ )
- Internal power-on reset
- Noise filter on SCL/SDA inputs
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - ◆ 2000 V Human-Body Model (A114-A)
  - ◆ 1000 V Charged-Device Model (C101)
- Packages offered: TSSOP32, HUQFN32, VFBGA36

## 2.1 Agile I/O features

- Output port configuration: bank selectable or pin selectable push-pull or open-drain output stages
- Interrupt status: read-only register identifies the source of an interrupt
- Bit-wise I/O programming features:
  - ◆ Output drive strength: four programmable drive strengths to reduce rise and fall times in low-capacitance applications
  - ◆ Input latch: Input Port register values changes are kept until the Input Port register is read
  - ◆ Pull-up/pull-down enable: floating input or pull-up/pull-down resistor enable
  - ◆ Pull-up/pull-down selection: 100 k $\Omega$  pull-up/pull-down resistor selection
  - ◆ Interrupt mask: mask prevents the generation of the interrupt when input changes state to prevent spurious interrupts

## 2.2 Additional Agile I/O Plus features

- Interrupt edge specification on a bit-by-bit basis
- Interrupt individual clear without disturbing other events
- Read all interrupt events without clear
- Switch debounce hardware
- General call software reset
- I<sup>2</sup>C software Device ID function

### 3. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCAL6524HE	L6524	HUQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.56 mm	SOT1426-1
PCAL6524DR	PCAL6524	TSSOP32 <sup>[1]</sup>	plastic thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm	SOT487-1
PCAL6524EV	524	VFBGA36	plastic very fine-pitch ball grid array package, body 2.6 x 2.6 mm	SOT1851-1

[1] Under development. Please contact your local NXP sales office for availability.

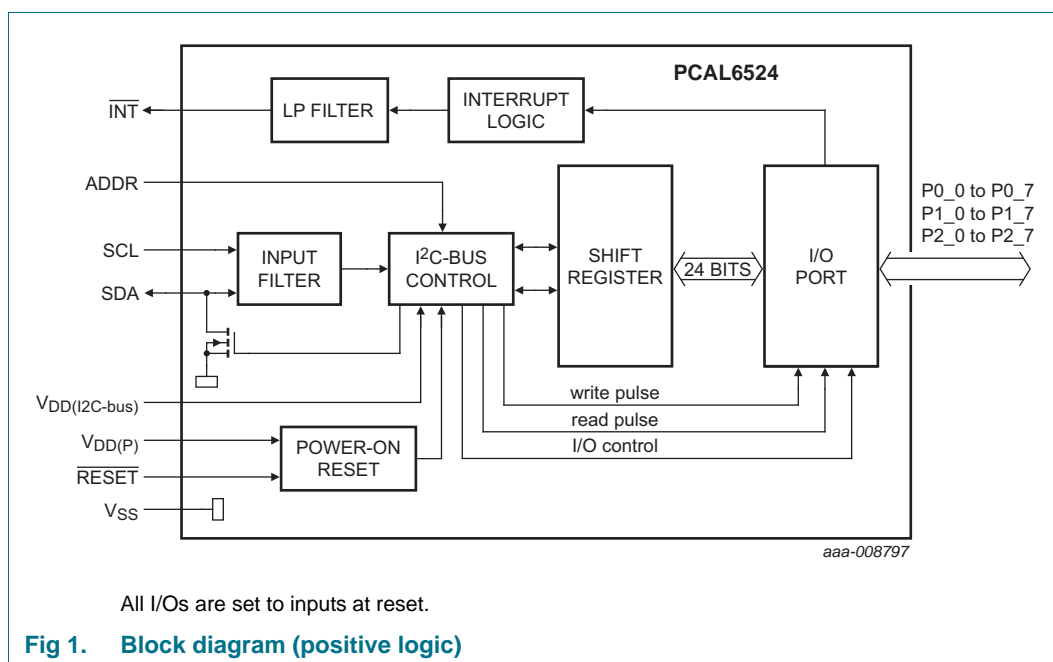
#### 3.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCAL6524HE	PCAL6524HEHP	HUQFN32	Reel 13" Q2/T3 *standard mark SMD	5000	T <sub>amb</sub> = -40 °C to +85 °C
PCAL6524DR	PCAL6524DRJ	TSSOP32 <sup>[1]</sup>	Reel 13" Q1/T1 *standard mark SMD	2500	T <sub>amb</sub> = -40 °C to +85 °C
PCAL6524EV	PCAL6524EVJ	VFBGA36	Reel 13" Q1/T1 *standard mark SMD	5000	T <sub>amb</sub> = -40 °C to +85 °C

[1] Under development. Please contact your local NXP sales office for availability.

### 4. Block diagram



5. Pinning information

5.1 Pinning

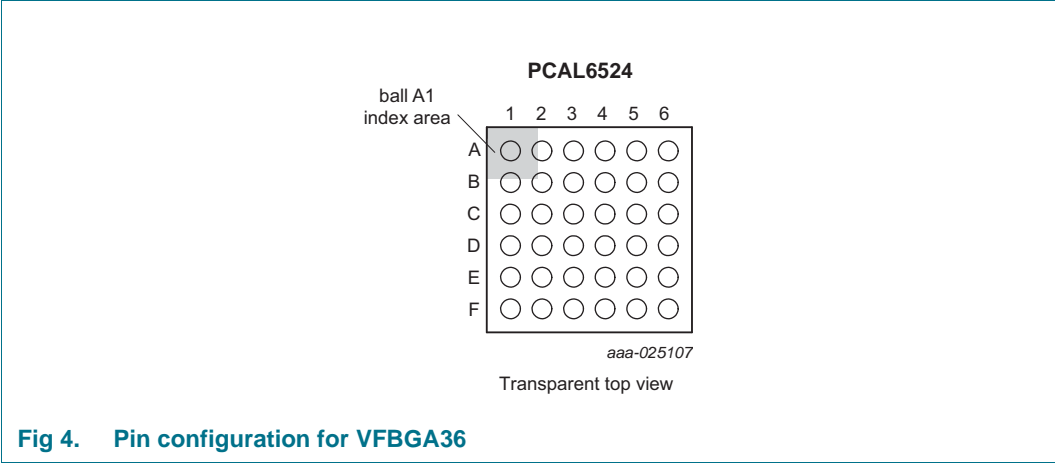
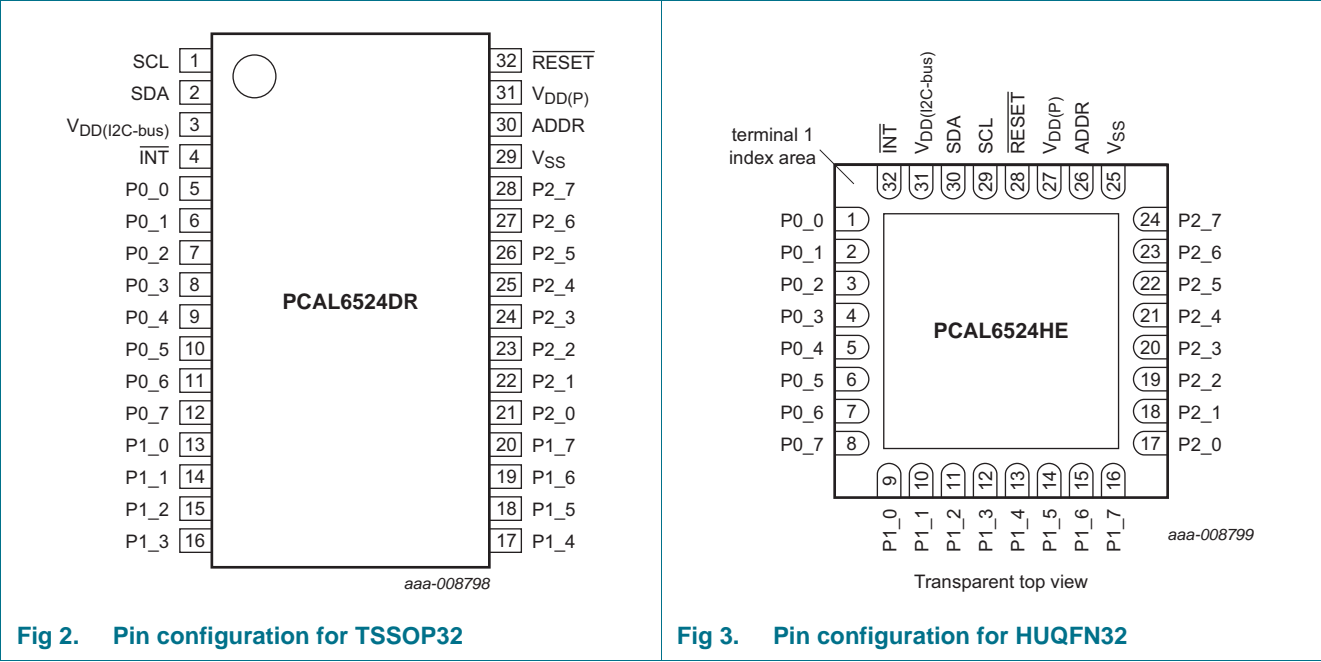


Fig 4. Pin configuration for VFBGA36

## 5.2 Pin description

Table 3. Pin description

Symbol	Pin			Type	Description
	VFBGA36	TSSOP32	HUQFN32		
SCL	A3	1	29	I	Serial clock line. Connect to V <sub>DD(I2C-bus)</sub> through a pull-up resistor.
SDA	A2	2	30	I/O	Serial data line. Connect to V <sub>DD(I2C-bus)</sub> through a pull-up resistor.
V <sub>DD(I2C-bus)</sub>	A1	3	31	power supply	Supply voltage of I <sup>2</sup> C-bus. Connect directly to the V <sub>DD</sub> of the external I <sup>2</sup> C-bus master. Provides voltage-level translation.
$\overline{\text{INT}}$	C4	4	32	O	Interrupt output. Connect to V <sub>DD(I2C-bus)</sub> or V <sub>DD(P)</sub> through a pull-up resistor.
P0_0 <sup>[1]</sup>	B1	5	1	I/O	Port 0 input/output 0.
P0_1 <sup>[1]</sup>	D4	6	2	I/O	Port 0 input/output 1.
P0_2 <sup>[1]</sup>	C1	7	3	I/O	Port 0 input/output 2.
P0_3 <sup>[1]</sup>	D2	8	4	I/O	Port 0 input/output 3.
P0_4 <sup>[1]</sup>	D1	9	5	I/O	Port 0 input/output 4.
P0_5 <sup>[1]</sup>	E1	10	6	I/O	Port 0 input/output 5.
P0_6 <sup>[1]</sup>	D3	11	7	I/O	Port 0 input/output 6.
P0_7 <sup>[1]</sup>	F1	12	8	I/O	Port 0 input/output 7.
P1_0 <sup>[2]</sup>	E2	13	9	I/O	Port 1 input/output 0.
P1_1 <sup>[2]</sup>	F2	14	10	I/O	Port 1 input/output 1.
P1_2 <sup>[2]</sup>	E3	15	11	I/O	Port 1 input/output 2.
P1_3 <sup>[2]</sup>	F3	16	12	I/O	Port 1 input/output 3.
P1_4 <sup>[2]</sup>	F4	17	13	I/O	Port 1 input/output 4.
P1_5 <sup>[2]</sup>	E4	18	14	I/O	Port 1 input/output 5.
P1_6 <sup>[2]</sup>	F5	19	15	I/O	Port 1 input/output 6.
P1_7 <sup>[2]</sup>	E5	20	16	I/O	Port 1 input/output 7.
P2_0 <sup>[3]</sup>	F6	21	17	I/O	Port 2 input/output 0.
P2_1 <sup>[3]</sup>	E6	22	18	I/O	Port 2 input/output 1.
P2_2 <sup>[3]</sup>	D5	23	19	I/O	Port 2 input/output 2.
P2_3 <sup>[3]</sup>	D6	24	20	I/O	Port 2 input/output 3.
P2_4 <sup>[3]</sup>	C5	25	21	I/O	Port 2 input/output 4.
P2_5 <sup>[3]</sup>	C6	26	22	I/O	Port 2 input/output 5.
P2_6 <sup>[3]</sup>	B5	27	23	I/O	Port 2 input/output 6.
P2_7 <sup>[3]</sup>	B6	28	24	I/O	Port 2 input/output 7.
V <sub>SS</sub>	A6	29	25	ground	Supply ground.
ADDR	A5	30	26	I	Address input. Connect directly to V <sub>DD(I2C-bus)</sub> , ground, SCL or SDA.
V <sub>DD(P)</sub>	A4	31	27	power supply	Supply voltage of PCAL6524 for Port P. 0.1 uF bypass capacitor required on this supply located as close to package as practical.

Table 3. Pin description ...continued

Symbol	Pin			Type	Description
	VFBGA36	TSSOP32	HUQFN32		
RESET	B4	32	28	I	Active LOW reset input. Connect to V <sub>DD(I2C-bus)</sub> through a pull-up resistor if no active connection is used.
n.c.	B2, B3, C2, C3	-	-	n.c.	Not connected

[1] Pins P0\_0 to P0\_7 correspond to bits P0.0 to P0.7. At power-on, all I/Os are configured as inputs.

[2] Pins P1\_0 to P1\_7 correspond to bits P1.0 to P1.7. At power-on, all I/Os are configured as inputs.

[3] Pins P2\_0 to P2\_7 correspond to bits P2.0 to P2.7. At power-on, all I/Os are configured as inputs.

## 6. Functional description

Refer to [Figure 1 “Block diagram \(positive logic\)”](#).

### 6.1 Device address

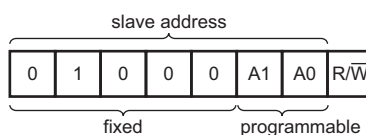
Following a START condition, the bus master must send the target slave address followed by a read ( $R/\overline{W} = 1$ ) or write ( $R/\overline{W} = 0$ ) operation bit. The slave address of the PCAL6524 is shown in [Figure 5](#). Slave address pin ADDR chooses one of four slave addresses.

[Table 4](#) shows all four slave addresses by connecting the ADDR pin to SCL, SDA, V<sub>SS</sub>, or V<sub>DD</sub>.

Table 4. PCAL6524 address map

ADDR	Device family high-order address bits					Variable portion of address		Address
	A6	A5	A4	A3	A2	A1	A0	
SCL	0	1	0	0	0	0	0	40h
SDA	0	1	0	0	0	0	1	42h
V <sub>SS</sub>	0	1	0	0	0	1	0	44h
V <sub>DD</sub>	0	1	0	0	0	1	1	46h

The last bit of the first byte defines the reading from or writing to the PCAL6524. When set to logic 1 a read is selected, while logic 0 selects a write operation.



aaa-011036

Fig 5. PCAL6524 address

## 6.2 Interface definition

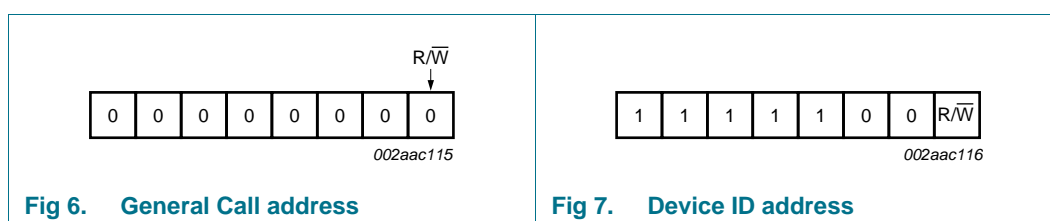
Table 5. Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C-bus slave address	L	H	L	L	L	A1	A0	R/ $\overline{W}$
I/O data bus	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

## 6.3 Software Reset Call, and device ID addresses

Two other different addresses can be sent to the device.

- General Call address: allows to reset the device through the I<sup>2</sup>C-bus upon reception of the right I<sup>2</sup>C-bus sequence. See [Section 6.3.1 “Software Reset”](#) for more information.
- Device ID address: allows to read ID information from the device (manufacturer, part identification, revision). See [Section 6.3.2 “Device ID \(PCAL6524 ID field\)”](#) for more information.



### 6.3.1 Software Reset

The Software Reset Call allows all the devices in the I<sup>2</sup>C-bus to be reset to the power-up state value through a specific formatted I<sup>2</sup>C-bus command. To be performed correctly, it implies that the I<sup>2</sup>C-bus is functional and that there is no device hanging the bus.

The Software Reset sequence is defined as following:

1. A START command is sent by the I<sup>2</sup>C-bus master.
2. The reserved General Call I<sup>2</sup>C-bus address '0000 000' with the R/ $\overline{W}$  bit set to 0 (write) is sent by the I<sup>2</sup>C-bus master.
3. The device acknowledges after seeing the General Call address '0000 0000' (00h) only. If the R/ $\overline{W}$  bit is set to 1 (read), no acknowledge is returned to the I<sup>2</sup>C-bus master.
4. Once the General Call address has been sent and acknowledged, the master sends 1 byte. The value of the byte must be equal to 06h.
  - a. The device acknowledges this value only. If the byte is not equal to 06h, the device does not acknowledge it.

If more than 1 byte of data is sent, the device does not acknowledge any more.



- Once the right byte has been sent and correctly acknowledged, the master sends a STOP command to end the Software Reset sequence: the device then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time. If the master sends a Repeated START instead, no reset is performed.

The I<sup>2</sup>C-bus master must interpret a non-acknowledge from the device (at any time) as a 'Software Reset Abort'. The device does not initiate a reset of its registers.

The unique sequence that initiates a Software Reset is described in [Figure 8](#).

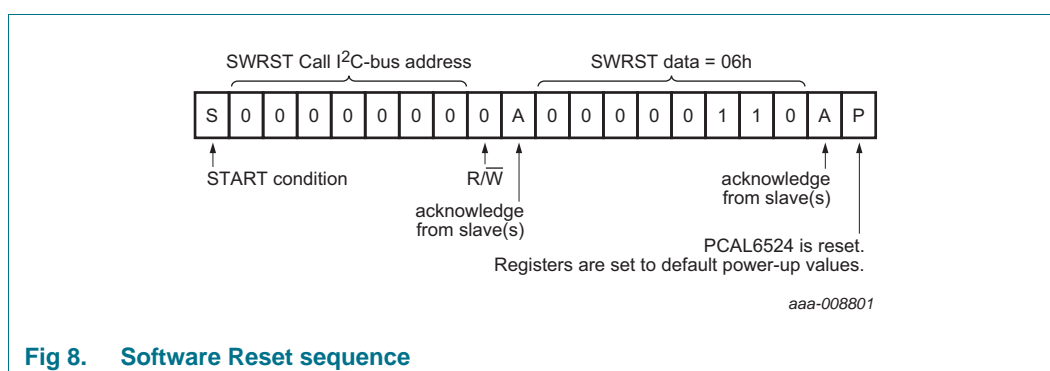


Fig 8. Software Reset sequence

### 6.3.2 Device ID (PCAL6524 ID field)

The Device ID field is a 3-byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer (for example, NXP).
- 9 bits with the part identification, assigned by manufacturer.
- 3 bits with the die revision, assigned by manufacturer (for example, Rev X).

The Device ID is read-only, hardwired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I<sup>2</sup>C-bus address followed by the R/W bit set to 0 (write): '1111 1000'.
3. The master sends the I<sup>2</sup>C-bus slave address of the slave device it needs to identify. The LSB is a 'Don't care' value. Only one device must acknowledge this byte (the one that has the I<sup>2</sup>C-bus slave address).
4. The master sends a Re-START command.

**Remark:** A STOP command followed by a START command will reset the slave state machine and the Device ID read cannot be performed. Also, a STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID Read cannot be performed.

5. The master sends the Reserved Device ID I<sup>2</sup>C-bus address followed by the R/W bit set to 1 (read): '1111 1001'.
6. The Device ID Read can be done, starting with the 12 manufacturer bits (first byte + 4 MSB of the second byte), followed by the 9 part identification bits (4 LSBs of the second byte + 5 MSBs of the third byte), and then the 3 die revision bits (3 LSBs of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

**Remark:** The reading of the Device ID can be stopped anytime by sending a NACK command.

If the master continues to ACK the bytes after the third byte, the slave rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

For the PCAL6524, the Device ID is as shown in [Figure 9](#).

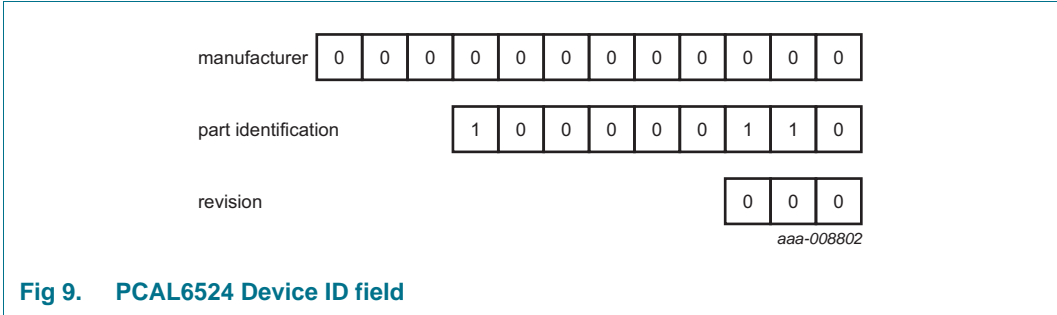
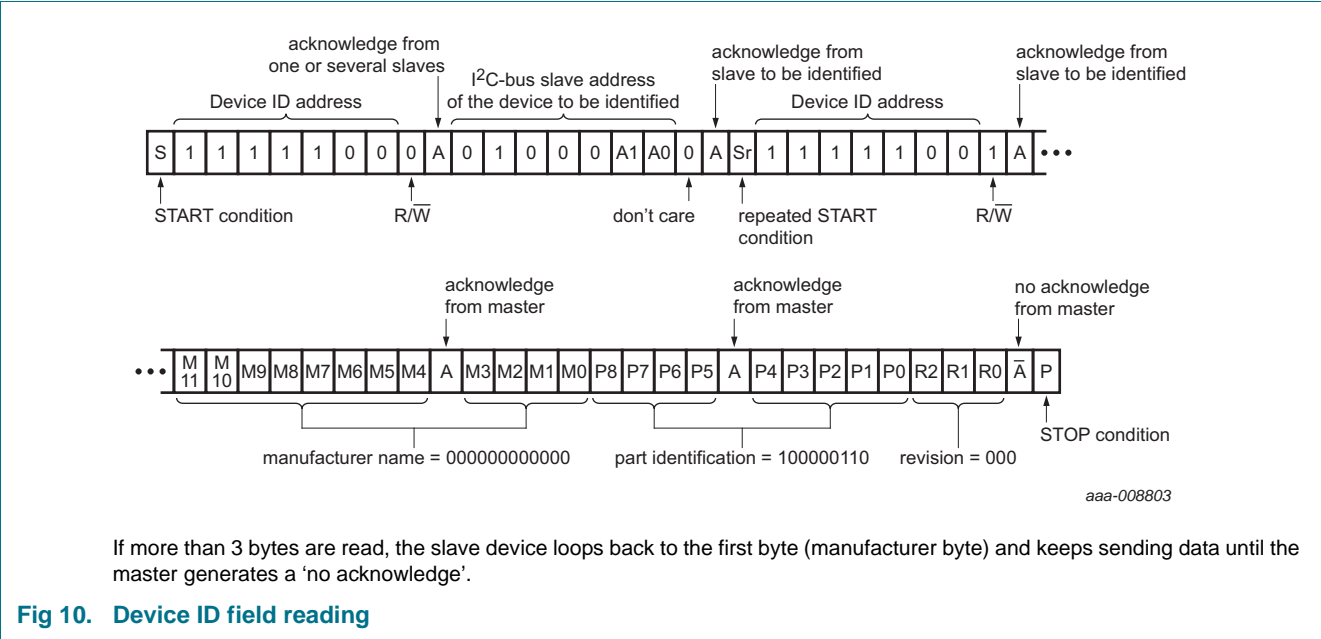


Fig 9. PCAL6524 Device ID field



If more than 3 bytes are read, the slave device loops back to the first byte (manufacturer byte) and keeps sending data until the master generates a 'no acknowledge'.

Fig 10. Device ID field reading

6.4 Pointer register and command byte

Following the successful acknowledgement of the slave address byte, the bus master sends a command byte, which is write only and stored in the pointer register in the PCAL6524. The lowest 7 bits (B[6:0] in [Table 6](#)) are used as a pointer to determine which register is accessed and the highest bit is used as Auto-Increment (AI) as shown in [Figure 11](#). At power-up, hardware or software reset, the pointer register defaults to 00h, with the AI bit set to '0' and the lowest seven bits set to '000 0000'.

When the Auto-Increment bit is set (AI = 1), the seven low-order bits of the pointer register are automatically incremented after a read or write until a STOP condition is encountered. This allows the user to program the registers sequentially without modifying the pointer register. The contents of these bits will roll over to '000 0000' after the last register (address = 76h) is accessed. Unimplemented register addresses (reserved registers) are skipped. If more than 52 bytes are written, the address will loop back to the register which is indicated by the seven low-order bits in the pointer register, and previously-written data will be overwritten. A STOP condition will keep the pointer register value in the last read or write location.

When the Auto-Increment bit is cleared (AI = 0), the 2 least significant bits are automatically incremented after a read or write for 3-register group which allows the user to program each of the 3-register group sequentially. If more than 3 bytes of data are read or written when AI is 0, previous data in the selected registers will be overwritten. For example: if input port 1 is read first, the next 2nd byte will be input port 2, and next 3rd byte will be input port 0, there is no limit on the number of data bytes for this read operation. There are two special 6-register groups: output drive strength (40h~45h) and interrupt edge (60h~65h) registers will allow user to program each of the 6-register group sequentially. Only Output port configuration register location (5Ch) remains in the same location after a successive read or write.

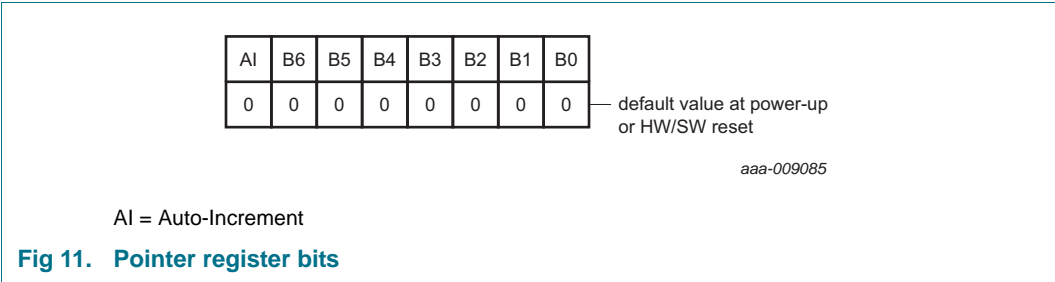


Table 6. Command byte

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx <sup>[1]</sup>
0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx <sup>[1]</sup>
0	0	0	0	0	1	0	02h	Input port 2	read byte	xxxx xxxx <sup>[1]</sup>
0	0	0	0	0	1	1	03h	reserved <sup>[3]</sup>	reserved	reserved
0	0	0	0	1	0	0	04h	Output port 0	read/write byte	1111 1111
0	0	0	0	1	0	1	05h	Output port 1	read/write byte	1111 1111
0	0	0	0	1	1	0	06h	Output port 2	read/write byte	1111 1111
0	0	0	0	1	1	1	07h	reserved <sup>[3]</sup>	reserved	reserved
0	0	0	1	0	0	0	08h	Polarity Inversion port 0	read/write byte	0000 0000
0	0	0	1	0	0	1	09h	Polarity Inversion port 1	read/write byte	0000 0000
0	0	0	1	0	1	0	0Ah	Polarity Inversion port 2	read/write byte	0000 0000
0	0	0	1	0	1	1	0Bh	reserved <sup>[3]</sup>	reserved	reserved
0	0	0	1	1	0	0	0Ch	Configuration port 0	read/write byte	1111 1111
0	0	0	1	1	0	1	0Dh	Configuration port 1	read/write byte	1111 1111
0	0	0	1	1	1	0	0Eh	Configuration port 2	read/write byte	1111 1111
-	-	-	-	-	-	-	0Fh to 3Fh	reserved <sup>[3]</sup>	reserved	reserved
1	0	0	0	0	0	0	40h	Output drive strength register port 0A	read/write byte	1111 1111
1	0	0	0	0	0	1	41h	Output drive strength register port 0B	read/write byte	1111 1111
1	0	0	0	0	1	0	42h	Output drive strength register port 1A	read/write byte	1111 1111
1	0	0	0	0	1	1	43h	Output drive strength register port 1B	read/write byte	1111 1111
1	0	0	0	1	0	0	44h	Output drive strength register port 2A	read/write byte	1111 1111
1	0	0	0	1	0	1	45h	Output drive strength register port 2B	read/write byte	1111 1111
1	0	0	0	1	1	0	46h	reserved <sup>[3]</sup>	reserved	reserved
1	0	0	0	1	1	1	47h	reserved <sup>[3]</sup>	reserved	reserved
1	0	0	1	0	0	0	48h	Input latch register port 0	read/write byte	0000 0000
1	0	0	1	0	0	1	49h	Input latch register port 1	read/write byte	0000 0000
1	0	0	1	0	1	0	4Ah	Input latch register port 2	read/write byte	0000 0000
1	0	0	1	0	1	1	4Bh	reserved <sup>[3]</sup>	reserved	reserved
1	0	0	1	1	0	0	4Ch	Pull-up/pull-down enable register port 0	read/write byte	0000 0000
1	0	0	1	1	0	1	4Dh	Pull-up/pull-down enable register port 1	read/write byte	0000 0000
1	0	0	1	1	1	0	4Eh	Pull-up/pull-down enable register port 2	read/write byte	0000 0000
1	0	0	1	1	1	1	4Fh	reserved <sup>[3]</sup>	reserved	reserved
1	0	1	0	0	0	0	50h	Pull-up/pull-down selection register port 0	read/write byte	1111 1111
1	0	1	0	0	0	1	51h	Pull-up/pull-down selection register port 1	read/write byte	1111 1111
1	0	1	0	0	1	0	52h	Pull-up/pull-down selection register port 2	read/write byte	1111 1111

Table 6. Command byte ...continued

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
1	0	1	0	0	1	1	53h	reserved <sup>[3]</sup>	reserved	reserved
1	0	1	0	1	0	0	54h	Interrupt mask register port 0	read/write byte	1111 1111
1	0	1	0	1	0	1	55h	Interrupt mask register port 1	read/write byte	1111 1111
1	0	1	0	1	1	0	56h	Interrupt mask register port 2	read/write byte	1111 1111
1	0	1	0	1	1	1	57h	reserved <sup>[3]</sup>	reserved	reserved
1	0	1	1	0	0	0	58h	Interrupt status register port 0	read byte	0000 0000
1	0	1	1	0	0	1	59h	Interrupt status register port 1	read byte	0000 0000
1	0	1	1	0	1	0	5Ah	Interrupt status register port 2	read byte	0000 0000
1	0	1	1	0	1	1	5Bh	reserved <sup>[3]</sup>	reserved	reserved
1	0	1	1	1	0	0	5Ch <sup>[2]</sup>	Output port configuration register	read/write byte	0000 0000
1	0	1	1	1	0	1	5Dh	reserved <sup>[3]</sup>	reserved	reserved
1	0	1	1	1	1	0	5Eh	reserved <sup>[3]</sup>	reserved	reserved
1	0	1	1	1	1	1	5Fh	reserved <sup>[3]</sup>	reserved	reserved
1	1	0	0	0	0	0	60h	Interrupt edge register port 0A	read/write byte	0000 0000
1	1	0	0	0	0	1	61h	Interrupt edge register port 0B	read/write byte	0000 0000
1	1	0	0	0	1	0	62h	Interrupt edge register port 1A	read/write byte	0000 0000
1	1	0	0	0	1	1	63h	Interrupt edge register port 1B	read/write byte	0000 0000
1	1	0	0	1	0	0	64h	Interrupt edge register port 2A	read/write byte	0000 0000
1	1	0	0	1	0	1	65h	Interrupt edge register port 2B	read/write byte	0000 0000
1	1	0	0	1	1	0	66h	reserved <sup>[3]</sup>	reserved	reserved
1	1	0	0	1	1	1	67h	reserved <sup>[3]</sup>	reserved	reserved
1	1	0	1	0	0	0	68h	Interrupt clear register port 0	write byte	0000 0000
1	1	0	1	0	0	1	69h	Interrupt clear register port 1	write byte	0000 0000
1	1	0	1	0	1	0	6Ah	Interrupt clear register port 2	write byte	0000 0000
1	1	0	1	0	1	1	6Bh	reserved <sup>[3]</sup>	reserved	reserved
1	1	0	1	1	0	0	6Ch	Input status port 0	read byte	xxxx xxxx <sup>[1]</sup>
1	1	0	1	1	0	1	6Dh	Input status port 1	read byte	xxxx xxxx <sup>[1]</sup>
1	1	0	1	1	1	0	6Eh	Input status port 2	read byte	xxxx xxxx <sup>[1]</sup>
1	1	0	1	1	1	1	6Fh	reserved <sup>[3]</sup>	reserved	reserved
1	1	1	0	0	0	0	70h	Individual pin output port 0 configuration register	read/write byte	0000 0000
1	1	1	0	0	0	1	71h	Individual pin output port 1 configuration register	read/write byte	0000 0000
1	1	1	0	0	1	0	72h	Individual pin output port 2 configuration register	read/write byte	0000 0000
1	1	1	0	0	1	1	73h	reserved <sup>[3]</sup>	reserved	reserved
1	1	1	0	1	0	0	74h	Switch debounce enable 0	read/write byte	0000 0000
1	1	1	0	1	0	1	75h	Switch debounce enable 1	read/write byte	0000 0000

Table 6. Command byte ...continued

Pointer register bits							Command byte (hexadecimal)	Register	Protocol	Power-up default
B6	B5	B4	B3	B2	B1	B0				
1	1	1	0	1	1	0	76h	Switch debounce count	read/write byte	0000 0000
-	-	-	-	-	-	-	77h to 7Fh	reserved <sup>[3]</sup>	reserved	reserved

[1] Undefined.

[2] Successive read and write accesses to remain at this register address.

[3] These registers marked "reserved" should not be written, and the master will not be acknowledged when accessed.

## 6.5 Register descriptions

### 6.5.1 Input port registers (00h, 01h, 02h)

The Input port registers (registers 00h, 01h, 02h) reflect the incoming logic levels of the pins. The Input port registers are read only; writes to these registers have no effect and the transaction will be acknowledged (ACK). The default value 'X' is determined by the externally applied logic level. If a pin is configured as an output (registers 04h, 05h, 06h), the port value is equal to the actual voltage level on that pin. If the output is configured as open-drain (register 5Ch and registers 70h, 71h, 72h), the input port value is forced to 0. An Input port register group read operation is performed as described in [Section 7.2](#).

After reading input port registers, all interrupts will be cleared.

**Table 7. Input port 0 register (address 00h)**

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

**Table 8. Input port 1 register (address 01h)**

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

**Table 9. Input port 2 register (address 02h)**

Bit	7	6	5	4	3	2	1	0
Symbol	I2.7	I2.6	I2.5	I2.4	I2.3	I2.2	I2.1	I2.0
Default	X	X	X	X	X	X	X	X

### 6.5.2 Output port registers (04h, 05h, 06h)

The Output port registers (registers 04h, 05h, 06h) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. A register group write is described in [Section 7.1](#) and a register group read is described in [Section 7.2](#).

**Table 10. Output port 0 register (address 04h)**

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

**Table 11. Output port 1 register (address 05h)**

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

Table 12. Output port 2 register (address 06h)

Bit	7	6	5	4	3	2	1	0
Symbol	O2.7	O2.6	O2.5	O2.4	O2.3	O2.2	O2.1	O2.0
Default	1	1	1	1	1	1	1	1

### 6.5.3 Polarity inversion registers (08h, 09h, 0Ah)

The Polarity inversion registers (registers 08h, 09h, 0Ah) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained. A register group write is described in [Section 7.1](#) and a register group read is described in [Section 7.2](#).

Table 13. Polarity inversion port 0 register (address 08h)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 14. Polarity inversion port 1 register (address 09h)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

Table 15. Polarity inversion port 2 register (address 0Ah)

Bit	7	6	5	4	3	2	1	0
Symbol	N2.7	N2.6	N2.5	N2.4	N2.3	N2.2	N2.1	N2.0
Default	0	0	0	0	0	0	0	0

### 6.5.4 Configuration registers (0Ch, 0Dh, 0Eh)

The Configuration registers (registers 0Ch, 0Dh, 0Eh) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register group write is described in [Section 7.1](#) and a register group read is described in [Section 7.2](#).

Table 16. Configuration port 0 register (address 0Ch)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 17. Configuration port 1 register (address 0Dh)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1



Table 18. Configuration port 2 register (address 0Eh)

Bit	7	6	5	4	3	2	1	0
Symbol	C2.7	C2.6	C2.5	C2.4	C2.3	C2.2	C2.1	C2.0
Default	1	1	1	1	1	1	1	1

### 6.5.5 Output drive strength registers (40h, 41h, 42h, 43h, 44h, 45h)

The Output drive strength registers control the output drive level of the GPIO. Each GPIO can be configured independently to a certain output current level by two register control bits. For example Port 0.7 is controlled by register 41h CC0.7 (bits [7:6]), Port 0.6 is controlled by register 41h CC0.6 (bits [5:4]). The output drive level of the GPIO is programmed 00b = 0.25×, 01b = 0.5×, 10b = 0.75× or 11b = 1× of the drive capability of the I/O. See [Section 8.1 “Output drive strength control”](#) for more details. A register group write operation is described in [Section 7.1](#). A register group read operation is described in [Section 7.2](#).

Table 19. Current control port 0A register (address 40h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.3		CC0.2		CC0.1		CC0.0	
Default	1	1	1	1	1	1	1	1

Table 20. Current control port 0B register (address 41h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC0.7		CC0.6		CC0.5		CC0.4	
Default	1	1	1	1	1	1	1	1

Table 21. Current control port 1A register (address 42h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.3		CC1.2		CC1.1		CC1.0	
Default	1	1	1	1	1	1	1	1

Table 22. Current control port 1B register (address 43h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC1.7		CC1.6		CC1.5		CC1.4	
Default	1	1	1	1	1	1	1	1

Table 23. Current control port 2A register (address 44h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC2.3		CC2.2		CC2.1		CC2.0	
Default	1	1	1	1	1	1	1	1

Table 24. Current control port 2B register (address 45h)

Bit	7	6	5	4	3	2	1	0
Symbol	CC2.7		CC2.6		CC2.5		CC2.4	
Default	1	1	1	1	1	1	1	1

### 6.5.6 Input latch registers (48h, 49h, 4Ah)

The input latch registers (registers 48h, 49h, 4Ah) enable and disable the input latch of the I/O pins. These registers are effective only when the pin is configured as an input port. When an input latch register bit is 0, the corresponding input pin state is not latched. A state change in the corresponding input pin generates an interrupt. A read of the input register clears the interrupt. If the input goes back to its initial logic state before the input port register is read, then the interrupt is cleared.

When an input latch register bit is 1, the corresponding input pin state is latched. A change of state of the input generates an interrupt and the input logic value is loaded into the corresponding bit of the input port register (registers 0, 1 and 2). A read of the input port register clears the interrupt. If the input pin returns to its initial logic state before the input port register is read, then the interrupt is not cleared and the corresponding bit of the input port register keeps the logic value that initiated the interrupt. See [Figure 21](#).

For example, if the P0\_4 input was as logic 0 and the input goes to logic 1 then back to logic 0, the input port 0 register will capture this change and an interrupt is generated (if unmasked). When the read is performed on the input port 0 register, the interrupt is cleared, assuming there were no additional input(s) that have changed, and bit 4 of the input port 0 register will read '1'. The next read of the input port register bit 4 register should now read '0'.

An interrupt remains active when a non-latched input simultaneously switches state with a latched input and then returns to its original state. A read of the input register reflects only the change of state of the latched input and also clears the interrupt. The interrupt is cleared if the input latch register changes from latched to non-latched configuration and I/O pin returns to its original state.

If the input pin is changed from latched to non-latched input, a read from the input port register reflects the current port logic level. If the input pin is changed from non-latched to latched input, the read from the input register reflects the latched logic level. A register group write operation is described in [Section 7.1](#). A register group read operation is described in [Section 7.2](#).

**Table 25. Input latch port 0 register (address 48h)**

Bit	7	6	5	4	3	2	1	0
Symbol	L0.7	L0.6	L0.5	L0.4	L0.3	L0.2	L0.1	L0.0
Default	0	0	0	0	0	0	0	0

**Table 26. Input latch port 1 register (address 49h)**

Bit	7	6	5	4	3	2	1	0
Symbol	L1.7	L1.6	L1.5	L1.4	L1.3	L1.2	L1.1	L1.0
Default	0	0	0	0	0	0	0	0

**Table 27. Input latch port 2 register (address 4Ah)**

Bit	7	6	5	4	3	2	1	0
Symbol	L2.7	L2.6	L2.5	L2.4	L2.3	L2.2	L2.1	L2.0
Default	0	0	0	0	0	0	0	0

### 6.5.7 Pull-up/pull-down enable registers (4Ch, 4Dh, 4Eh)

The pull-up and pull-down enable registers allow the user to enable or disable pull-up/pull-down resistors on the I/O pins. Setting the bit to logic 1 enables the selection of pull-up/pull-down resistors. Setting the bit to logic 0 disconnects the pull-up/pull-down resistors from the I/O pins. Also, the resistors will be disconnected when the outputs are configured as open-drain outputs (see [Section 6.5.11](#) and [Section 6.5.15](#)). Use the pull-up/pull-down registers to select either a pull-up or pull-down resistor. A register group write operation is described in [Section 7.1](#). A register group read operation is described in [Section 7.2](#).

**Table 28. Pull-up/pull-down enable port 0 register (address 4Ch)**

Bit	7	6	5	4	3	2	1	0
Symbol	PE0.7	PE0.6	PE0.5	PE0.4	PE0.3	PE0.2	PE0.1	PE0.0
Default	0	0	0	0	0	0	0	0

**Table 29. Pull-up/pull-down enable port 1 register (address 4Dh)**

Bit	7	6	5	4	3	2	1	0
Symbol	PE1.7	PE1.6	PE1.5	PE1.4	PE1.3	PE1.2	PE1.1	PE1.0
Default	0	0	0	0	0	0	0	0

**Table 30. Pull-up/pull-down enable port 2 register (address 4Eh)**

Bit	7	6	5	4	3	2	1	0
Symbol	PE2.7	PE2.6	PE2.5	PE2.4	PE2.3	PE2.2	PE2.1	PE2.0
Default	0	0	0	0	0	0	0	0

### 6.5.8 Pull-up/pull-down selection registers (50h, 51h, 52h)

The I/O port can be configured to have pull-up or pull-down resistor by programming the pull-up/pull-down selection register. Setting a bit to logic 1 selects a 100 k $\Omega$  pull-up resistor for that I/O pin. Setting a bit to logic 0 selects a 100 k $\Omega$  pull-down resistor for that I/O pin. If the pull-up/down feature is disconnected, writing to this register will have no effect on I/O pin. Typical value is 100 k $\Omega$  with minimum of 50 k $\Omega$  and maximum of 150 k $\Omega$ . A register group write operation is described in [Section 7.1](#). A register group read operation is described in [Section 7.2](#).

**Table 31. Pull-up/pull-down selection port 0 register (address 50h)**

Bit	7	6	5	4	3	2	1	0
Symbol	PUD0.7	PUD0.6	PUD0.5	PUD0.4	PUD0.3	PUD0.2	PUD0.1	PUD0.0
Default	1	1	1	1	1	1	1	1

**Table 32. Pull-up/pull-down selection port 1 register (address 51h)**

Bit	7	6	5	4	3	2	1	0
Symbol	PUD1.7	PUD1.6	PUD1.5	PUD1.4	PUD1.3	PUD1.2	PUD1.1	PUD1.0
Default	1	1	1	1	1	1	1	1

**Table 33. Pull-up/pull-down selection port 2 register (address 52h)**

Bit	7	6	5	4	3	2	1	0
Symbol	PUD2.7	PUD2.6	PUD2.5	PUD2.4	PUD2.3	PUD2.2	PUD2.1	PUD2.0
Default	1	1	1	1	1	1	1	1

### 6.5.9 Interrupt mask registers (54h, 55h, 56h)

Interrupt mask registers are set to logic 1 upon power-on, disabling interrupts during system start-up. Interrupts may be enabled by setting corresponding mask bits to logic 0.

If an input changes state and the corresponding bit in the Interrupt mask register is set to 1, the interrupt is masked and the interrupt pin will not be asserted. If the corresponding bit in the Interrupt mask register is set to 0, the interrupt pin will be asserted.

When an input changes state and the resulting interrupt is masked (interrupt mask bit is 1), setting the input mask register bit to 0 will cause the interrupt pin to be asserted. If the interrupt mask bit of an input that is currently the source of an interrupt is set to 1, the interrupt pin will be de-asserted. A register group write operation is described in [Section 7.1](#). A register group read operation is described in [Section 7.2](#).

**Table 34. Interrupt mask port 0 register (address 54h) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	M0.7	M0.6	M0.5	M0.4	M0.3	M0.2	M0.1	M0.0
Default	1	1	1	1	1	1	1	1

**Table 35. Interrupt mask port 1 register (address 55h) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	M1.7	M1.6	M1.5	M1.4	M1.3	M1.2	M1.1	M1.0
Default	1	1	1	1	1	1	1	1

**Table 36. Interrupt mask port 2 register (address 56h) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	M2.7	M2.6	M2.5	M2.4	M2.3	M2.2	M2.1	M2.0
Default	1	1	1	1	1	1	1	1

### 6.5.10 Interrupt status registers (58h, 59h, 5Ah)

The read-only interrupt status registers are used to identify the source of an interrupt. When read, a logic 1 indicates that the corresponding input pin was the source of the interrupt. A logic 0 indicates that the input pin is not the source of an interrupt.

When a corresponding bit in the interrupt mask register is set to 1 (masked), the interrupt status bit will return logic 0. A register group read operation is described in [Section 7.2](#).

**Table 37. Interrupt status port 0 register (address 58h) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	S0.7	S0.6	S0.5	S0.4	S0.3	S0.2	S0.1	S0.0
Default	0	0	0	0	0	0	0	0

**Table 38. Interrupt status port 1 register (address 59h) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	S1.7	S1.6	S1.5	S1.4	S1.3	S1.2	S1.1	S1.0
Default	0	0	0	0	0	0	0	0

**Table 39. Interrupt status port 2 register (address 5Ah) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	S2.7	S2.6	S2.5	S2.4	S2.3	S2.2	S2.1	S2.0
Default	0	0	0	0	0	0	0	0

### 6.5.11 Output port configuration register (5Ch)

The output port configuration register selects port-wise push-pull or open-drain I/O stage. A logic 0 configures the I/O as push-pull (Q1 and Q2 are active, see [Figure 12](#)). A logic 1 configures the I/O as open-drain (Q1 is disabled, Q2 is active) and the recommended command sequence is to program this register (5Ch) before the Configuration register (0Ch, 0Dh, 0Eh) sets the port pins as outputs.

ODEN0 configures Port 0\_x, ODEN1 configures Port 1\_x, and ODEN2 configures Port 2\_x.

Individual pins may be programmed as open-drain or push-pull by programming Individual Pin Output Configuration registers (70h, 71h, 72h). See Section 6.5.15 for more information.

A register group read or write operation is not allowed on this register. Successive read or write accesses will remain at this register address.

**Table 40. Output port configuration register (address 5Ch)**

Bit	7	6	5	4	3	2	1	0
Symbol	reserved					ODEN2	ODEN1	ODEN0
Default	0	0	0	0	0	0	0	0

### 6.5.12 Interrupt edge registers (60h, 61h, 62h and 63h, 64h, 65h)

The interrupt edge registers determine what action on an input pin will cause an interrupt along with the Interrupt Mask registers (54h, 55h and 56h). If the Interrupt is enabled (set '0' in the Mask register) and the action at the corresponding pin matches the required activity, the INT output will become active. The default value for each pin is 00b or level triggered, meaning a level change on the pin will cause an interrupt event. A level triggered action means a change in logic state (HIGH-to-LOW or LOW-to-HIGH), since the last read of the Input port (00h, 01h or 02h) which can be latched with a corresponding '1' set in the Input Latch register (48h, 49h, 4Ah). If the Interrupt edge register entry is set to 11b, any edge, positive- or negative-going, causes an interrupt event. If an entry is 01b, only a positive-going edge will cause an interrupt event, while a 10b will require a negative-going edge to cause an interrupt event. These edge interrupt events are latched, regardless of the status of the Input Latch register (48h, 49h, 4Ah). These edged interrupts can be cleared in a number of ways: Reading input port registers (00h, 01h, 02h); setting the Interrupt Mask register (54h, 55h, 56h) to 1 (masked); setting the Interrupt Clear register (68h, 69h, 6Ah) to 1 (this is a write-only register); resetting the Interrupt Edge register (60h to 65h) back to 0. A register group write operation is described in [Section 7.1](#). A register group read operation is described in [Section 7.2](#).

Table 41. Interrupt edge port 0A register (address 60h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.3		IE0.2		IE0.1		IE0.0	
Default	0	0	0	0	0	0	0	0

Table 42. Interrupt edge port 0B register (address 61h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE0.7		IE0.6		IE0.5		IE0.4	
Default	0	0	0	0	0	0	0	0

Table 43. Interrupt edge port 1A register (address 62h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.3		IE1.2		IE1.1		IE1.0	
Default	0	0	0	0	0	0	0	0

Table 44. Interrupt edge port 1B register (address 63h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE1.7		IE1.6		IE1.5		IE1.4	
Default	0	0	0	0	0	0	0	0

Table 45. Interrupt edge port 2A register (address 64h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE2.3		IE2.2		IE2.1		IE2.0	
Default	0	0	0	0	0	0	0	0

Table 46. Interrupt edge port 2B register (address 65h)

Bit	7	6	5	4	3	2	1	0
Symbol	IE2.7		IE2.6		IE2.5		IE2.4	
Default	0	0	0	0	0	0	0	0

Table 47. Interrupt edge bits (IEx.x)

Bit 1	Bit 0	Description
0	0	level-triggered interrupt
0	1	positive-going (rising) edge triggered interrupt
1	0	negative-going (falling) edge triggered interrupt
1	1	any edge (positive or negative-going) triggered interrupt

### 6.5.13 Interrupt clear registers (68h, 69h, 6Ah)

The write-only interrupt clear registers clear individual interrupt sources (status bit). Setting an individual bit or any combination of bits to logic 1 will reset the corresponding interrupt source, so if that source was the only event causing an interrupt, the  $\overline{\text{INT}}$  will be cleared. After writing a logic 1 the bit returns to logic 0. A register group write operation is described in [Section 7.1](#).

**Table 48. Interrupt clear port 0 register (address 68h) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	IC0.7	IC0.6	IC0.5	IC0.4	IC0.3	IC0.2	IC0.1	IC0.0
Default	0	0	0	0	0	0	0	0

**Table 49. Interrupt clear port 1 register (address 69h) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	IC1.7	IC1.6	IC1.5	IC1.4	IC1.3	IC1.2	IC1.1	IC1.0
Default	0	0	0	0	0	0	0	0

**Table 50. Interrupt clear port 2 register (address 6Ah) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	IC2.7	IC2.6	IC2.5	IC2.4	IC2.3	IC2.2	IC2.1	IC2.0
Default	0	0	0	0	0	0	0	0

### 6.5.14 Input status registers (6Ch, 6Dh, 6Eh)

The read-only input status registers function exactly like Input Port 0, 1 and 2 (00h, 01h, 02h) without resetting the interrupt logic. This allows inspection of the actual state of the input pins without upsetting internal logic. If the pin is configured as an input, the port read is unaffected by input latch logic or other features, the state of the register is simply a reflection of the current state of the input pins. If a pin is configured as an output by the Configuration register (0Ch, 0Dh, 0Eh), and is also configured as open-drain (register 5Ch and 70h, 71h, 72h), the read for that pin will always return 0, otherwise that state of that pin is returned. A register group read operation is described in [Section 7.2](#).

**Table 51. Input status port 0 register (address 6Ch) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	IIO.7	IIO.6	IIO.5	IIO.4	IIO.3	IIO.2	IIO.1	IIO.0
Default	X	X	X	X	X	X	X	X

**Table 52. Input status port 1 register (address 6Dh) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

**Table 53. Input status port 2 register (address 6Eh) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	I2.7	I2.6	I2.5	I2.4	I2.3	I2.2	I2.1	I2.0
Default	X	X	X	X	X	X	X	X

### 6.5.15 Individual pin output configuration registers (70h, 71h, 72h)

The individual pin output configuration registers modify output configuration (push-pull or open-drain) set by the Output Port Configuration register (5Ch).

If the ODENx bit is set at logic 0 (push-pull), any bit set to logic 1 in the IOCRx register will reverse the output state of that pin only to open-drain. When ODENx bit is set at logic 1 (open-drain), a logic 1 in IOCRx will set that pin to push-pull.

The recommended command sequence to program the output pin is to program ODENx (5Ch), the IOCRx, and finally the Configuration register (0Ch, 0Dh, 0Eh) to set the pins as outputs. A register group write operation is described in [Section 7.1](#). A register group read operation is described in [Section 7.2](#).

**Table 54. Individual pin output configuration register 0 (address 70h) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR0.7	IOCR0.6	IOCR0.5	IOCR0.4	IOCR0.3	IOCR0.2	IOCR0.1	IOCR0.0
Default	0	0	0	0	0	0	0	0

**Table 55. Individual pin output configuration register 1 (address 71h) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR1.7	IOCR1.6	IOCR1.5	IOCR1.4	IOCR1.3	IOCR1.2	IOCR1.1	IOCR1.0
Default	0	0	0	0	0	0	0	0

**Table 56. Individual pin output configuration register 2 (address 72h) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	IOCR2.7	IOCR2.6	IOCR2.5	IOCR2.4	IOCR2.3	IOCR2.2	IOCR2.1	IOCR2.0
Default	0	0	0	0	0	0	0	0



### 6.5.16 Switch debounce enable registers (74h, 75h)

The switch debounce enable registers enable the switch debounce function for Port 0 and Port 1 pins. If a pin on Port 0 or Port 1 is designated as an input, a logic 1 in the Switch debounce enable register will connect debounce logic to that pin. If a pin is assigned as an output (via Configuration Port 0 or Port 1 register) the debounce logic is not connected to that pin and it will function as a normal output. The switch debounce logic requires an oscillator time base input and if this function is used, P0\_0 is designated as the oscillator input. If P0\_0 is not configured as input and if SD0.0 is not set to logic 1, then switch debounce logic is not connected to any pin. See [Section 6.10 "Switch debounce circuitry"](#) for additional information about Switch debounce logic functionality.

**Table 57. Switch debounce enable Port 0 register (address 74h) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	SD0.7	SD0.6	SD0.5	SD0.4	SD0.3	SD0.2	SD0.1	SD0.0
Default	0	0	0	0	0	0	0	0

**Table 58. Switch debounce enable Port 1 register (address 75h) bit description**

Bit	7	6	5	4	3	2	1	0
Symbol	SD1.7	SD1.6	SD1.5	SD1.4	SD1.3	SD1.2	SD1.1	SD1.0
Default	0	0	0	0	0	0	0	0

### 6.5.17 Switch debounce count register (76h)

The switch debounce count register is used to count the debounce time that the switch debounce logic uses to determine if a switch connected to one of the Port 0 or Port 1 pins finally stays open (logic 1) or closed (logic 0). This number, together with the oscillator frequency supplied to P0\_0, determines the debounce time (for example, the debounce time will be 10  $\mu$ s if this register is set to 0Ah and external oscillator frequency is 1 MHz). See [Section 6.10 "Switch debounce circuitry"](#) for further information.

**Table 59. Switch debounce count register (address 76h) bit description [\[1\]](#)**

Bit	7	6	5	4	3	2	1	0
Symbol	SDC0.7	SDC0.6	SDC0.5	SDC0.4	SDC0.3	SDC0.2	SDC0.1	SDC0.0
Default	0	0	0	0	0	0	0	0

[1] The switch debounce logic is disabled if this register is set to 00h.

## 6.6 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above  $V_{DD(P)}$  to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either  $V_{DD(P)}$  or  $V_{SS}$ . The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation. To avoid internal noise generation when multiple outputs switch simultaneously, a 0.1  $\mu$ F bypass capacitor is required on the  $V_{DD(P)}$  pin as close to the package as practical.

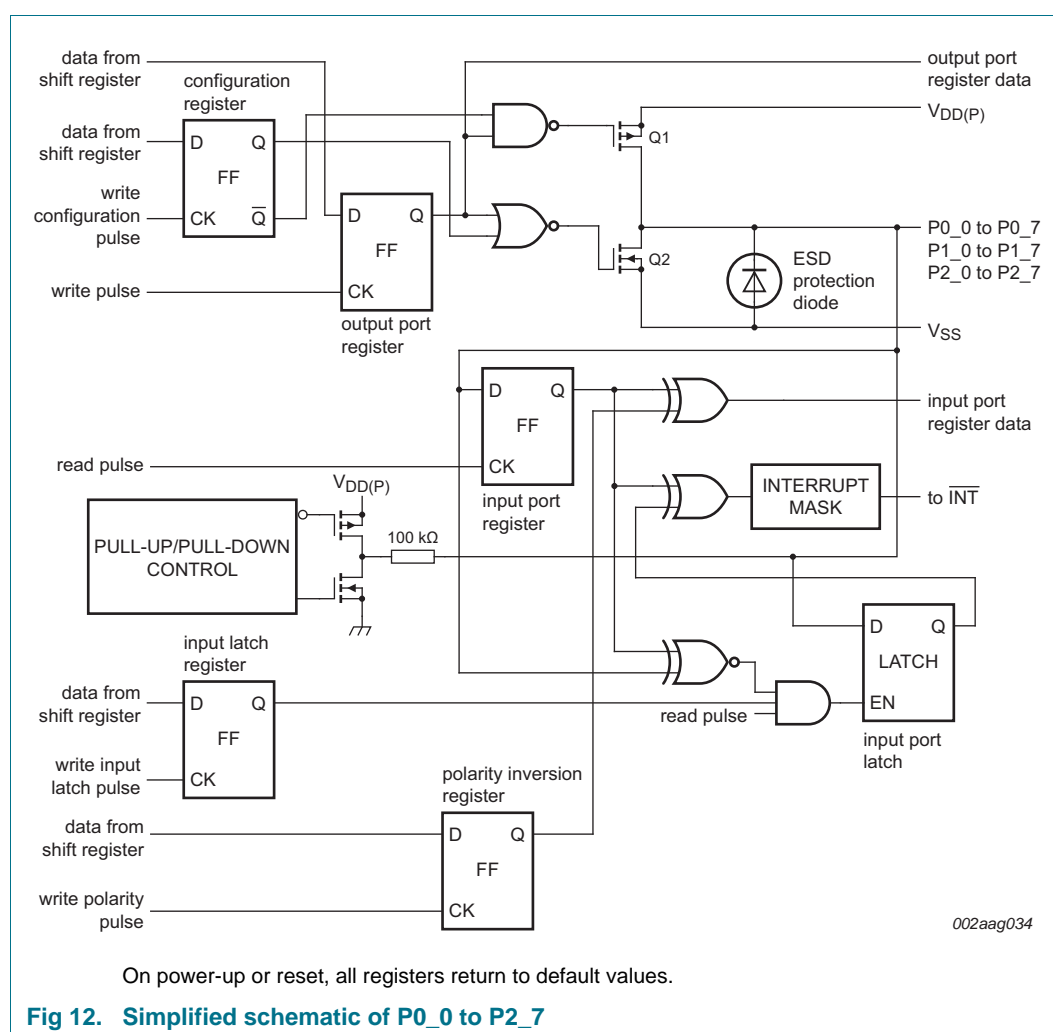


Fig 12. Simplified schematic of P0\_0 to P2\_7

## 6.7 Power-on reset

When power (from 0 V) is applied to  $V_{DD(P)}$ , an internal power-on reset holds the PCAL6524 in a reset condition until  $V_{DD(P)}$  has reached  $V_{POR}$ . At that time, the reset condition is released and the PCAL6524 registers and I<sup>2</sup>C-bus/SMBus state machine initializes to their default states. After that,  $V_{DD(P)}$  must be lowered to below  $V_{POR}$  and back up to the operating voltage for a power-reset cycle. See [Section 8.2 "Power-on reset requirements"](#).

## 6.8 Reset input ( $\overline{\text{RESET}}$ )

The  $\overline{\text{RESET}}$  input can be asserted to initialize the system while keeping the  $V_{\text{DD(P)}}$  at its operating level. A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin LOW for a minimum of  $t_{\text{w(rst)}}$ . The PCAL6524 registers and I<sup>2</sup>C-bus/SMBus state machine are changed to their default state once  $\overline{\text{RESET}}$  is LOW (0). When  $\overline{\text{RESET}}$  is HIGH (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pull-up resistor to  $V_{\text{DD(I2C-bus)}}$  if no active connection is used.

## 6.9 Interrupt output ( $\overline{\text{INT}}$ )

The  $\overline{\text{INT}}$  output has an open-drain structure and requires pull-up resistor to  $V_{\text{DD(P)}}$  or  $V_{\text{DD(I2C-bus)}}$  depending on the application. When any current input port state differs from its corresponding input port register state, the interrupt output pin is asserted (logic 0) to indicate the system master (MCU) that one of input port states has changed. A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the input port register.

In order to enable the interrupt output, the following three conditions must be satisfied:

- The GPIO must be configured as an input port by writing "1" to configuration port registers (0Ch, 0Dh, 0Eh)
- The interrupt mask registers (54h, 55h, 56h) must set to "0" to unmask interrupt sources.
- The interrupt edge registers (60h to 65h) select what action on each input pin will cause an interrupt; there are four different interrupt trigger modes: level trigger, rising-edge trigger, falling-edge trigger, or any edge trigger.

The input latch registers (48h, 49h, 4Ah) control each input pin either to enable latched input state or non-latched input state. When input pin is set to latch state, it will hold or latch the input pin state (keep the logic value) and generate an interrupt until the master can service the interrupt. This minimizes the host's interrupt service response for fast moving inputs.

Any interrupt status bit can be cleared and  $\overline{\text{INT}}$  pin de-asserted by using one of the following methods and conditions:

- Power on reset (POR), hardware reset from  $\overline{\text{RESET}}$  pin, or software reset call
- Read input port registers (00h, 01h, 02h)
- Write logic 1 to interrupt clear registers (68h, 69h, 6Ah)
- Write logic 1 to interrupt mask registers (54h, 55h, 56h)
- Write logic 0 to configuration registers (0Ch, 0Dh, 0Eh), set pin as output port.
- Input pin goes back to its initial state in level trigger and non-latch mode
- Input pin goes back to its initial state in level trigger and change latch to non-latch mode
- Change the interrupt trigger mode from level trigger to edge trigger or vice versa in interrupt edge registers

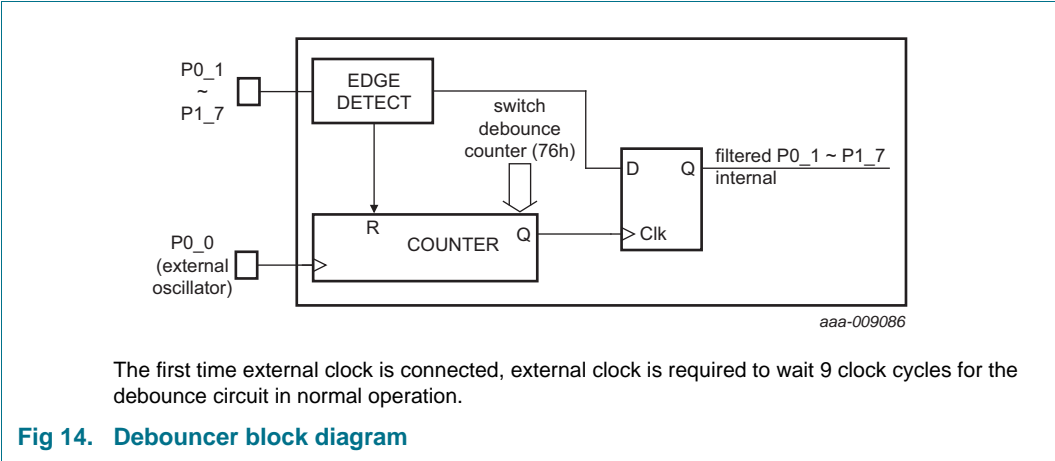
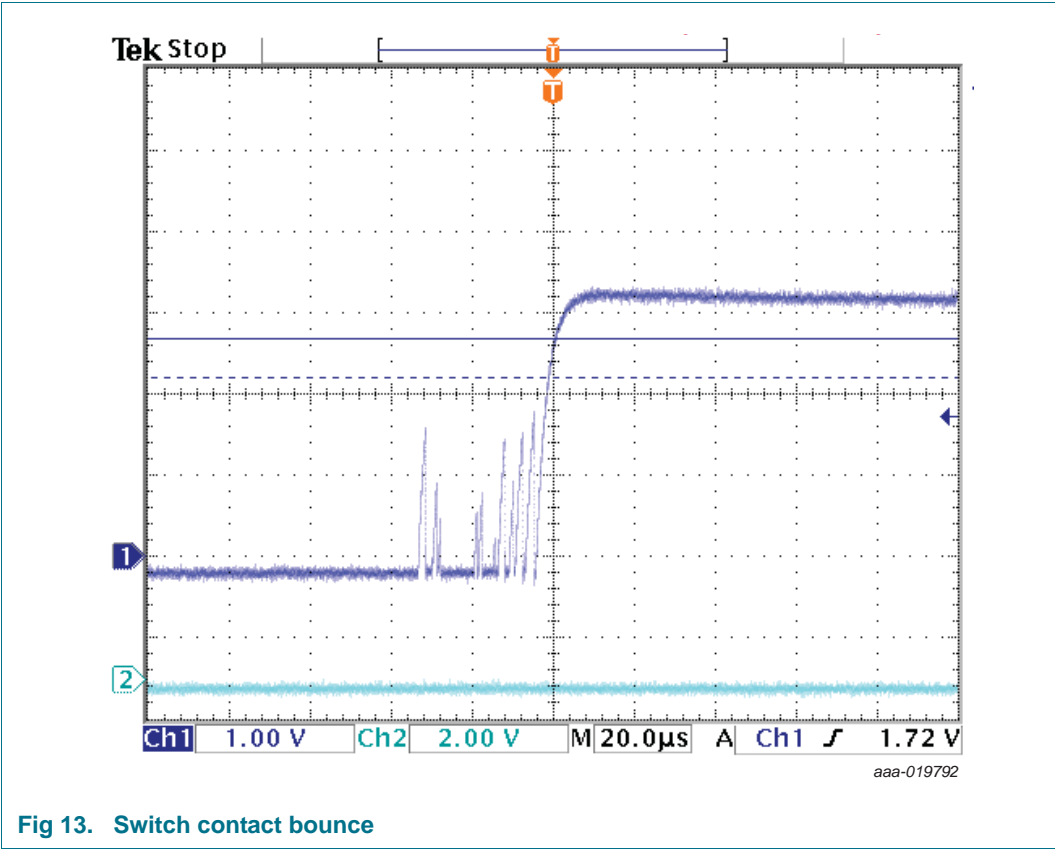
When using the input latch feature, the input pin state is latched. The interrupt is de-asserted only when data is read from the port that generated the interrupt. The interrupt reset occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the inputs after resetting is detected and is transmitted as INT.

## 6.10 Switch debounce circuitry

Mechanical switches do not make clean make-or-break connections and the contacts can 'bounce' for a significant period of time before settling into a steady-state condition. This can confuse fast processors and make the physical interface difficult to design and the software interface difficult to make reliable.

The PCAL6524 implements hardware to ease the hardware interface by debouncing switch closures with dedicated circuitry. P0\_1 to P0\_7, P1\_0 to P1\_7 can connect to this debounce hardware on a pin-by-pin basis. These switch debouncers remove bounce when a switch opens or closes by requiring that sequentially clocked inputs remain in the same state for a number of sampling periods. The output does not change until the input is stable for a programmable duration. The circuit block diagram ([Figure 14](#)) shows the functional blocks consisting of an external oscillator, counter, edge detector, and D flip-flop. When the switch input state changes, the edge detector will reset the counter. When the switch input state is stable for the full qualification period, the counter clocks the flip-flop, updating the output. [Figure 15](#) shows the typical opening and closing switch debounce operation timing.

To use the debounce circuitry, set the port pins (P0\_1 to P0\_7, and P1\_0 to P1\_7) with switches attached in the Switch Debounce Enable 0 and 1 registers (74h, 75h). Connect an external oscillator signal on P0\_0, which serves as a time base to the debounce timer. Finally, set a delay time in the Switch Debounce Count register (76h). The combination of time base of the external oscillator and the debounce count sets the qualification debounce period or  $t_{DP}$  in [Figure 15](#). Note that all debounce counters will use the same time base and count, but they all function independently.



The first time external clock is connected, external clock is required to wait 9 clock cycles for the debounce circuit in normal operation.

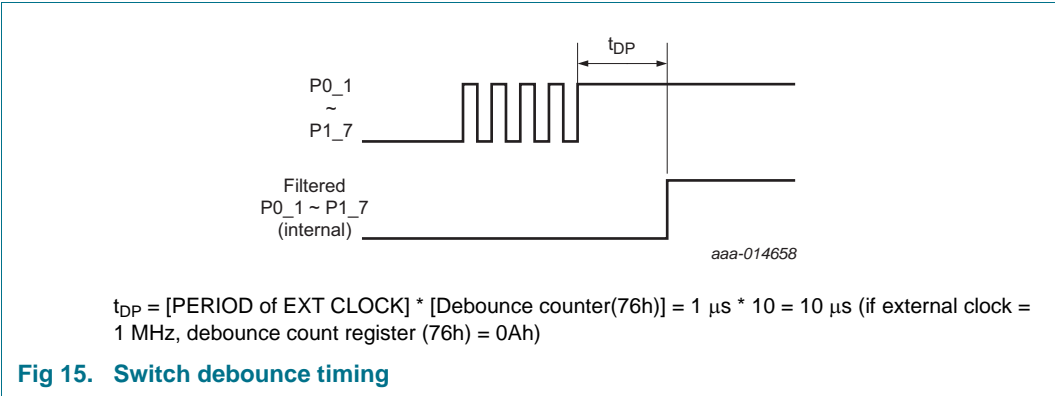


Fig 15. Switch debounce timing

## 7. Bus transactions

The PCAL6524 is an I<sup>2</sup>C-bus slave device. Data is exchanged between the master and PCAL6524 through write and read commands using I<sup>2</sup>C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 7.1 Write commands

Data is transmitted to the PCAL6524 by sending the device address with the Least Significant Bit (LSB) set to a logic 0 (see [Figure 5](#) for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte.

Many of the registers within the PCAL6524 are configured to operate as register triples. The groups are input ports, output ports, polarity inversion and configuration registers, as well as Input latch, Pull-up/pull-down enable and selection registers, Interrupt mask and Interrupt status, Interrupt clear, and Input port (status) without Interrupt clear registers, Individual pin output port configuration registers, and switch debounce registers. After sending data to one register, the next data byte is sent to the next register in the group. For example, if the first byte is sent to Output Port 1 (register 05h), the next byte is stored in Output Port 2 (register 06h). The next byte sent is stored in Output Port 0 (register 04h) and the next byte will overwrite Output Port 1 (register 05h). Since every new write access after a STOP condition requires a Command byte, which sets the Pointer register, the next new write access will be to an arbitrary register.

There is no limit on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register group independently of the other registers or the host can simply update a single register.

There are two 6-register groups: Output drive strength (40h to 45h) and interrupt edge (60h to 65h) registers which can be programmed continuously in this group.

There is one register that is not part of a register group: Output port configuration (5Ch). When this register is accessed multiple times, the register address remains fixed on the same address.

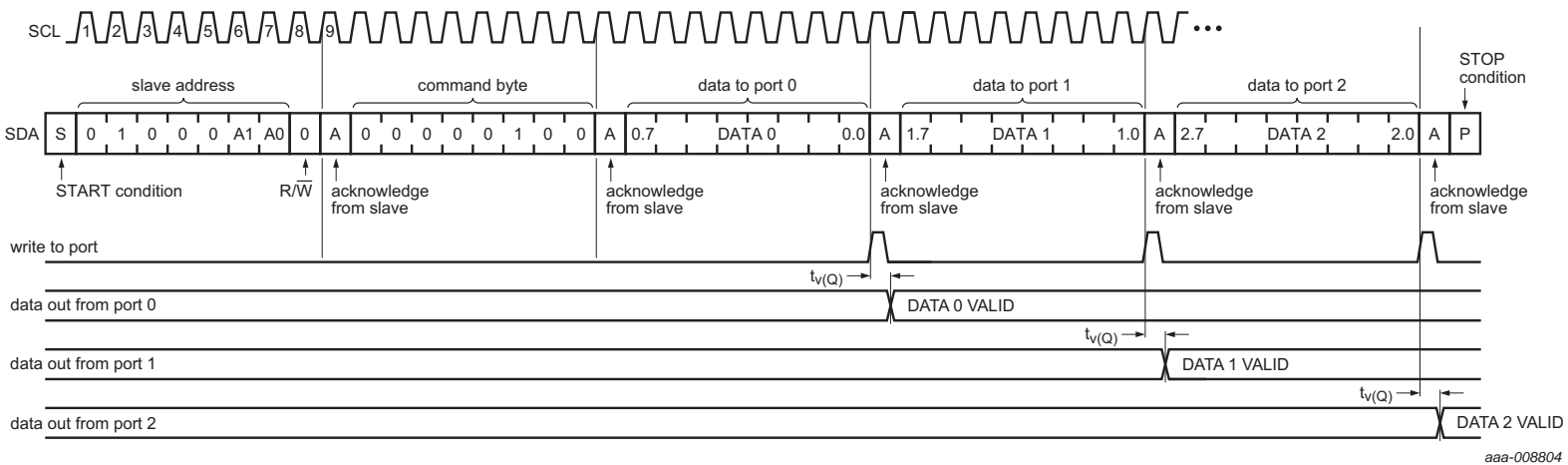


Fig 16. Write to Output port register

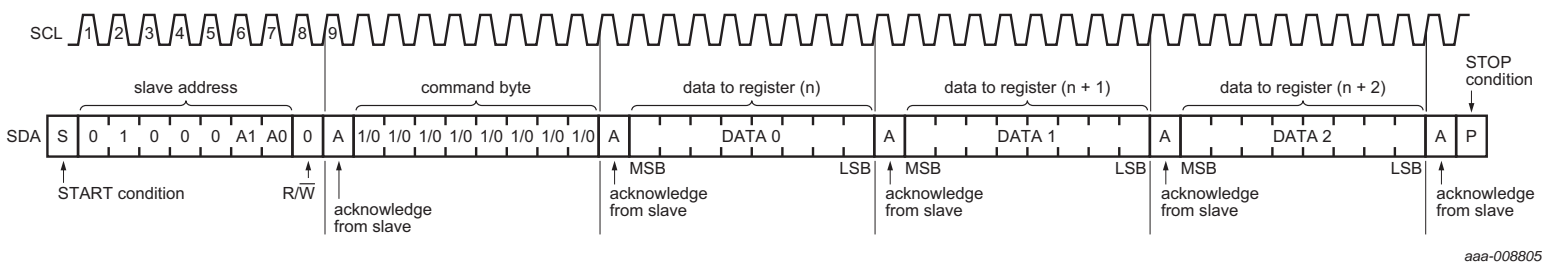


Fig 17. Write to device registers (operate as register triples)



## 7.2 Read commands

To read data from the PCAL6524, the bus master must first send the PCAL6524 address with the least significant bit set to a logic 0 (see [Figure 5](#) for device address).

The command byte is sent after the address and determines which register is to be accessed.

After a restart or a STOP followed by a START condition, the device address is sent again, but this time the least significant bit is set to a logic 1 to read data. Data from the register defined by the command byte is sent by the PCAL6524 (see [Figure 18](#) to [Figure 21](#)). Additional bytes may be read after the first byte read is complete and will reflect the next register in the group. For example, if Input Port 1 is read, the next byte read is Input Port 2. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

After a subsequent restart or a STOP followed by a START condition, the command byte contains the value of the next register to be read in the group. For example, if Input Port 1 was read last before the restart, the register that is read after the restart is the Input Port 2.

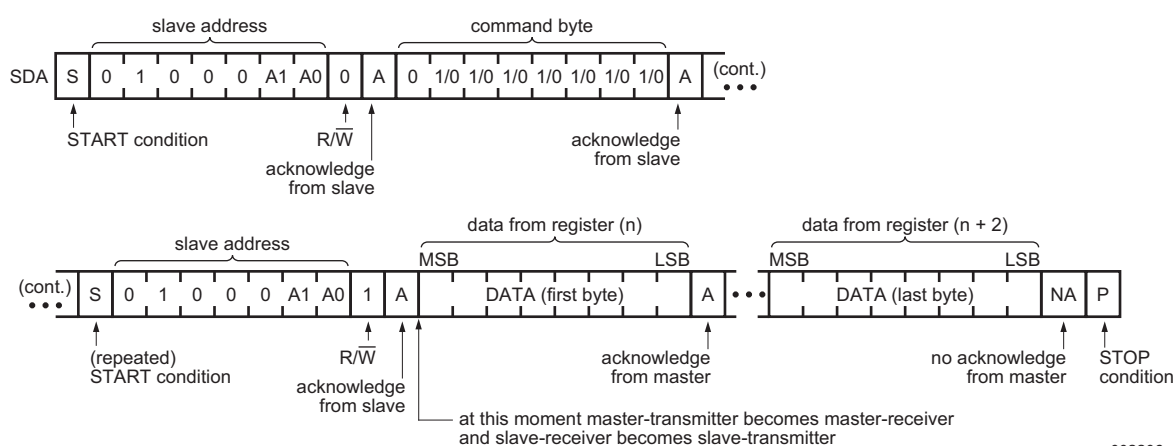
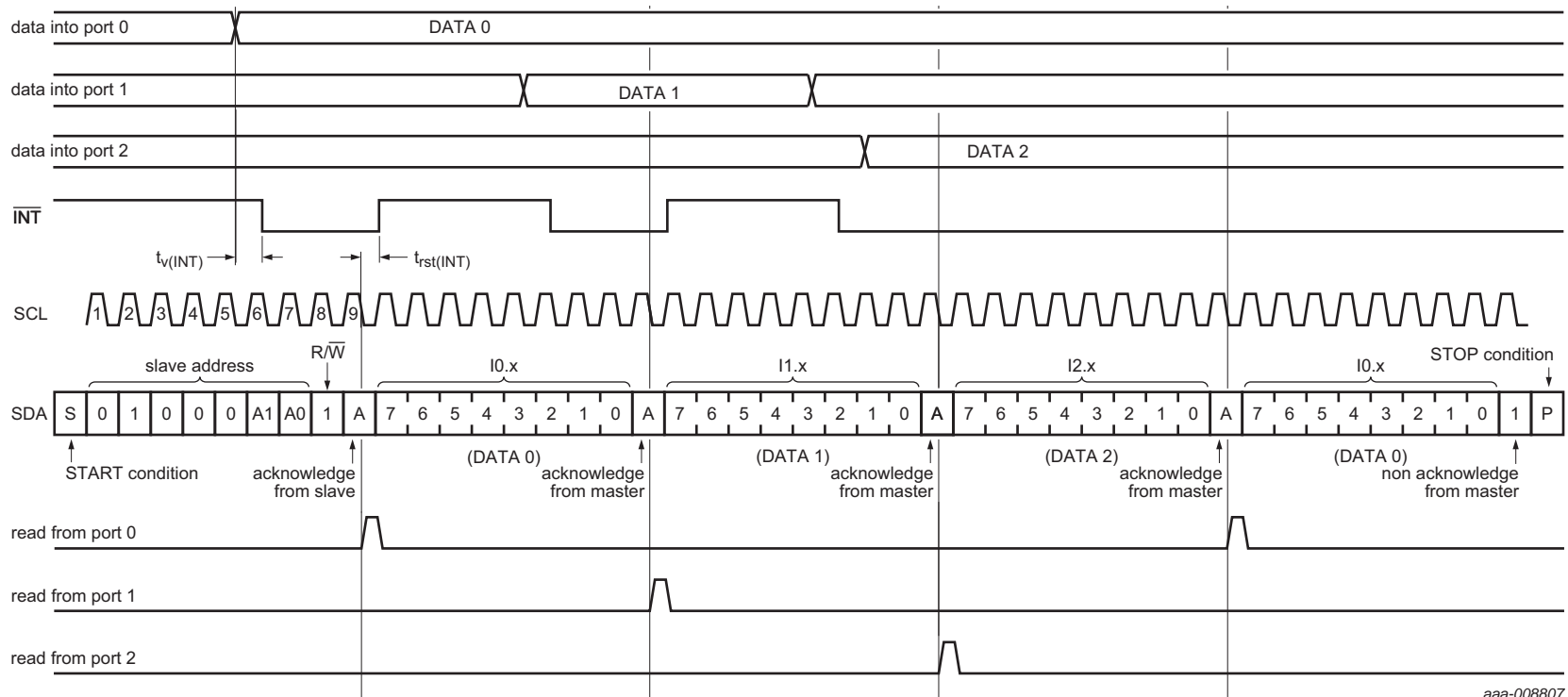


Fig 18. Read from device registers (operate as register triples)

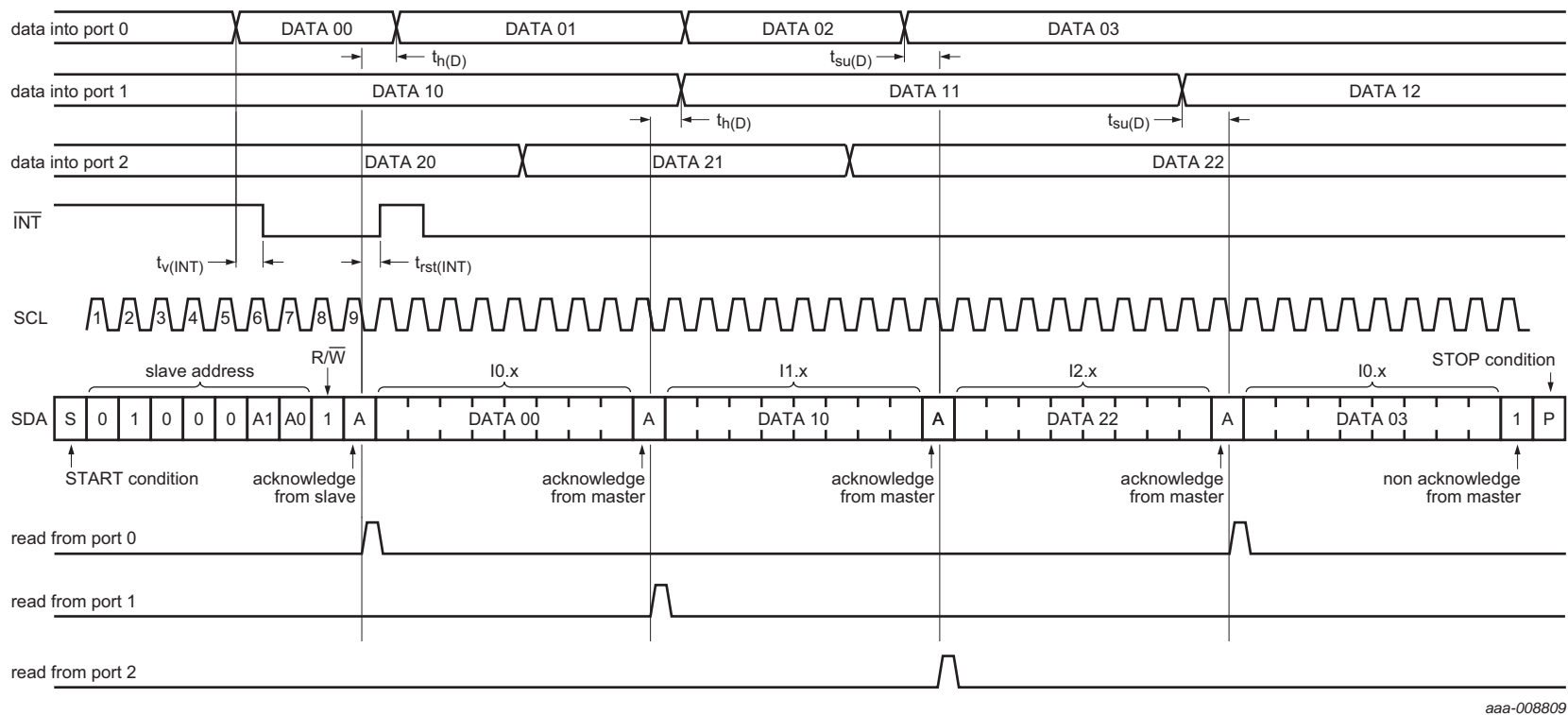


aaa-008807

**Remark:** Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfers and a restart between the initial slave address call and actual data transfer from P port (see [Figure 18](#)).

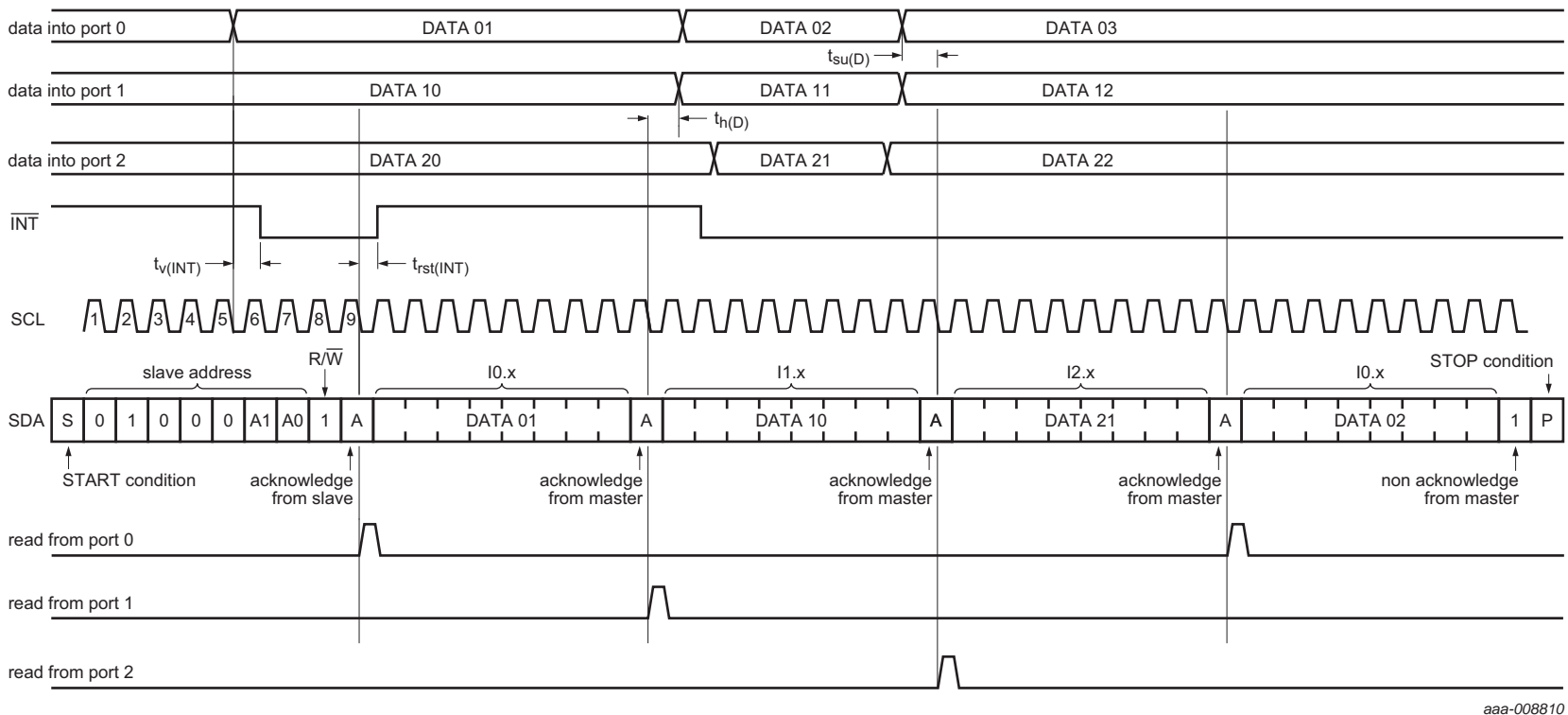
**Fig 19. Read input port register (non-latched), scenario 1**



**Remark:** Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfers and a restart between the initial slave address call and actual data transfer from P port (see [Figure 18](#)).

**Fig 20. Read input port register (non-latched), scenario 2**

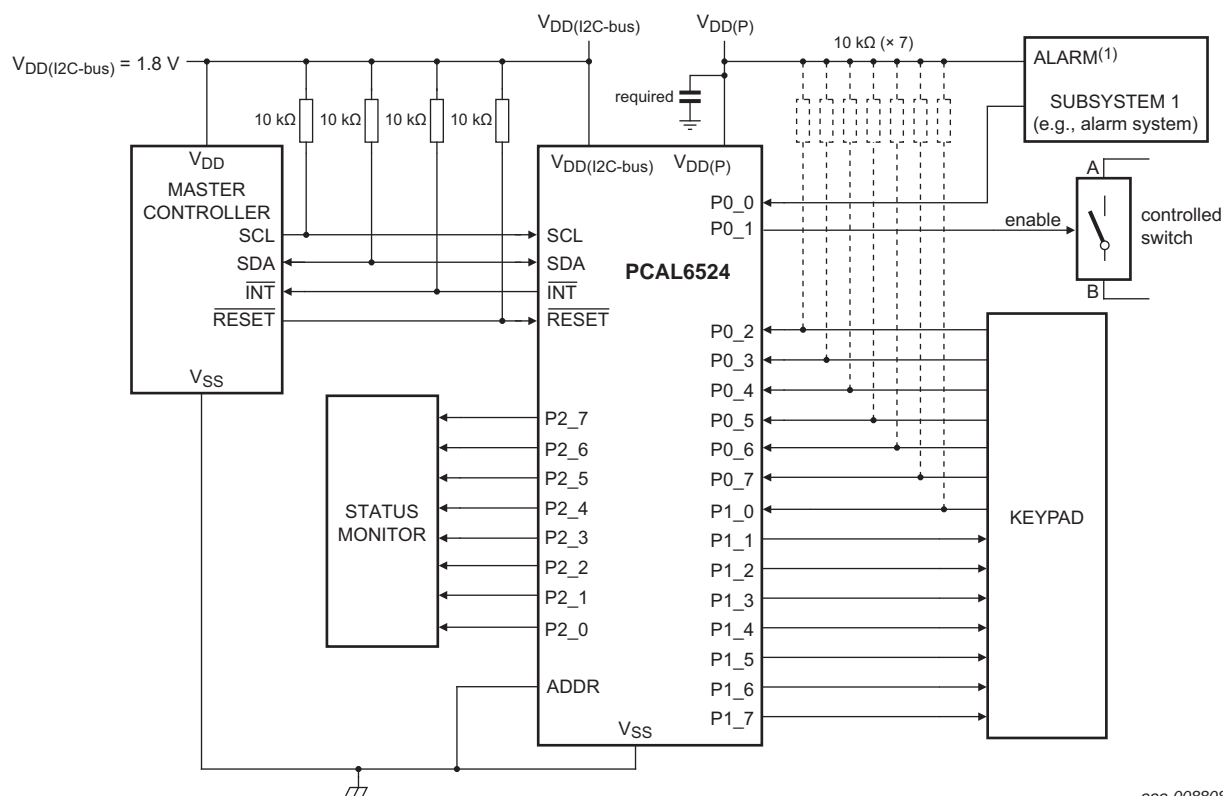


**Remark:** Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfers and a restart between the initial slave address call and actual data transfer from P port (see [Figure 18](#)).

**Fig 21. Read input port register (latch enabled), scenario 3**

## 8. Application design-in information



aaa-008808

Device address configured as 0100 010x for this example.

P0\_0 and P0\_2 through P1\_0 are configured as inputs.

P0\_1 and P1\_1 through P1\_7, and P2\_0 through P2\_7 are configured as outputs.

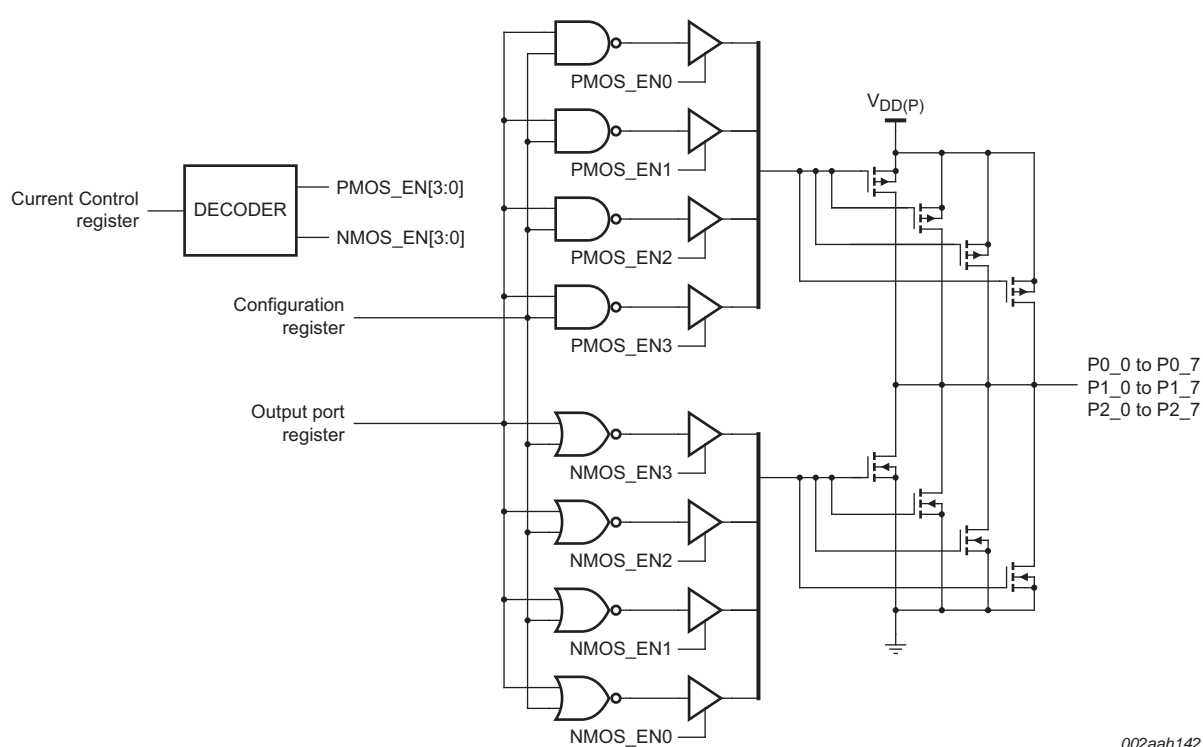
- (1) External resistors are required for inputs (on P port) that may float. If a driver to an input will never let the input float, a resistor is not needed with internal pull-up or pull-down resistor option. If an output in the P port is configured as an output, there is no need for external pull-up resistors.

**Fig 22. Typical application**

## 8.1 Output drive strength control

The Output drive strength registers allow the user to control the output drive level of the GPIO. Each GPIO can be configured independently to one of the four possible output current levels. By programming these bits the user is changing the number of transistor pairs or 'fingers' that drive the I/O pad.

[Figure 23](#) shows a simplified output stage. The behavior of the pad is affected by the Configuration register, the output port data, and the current control register. When the Current Control register bits are programmed to 01b, then only two of the fingers are active, reducing the current drive capability by 50 %.



**Fig 23. Simplified output stage**

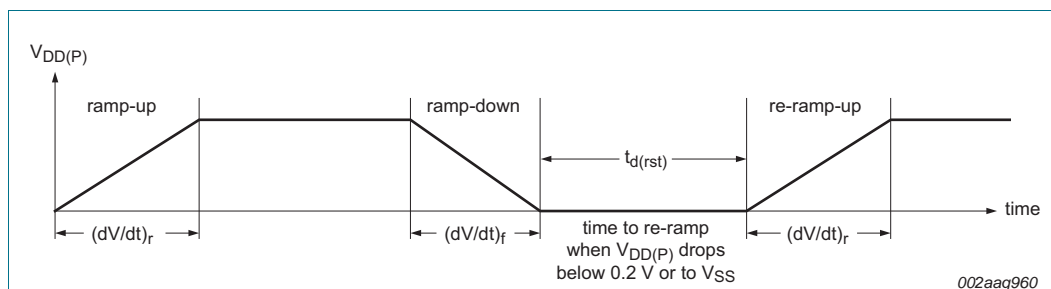
Reducing the current drive capability may be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. This peak current runs through  $V_{DD}$  and  $V_{SS}$  package inductance and will create noise (some radiated, but more critically Simultaneous Switching Noise (SSN)). In other words, switching many outputs at the same time will create ground and supply noise. The output drive strength control through the Output Drive Strength registers allows the user to mitigate SSN issues without the need of additional external components.

In any case, a 0.1 uF bypass capacitor is required on the  $V_{DD(P)}$  pin, located as close to the package as practical.

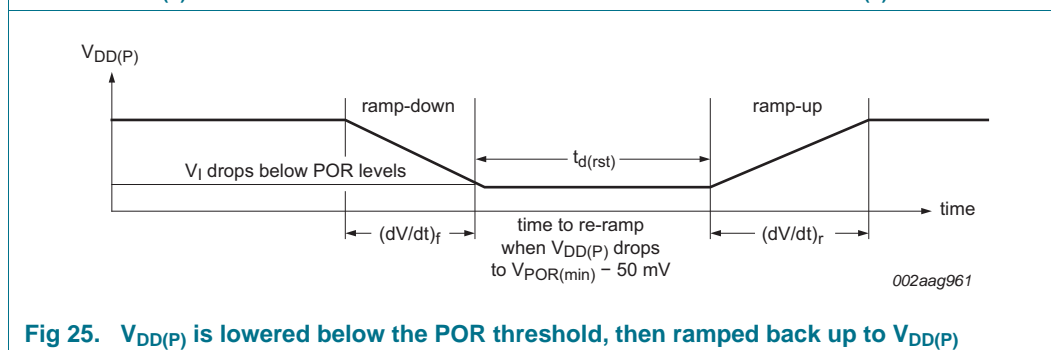
## 8.2 Power-on reset requirements

In the event of a glitch or data corruption, PCAL6524 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 24](#) and [Figure 25](#).



**Fig 24.  $V_{DD(P)}$  is lowered below 0.2 V or to 0 V and then ramped up to  $V_{DD(P)}$**



**Fig 25.  $V_{DD(P)}$  is lowered below the POR threshold, then ramped back up to  $V_{DD(P)}$**

[Table 60](#) specifies the performance of the power-on reset feature for PCAL6524 for both types of power-on reset.

**Table 60. Recommended supply sequencing and ramp rates**

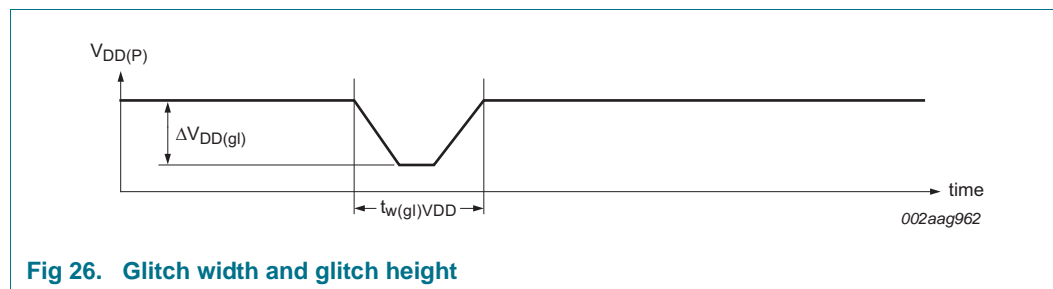
$T_{amb} = 25 \text{ }^{\circ}\text{C}$  (unless otherwise noted). Not tested; specified by design.

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$(dV/dt)_f$	fall rate of change of voltage	<a href="#">Figure 24</a>	0.1	-	2000	ms
$(dV/dt)_r$	rise rate of change of voltage	<a href="#">Figure 24</a>	0.1	-	2000	ms
$t_{d(rst)}$	reset delay time	<a href="#">Figure 24</a> ; re-ramp time when $V_{DD(P)}$ drops below 0.2 V or to $V_{SS}$	1	-	-	$\mu\text{s}$
		<a href="#">Figure 25</a> ; re-ramp time when $V_{DD(P)}$ drops to $V_{POR(min)} - 50 \text{ mV}$	1	-	-	$\mu\text{s}$
$\Delta V_{DD(gl)}$	glitch supply voltage difference	<a href="#">Figure 26</a> [1]	-	-	1.0	V
$t_{w(gl)VDD}$	supply voltage glitch pulse width	<a href="#">Figure 26</a> [2]	-	-	10	$\mu\text{s}$
$V_{POR(trip)}$	power-on reset trip voltage	falling $V_{DD(P)}$	0.7	-	-	V
		rising $V_{DD(P)}$	-	-	1.5	V

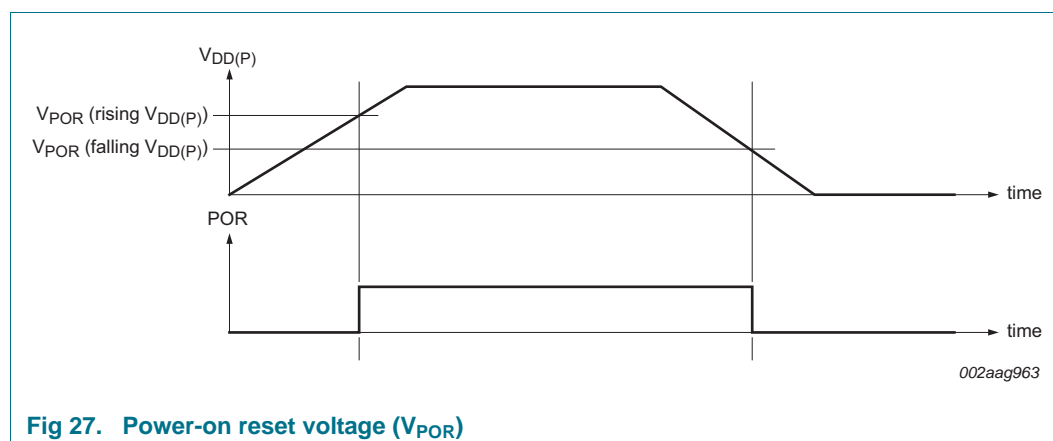
[1] Level that  $V_{DD(P)}$  can glitch down to with a ramp rate at  $0.4 \mu\text{s/V}$ , but not cause a functional disruption when  $t_{w(gl)VDD} < 1 \mu\text{s}$ .

[2] Glitch width that will not cause a functional disruption when  $\Delta V_{DD(gl)} = 0.5 \times V_{DD(P)}$ .

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width ( $t_{w(gl)VDD}$ ) and glitch height ( $\Delta V_{DD(gl)}$ ) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 26](#) and [Table 60](#) provide more information on how to measure these specifications.



$V_{POR}$  is critical to the power-on reset.  $V_{POR}$  is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C-bus/SMBus state machine are initialized to their default states. The value of  $V_{POR}$  differs based on the  $V_{DD}$  being lowered to or from 0 V. [Figure 27](#) and [Table 60](#) provide more details on this specification.



### 8.3 Device current consumption with internal pull-up and pull-down resistors

The PCAL6524 integrates programmable pull-up and pull-down resistors to eliminate external components when pins are configured as inputs and pull-up or pull-down resistors are required (for example, nothing is driving the inputs to the power supply rails. Since these pull-up and pull-down resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

The pull-up or pull-down function is selected in registers 50h, 51h and 52h, while the resistor is connected by the enable registers 4Ch, 4Dh and 4Eh. The configuration of the resistors is shown in [Figure 12](#).

If the resistor is configured as a pull-up, that is, connected to  $V_{DD}$ , a current will flow from the  $V_{DD(P)}$  pin through the resistor to ground when the pin is held LOW. This current will appear as additional  $I_{DD}$  upsetting any current consumption measurements.



In the same manner, if the resistor is configured as a pull-down and the pin is held HIGH, current will flow from the power supply through the pin to the  $V_{SS}$  pin. While this current will not be measured as part of  $I_{DD}$ , one must be mindful of the 200 mA limiting value through  $V_{SS}$ .

The pull-up and pull-down resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 k $\Omega$  with a nominal 100 k $\Omega$  value. Any current flow through these resistors is additive by the number of pins held HIGH or LOW and the current can be calculated by Ohm's law. See [Figure 31](#) for a graph of supply current vs the number of pull-up resistors.

## 8.4 I<sup>2</sup>C-bus error recovery techniques

There are a number of techniques to recover from error conditions on the I<sup>2</sup>C-bus. Slave devices like the PCAL6524 use a state machine to implement the I<sup>2</sup>C protocol and expect a certain sequence of events to occur to function properly. Unexpected events at the I<sup>2</sup>C master can wreak havoc with the slaves connected on the bus. However, it is usually possible to recover deterministically to a known bus state with careful protocol manipulation.

A hard slave reset, either through power-on reset or by activating the  $\overline{RESET}$  pin, will set the device back into the default state. Of course, this means the input/output pins and their configuration will be lost, which might cause some system issues.

A STOP condition, which is only initiated by the master, will reset the slave state machine into a known condition where SDA is not driven LOW by the slave and logically, the slave is waiting for a START condition. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH.

If the master is interrupted during a packet transmission, the slave may be sending data or performing an Acknowledge, driving the I<sup>2</sup>C-bus SDA line LOW. Since SDA is LOW, it effectively blocks any other I<sup>2</sup>C-bus transaction. A deterministic method to clear this situation, once the master recognizes a 'stuck bus' state, is for the master to blindly transmit nine clocks on SCL. If the slave was transmitting data or acknowledging, nine or more clocks ensures the slave state machine returns to a known, idle state since the protocol calls for eight data bits and one ACK bit. It does not matter when the slave state machine finishes its transmission, extra clocks will be recognized as STOP conditions.

The PCAL6524 SCL pin is an input only. If SCL is stuck LOW, then only the bus master or a slave performing a clock stretch operation can cause this condition.

With careful design of the bus master error recovery firmware, many I<sup>2</sup>C-bus protocol problems can be avoided.

## 9. Limiting values

**Table 61. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(I2C-bus)}$	I <sup>2</sup> C-bus supply voltage		-0.5	+4.0	V
$V_{DD(P)}$	supply voltage port P		-0.5	+6.5	V
$V_{I(P)}$	input voltage on all ports	[1]	-0.5	+6.5	V
$V_{O(P)}$	output voltage on all ports	[1]	-0.5	+6.5	V
$V_{I(I)}$	input voltage on I <sup>2</sup> C-bus, $\overline{RESET}$ , ADDR		-0.5	+4.0	V
$V_{O(I)}$	output voltage on I <sup>2</sup> C-bus, $\overline{INT}$		-0.5	+4.0	V
$I_{IK}$	input clamping current	ADDR, $\overline{RESET}$ , SCL; $V_I < 0$ V	-	±20	mA
$I_{OK}$	output clamping current	$\overline{INT}$ ; $V_O < 0$ V	-	±20	mA
$I_{IOK}$	input/output clamping current	P port; $V_O < 0$ V or $V_O > V_{DD(P)}$	-	±20	mA
		SDA; $V_O < 0$ V or $V_O > V_{DD(I2C-bus)}$	-	±20	mA
$I_{OL}$	LOW-level output current	continuous; P port; $V_O = 0$ V to $V_{DD(P)}$	-	50	mA
		continuous; SDA, $\overline{INT}$ ; $V_O = 0$ V to $V_{DD(I2C-bus)}$	-	25	mA
$I_{OH}$	HIGH-level output current	continuous; P port; $V_O = 0$ V to $V_{DD(P)}$	-	25	mA
$I_{DD}$	supply current	continuous through $V_{SS}$	-	200	mA
$I_{DD(P)}$	supply current port P	continuous through $V_{DD(P)}$	-	160	mA
$I_{DD(I2C-bus)}$	I <sup>2</sup> C-bus supply current	continuous through $V_{DD(I2C-bus)}$	-	10	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_{j(max)}$	maximum junction temperature		-	125	°C

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 10. Recommended operating conditions

Table 62. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(I2C-bus)}$	I <sup>2</sup> C-bus supply voltage		0.8	3.6	V
$V_{DD(P)}$	supply voltage port P	A 0.1 uF bypass capacitor is required on $V_{DD(P)}$ pin as close to the package as practical	1.65	5.5	V
$V_{IH}$	HIGH-level input voltage	SCL, SDA, $\overline{RESET}$ , ADDR			
		$V_{DD(I2C-bus)} \leq 1.1\text{ V}$	$0.8 \times V_{DD(I2C-bus)}$	3.6	V
		$V_{DD(I2C-bus)} > 1.1\text{ V}$	$0.7 \times V_{DD(I2C-bus)}$	3.6	V
		P2_7 to P0_0	$0.7 \times V_{DD(P)}$	5.5	V
$V_{IL}$	LOW-level input voltage	SCL, SDA, $\overline{RESET}$ , ADDR			
		$V_{DD(I2C-bus)} \leq 1.1\text{ V}$	-0.5	$0.2 \times V_{DD(I2C-bus)}$	V
		$V_{DD(I2C-bus)} > 1.1\text{ V}$	-0.5	$0.3 \times V_{DD(I2C-bus)}$	V
		P2_7 to P0_0	-0.5	$0.3 \times V_{DD(P)}$	V
$I_{OH}$	HIGH-level output current	P2_7 to P0_0	-	10	mA
$I_{OL}$	LOW-level output current	P2_7 to P0_0	-	25	mA
$T_{amb}$	ambient temperature	operating in free air	-40	+85	°C

## 11. Thermal characteristics

**Table 63. Thermal characteristics**

Symbol	Parameter	Conditions	Value (typ)	Unit
R <sub>th(j-a)</sub>	Thermal resistance from junction to ambient on a JEDEC 2S2P board <sup>[1]</sup>	TSSOP32 package	78.1	°C/W
		HUQFN32 package	34.6	°C/W

[1] The package thermal resistance is calculated in accordance with JESD 51-7.

## 12. Static characteristics

**Table 64. Static characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{DD(I2C-bus)} = 0.8\text{ V}$  to  $3.6\text{ V}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>IK</sub>	input clamping voltage	I <sub>I</sub> = -18 mA	-1.2	-	-	V
V <sub>POR</sub>	power-on reset voltage	V <sub>I</sub> = V <sub>DD(P)</sub> or V <sub>SS</sub> ; I <sub>O</sub> = 0 mA	-	1.2	1.5	V
V <sub>OH</sub>	HIGH-level output voltage <sup>[2]</sup>	P port; I <sub>OH</sub> = -8 mA; CCX.X = 11b				
		V <sub>DD(P)</sub> = 1.65 V	1.2	-	-	V
		V <sub>DD(P)</sub> = 2.3 V	1.8	-	-	V
		V <sub>DD(P)</sub> = 3 V	2.6	-	-	V
		V <sub>DD(P)</sub> = 4.5 V	4.1	-	-	V
		P port; I <sub>OH</sub> = -2.5 mA and CCX.X = 00b; I <sub>OH</sub> = -5 mA and CCX.X = 01b; I <sub>OH</sub> = -7.5 mA and CCX.X = 10b; I <sub>OH</sub> = -10 mA and CCX.X = 11b;				
		V <sub>DD(P)</sub> = 1.65 V	1.1	-	-	V
		V <sub>DD(P)</sub> = 2.3 V	1.7	-	-	V
		V <sub>DD(P)</sub> = 3 V	2.5	-	-	V
		V <sub>DD(P)</sub> = 4.5 V	4.0	-	-	V
V <sub>OL</sub>	LOW-level output voltage <sup>[2]</sup>	P port; I <sub>OL</sub> = 8 mA; CCX.X = 11b				
		V <sub>DD(P)</sub> = 1.65 V	-	-	0.45	V
		V <sub>DD(P)</sub> = 2.3 V	-	-	0.25	V
		V <sub>DD(P)</sub> = 3 V	-	-	0.25	V
		V <sub>DD(P)</sub> = 4.5 V	-	-	0.20	V
		P port; I <sub>OL</sub> = 2.5 mA and CCX.X = 00b; I <sub>OL</sub> = 5 mA and CCX.X = 01b; I <sub>OL</sub> = 7.5 mA and CCX.X = 10b; I <sub>OL</sub> = 10 mA and CCX.X = 11b;				
		V <sub>DD(P)</sub> = 1.65 V	-	-	0.5	V
		V <sub>DD(P)</sub> = 2.3 V	-	-	0.3	V
		V <sub>DD(P)</sub> = 3 V	-	-	0.25	V
		V <sub>DD(P)</sub> = 4.5 V	-	-	0.2	V

Table 64. Static characteristics ...continued

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{DD(I2C-bus)} = 0.8\text{ V}$  to  $3.6\text{ V}$ ; unless otherwise specified.

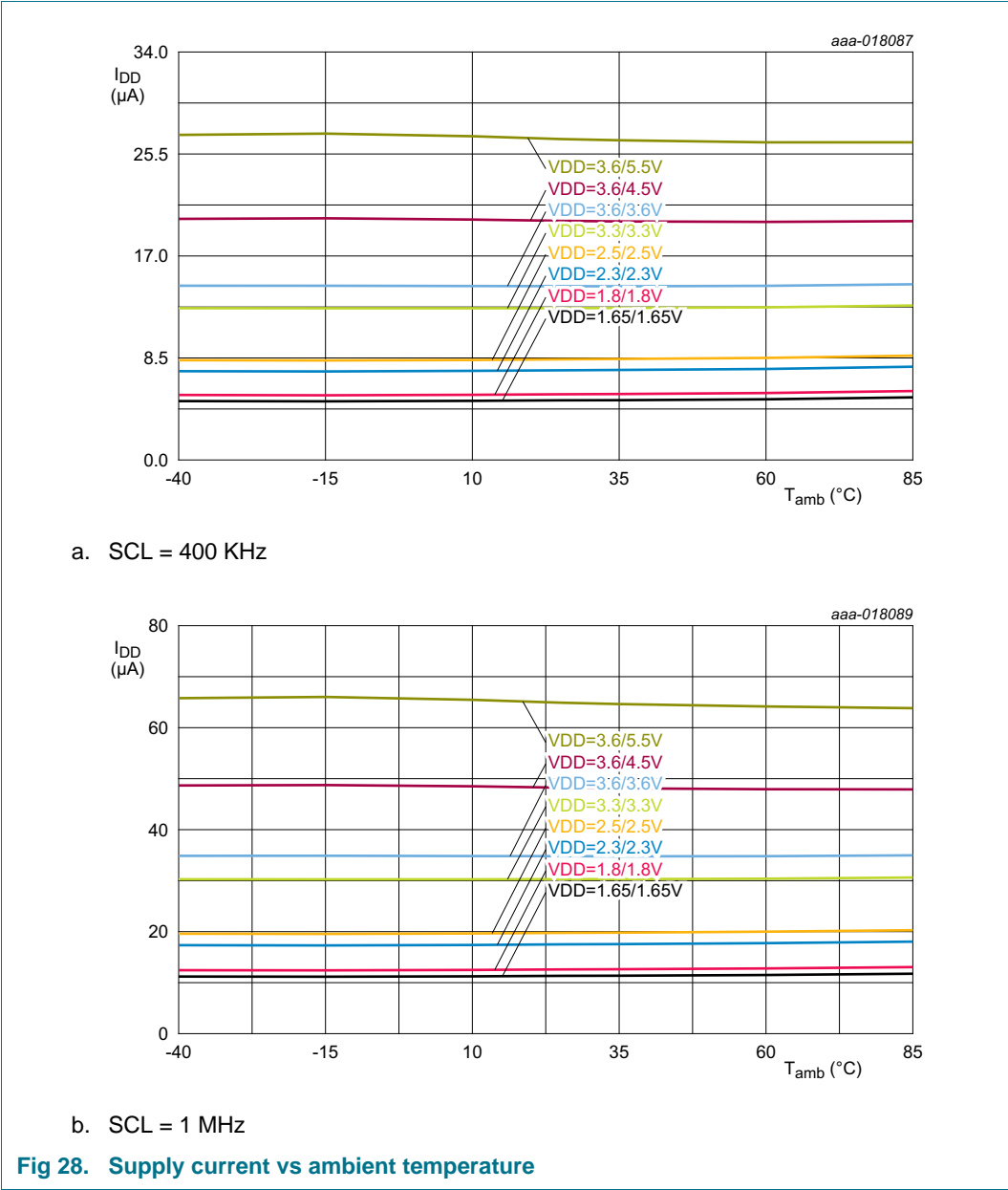
Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$I_{OL}$	LOW-level output current <sup>[3]</sup>	SDA				
		$V_{OL} = 0.4\text{ V}$ ; $V_{DD(I2C-bus)} \leq 2\text{ V}$	15	-	-	mA
		$V_{OL} = 0.4\text{ V}$ ; $V_{DD(I2C-bus)} > 2\text{ V}$	20	-	-	mA
		$\overline{\text{INT}}$ ; $V_{OL} = 0.4\text{ V}$ ; $V_{DD(P)} = 1.65\text{ V}$ to $5.5\text{ V}$	3	<sup>[4]</sup>	-	mA
$I_I$	input current	ADDR, SCL, SDA, $\overline{\text{RESET}}$ ; $V_{DD(P)} = 1.65\text{ V}$ to $5.5\text{ V}$ ; $V_I = V_{DD(I2C-bus)}$ or $V_{SS}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{IH}$	HIGH-level input current	P port; $V_I = V_{DD(P)}$ ; $V_{DD(P)} = 1.65\text{ V}$ to $5.5\text{ V}$	-	-	1	$\mu\text{A}$
$I_{IL}$	LOW-level input current	P port; $V_I = V_{SS}$ ; $V_{DD(P)} = 1.65\text{ V}$ to $5.5\text{ V}$	-	-	1	$\mu\text{A}$
$I_{DD}$	supply current	Clocked mode; $I_{DD(I2C-bus)} + I_{DD(P)}$ ; SDA, P port, ADDR, $\overline{\text{RESET}}$ ; $V_I$ on ADDR, SDA and $\overline{\text{RESET}} = V_{DD(I2C-bus)}$ or $V_{SS}$ ; $V_I$ on P port = $V_{DD(P)}$ ; $I_O = 0\text{ mA}$ ; I/O = inputs				
		$V_{DD(P)} = 3.6\text{ V}$ to $5.5\text{ V}$ ; $f_{SCL} = 0\text{ kHz}$	-	3	7	$\mu\text{A}$
		$V_{DD(P)} = 2.3\text{ V}$ to $3.6\text{ V}$ ; $f_{SCL} = 0\text{ kHz}$	-	2	5	$\mu\text{A}$
		$V_{DD(P)} = 1.65\text{ V}$ to $2.3\text{ V}$ ; $f_{SCL} = 0\text{ kHz}$	-	1.5	3	$\mu\text{A}$
		$V_{DD(P)} = 3.6\text{ V}$ to $5.5\text{ V}$ ; $f_{SCL} = 400\text{ kHz}$	-	27	45	$\mu\text{A}$
		$V_{DD(P)} = 2.3\text{ V}$ to $3.6\text{ V}$ ; $f_{SCL} = 400\text{ kHz}$	-	12	25	$\mu\text{A}$
		$V_{DD(P)} = 1.65\text{ V}$ to $2.3\text{ V}$ ; $f_{SCL} = 400\text{ kHz}$	-	7.5	15	$\mu\text{A}$
		$V_{DD(P)} = 3.6\text{ V}$ to $5.5\text{ V}$ ; $f_{SCL} = 1\text{ MHz}$	-	70	110	$\mu\text{A}$
		$V_{DD(P)} = 2.3\text{ V}$ to $3.6\text{ V}$ ; $f_{SCL} = 1\text{ MHz}$	-	30	60	$\mu\text{A}$
		$V_{DD(P)} = 1.65\text{ V}$ to $2.3\text{ V}$ ; $f_{SCL} = 1\text{ MHz}$	-	20	40	$\mu\text{A}$
		Active mode; $I_{DD(I2C-bus)} + I_{DD(P)}$ ; P port, ADDR, $\overline{\text{RESET}}$ ; $V_I$ on ADDR, $\overline{\text{RESET}} = V_{DD(I2C-bus)}$ ; $V_I$ on P port = $V_{DD(P)}$ ; $I_O = 0\text{ mA}$ ; I/O = inputs; continuous register read				
		$V_{DD(P)} = 3.6\text{ V}$ to $5.5\text{ V}$ ; $f_{SCL} = 400\text{ kHz}$	-	150	250	$\mu\text{A}$
		$V_{DD(P)} = 2.3\text{ V}$ to $3.6\text{ V}$ ; $f_{SCL} = 400\text{ kHz}$	-	120	200	$\mu\text{A}$
		$V_{DD(P)} = 1.65\text{ V}$ to $2.3\text{ V}$ ; $f_{SCL} = 400\text{ kHz}$	-	75	150	$\mu\text{A}$
		$V_{DD(P)} = 3.6\text{ V}$ to $5.5\text{ V}$ ; $f_{SCL} = 1\text{ MHz}$	-	450	625	$\mu\text{A}$
		$V_{DD(P)} = 2.3\text{ V}$ to $3.6\text{ V}$ ; $f_{SCL} = 1\text{ MHz}$	-	270	500	$\mu\text{A}$
		$V_{DD(P)} = 1.65\text{ V}$ to $2.3\text{ V}$ ; $f_{SCL} = 1\text{ MHz}$	-	160	210	$\mu\text{A}$
		with pull-ups enabled; $I_{DD(I2C-bus)} + I_{DD(P)}$ ; P port, ADDR, $\overline{\text{RESET}}$ ; $V_I$ on ADDR, SCL, SDA and $\overline{\text{RESET}} = V_{DD(I2C-bus)}$ or $V_{SS}$ ; $V_I$ on P port = $V_{SS}$ ; $I_O = 0\text{ mA}$ ; I/O = inputs with pull-up enabled; $f_{SCL} = 0\text{ kHz}$				
		$V_{DD(P)} = 1.65\text{ V}$ to $5.5\text{ V}$	-	1.7	2.5	mA
$\Delta I_{DD}$	additional quiescent supply current <sup>[5]</sup>	ADDR, SCL, SDA, $\overline{\text{RESET}}$ ; one input at $V_{DD(I2C-bus)} - 0.6\text{ V}$ , other inputs at $V_{DD(I2C-bus)}$ or $V_{SS}$ ; $V_{DD(P)} = 1.65\text{ V}$ to $5.5\text{ V}$	-	-	25	$\mu\text{A}$
		P port; one input at $V_{DD(P)} - 0.6\text{ V}$ , other inputs at $V_{DD(P)}$ or $V_{SS}$ ; $V_{DD(P)} = 1.65\text{ V}$ to $5.5\text{ V}$	-	-	80	$\mu\text{A}$

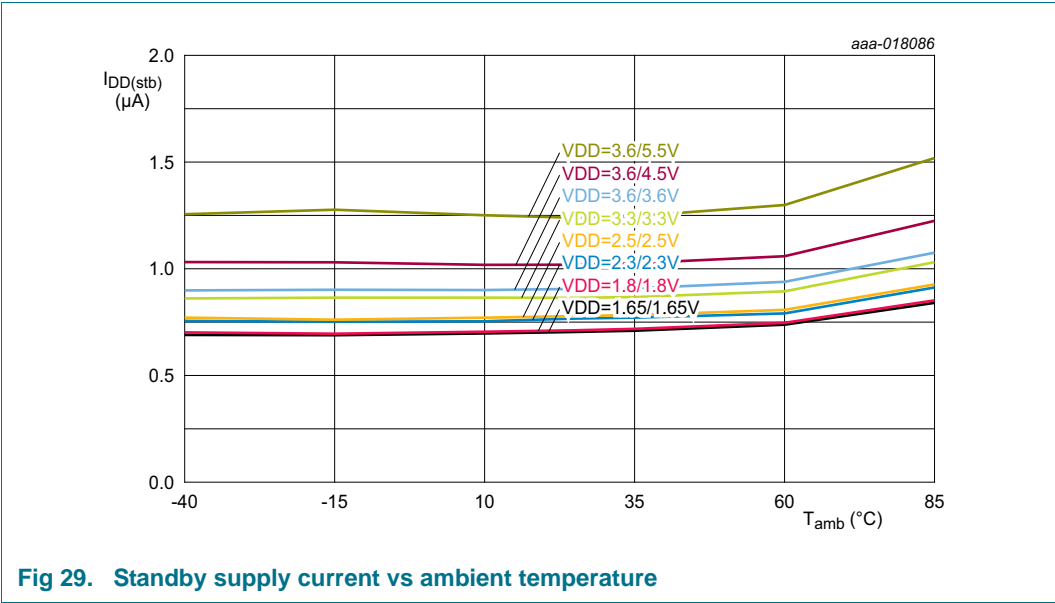
**Table 64. Static characteristics ...continued** $T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{DD(I2C-bus)} = 0.8\text{ V}$  to  $3.6\text{ V}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$C_i$	input capacitance <sup>[6]</sup>	$V_I = V_{DD(I2C-bus)}$ or $V_{SS}$ ; $V_{DD(P)} = 1.65\text{ V}$ to $5.5\text{ V}$	-	6	-	pF
$C_{io}$	input/output capacitance <sup>[6]</sup>	$V_{I/O} = V_{DD(I2C-bus)}$ or $V_{SS}$ ; $V_{DD(P)} = 1.65\text{ V}$ to $5.5\text{ V}$	-	7	-	pF
		$V_{I/O} = V_{DD(P)}$ or $V_{SS}$ ; $V_{DD(P)} = 1.65\text{ V}$ to $5.5\text{ V}$	-	7.5	-	pF
$R_{pu(int)}$	internal pull-up resistance	input/output	50	100	150	k $\Omega$
$R_{pd(int)}$	internal pull-down resistance	input/output	50	100	150	k $\Omega$

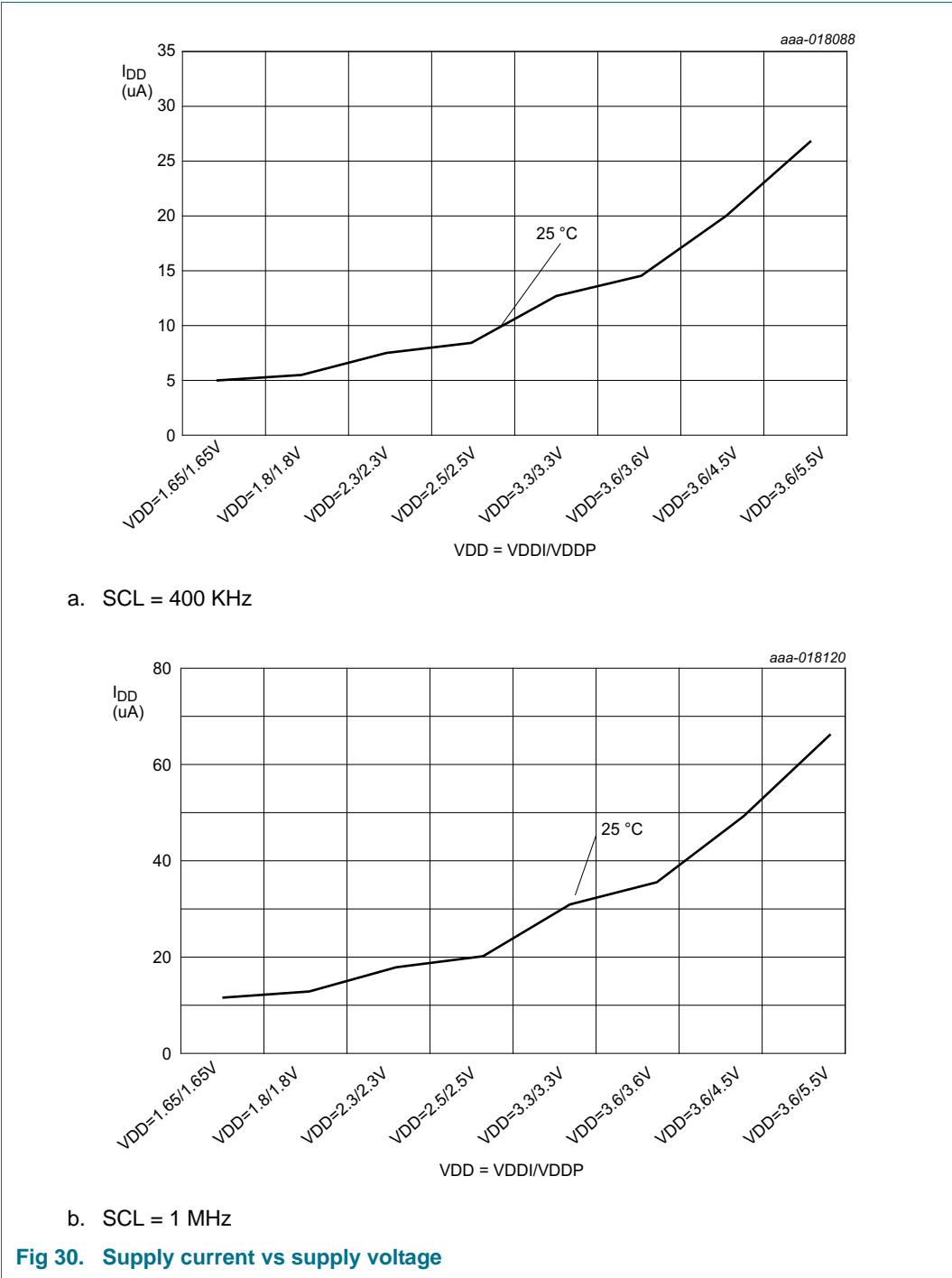
- [1] For  $I_{DD}$ , all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V or 3.6 V  $V_{DD}$ ) and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ . Except for  $I_{DD}$ , the typical values are at  $V_{DD(P)} = V_{DD(I2C-bus)} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .
- [2] The total current sourced by all I/Os must be limited to 160 mA.
- [3] Each I/O must be externally limited to a maximum of 25 mA and each octal (P0\_0 to P0\_7 and P1\_0 to P1\_7) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
- [4] Typical value for  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .  $V_{OL} = 0.4\text{ V}$  and  $V_{DD(I2C-bus)} = V_{DD(P)} = 3.3\text{ V}$ . Typical value for  $V_{DD(I2C-bus)} = V_{DD(P)} < 2.5\text{ V}$ ,  $V_{OL} = 0.6\text{ V}$ .
- [5] Internal pull-up/pull-down resistors disabled.
- [6] Value not tested in production, but guaranteed by design and characterization.

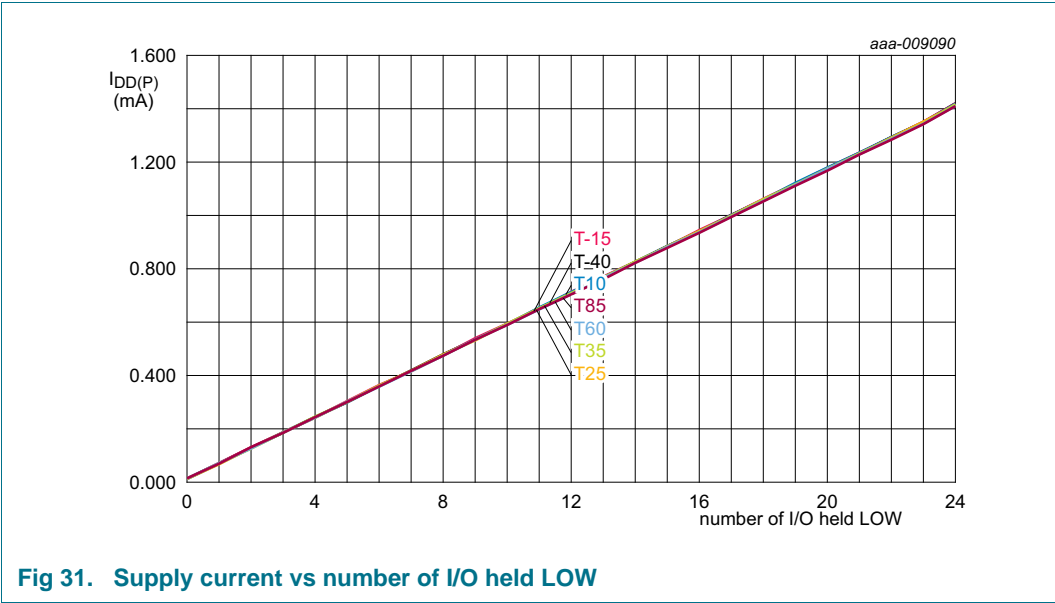
12.1 Typical characteristics

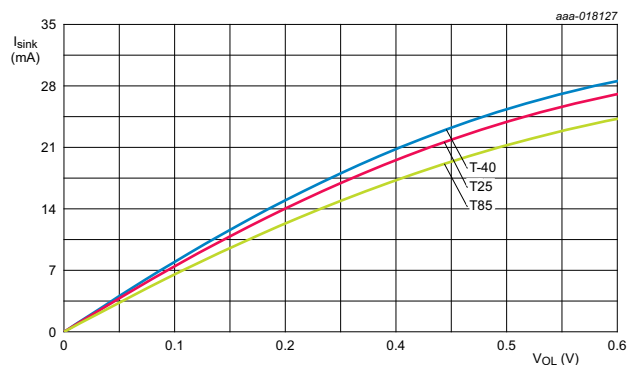




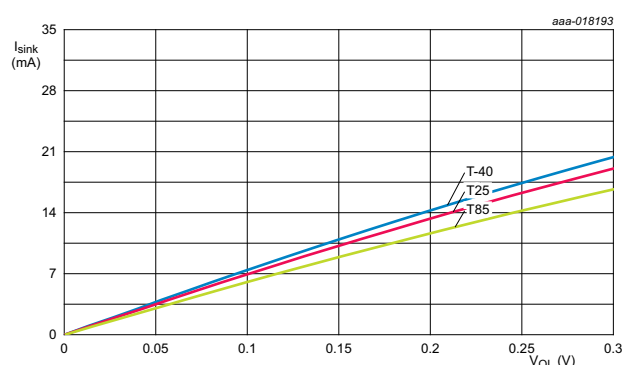




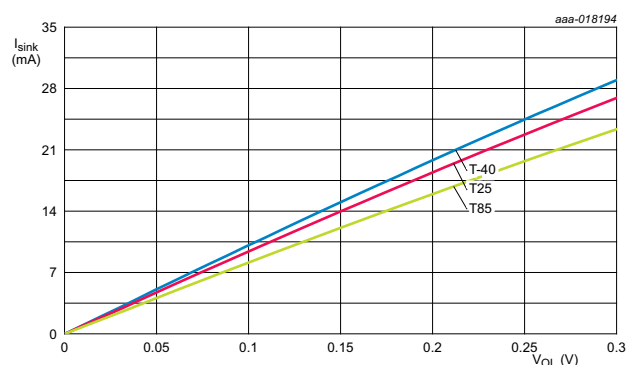




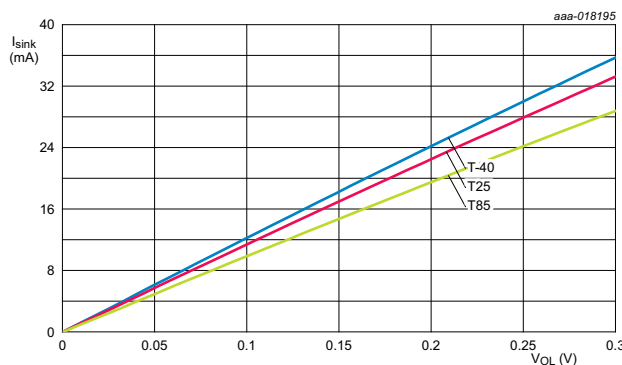
a.  $V_{DD(P)} = 1.65 \text{ V}$



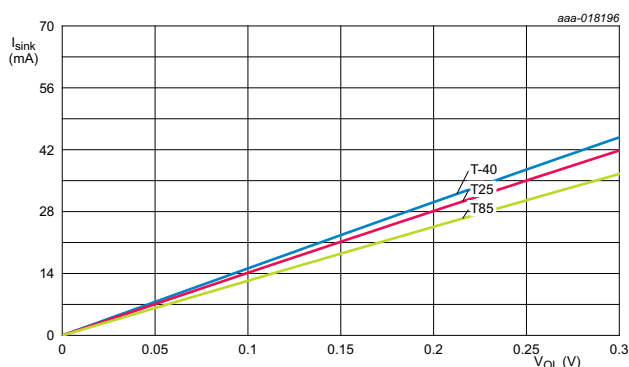
b.  $V_{DD(P)} = 1.8 \text{ V}$



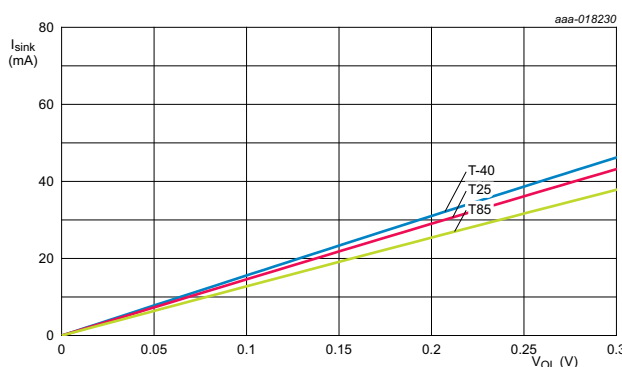
c.  $V_{DD(P)} = 2.5 \text{ V}$



d.  $V_{DD(P)} = 3.3 \text{ V}$

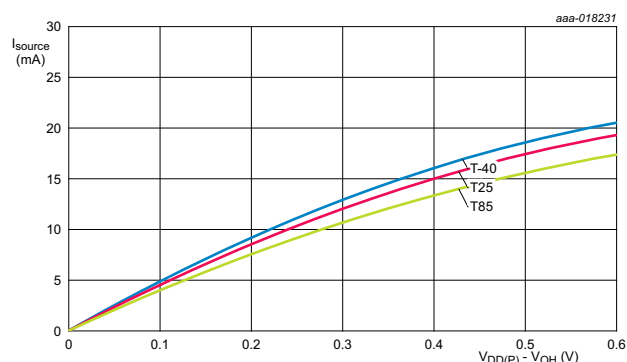


e.  $V_{DD(P)} = 5 \text{ V}$

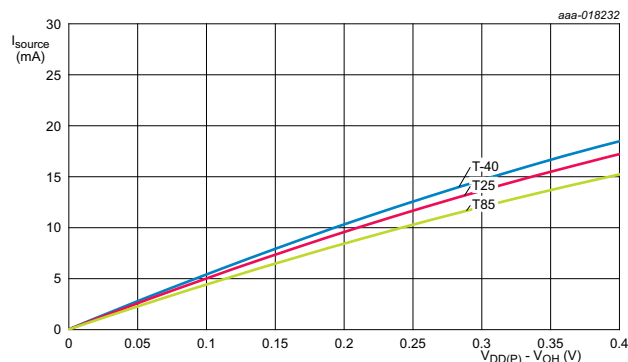


f.  $V_{DD(P)} = 5.5 \text{ V}$

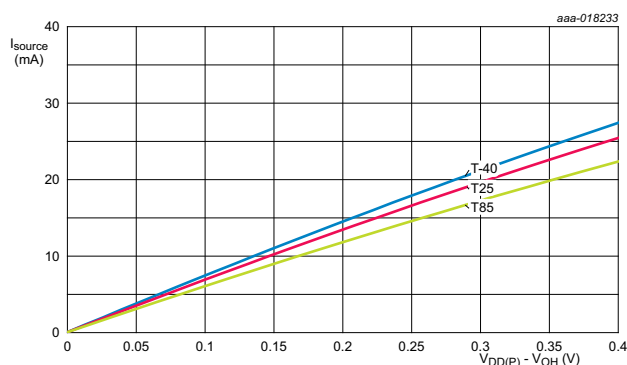
Fig 32. I/O sink current vs LOW-level output voltage



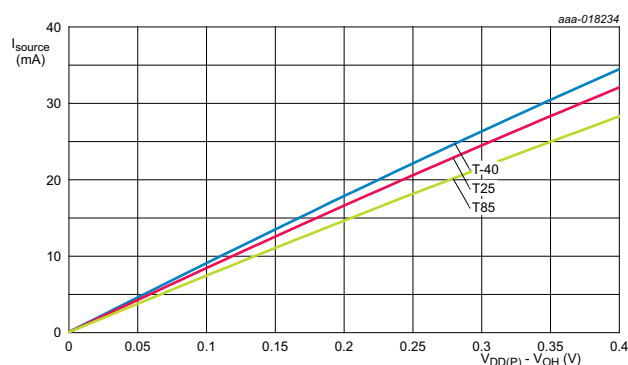
a.  $V_{DD(P)} = 1.65 \text{ V}$



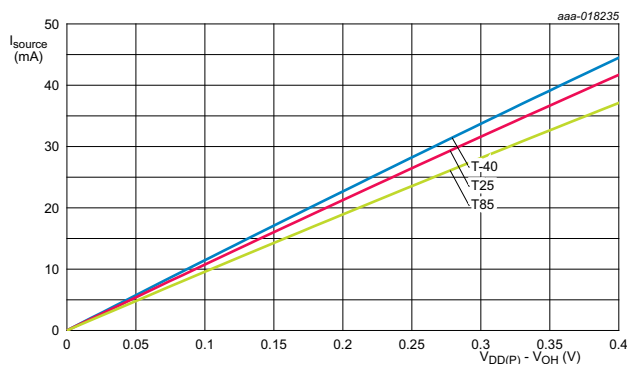
b.  $V_{DD(P)} = 1.8 \text{ V}$



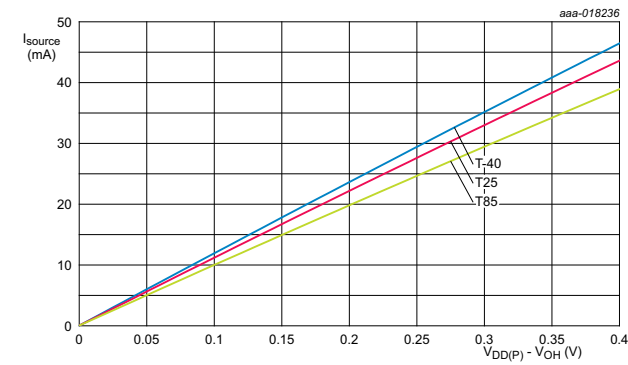
c.  $V_{DD(P)} = 2.5 \text{ V}$



d.  $V_{DD(P)} = 3.3 \text{ V}$

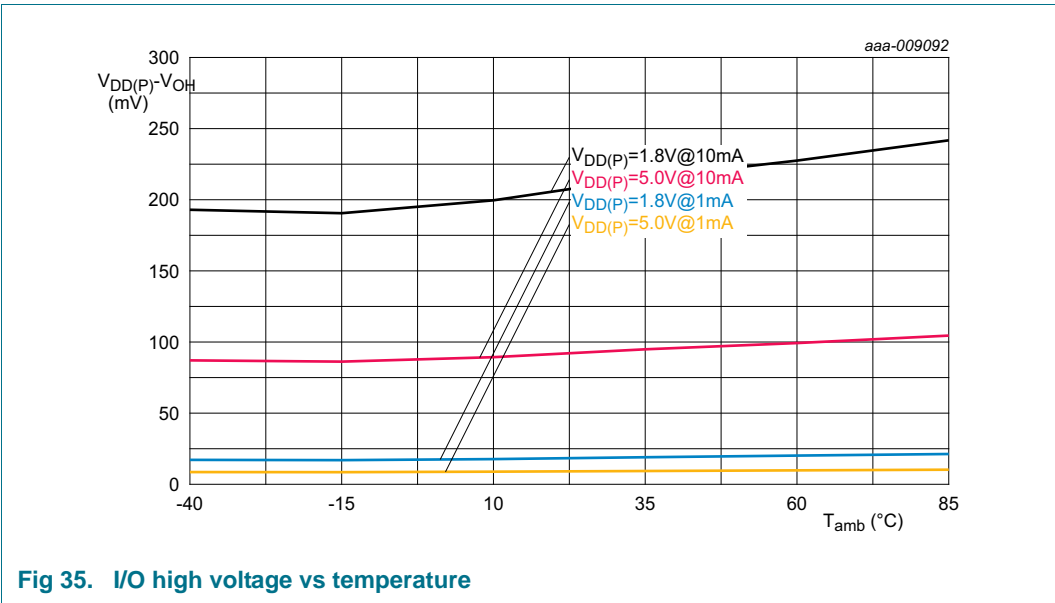
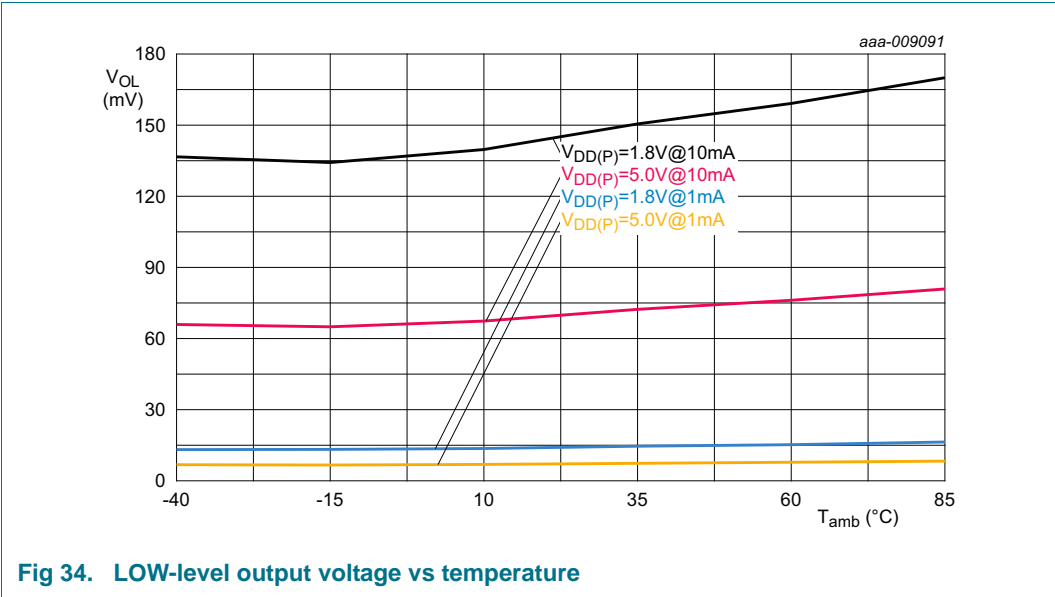


e.  $V_{DD(P)} = 5 \text{ V}$



f.  $V_{DD(P)} = 5.5 \text{ V}$

Fig 33. I/O source current vs HIGH-level output voltage



### 13. Dynamic characteristics

**Table 65. I<sup>2</sup>C-bus interface timing requirements**

Over recommended operating free air temperature range, unless otherwise specified. See [Figure 37](#).

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Fast-mode Plus I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f <sub>SCL</sub>	SCL clock frequency		0	100	0	400	0	1000	kHz
t <sub>HIGH</sub>	HIGH period of the SCL clock		4	-	0.6	-	0.26	-	μs
t <sub>LOW</sub>	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	μs
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter		0	50	0	50	0	50	ns
t <sub>SU;DAT</sub>	data set-up time		250	-	100	-	50	-	ns
t <sub>HD;DAT</sub>	data hold time		0	-	0	-	0	-	ns
t <sub>r</sub>	rise time of both SDA and SCL signals	[1]	-	1000	20	300	-	120	ns
t <sub>f</sub>	fall time of both SDA and SCL signals	[1]	-	300	20 × (V <sub>DD</sub> / 5.5 V)	300	-	120	ns
t <sub>BUF</sub>	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	μs
t <sub>SU;STA</sub>	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	μs
t <sub>HD;STA</sub>	hold time (repeated) START condition		4	-	0.6	-	0.26	-	μs
t <sub>SU;STO</sub>	set-up time for STOP condition		4	-	0.6	-	0.26	-	μs
t <sub>VD;DAT</sub>	data valid time	SCL LOW to SDA output valid	-	3.45	-	0.9	-	0.45	μs
t <sub>VD;ACK</sub>	data valid acknowledge time	ACK signal from SCL LOW to SDA (out) LOW	-	3.45	-	0.9	-	0.45	μs

[1] Value not tested in production, but guaranteed by design and characterization.

**Table 66. Reset timing requirements**

Over recommended operating free air temperature range, unless otherwise specified. See [Figure 39](#).

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Fast-mode Plus I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	Min	Max	
t <sub>w(rst)</sub>	reset pulse width		150	-	150	-	150	-	ns
t <sub>rec(rst)</sub>	reset recovery time		500	-	500	-	500	-	ns
t <sub>rst</sub>	reset time	[1]	600	-	600	-	600	-	ns

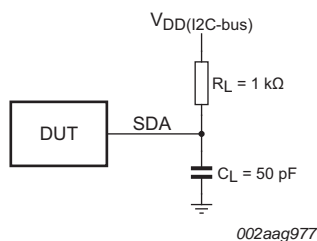
[1] Minimum time for SDA to become HIGH or minimum time to wait before doing a START.

**Table 67. Switching characteristics**

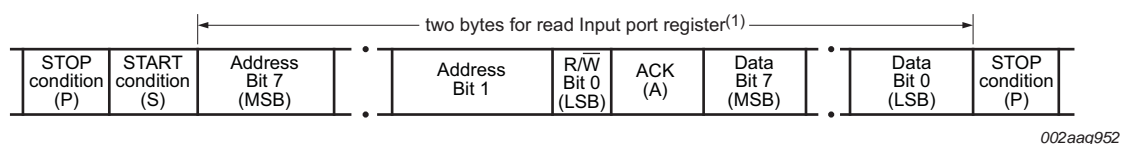
Over recommended operating free air temperature range;  $C_L \leq 100$  pF; unless otherwise specified. See [Figure 38](#).

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Fast-mode Plus I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	Min	Max	
$t_{V(INT)}$	valid time on pin $\overline{INT}$	from P port to $\overline{INT}$	-	1	-	1	-	1	$\mu$ s
$t_{rst(INT)}$	reset time on pin $\overline{INT}$	from SCL to $\overline{INT}$	-	1	-	1	-	1	$\mu$ s
$t_{V(Q)}$	data output valid time	from SCL to P port	-	400	-	400	-	400	ns
$t_{su(D)}$	data input set-up time	from P port to SCL	0	-	0	-	0	-	ns
$t_{h(D)}$	data input hold time	from P port to SCL	300	-	300	-	300	-	ns

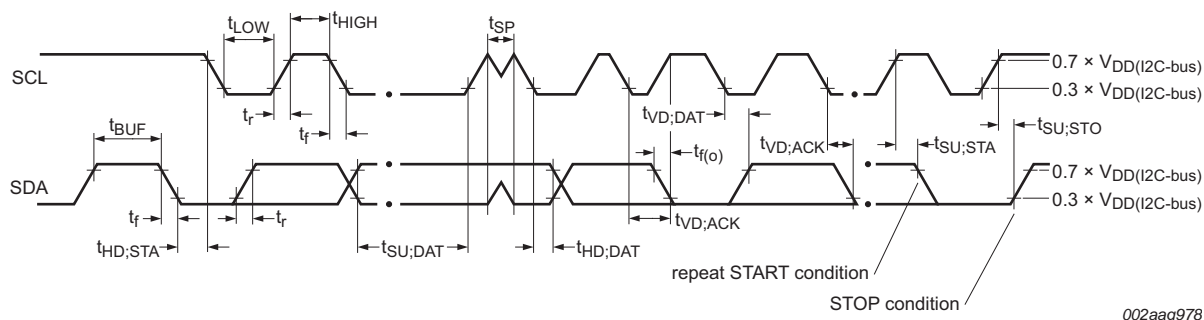
## 14. Parameter measurement information



a. SDA load configuration



b. Transaction format



c. Voltage waveforms

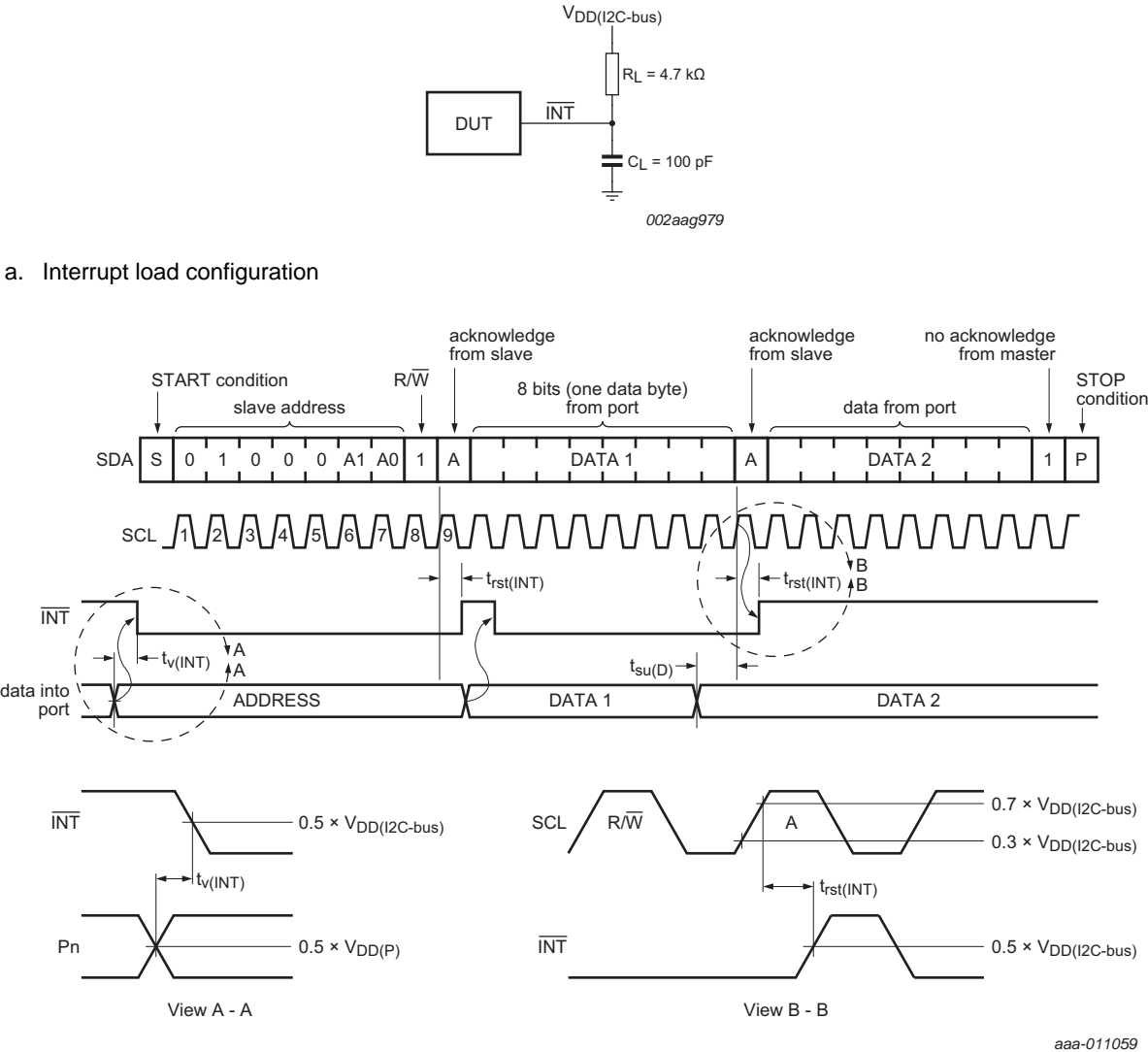
$C_L$  includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz;  $Z_o = 50 \Omega$ ;  $t_r/t_f \leq 30$  ns.

All parameters and waveforms are not applicable to all devices.

Byte 1 = I<sup>2</sup>C-bus address; Byte 2, byte 3 = P port data.

**Fig 36. I<sup>2</sup>C-bus interface load circuit and voltage waveforms**



b. Voltage waveforms

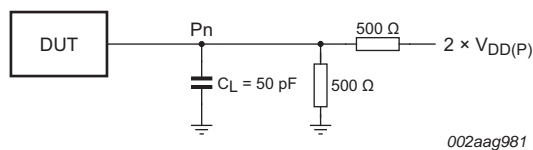
$C_L$  includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ;  $Z_o = 50\ \Omega$ ;  $t_r/t_f \leq 30\text{ ns}$ .

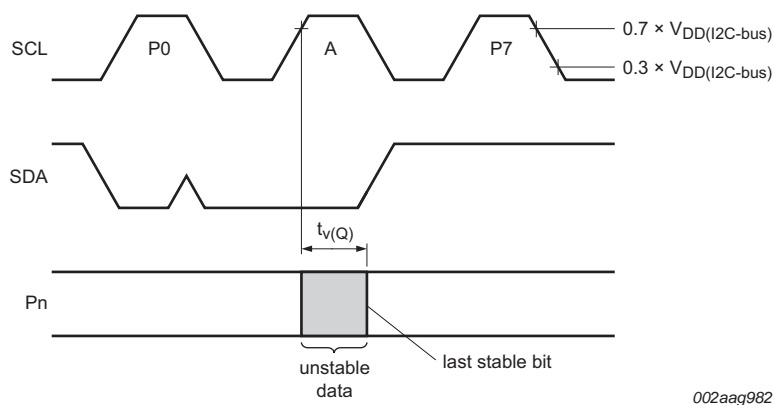
All parameters and waveforms are not applicable to all devices.

**Fig 37. Interrupt load circuit and voltage waveforms**

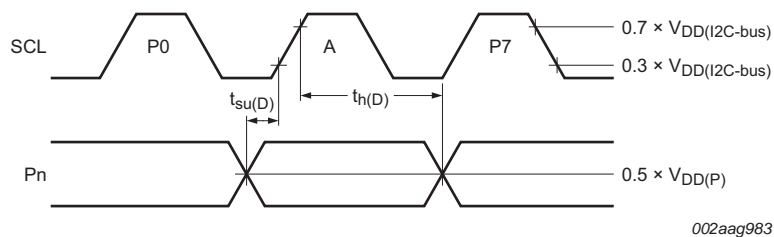




a. P port load configuration



b. Write mode ( $\overline{R/\overline{W}} = 0$ )



c. Read mode ( $\overline{R/\overline{W}} = 1$ )

C<sub>L</sub> includes probe and jig capacitance.

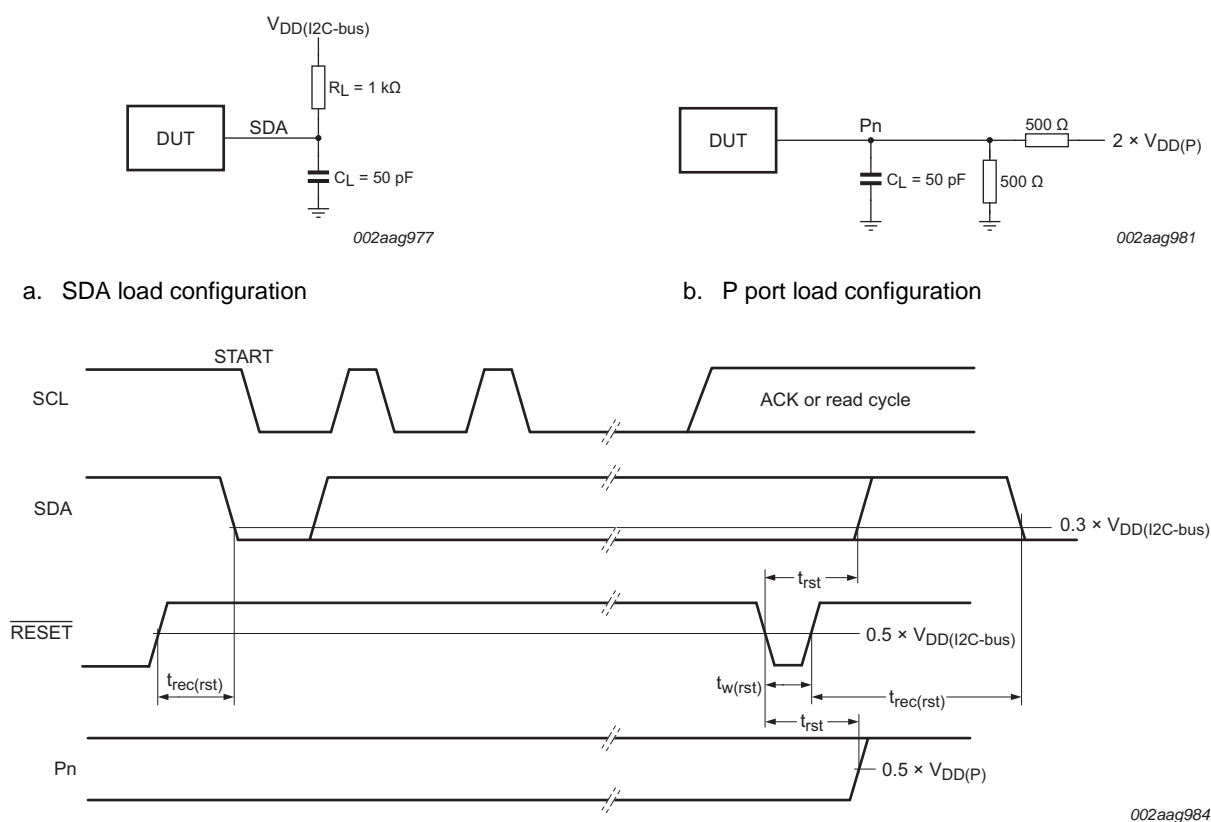
t<sub>v(Q)</sub> is measured from 0.7 × V<sub>DD(I2C-bus)</sub> on SCL to 50 % I/O (P<sub>n</sub>) output.

All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z<sub>o</sub> = 50 Ω; t<sub>r</sub>/t<sub>f</sub> ≤ 30 ns.

The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

Fig 38. P port load circuit and voltage waveforms



### c. RESET timing

$C_L$  includes probe and jig capacitance.

All inputs are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ;  $Z_o = 50 \Omega$ ;  $t_r/t_f \leq 30 \text{ ns}$ .

The outputs are measured one at a time, with one transition per measurement.

I/Os are configured as inputs.

All parameters and waveforms are not applicable to all devices.

**Fig 39. Reset load circuits and voltage waveforms**

15. Package outline

HUQFN32: plastic thermal enhanced ultra thin quad flat package; no leads;  
32 terminals; body 5 x 5 x 0.56 mm

SOT1426-1

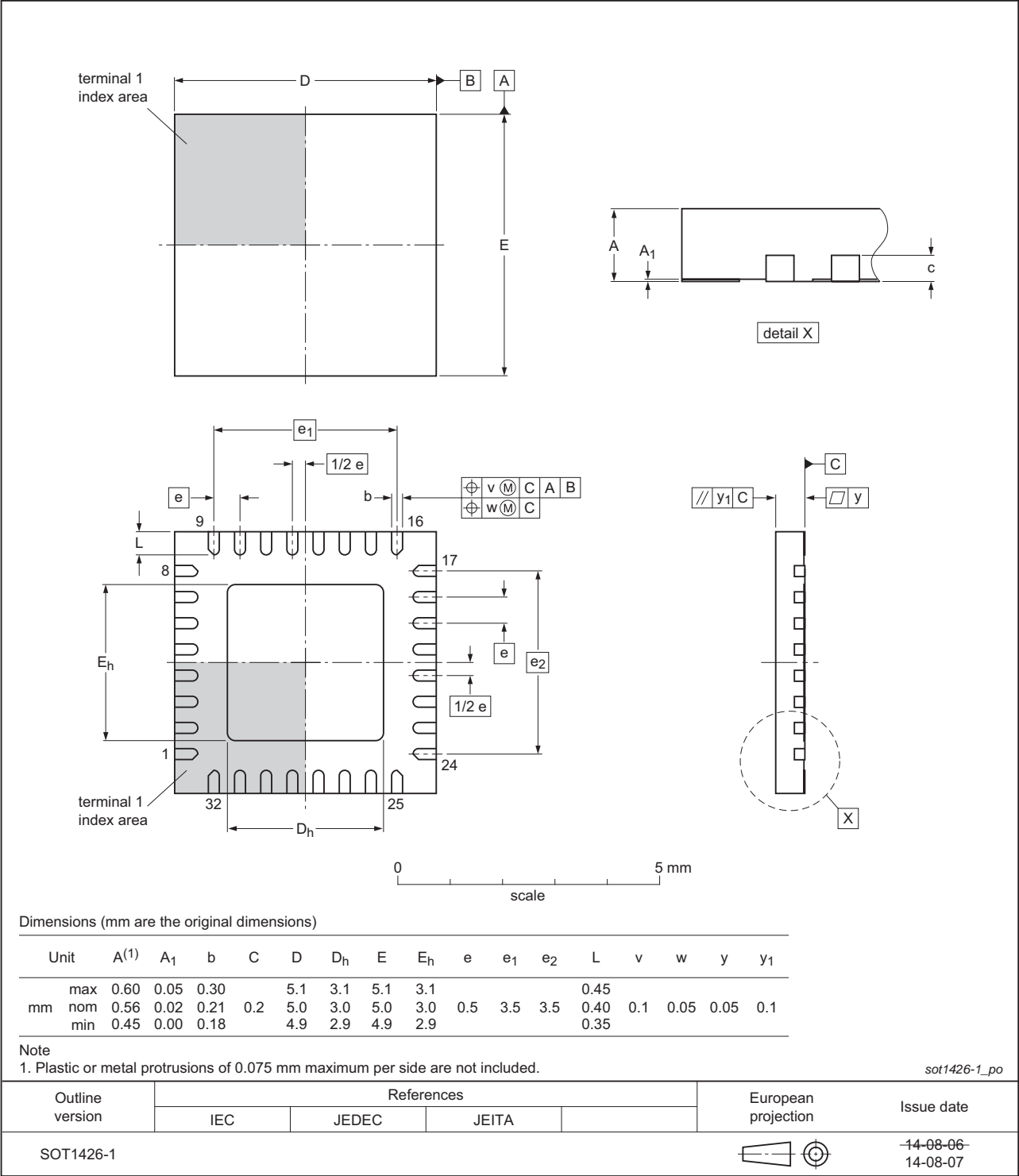


Fig 40. Package outline SOT1426-1 (HUQFN32)

TSSOP32: plastic thin shrink small outline package; 32 leads; body width 6.1 mm;  
lead pitch 0.65 mm

SOT487-1

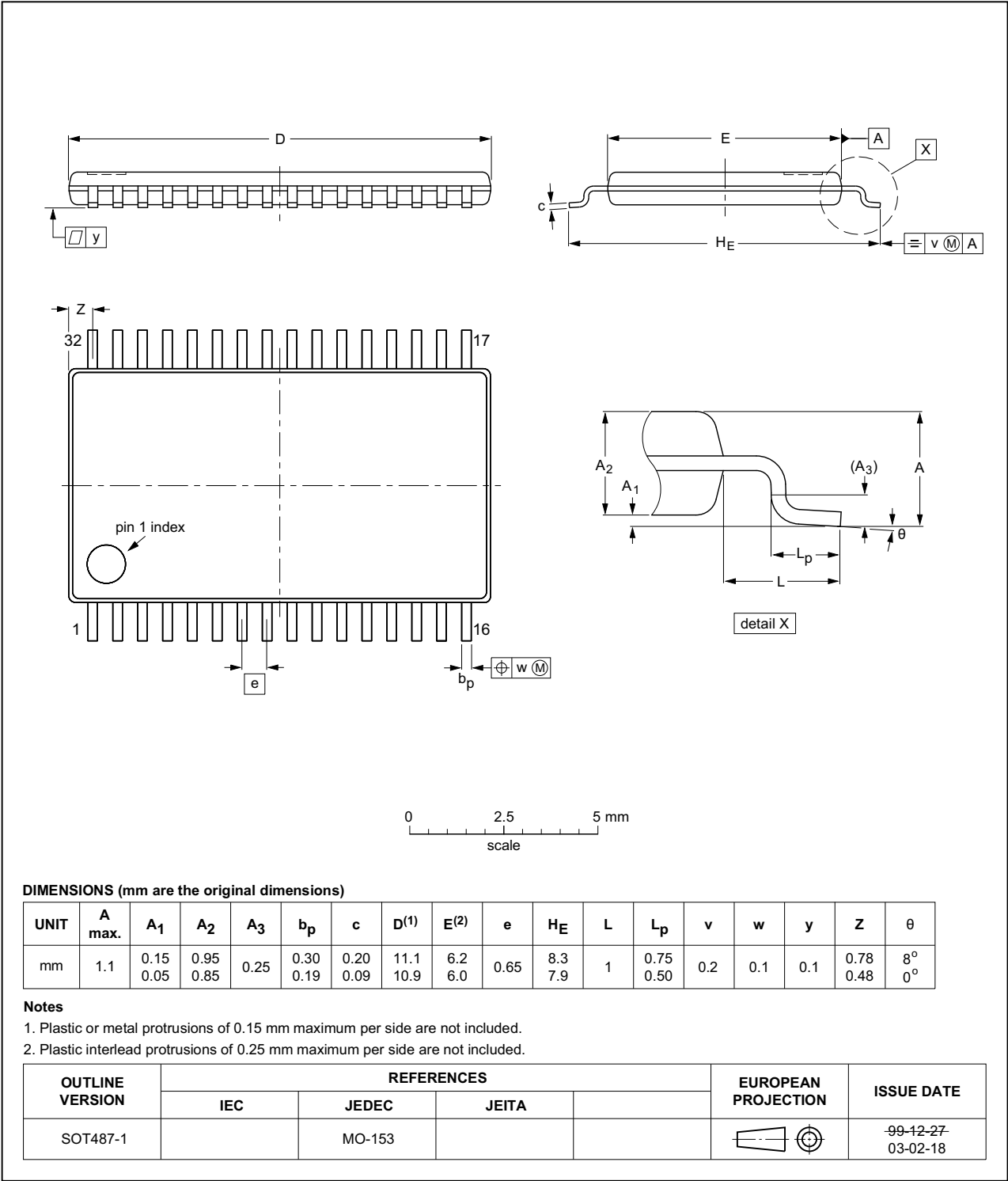


Fig 41. Package outline SOT487-1 (TSSOP32)

VFBGA36: plastic very thin fine-pitch ball grid array package; 36 balls

SOT1851-1

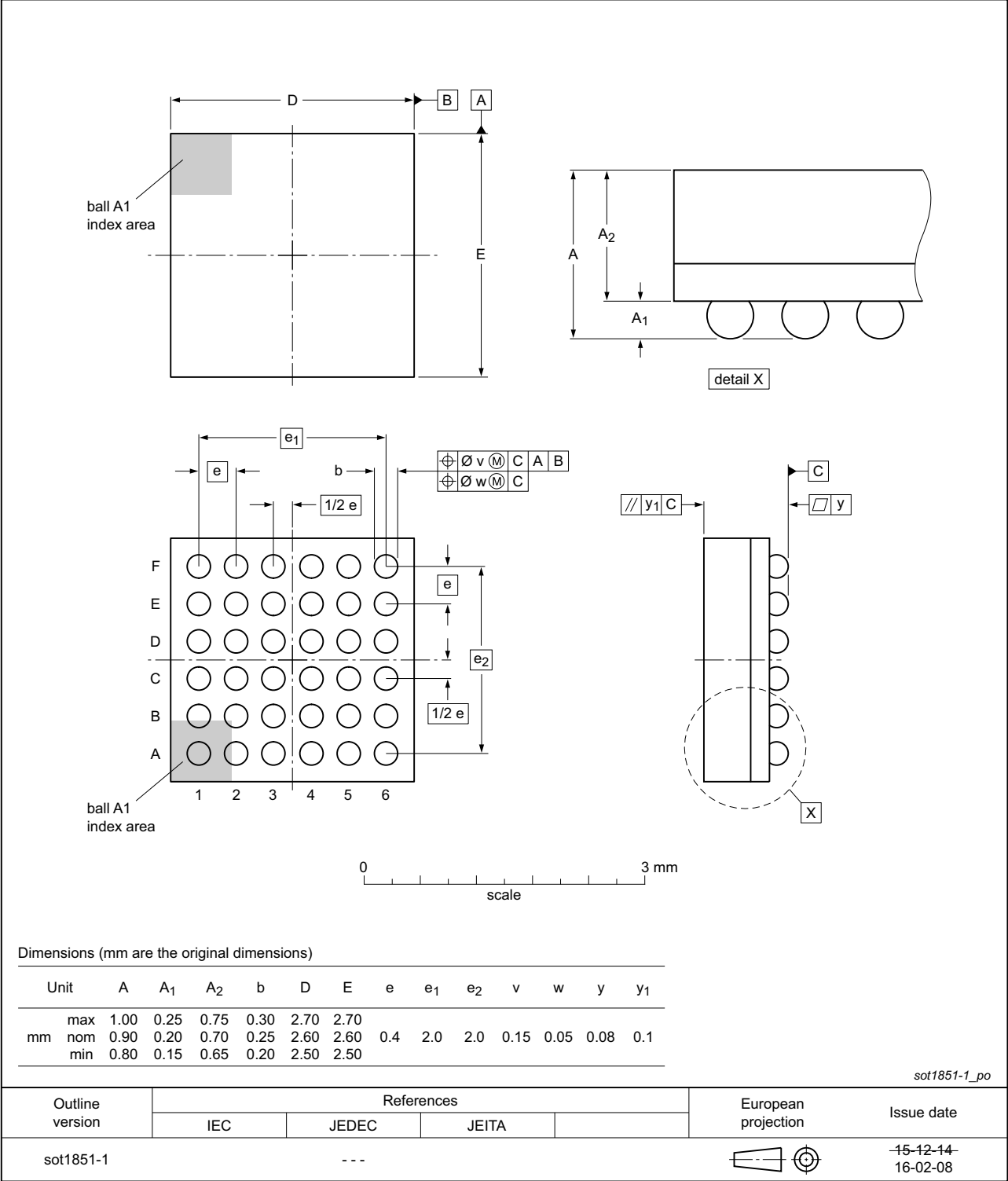


Fig 42. Package outline SOT1851-1 (VFBGA36)

## 16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leadless or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leadless SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leadless packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 43](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 68](#) and [69](#)

**Table 68. SnPb eutectic process (from J-STD-020D)**

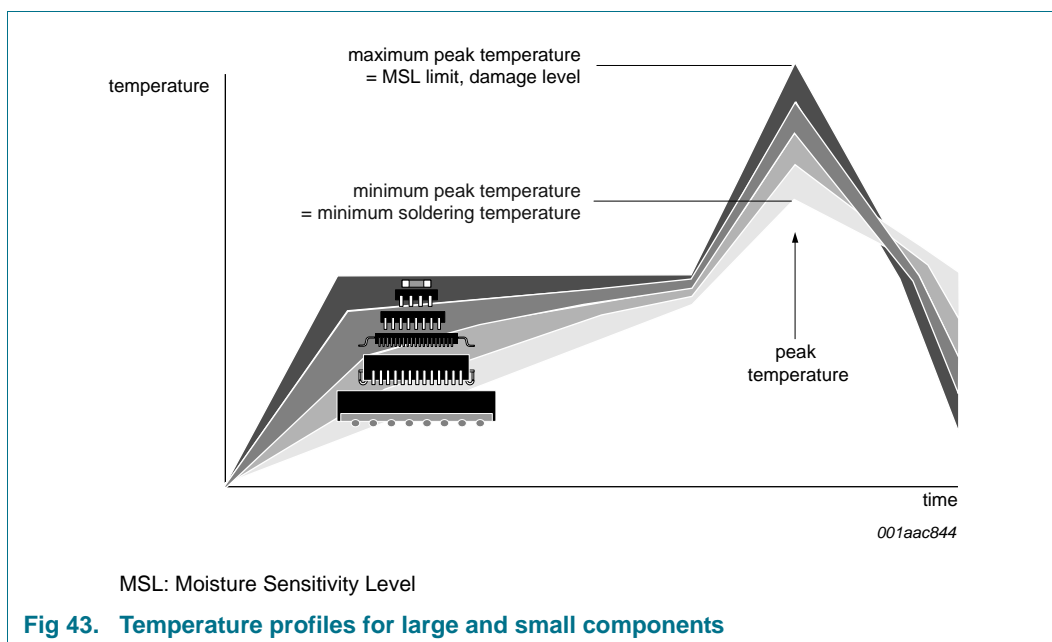
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 69. Lead-free process (from J-STD-020D)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 43](#).



For further information on temperature profiles, refer to Application Note *AN10365* “Surface mount reflow soldering description”.



17. Soldering: PCB footprints

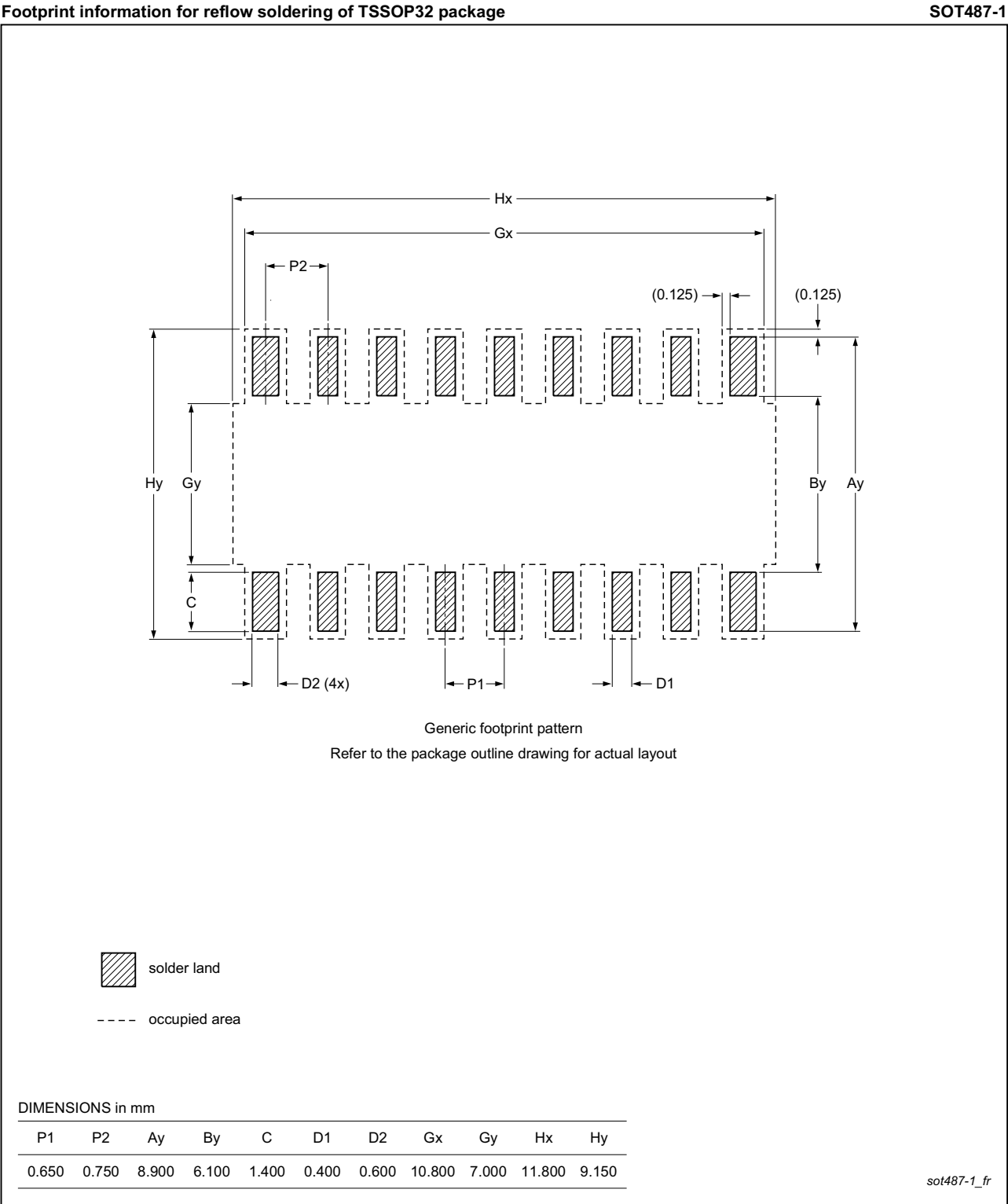
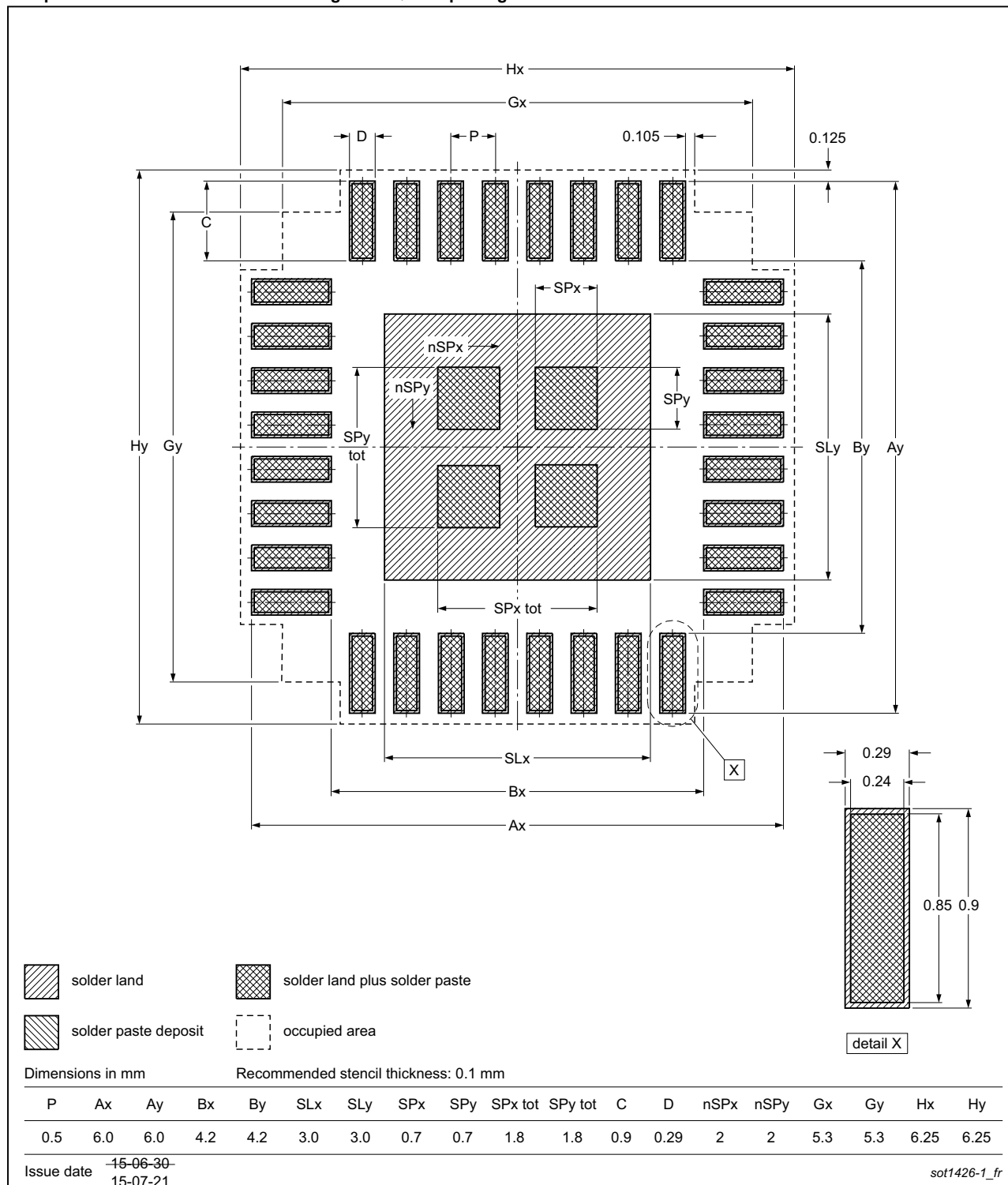


Fig 44. PCB footprint for SOT487-1 (TSSOP32); reflow soldering

### Footprint information for reflow soldering of HUQFN32 package

**SOT1426-1**



**Fig 45. PCB footprint for SOT1426-1 (HUQFN32); reflow soldering**

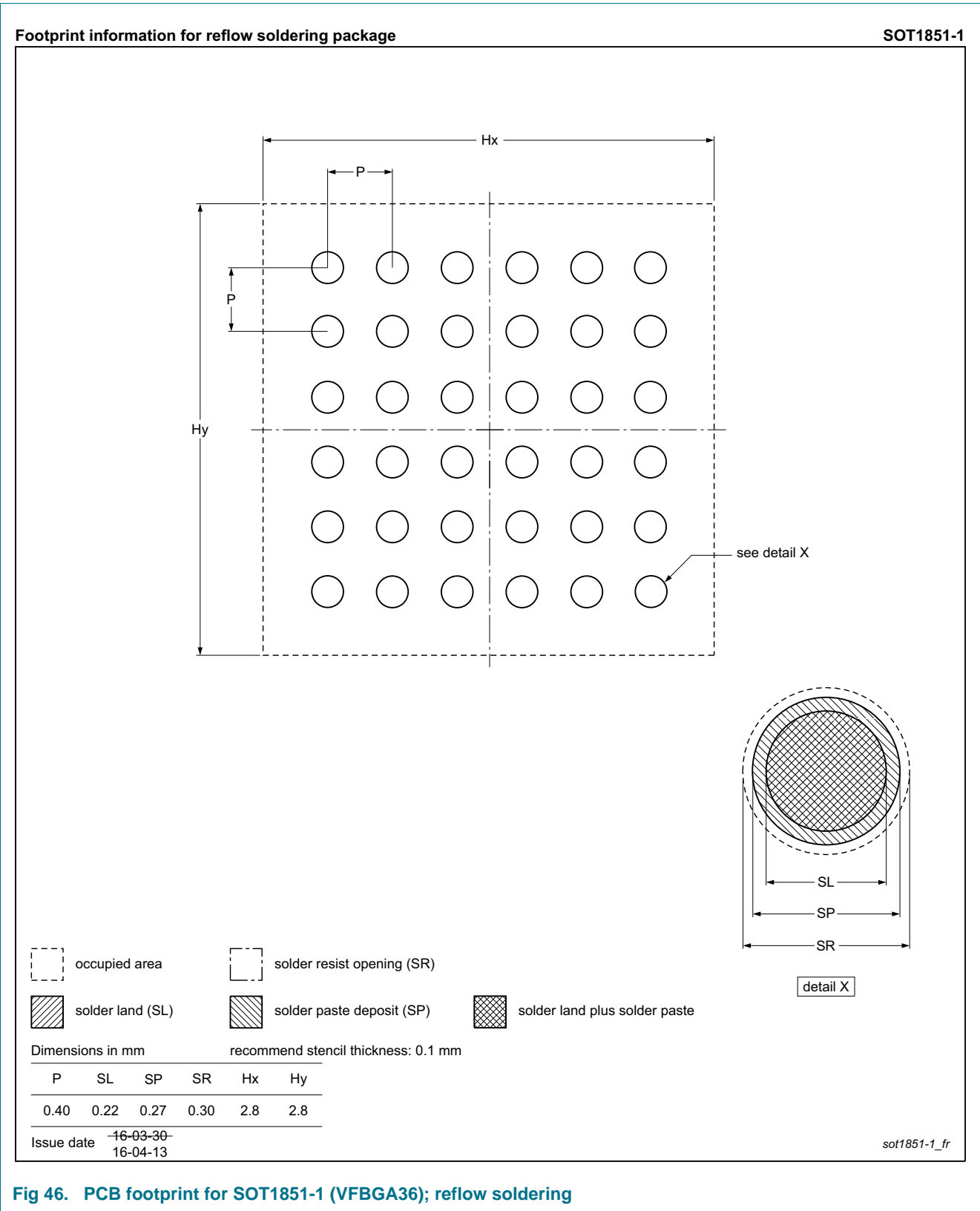


Fig 46. PCB footprint for SOT1851-1 (VFBGA36); reflow soldering

## 18. Abbreviations

Table 70. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light-Emitting Diode
LSB	Least Significant Bit
MSB	Most Significant Bit
NACK	Not ACKnowledge
PCB	Printed-Circuit Board
POR	Power-On Reset
PRR	Pulse Repetition Rate
SMBus	System Management Bus

## 19. Revision history

Table 71. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCAL6524 v.1.2	20161124	Product data sheet	-	PCAL6524 v.1.1
Modifications:	<ul style="list-style-type: none"> <li>Added PCAL6524EV</li> <li><a href="#">Table 2 "Ordering options"</a>: Removed PCAL6524HEAZ</li> <li>Added 0.1 uF bypass capacitor information for V<sub>DD(P)</sub></li> </ul>			
PCAL6524 v.1.1	20160921	Product data sheet	-	PCAL6524 v.1
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 61 "Limiting values"</a>: Updated V<sub>I</sub> and V<sub>O</sub></li> </ul>			
PCAL6524 v.1	20150922	Product data sheet	-	-

## 20. Legal information

### 20.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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