



STV270N4F3

N-channel 40 V, 1.25 mΩ, 270 A, PowerSO-10
STripFET™ III Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D (1)
STV270N4F3	40 V	< 1.5 mΩ	270 A

1. Current limited by package

- Conduction losses reduced
- Low profile, very low parasitic inductance

Applications

- Switching application

Description

This STripFET™ III Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance providing superior switching performances.

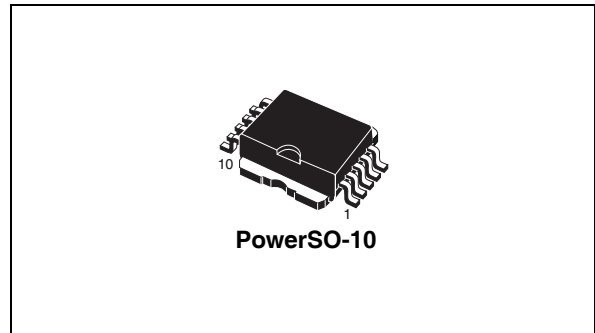


Figure 1. Internal schematic diagram and connection diagram (top view)

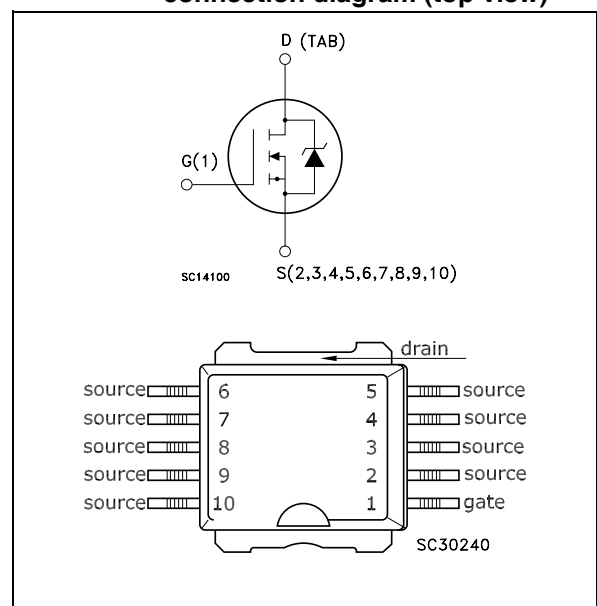


Table 1. Device summary

Order code	Marking	Package	Packaging
STV270N4F3	270N4F3	PowerSO-10	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	40	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	270	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	220	A
$I_{DM}^{(1)}$	Drain current (pulsed)	1080	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	1000	mJ
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature		

1. Current limited by package
2. This value is rated according to R_{thj-c}
3. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 80\text{ A}$, $V_{DD} = 32\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	35	$^\circ\text{C/W}$

1. When mounted on 1 inch² FR-4 2 oz Cu.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A$, $V_{GS} = 0$	40			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating}$, $T_c = 125^\circ C$			10 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{DS} = \pm 20 V$			± 200	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V$, $I_D = 80 A$		1.25	1.5	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10 V$, $I_D = 100 A$	-	200		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 V$, $f = 1 \text{ MHz}$, $V_{GS} = 0$	-	7500 1900 50		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 20 V$, $I_D = 160 A$, $V_{GS} = 10 V$ Figure 14	-	110 30 25	150	nC nC nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD} = 20 V$, $I_D = 80 A$ $R_G = 4.7 \Omega$, $V_{GS} = 10 V$ Figure 13	-	25 180	-	ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD} = 20 V$, $I_D = 80 A$ $R_G = 4.7 \Omega$, $V_{GS} = 10 V$, Figure 13	-	110 45	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		270	A
$I_{SD}^{(1)}$	Source-drain current (pulsed)		-		1080	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 80\text{ A}$, $V_{GS} = 0$	-		1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 160\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	70		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 32\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$	-	225		nC
I_{RRM}	Reverse recovery current	Figure 15	-	3.2		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics

Figure 2. Safe operating area

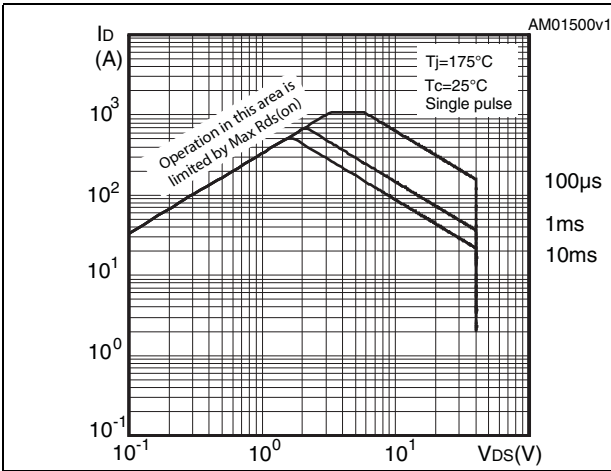


Figure 3. Thermal impedance

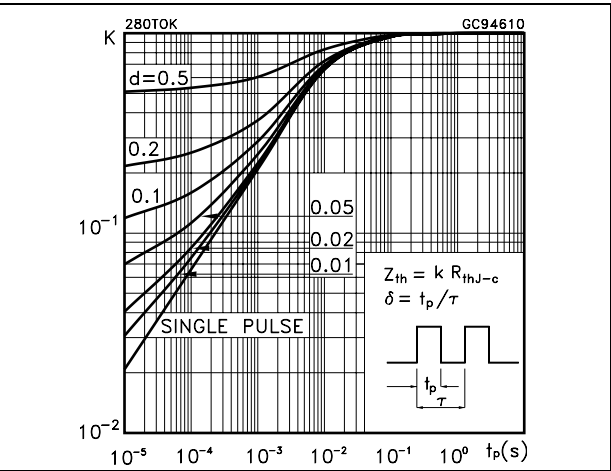


Figure 4. Output characteristics

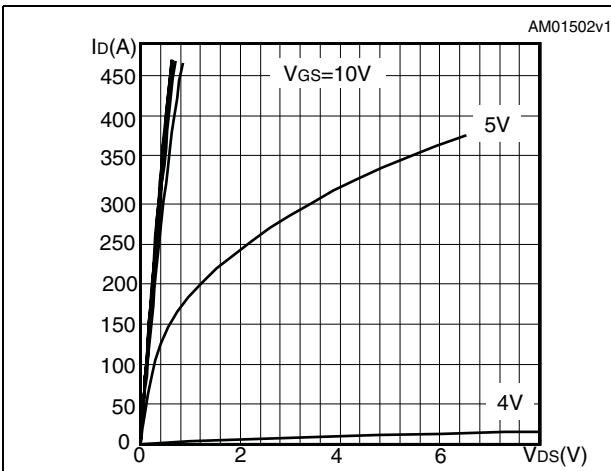


Figure 5. Transfer characteristics

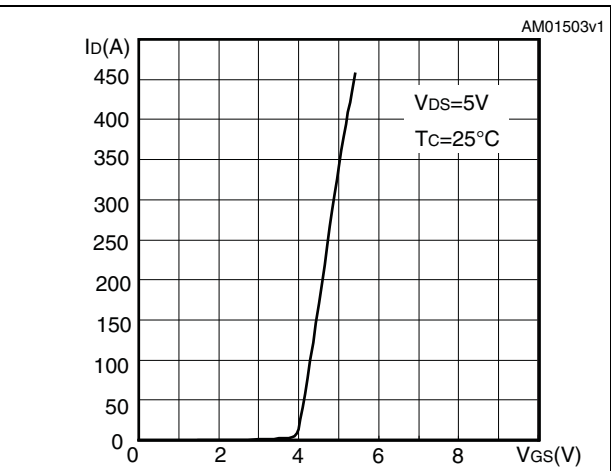


Figure 6. Static drain-source on resistance

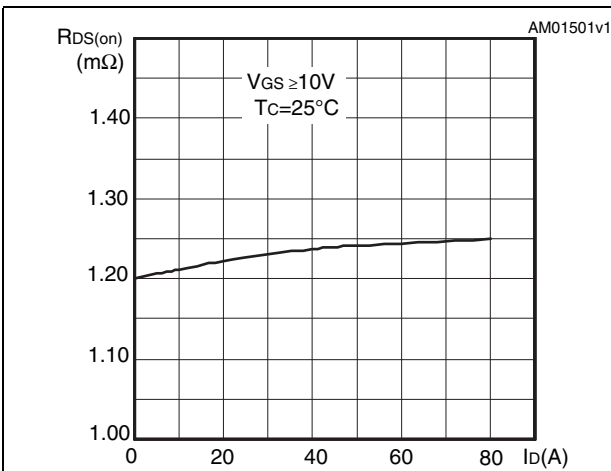


Figure 7. Normalized $B_{V_{DS}}$ vs temperature

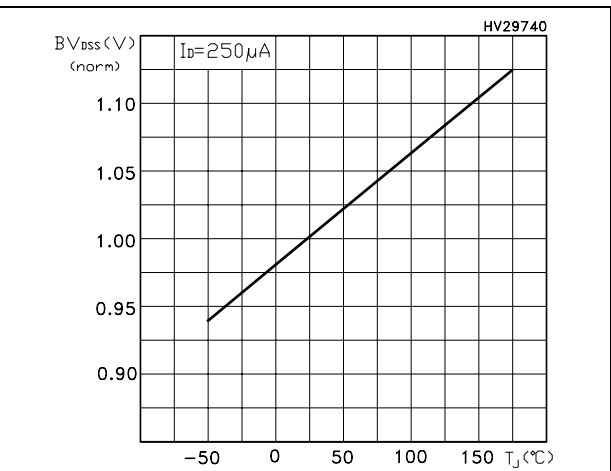


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

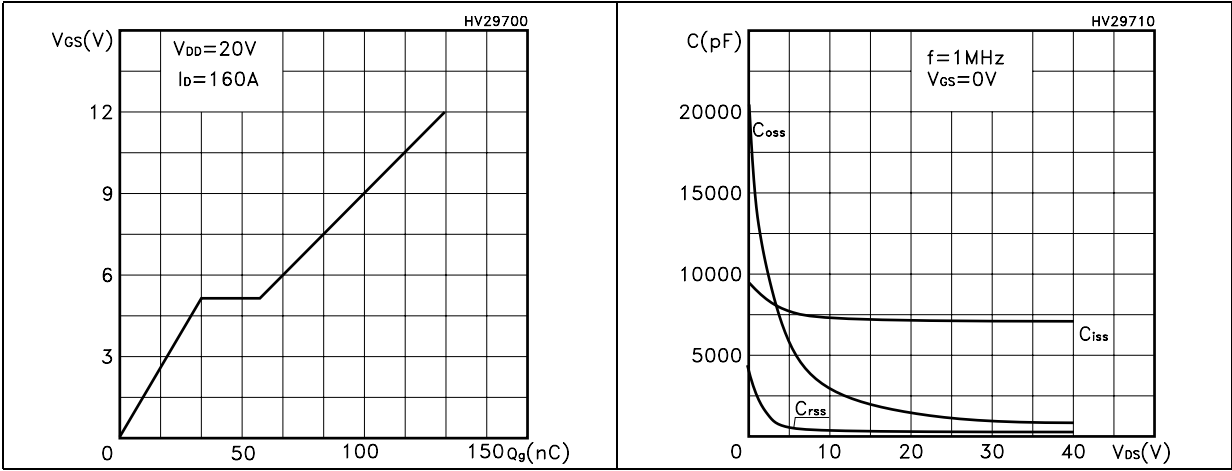


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

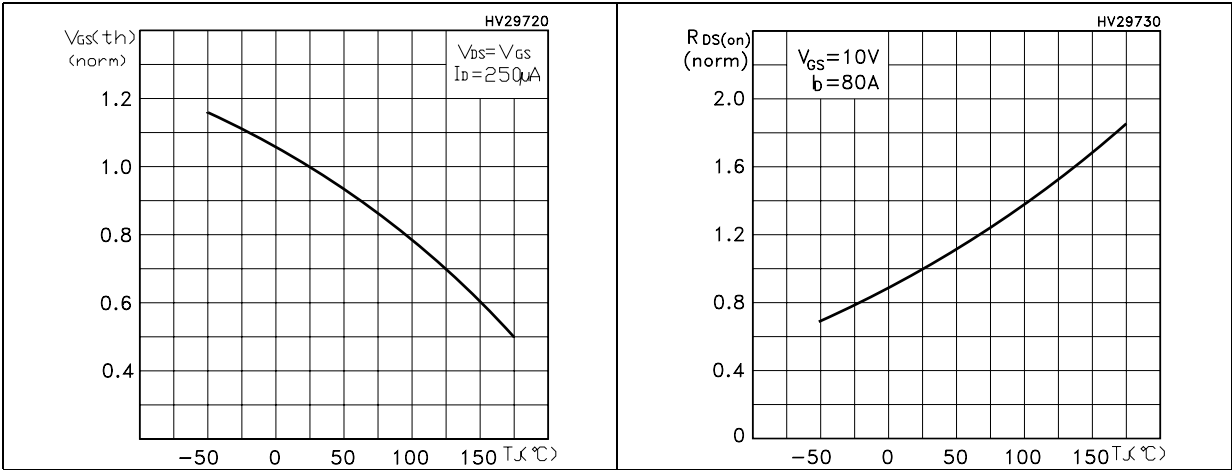
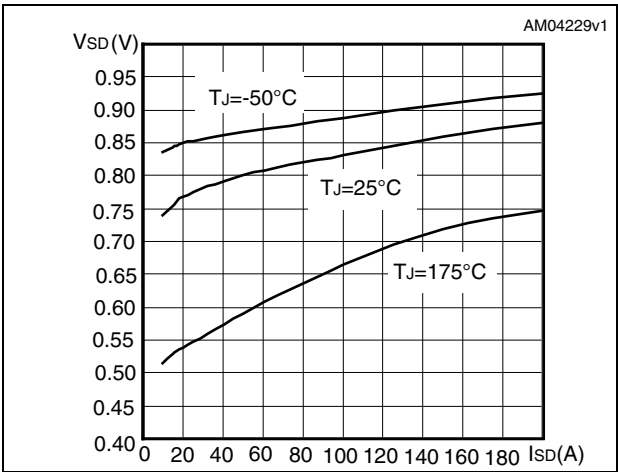


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

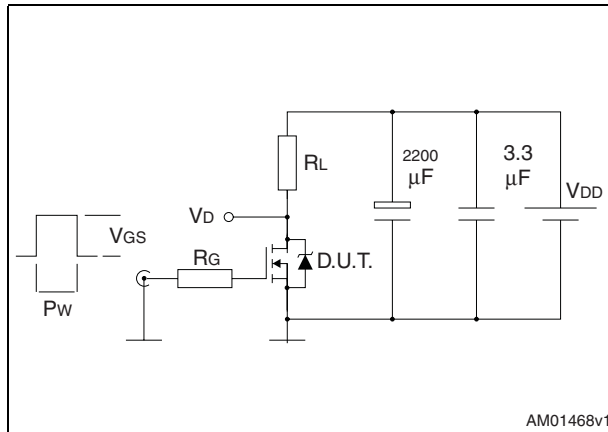


Figure 14. Gate charge test circuit

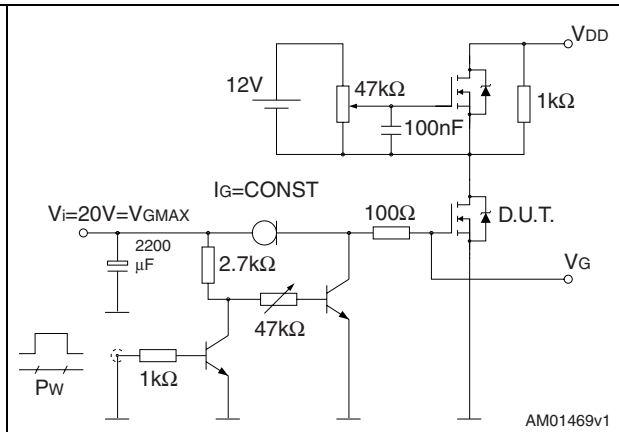


Figure 15. Test circuit for inductive load switching and diode recovery times

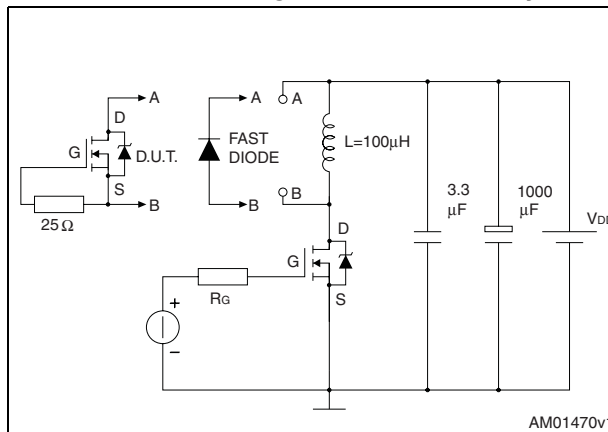


Figure 16. Unclamped inductive load test circuit

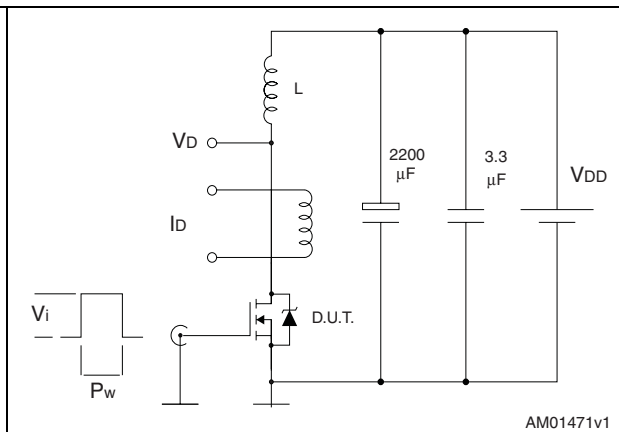


Figure 17. Unclamped inductive waveform

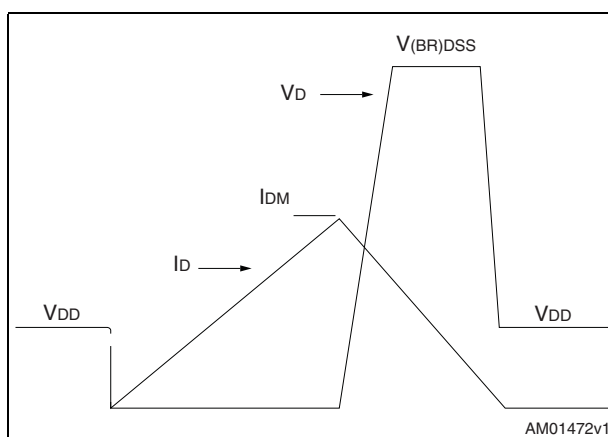
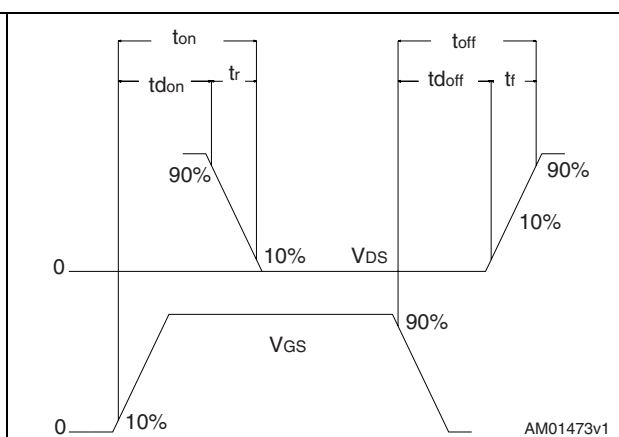


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

PowerSO-10 MECHANICAL DATA						
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
C	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
e		1.27			0.050	
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
F	1.25		1.35	0.049		0.053
h		0.50			0.002	
H	13.80		14.40	0.543		0.567
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
α	0°		8°			

The mechanical drawing illustrates the PowerSO-10 package from multiple perspectives. The top view shows a square package with 10 pins (5 on each side) and dimensions A, B, C, D, D1, E, E1, E2, E3, E4, F, and h. The side view shows the package height H and the lead length L. Detail 'A' shows the lead profile with dimensions A1 and α. A seating plane is indicated for the leads. A note specifies a tolerance of 0.10 for dimension A/B and 0.25 for dimension e.

0068039-C

5 Revision history

Table 8. Document revision history

Date	Revision	Changes
25-Oct-2007	1	Initial release
03-Apr-2008	2	I_D value has been updated.
01-Oct-2008	3	Document status promoted from preliminary data to datasheet
09-Mar-2009	4	$R_{thj-pcb}$ value has been changed in Table 3: Thermal data .
05-May-2009	5	Changed: Description and Figure 12: Source-drain diode forward characteristics
17-Jun-2009	6	Corrected typing error on cover page

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