

SN54BCT126A, SN74BCT126A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS252A – SEPTEMBER 1988 – REVISED APRIL 1994

- State-of-the-Art BiCMOS Design
Significantly Reduces I_{CCZ}
- ESD Protection Exceeds 2000 V Per
MIL-STD-883C, Method 3015
- 3-State Outputs Drive Bus Lines or Buffer
Memory Address Registers
- Package Options Include Plastic
Small-Outline (D) Packages, Ceramic Chip
Carriers (FK) and Flatpacks (W), and
Standard Plastic and Ceramic 300-mil
DIPs (J, N)

description

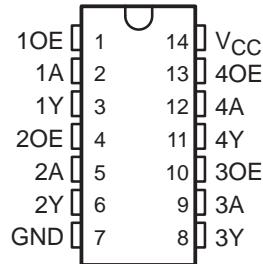
The 'BCT126A bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

The SN54BCT126A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74BCT126A is characterized for operation from 0°C to 70°C .

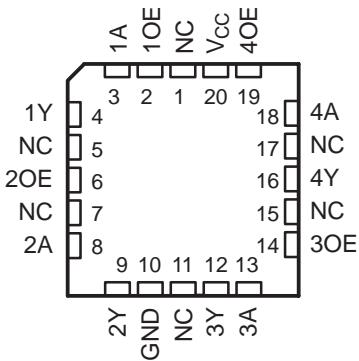
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT Y
OE	A	
H	H	H
H	L	L
L	X	Z

SN54BCT126A . . . J OR W PACKAGE
SN74BCT126A . . . D OR N PACKAGE
(TOP VIEW)



SN54BCT126A . . . FK PACKAGE
(TOP VIEW)

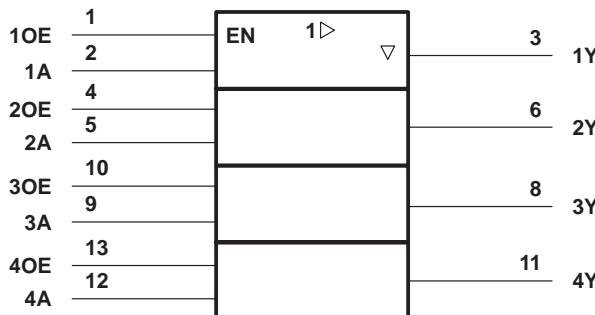


NC – No internal connection

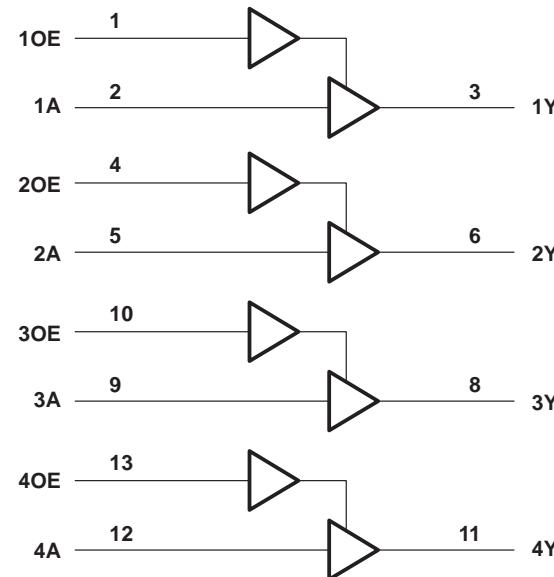
SN54BCT126A, SN74BCT126A QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS252A – SEPTEMBER 1988 – REVISED APRIL 1994

logic symbol



logic diagram (positive logic)



Pin numbers shown are for the J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		SN54BCT126A			SN74BCT126A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage		2		2			V
V _{IL}	Low-level input voltage			0.8			0.8	V
I _{IK}	Input clamp current			-18			-18	mA
I _{OH}	High-level output current			-12			-15	mA
I _{OL}	Low-level output current			48			64	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

SN54BCT126A, SN74BCT126A
QUADRUPLE BUS BUFFER GATES
WITH 3-STATE OUTPUTS

SCBS252A – SEPTEMBER 1988 – REVISED APRIL 1994

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54BCT126A			SN74BCT126A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5$ V	$I_{OH} = -3$ mA	2.4	3.3	2.4	3.3		V
		$I_{OH} = -12$ mA	2	3.2				
		$I_{OH} = -15$ mA			2	3.1		
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 48$ mA	0.38	0.55				V
		$I_{OL} = 64$ mA					0.42 0.55	
I_I	$V_{CC} = 0$, $V_I = 7$ V		0.1		0.1			mA
I_{IH}	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			35			25	μ A
I_{IL}	$V_{CC} = 5.5$ V, $V_I = 0.5$ V			-20			-20	μ A
I_{OZH}	$V_{CC} = 5.5$ V, $V_O = 2.7$ V			50			50	μ A
I_{OZL}	$V_{CC} = 5.5$ V, $V_O = 0.5$ V			-50			-50	μ A
I_{OS}^{\ddagger}	$V_{CC} = 5.5$ V, $V_O = 0$		-100	-225	-100	-225		mA
I_{CCH}	$V_{CC} = 5.5$ V, Outputs open		21	33	21	33		mA
I_{CCL}	$V_{CC} = 5.5$ V, Outputs open		35	51	35	51		mA
I_{CCZ}	$V_{CC} = 5.5$ V, Outputs open		5	10	5	10		mA
C_i	$V_{CC} = 5$ V, $V_I = 2.5$ V or 0.5 V		4		4			pF
C_o	$V_{CC} = 5$ V, $V_O = 2.5$ V or 0.5 V		9		9			pF

† All typical values are at $V_{CC} = 5$ V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $C_L = 50$ pF, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = 25^\circ C$	$V_{CC} = 4.5$ V to 5.5 V, $C_L = 50$ pF, $R1 = 500 \Omega$, $R2 = 500 \Omega$, $T_A = \text{MIN to MAX}^{\$}$			UNIT	
			'BCT126A			SN54BCT126A	SN74BCT126A	
			MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	1.5	3.6	4.9	1.5	5.6	1.5 6.3
			2.7	5.3	6.9	2.7	7.7	2.7 7.4
t_{PHL}	OE	Y	2.6	4.8	6.4	2.6	7.2	2.6 7.9
			3.7	6.4	8.3	3.7	10.5	3.7 10
t_{PZH}	OE	Y	3.2	6.6	8.2	3.2	9.6	3.2 10
			3.4	6.5	8	3.4	12.3	3.4 10.7

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1998, Texas Instruments Incorporated