

Features

Patent Number: 86474, 113235(R.O.C.), 5424740(U.S.A.)

- Universal specification
- Operating voltage: 2.0V~5.5V
- Low standby current
- Low memory retention current: 0.1μA (Typ.)
- Tone/pulse switchable
- Interface with LCD driver
- 32 digits for redialing
- Pause and P→T key for PBX
- 4×5 keyboard matrix
- Pulse rate control
- Make/Break ratio control
- 3.58MHz crystal or ceramic resonator
- Hand-free control
- Hold-line control
- Pause, P→T can be saved for redialing
- Keytone function
- Lock function
- Auto switching from pulse mode to tone mode in EM4
- Memory number: 15 memories

General Description

The HT9214 series tone/pulse dialers are CMOS LSIs for telecommunication systems.

The HT9214 series are offered in various packages from 22-pin DIP to 28-pin DIP. The 22-pin DIP version is suitable for low cost applications, while the 28-pin DIP version has versatile functions such as: Hold-line, Hand-free, IDD lock

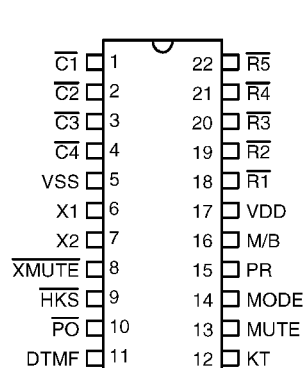
and LCD dialing number display interface, all of which are suitable for feature phone applications.

The HT9214 provides Redial, 4 one-touch and 10 two-touch memory dials for speed dialing in either pulse or tone mode.

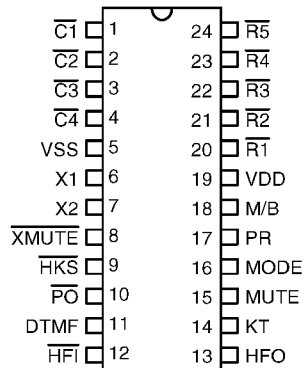
Selection Table

Function Item	Memory Dialing	Hold-Line	Hand-Free	LCD Interface	Flash Function	Flash Time (ms)	Pulse No.	Tone Duration (ms)	Inter-Tone-Pause (ms)	Lock Function	Package	Note
HT9214A	R/P EM1~EM4 M0~M9	—	—	—	Control	98/600	N	91	91	—	22 DIP	—
HT9214B	R/P EM1~EM4 M0~M9	—	√	—	Control	98/600	N	91	91	—	24 DIP	—
HT9214AL	R/P EM1~EM4 M0~M9	—	—	—	Control	98/600	N	91	91	√	22 DIP	PR=1
HT9214BL	R/P EM1~EM4 M0~M9	—	√	—	Control	98/600	N	91	91	√	24 DIP	PR=1
HT9214CL	R/P EM1~EM4 M0~M9	—	—	√	Control	98/600	N	91	91	√	24 DIP	PR=1
HT9214DL	R/P EM1~EM4 M0~M9	√	√	√	Control	98/600	N	91	91	√	28 DIP	PR=1

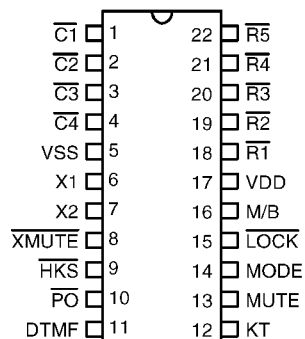
Pin Assignment



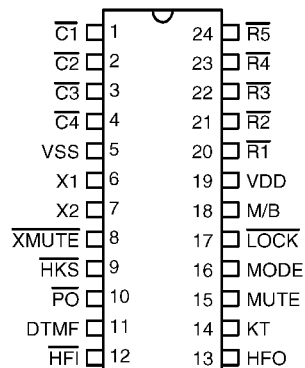
HT9214A
– 22 DIP



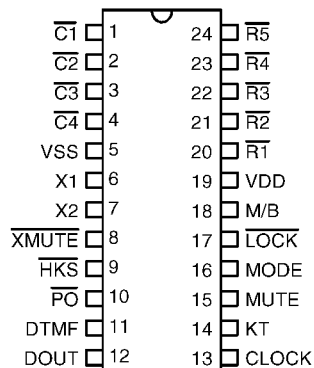
HT9214B
– 24 DIP



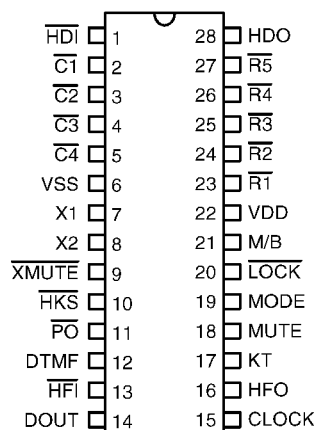
HT9214AL
– 22 DIP



HT9214BL
– 24 DIP

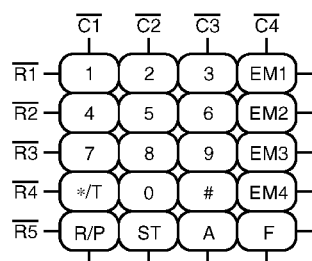


HT9214CL
– 24 DIP



HT9214DL
– 28 DIP

Keyboard Information



The block diagram illustrates the internal architecture of the TSC1000. It features several key components and their interconnections:

- Inputs:** C1, C4, R1, R5, X1, and X2 are external inputs. PR, M/B, LOCK, and KT are inputs from the TSC1000 module.
- Key Matrix:** The Key Column and Key Row blocks receive inputs from C1, C4, R1, and R5. They interface with the Key Function Encoder and the Encoder.
- Control and Timing:** The FSM (Finite State Machine) and WRM Counter (Write Refresh Memory Counter) are connected to the Control block. The ADDRL (Address) block is connected to the SRAM (Static Random Access Memory).
- SRAM and Data Path:** The SRAM is the central data storage, connected to the Control, Check, Tone Encoder, Converter, and Flash blocks.
- Output and Status:** The Check block outputs DOUT and CLOCK. The Tone Encoder outputs DTMF and Tone Out. The Converter outputs Pulse Out, which is connected to PO, MUTE, and XMUTE. The Flash block is connected to the Timer and Keytone Generator.
- Mode and Configuration:** The Mode In block is connected to the HD/HF (Headset/Handset) block. The Keytone Generator outputs KT.
- Internal Logic:** The Divider block receives X1 and X2 inputs. The Clock Generator block is connected to the Debounce block and the M/B (Master/Slave) block. The Timer block is connected to the M/B block and the Keytone Generator.

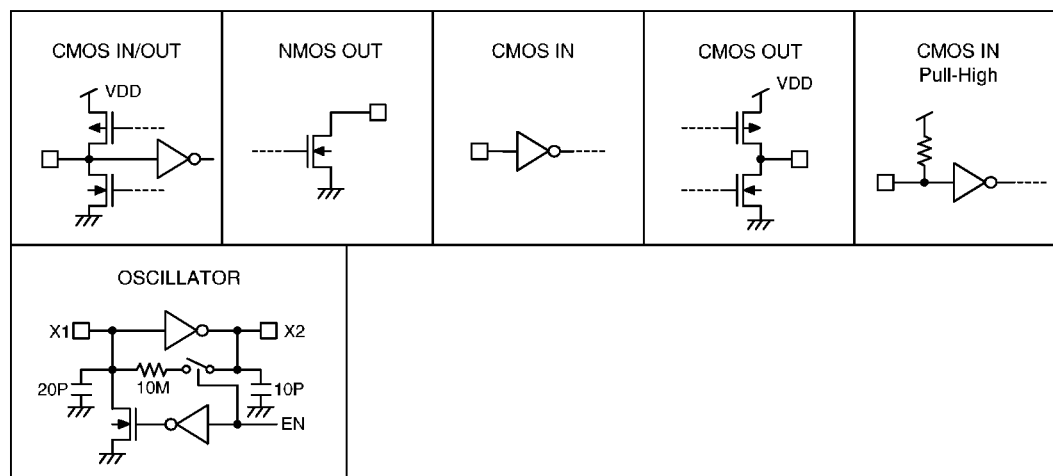
Pin Name	I/O	Internal Connection	Description
$\overline{C1}\sim\overline{C4}$ $\overline{R1}\sim\overline{R5}$	I/O	CMOS IN/OUT	These pins form a 4x5 keyboard matrix which can perform keyboard input detection. When on-hook ($\overline{HKS}$= high) all the pins are set high. While off-hook the column group ($\overline{C1}\sim\overline{C4}$) remains low and the row group ($\overline{R1}\sim\overline{R5}$) is set high for key input detection. An inexpensive single contact 4x5 keyboard can be used as an input device. Pressing a key connects a single column to a single row, and actuates the system oscillator that results in a dialing signal output. If more than two keys are pressed at the same time, no response occurs. The key-in debounce time is 20ms. Refer to the keyboard information for keyboard arrangement and to the functional description for dialing specification selection.
X1	I	OSCILLATOR	The system oscillator consists of an inverter, a bias resistor and the necessary load capacitor on chip. Connecting a standard 3.579545MHz crystal or ceramic resonator to the X1 and X2 terminals can implement the oscillator function. The oscillator is turned off in the standby mode, and is actuated whenever a keyboard entry is detected.
X2	O		

Pin Name	I/O	Internal Connection	Description
$\overline{\text{XMUTE}}$	O	CMOS OUT	$\overline{\text{XMUTE}}$ is a CMOS output structure pulled to VSS during dialing signal transmission. Otherwise, it remains "high". $\overline{\text{XMUTE}}$ is used to mute the speech circuit when transmitting the dial signal.
$\overline{\text{HKS}}$	I	CMOS IN Pull-High	This pin is used to monitor the status of the hook-switch and its combination with $\overline{\text{HFI}}$ can control the $\overline{\text{PO}}$ pin output to make or break the line. $\overline{\text{HKS}}=\text{VDD}$: On-hook state ($\overline{\text{PO}}=\text{low}$). Except $\overline{\text{HFI}}/\overline{\text{HDI}}$ (hand-free/hold-line control input), other functions are all disabled. $\overline{\text{HKS}}=\text{VSS}$: Off-hook state ($\overline{\text{PO}}=\text{high}$). The chip is in the standby mode and ready to receive the key input.
$\overline{\text{PO}}$	O	CMOS OUT	This pin is a CMOS output structure which by receiving the $\overline{\text{HKS}}$ and HFO signals, control the dialer to connect or disconnect the telephone line. $\overline{\text{PO}}$ outputs a low to break the line when $\overline{\text{HKS}}$ is high (on-hook) and HFO is low (hand-free inactive). $\overline{\text{PO}}$ outputs a high to make the line when $\overline{\text{HKS}}$ is low (off-hook) or HFO is high or HDO is high. During the off-hook state, this pin also outputs the dialing pulse train in pulse mode dialing. While in the tone mode, this pin is always high.
MODE	I	CMOS IN	This is an input pin, used for dialing mode selection either Tone mode or Pulse mode. $\text{MODE}=\text{VDD}$: Pulse mode $\text{MODE}=\text{VSS}$: Tone mode During pulse mode dialing, switching this pin to the tone mode changes the subsequent digit entry to tone mode. When the chips are in tone mode, switching to pulse mode will also be recognized.
MUTE	O	CMOS OUT	MUTE is a CMOS output structure pulled to VDD during Tone (DTMF) output transmission. Otherwise, it continuously remains "low".
DTMF	O	CMOS OUT	This pin is active only when the chip transmits tone dialing signals. Otherwise, it always outputs a low. The pin outputs tone signals to drive the external transmitter amplifier circuit. The load resistor should not be less than 5k Ω .
$\overline{\text{HDI}}$	I	CMOS IN Pull-High	This pin is a schmitt trigger input structure. Active low. Applying a negative going pulse to this pin can toggle the HDO output once. An external RC network is recommended for input debouncing. The pull-high resistance is 200k Ω typ.

Pin Name	I/O	Internal Connection	Description					
HDO	O	CMOS OUT	The HDO is a CMOS output structure. Its output is toggle-controlled by a negative transition on $\overline{\text{HDI}}$. When HDO is toggled high, $\overline{\text{PO}}$ keeps high to hold the line. The hold function can be released by setting HFO high or by an on-off-hook operation or by another $\overline{\text{HDI}}$ input. The HDO pin can directly drive the HT3810 series melody generators to produce a hold-line background melody. Refer to the functional description for the hold-line function.					
$\overline{\text{HFI}}$	I	CMOS IN Pull-High	This pin is a schmitt trigger input structure. Active low. Applying a negative going pulse to $\overline{\text{HFI}}$ can toggle HFO once and hence control the hand-free function. The pull-high resistance of $\overline{\text{HFI}}$ is 200k Ω typ. An external RC network is recommended for input debouncing.					
HFO	O	CMOS OUT	The HFO is a CMOS output structure. Its output is toggle-controlled by a negative transition on the $\overline{\text{HFI}}$ pin. When HFO is high, the hand-free function is enabled and $\overline{\text{PO}}$ outputs a high to connect the line. The hand-free function can be released by an on-off-hook operation or by another $\overline{\text{HFI}}$ input or by setting HDO high. Refer to the functional description for the hand-free functional operation.					
DOUT	O	NMOS OUT	NMOS open drain output pin. It outputs the BCD code of the dialing digits to the LCD driver chip (HT16XX series) or to the μC for dialing number display. Refer to the functional description for the detailed timing.					
CLOCK	O	NMOS OUT	NMOS open drain output. When dialing, it outputs a series of pulse trains for DOUT data synchronization. DOUT data is valid at the falling edge of the clock.					
KT	O	CMOS OUT	Keytone output pin. Outputs a 1.2kHz tone carrier when any key is pressed in the pulse mode or when the function keys are pressed in the Tone (DTMF) mode.					
M/B	I	CMOS IN	Make/Break ratio selection pin	Selection table				
				M/B Pin	PR Pin	M/B Rate	Flash Time	Pulse Rate
				1	1	2:3	600ms	10pps
PR	I	CMOS IN Pull-High	Pulse rate selection pin	0	1	1:2	98ms	10pps
				0	0	1:2	600ms	20pps
				1	0	IC testing mode		

Pin Name	I/O	Internal Connection	Description
$\overline{\text{TEST}}$	I	CMOS IN	For IC test only. $\overline{\text{TEST}}=\text{VDD}$ for normal operation
$\overline{\text{LOCK}}$	I/O	CMOS IN/OUT	This is a three-state input-output pin, used for controlling long distance call function with a lock-switch LOCK=OPEN: Normal dialing LOCK=VDD: "0, 9" is inhibited for use as the first key input LOCK=VSS: "0" is inhibited for use as the first key input
VDD	I	—	Positive power supply, 2.0V~5.5V for normal operation
VSS	I	—	Negative power supply

Approximate internal connection circuits



Absolute Maximum Ratings*

Supply Voltage	-0.3V to 6V	Storage Temperature	-50°C to 125°C
Input Voltage	V _{SS} -0.3 to V _{DD} +0.3V	Operating Temperature	-20°C to 75°C

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(F_{OSC}=3.5795MHz, T_a=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DD}	Operating Voltage	—	—	2	—	5.5	V
I _{DD}	Operating Current	2.5V	Pulse	—	0.2	1	mA
			Off-hook Keypad entry No load	—	0.6	2	mA
I _{STB}	Standby Current	1V	On-hook, no load No entry	—	—	1	μA
V _R	Memory Retention Voltage	—	—	1	—	5.5	V
I _R	Memory Retention Current	1V	On-hook	—	0.1	0.2	μA
V _{IL}	Input Low Voltage	—	—	V _{SS}	—	0.2V _{DD}	V
V _{IH}	Input High Voltage	—	—	0.8V _{DD}	—	V _{DD}	V
I _{OHXM}	Mute Pin Source Current ($\overline{\text{XMUTE}}$, MUTE)	2.5V	V _{OH} =2V	−1	—	—	mA
I _{OLXM}	Mute Pin Sink Current ($\overline{\text{XMUTE}}$, MUTE)	2.5V	V _{OL} =0.5V	1	—	—	mA
I $\overline{\text{HKS}}$	$\overline{\text{HKS}}$ Pin Input Current	2.5V	V $\overline{\text{HKS}}$ =2.5V	—	—	0.1	μA
R $\overline{\text{HFI}}$	$\overline{\text{HFI}}$ Pull-High Resistance	2.5V	V $\overline{\text{HFI}}$ =0V	—	200	—	kΩ
R $\overline{\text{HDI}}$	$\overline{\text{HDI}}$ Pull-High Resistance	2.5V	V $\overline{\text{HDI}}$ =0V	—	200	—	kΩ
R $\overline{\text{HKS}}$	$\overline{\text{HKS}}$ Pull-High Resistance	2.5V	V $\overline{\text{HKS}}$ =0V	—	1	—	MΩ
T _{F1}	Flash Time for F Key	—	M/B=V _{SS} , PR=V _{DD}	—	98	—	ms
T _{F2}	Flash Time for F Key	—	M/B=V _{DD} , PR=V _{DD}	—	600	—	ms
			M/B=V _{SS} , PR=V _{SS}				
I _{OH1}	Keypad Pin Source Current	2.5V	V _{OH} =0V	−4	—	−40	μA
I _{OL1}	Keypad Pin Sink Current	2.5V	V _{OL} =2.5V	200	400	—	μA
I _{OH2}	HFO Pin Source Current	2.5V	V _{OH} =2V	−1	—	—	mA
I _{OL2}	HFO Pin Sink Current	2.5V	V _{OL} =0.5V	1	—	—	mA
I _{OH3}	HDO Pin Source Current	2.5V	V _{OH} =2V	−1	—	—	mA
I _{OL3}	HDO Pin Sink Current	2.5V	V _{OL} =0.5V	1	—	—	mA
T _{FP}	Pause Time After Flash	—	Control key	—	0.2	—	s
T _{DB}	Key-in Debounce Time	—	—	—	20	—	ms
T _{KTD}	Keytone Delay	—	—	—	20	—	ms
T _{KTR}	Keytone Release	—	—	—	20	—	ms
F _{OSC}	System Frequency	—	Crystal=3.5795MHz	3.5759	3.5795	3.5831	MHz

Pulse Mode Electrical Characteristics

(F_{OSC}=3.5795MHz, T_a=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
I _{POH}	$\overline{\text{PO}}$ Output Source Current	2.5V	V _{OH} =2V	-0.2	—	—	mA
I _{POL}	$\overline{\text{PO}}$ Output Sink Current	2.5V	V _{OL} =0.5V	0.2	0.6	—	mA
PR	Pulse Rate	—	PR pin is connected to VDD	—	10	—	pps
			M/B=VSS, PR=VSS	—	20	—	pps
M/B	Make/Break Ratio	—	M/B=VSS	—	33:66	—	%
			M/B=VDD	—	40:60	—	
T _{PDP}	Pre-digit-pause Time	—	M/B ratio=40:60	—	40 (10pps)	—	ms
			M/B ratio=33:66	—	33 (10pps) 17 (20pps)	—	
T _{IDP}	Inter-digit-pause Time	—	Pulse rate=10pps	—	800	—	ms
			Pulse rate=20pps	—	600	—	ms
T _M	Pulse Make Duration	—	M/B ratio=33:66	—	33 (10pps) 17 (20pps)	—	ms
			M/B ratio=40:60	—	40 (10pps)	—	
T _B	Pulse Break Duration	—	M/B ratio=33:66	—	66 (10pps) 33 (20pps)	—	ms
			M/B ratio=40:60	—	60 (10pps)	—	

Tone Mode Electrical Characteristics

(F_{OSC}=3.5795MHz, Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{TDC}	DTMF Output DC Level	—	—	0.45V _{DD}	—	0.7V _{DD}	V
I _{TOL}	DTMF Sink Current	2.5V	V _{DTMF} =0.5V	0.1	—	—	mA
V _{TAC}	DTMF Output AC Level	—	Row group, R _L =5kΩ	0.12	0.155	0.18	V _{rms}
R _L	DTMF Output Load	2.5V	THD≤-23dB	5	—	—	kΩ
A _{CR}	Column Pre-emphasis	2.5V	Row group=0dB	1	2	3	dB
THD	Tone Signal Distortion	2.5V	R _L =5kΩ	—	-30	-23	dB
T _{TMIN}	Minimum Tone Duration	—	Auto-redial	—	91	—	ms
T _{ITPM}	Minimum Inter-tone Pause	—	Auto-redial	—	91	—	ms

$$\text{THD (Distortion) (dB)} = 20 \log \left(\frac{\sqrt{V_1^2 + V_2^2 + \dots + V_n^2}}{\sqrt{V_i^2 + V_h^2}} \right)$$

V_i, V_h: Row group and column group signals

V₁, V₂, ... V_n: Harmonic signals (BW=300Hz~3500Hz)

Functional Description
Keyboard matrix

$\overline{\text{C1}} \sim \overline{\text{C4}}$ and $\overline{\text{R1}} \sim \overline{\text{R5}}$ form a keyboard matrix. Together with a standard 4×5 keyboard, the keyboard matrix is used for dialing entries. The keyboard arrangement for the HT9214 series is shown in the **Keyboard Information**.

Tone frequency

Tone Name	Output Frequency (Hz)		% Error
	Specified	Actual	
$\overline{\text{R1}}$	697	699	+0.29%
$\overline{\text{R2}}$	770	766	-0.52%
$\overline{\text{R3}}$	852	847	-0.59%
$\overline{\text{R4}}$	941	948	+0.74%
$\overline{\text{C1}}$	1209	1215	+0.50%
$\overline{\text{C2}}$	1336	1332	-0.30%
$\overline{\text{C3}}$	1477	1472	-0.34%

Note: % Error does not contain the crystal frequency drift

M/B ratio selection table

M/B Pin	PR Pin	M/B Ratio (%)
VDD	VDD	40:60
VSS	—	33:66
VDD	VSS	Test Mode

Flash function/time (duration) selection table

M/B Pin	PR Pin	Flash Function	Flash Time (T _F)
VSS	VDD	Control	98ms
VSS	VSS	Control	600ms
VDD	VDD	Control	600ms
VDD	VSS	Test Mode	

Pause and P→T duration table

T _P (sec)	T _{P→T} (sec)
3.6	3.6

Pulse number table

Keypad	Output Pulse Number
Digit Key	Normal N
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
0	10
*/T	P→T
#	Ignored

Tone duration and pause in redial function

Parameter	Symbol	Typ.	Unit
Minimum Tone Duration	T _{TMIN}	91	ms
Minimum Inter-tone Pause	T _{ITPM}	91	ms
Cycle Time	T _C	182	ms

Hand-free function operation

- Hand-free function execution
When HFO is low, a falling edge triggers the $\overline{\text{HFI}}$, enabling the Hand-free function (HFO becomes high).
- Reset Hand-free function
When HFO is high, the Hand-free function is enabled and can be reset by:
 - Off-hook
 - Applying a falling edge to $\overline{\text{HFI}}$
 - Changing the HDO pin from low to high

Hand-free function table

Current State			Input			Next State	
$\overline{\text{HKS}}$	HFO	HDO	$\overline{\text{HDI}}$	$\overline{\text{HFI}}$	$\overline{\text{HKS}}$	HFO	HDO
H	L	X	H	H	An	L	An
H	L	X	H	$\downarrow$	An	H	L
H	H	X	H	$\downarrow$	An	L	An
H	X	L	H	H	L	L	L
L	L	X	H	H	An	L	An
L	L	X	H	$\downarrow$	An	H	L
L	H	L	H	$\downarrow$	An	L	An
L	X	X	H	H	H	An	An
X	X	L	$\downarrow$	H	An	L	H

H: Logic HIGH X: Don't care $\uparrow$: Rising edge
 L: Logic LOW An: Unchanged $\downarrow$: Falling edge

Hold-line function operation

- Hold-line function execution

When HDO is low, a falling edge triggers $\overline{\text{HDI}}$, enabling the Hold-line function (HDO becomes high). The $\overline{\text{XMUTE}}$ remains low when HDO is high.

- Reset Hold-line function

When HDO is high, the Hold-line function is enabled and can be reset by:

- Off-hook
- Applying a falling edge to $\overline{\text{HDI}}$
- Changing the HFO pin from low to high

- Hold-line function table

Current State			Input			Next State	
$\overline{\text{HKS}}$	HDO	HFO	$\overline{\text{HFI}}$	$\overline{\text{HDI}}$	$\overline{\text{HKS}}$	HDO	HFO
H	L	X	H	H	An	L	An
H	L	X	H	$\downarrow$	An	H	L
H	H	L	H	$\downarrow$	An	L	An
H	X	X	H	H	L	L	L
L	L	X	H	H	An	L	An
L	L	X	H	$\downarrow$	An	H	L
L	H	L	H	$\downarrow$	An	L	An
L	X	X	H	H	H	An	An
X	X	L	$\downarrow$	H	An	L	H

H: Logic HIGH X: Don't care $\uparrow$: Rising edge
L: Logic LOW An: Unchanged $\downarrow$: Falling edge

DOUT BCD code

When dialing, the corresponding 4-bit BCD codes are serially presented on DOUT from MSB to LSB. The data of DOUT is valid at the falling edge of the CLOCK pin.

The following table lists the BCD codes corresponding to the keyboard input.

Key-In	BCD Code	Key-In	BCD Code
1	0001	8	1000
2	0010	9	1001
3	0011	0	1010
4	0100	*/T	1101
5	0101	#	1100
6	0110	F	1011
7	0111	P	1110

Key definition

- 0,1,2,3,4,5,6,7,8,9 keys

These are dialing number input keys for both the pulse mode and the tone mode operations.

- */T

This key executes the P→T function and waits a $T_{P \rightarrow T}$ duration in the pulse mode. On the other hand, the */T key executes the * function in the tone mode.

- #

This is a dialing signal key for the tone mode only, no response in the pulse mode.

- R/P

Redial and pause function key. If it is pressed as the first key after off-hook, this key executes the redial function. Otherwise, it works as the pause key.

- ST

Store key. The execution of this key actuates the store memory function with (or without) dialing output. During the dialing signal transmission, the ST key is inhibited.

- F

The flash key is a control key. Pressing the F key will force the $\overline{PO}$ pin to be "low" for the T_F duration and is then followed by T_{FP} (sec).

M/B Pin	PR Pin	Flash Time
VSS	VDD	98ms
VSS	VSS	600ms
VDD	VDD	600ms

- EM1~EM3

One-touch memory dialing key. For speed-calling convenience, they provide memory dialing in either pulse or tone mode.

- EM4

The EM4 is a special memory dialing for automatic switching function from pulse to tone (DTMF) mode if the dialing contents include P key (to see the keyboard operation). Otherwise the EM4 speed dialing is the same as EM1~EM3.

- A

Auto key. When this key is pressed before pressing any of the digital keys (0~9) it executes the two-touch memory dialing function.

Keyboard operation

All of the following operations are described under on-off-hook or on-hook condition with the hand-free active condition.

- Normal dialing

- Pulse mode

- (a) without */T

Keyboard input: **D1** **D2** ... **Dn**

Dialing output: D1 D2 ... Dn

RM: D1 D2 ... Dn

- (b) with */T

Keyboard input: **D1** **D2** ... **Dn** ***/T** **Dn+1** ... **Dm**

Dialing output: **D1** **D2** ... **Dn** $T_P \rightarrow T$ **Dn+1** ... **Dm**
Pulse Tone

RM: D1 D2 ... Dn */T Dn+1 ... Dm

- Tone mode

- (a) without */T

Keyboard input: **D1** **D2** ... **Dn**

Dialing output: D1 D2 ... Dn

RM: D1 D2 ... Dn

- (b) with */T

Keyboard input: **D1** **D2** ... **Dn** ***/T** **Dn+1** ... **Dm**

Dialing output: D1 D2 ... Dn * Dn+1 ... Dm

RM: D1 D2 ... Dn * Dn+1 ... Dm

Note: The maximum capacity of the RM memory is 32 digits. When more than 32 digits are entered, the signal is transmitted but the redial function is inhibited.

- Redial

- Pulse mode

- (a) without */T

RM content: D1 D2 ... Dn

Keyboard input: **R/P**

Dialing output: D1 D2 ... Dn

RM: Unchanged

- (b) with */T

RM content: D1 D2 ... Dn */T Dn+1 ... Dm

Keyboard input: **R/P**

Dialing output: **D1** **D2** ... **Dn** $T_P \rightarrow T$ **Dn+1** ... **Dm**
Pulse Tone

RM: Unchanged

- Tone mode

- (a) without */T

RM content: D1 D2 ... Dn

Keyboard input: **R/P**

Dialing output: D1 D2 ... Dn

RM: Unchanged

- (b) with */T

RM content: D1 D2 ... Dn */T Dn+1 ... Dm

Keyboard input: **R/P**

Dialing output: D1 D2 ... Dn * Dn+1 ... Dm

RM: Unchanged

- Memory store

- One-touch memory store (EM1~EM4)

- (a) without dialing output

Keyboard input: **ST** **D1** **D2** ... **Dn** **ST** **EMa**

Dialing output:

EMa: D1 D2 ... Dn

RM: D1 D2 ... Dn

- (b) with dialing output

Keyboard input: **D1** **D2** ... **Dn** **ST** **ST** **EMa**

Dialing output: D1 D2 ... Dn

EMa: D1 D2 ... Dn

RM: D1 D2 ... Dn

- Two-touch memory store

- (a) without dialing output

Keyboard input: **ST** **D1** **D2** ... **Dn** **ST** **a**

Dialing output:

Ma: D1 D2 ... Dn

RM: D1 D2 ... Dn

- (b) with dialing output

Keyboard input: **D1** **D2** ... **Dn** **ST** **ST** **a**

Dialing output: D1 D2 ... Dn

Ma: D1 D2 ... Dn

RM: D1 D2 ... Dn

Note: If the dialing number exceeds 32 digits, the memory store is inhibited.

However, if the dialing number is not more than 32 digits the memory will store a max. of 16 digits .

EMa=EM1~EM4, Ma=M0~M9, a=0~9

- Memory dialing

- One-touch memory dialing (EM1~EM3)

EMa content: D1 D2 ... Dn

Keyboard input: **EMa**

Dialing output: D1 D2 ... Dn

EMa: Unchanged

RM: D1 D2 ... Dn

- One-touch memory dialing (EM4) with P key in the pulse mode

EM4 content: D1 D2 ... Dn P Dn+1 ... Dm

Keyboard input: **EM4**

Dialing output: D1 D2 ... Dn TP→T Dn+1 ... Dm
Pulse Tone

EM4: Unchanged

RM: D1 D2 ... Dn

- One-touch memory dialing (EM4) without P key in the pulse mode

EM4 content: D1 D2 ... Dn Dn+1 ... Dm

Keyboard input: **EM4**

Dialing output: D1 D2 ... Dn Dn+1 ... Dm

EM4: Unchanged

RM: D1 D2 ... Dn Dn+1 ... Dm

- Two-touch memory dialing (M0~M9)

Ma content: D1 D2 ... Dn

Keyboard input: **A** **a**

Dialing output: D1 D2 ... Dn

Ma: Unchanged

RM: D1 D2 ... Dn

Note: EMa=EM1~EM3, Ma=M0~M9, a=0~9

The EM4 memory dialing is the same as EM1~EM3 in the tone (DTMF) mode.

- Chain dialing

EM1 content: D1 D2 ... Dn

EM2 content: Dn+1 ... Dm

M1 content: Dm+1 ... DI

M2 content: DI+1 ... Dk

Keyboard input: D1D2D3A1A2EM1EM2

Dialing output: D1 D2 D3 Dm+1 ... DI DI+1 ... Dk D1 D2 ... Dn Dn+1 ... Dm

EM1/EM2/M1/M2: Unchanged

RM: D1 D2 D3 Dm+1 ... DI DI+1 ... Dk D1 D2 ... Dn Dn+1 ... Dm

Note: The maximum capacity of the RM memory is 32 digits. When the dialing number exceeds 32 digits, redialing is inhibited and $\overline{PO}=VDD$

- Flash

Keyboard input: D1D2 ... DnFDn+1 ... Dm

Dialing output: D1 D2 ... Dn Tf TFP Dn+1 ... Dm

RM: Dn+1 ... Dm

Note: Tf: break a flash time

- Pause

Keyboard input: D1D2 ... DnR/PDn+1 ... Dm

Dialing output: D1 D2 ... Dn Tp Dn+1 ... Dm

RM: D1 D2 ... Dn P Dn+1 ... Dm

- Note

RM: Redial memory

D1 D2 ... Dn: 0~9

Dn+1 ... Dm: 0~9, *, #

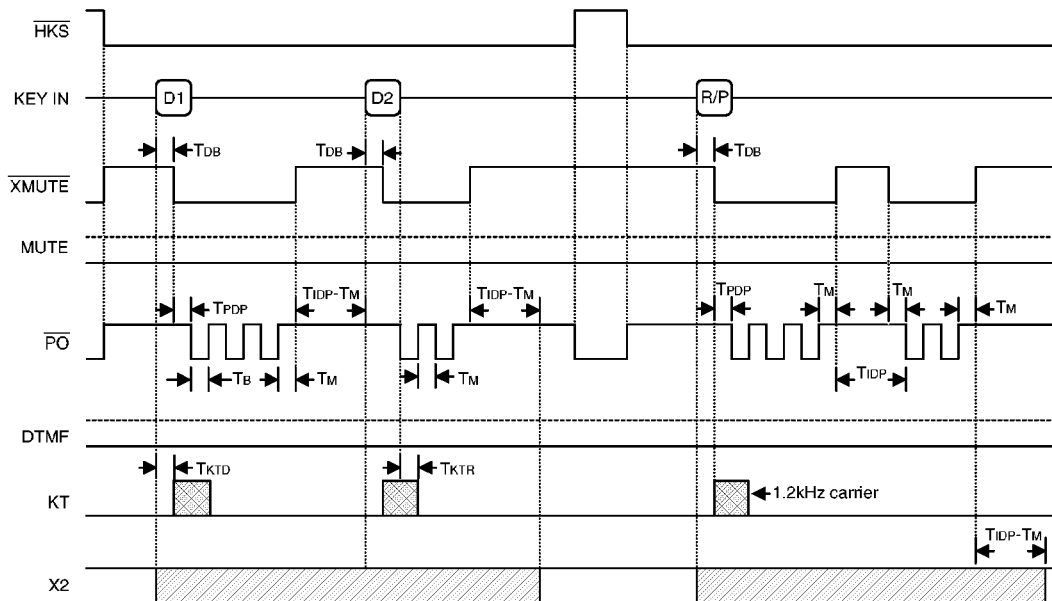
Dm+1 ... DI: 0~9, *, #

DI+1 ... Dk: 0~9, *, #

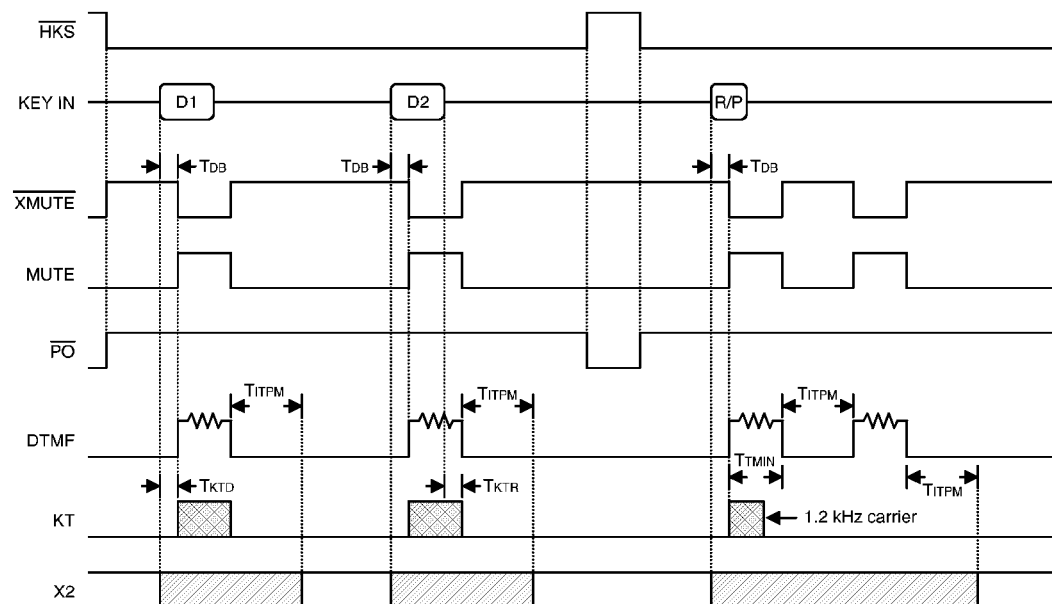
Timing Diagrams

Normal dialing

• Pulse mode

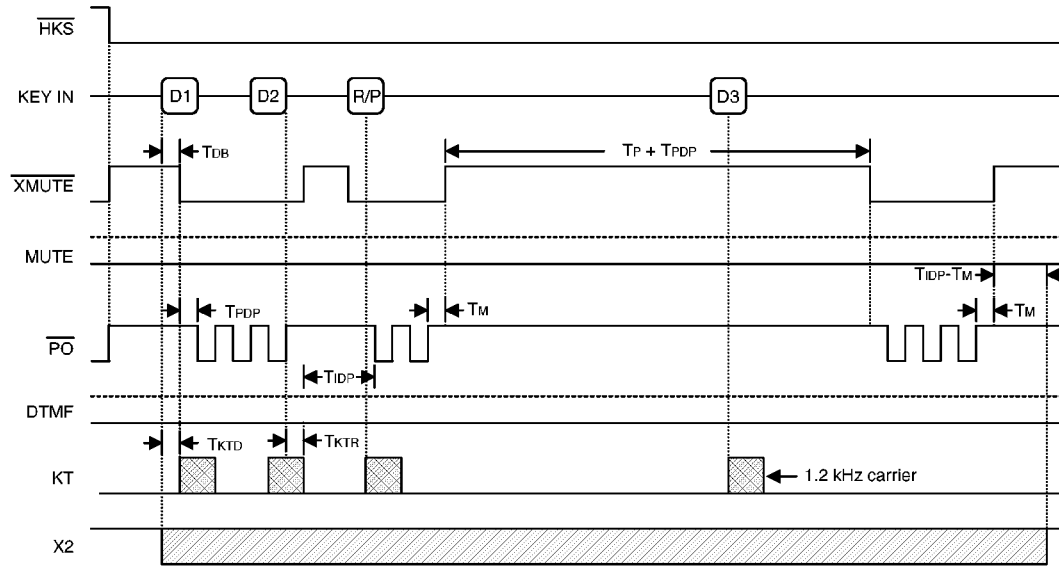


• Tone mode

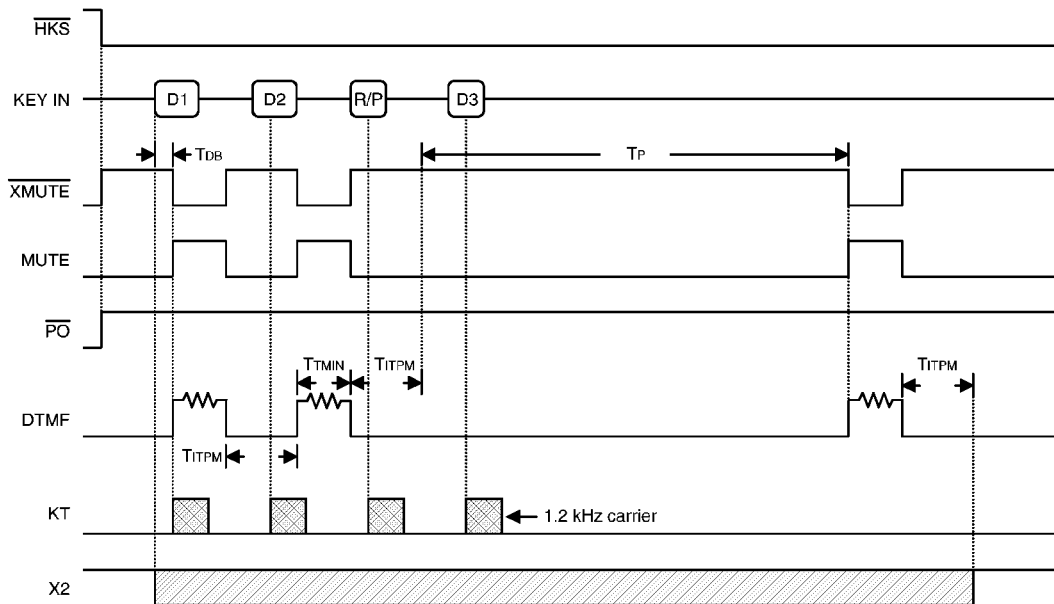


Dialing with pause key

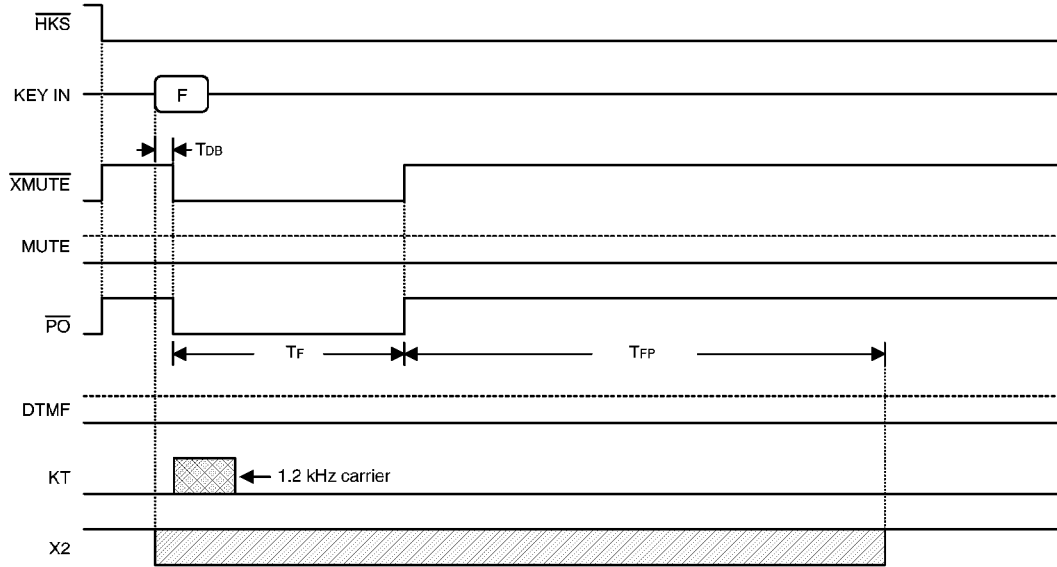
• Pulse mode



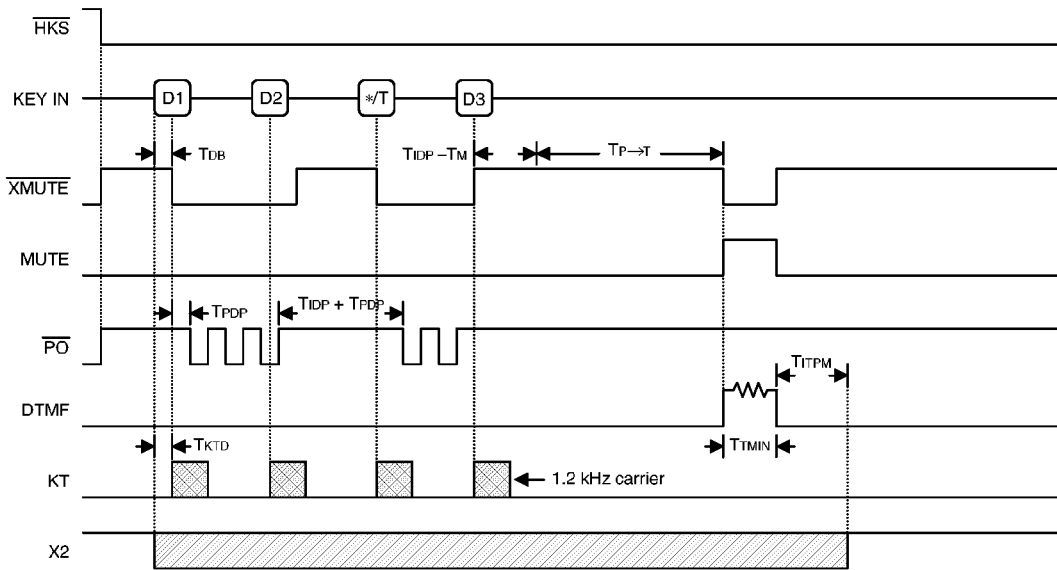
• Tone mode



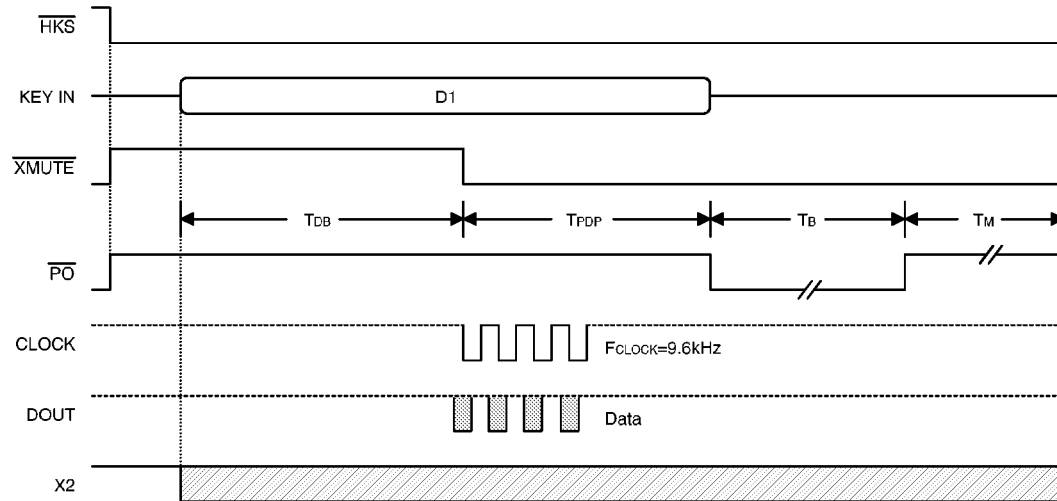
Flash key operation



Pulse→Tone operation

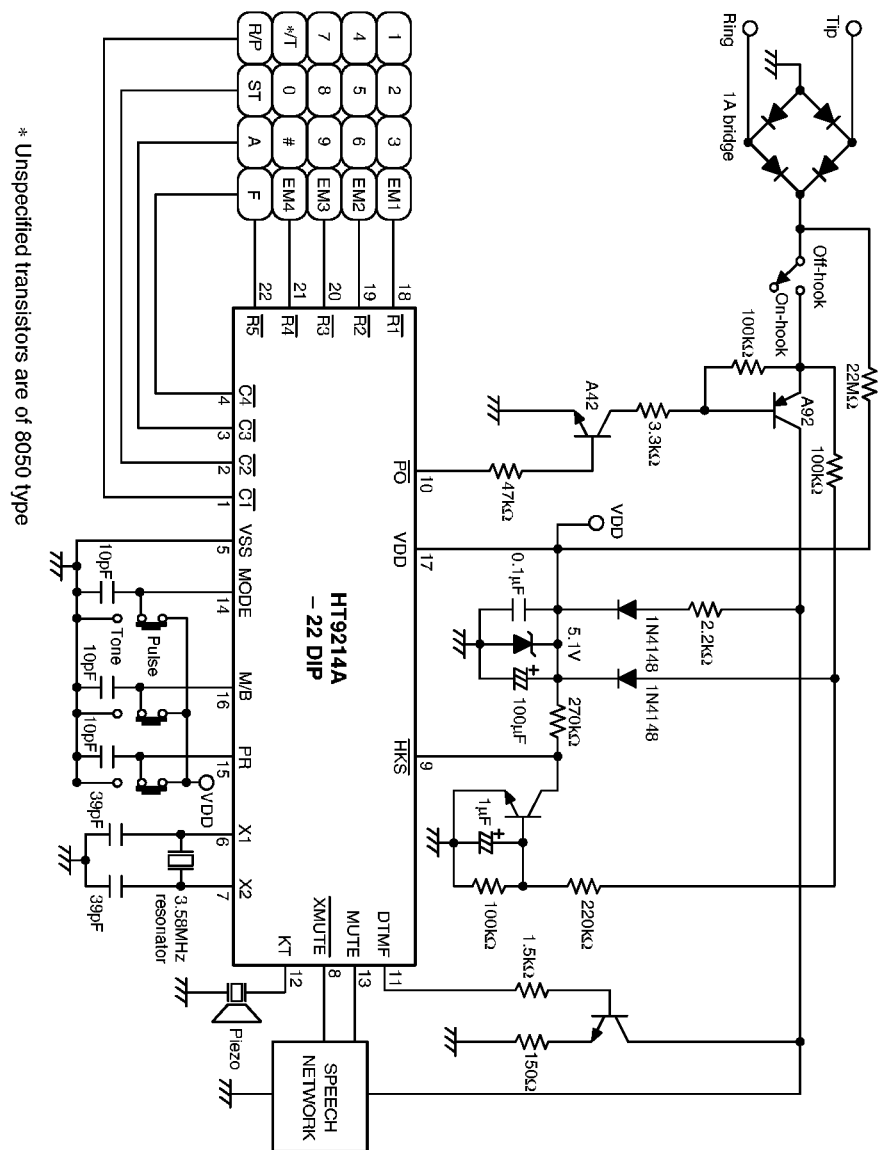


CLOCK & DOUT operation



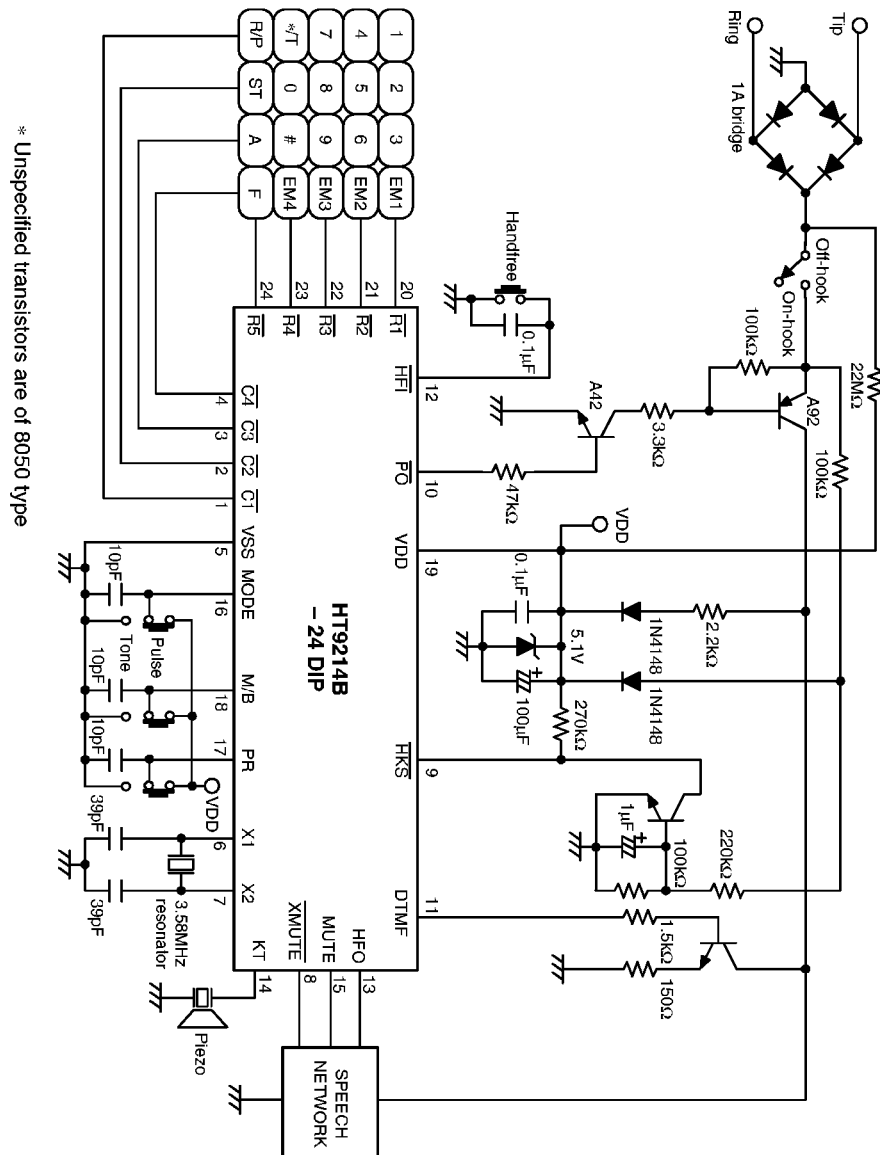
Note: D1=D3=3
D2=2

Application circuit 1

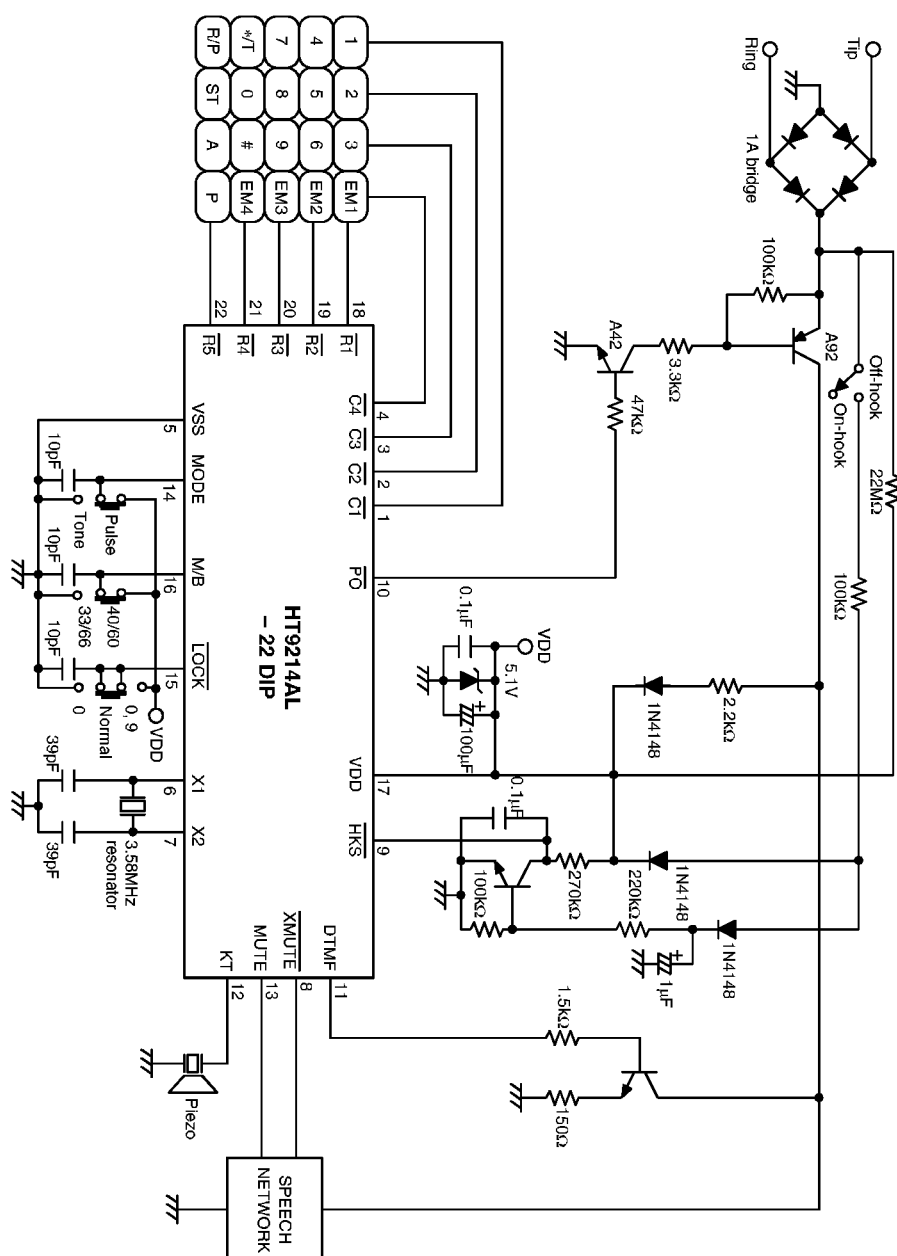


* Unspecified transistors are of 8050 type

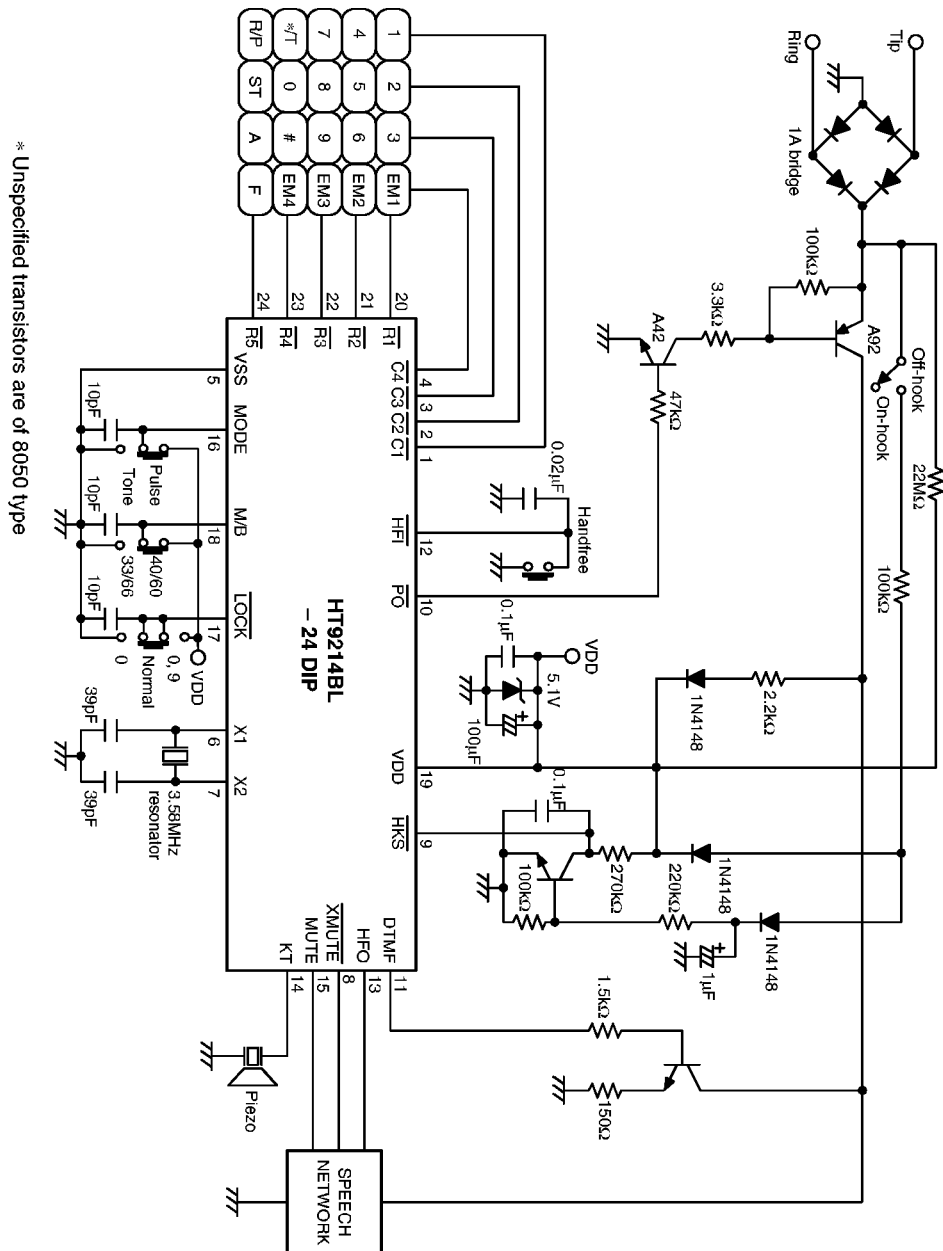
Application circuit 2



* Unspecified transistors are of 8050 type



Application circuit 4



* Unspecified transistors are of 8050 type

* Unspecified transistors are of 8050 type

