



## **iCE40™ LP/HX Family Data Sheet**

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DS1040 Version 02.1, March 2013

## Features

### ■ Flexible Logic Architecture

- Four devices with 384 to 7,680 LUT4s and 21 to 206 I/Os

### ■ Ultra Low Power Devices

- Advanced 40 nm low power process
- As low as 25  $\mu$ W standby power
- Programmable low swing differential I/Os

### ■ Embedded and Distributed Memory

- Up to 128 Kbits sysMEM™ Embedded Block RAM

### ■ Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells

### ■ High Performance, Flexible I/O Buffer

- Programmable sysIO™ buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8
  - LVDS25E, subLVDS
  - Schmitt trigger inputs, to 200 mV typical hysteresis
- Programmable pull-up mode

### ■ Flexible On-Chip Clocking

- Eight low-skew global clock resources
- Up to two analog PLLs per device

### ■ Flexible Device Configuration

- SRAM is configured through:
  - Standard SPI Interface
  - Internal Nonvolatile Configuration Memory (NVCM)

### ■ Broad Range of Package Options

- QFN, VQFP, TQFP, ucBGA, caBGA, and csBGA package options
- Small footprint package options
  - As small as 2.5x2.5mm
- Advanced halogen-free packaging

**Table 1-1. iCE40 Family Selection Guide**

| Part Number                      | LP384 | LP1K                                  | LP4K               | LP8K               | HX1K           | HX4K  | HX8K  |
|----------------------------------|-------|---------------------------------------|--------------------|--------------------|----------------|-------|-------|
| Logic Cells (LUT + Flip-Flop)    | 384   | 1,280                                 | 3,520              | 7,680              | 1,280          | 3,520 | 7,680 |
| RAM4K Memory Blocks              | 0     | 16                                    | 20                 | 32                 | 16             | 20    | 32    |
| RAM4K RAM bits                   | 0     | 64K                                   | 80K                | 128K               | 64K            | 80K   | 128K  |
| Phase-Locked Loops (PLLs)        | 0     | 1 <sup>1</sup>                        | 2 <sup>2</sup>     | 2                  | 1 <sup>1</sup> | 2     | 2     |
| Maximum Programmable I/O Pins    | 63    | 95                                    | 167                | 178                | 95             | 95    | 206   |
| Maximum Differential Input Pairs | 8     | 12                                    | 20                 | 23                 | 11             | 12    | 26    |
| Package                          | Code  | Programmable I/O: Max Inputs (LVDS25) |                    |                    |                |       |       |
| 32 QFN<br>(5 x 5mm, 0.5mm)       | SG32  | 21(4)                                 |                    |                    |                |       |       |
| 36 ucBGA<br>(2.5 x 2.5mm, 0.4mm) | CM36  | 25(3)                                 | 25(3) <sup>1</sup> |                    |                |       |       |
| 49 ucBGA<br>(3 x 3mm, 0.4mm)     | CM49  | 37(6)                                 | 35(5)              |                    |                |       |       |
| 81 ucBGA<br>(4 x 4mm, 0.4mm)     | CM81  | 55(3)                                 | 63(8)              | 63(9) <sup>2</sup> |                |       |       |
| 81 csBGA<br>(5 x 5mm, 0.5mm)     | CB81  |                                       | 62(9) <sup>1</sup> |                    |                |       |       |
| 84 QFN<br>(7 x 7mm, 0.5mm)       | QN84  |                                       | 67(7) <sup>1</sup> |                    |                |       |       |

**Table 1-1. iCE40 Family Selection Guide (Cont.)**

| Package                              | Code  | LP384                                 | LP1K    | LP4K     | LP8K     | HX1K               | HX4K    | HX8K    |
|--------------------------------------|-------|---------------------------------------|---------|----------|----------|--------------------|---------|---------|
|                                      |       | Programmable I/O: Max Inputs (LVDS25) |         |          |          |                    |         |         |
| 100 VQFP<br>(14 x 14mm, 0.5mm)       | VQ100 |                                       |         |          |          | 72(9) <sup>1</sup> |         |         |
| 121 ucBGA<br>(5 x 5mm, 0.4mm)        | CM121 |                                       | 95 (12) | 93 (13)  | 93 (13)  |                    |         |         |
| 121 csBGA<br>(6 x 6mm, 0.5mm)        | CB121 |                                       | 92 (12) |          |          |                    |         |         |
| 132 csBGA<br>(8 x 8mm, 0.5mm)        | CB132 |                                       |         |          |          | 95(11)             | 95(12)  | 95(12)  |
| 144 TQFP<br>(20 x 20mm, 0.5mm)       | TQ144 |                                       |         |          |          | 96(12)             | 107(14) |         |
| 225 ucBGA<br>(7 x 7mm, 0.4mm)        | CM225 |                                       |         | 167 (20) | 178 (23) |                    |         | 178(23) |
| 256-ball caBGA<br>(14 x 14mm, 0.8mm) | CT256 |                                       |         |          |          |                    |         | 206(26) |

1. No PLL available on the 36 ucBGA, 81 csBGA, 84 QFN and 100 VQFP packages.

2. Only one PLL available on the 81 ucBGA package.

## Introduction

The iCE40 family of ultra-low power, non-volatile FPGAs has four devices with densities ranging from 384 to 7680 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices feature Embedded Block RAM (EBR), Non-volatile Configuration Memory (NVCM) and Phase Locked Loops (PLLs). These features allow the devices to be used in low-cost, high-volume consumer and system applications.

The iCE40 devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as programmable low-swing differential I/Os and the ability to turn off on-chip PLLs dynamically. These features help manage static and dynamic power consumption, resulting in low static power for all members of the family. The iCE40 devices are available in two versions – ultra low power (LP) and high performance (HX) devices.

The iCE40 FPGAs are available in a broad range of advanced halogen-free packages ranging from the space saving 2.5x2.5 mm micro chip-scale BGA to the PCB-friendly 20x20 mm TQFP. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The iCE40 devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash or be configured by an external master such as a CPU.

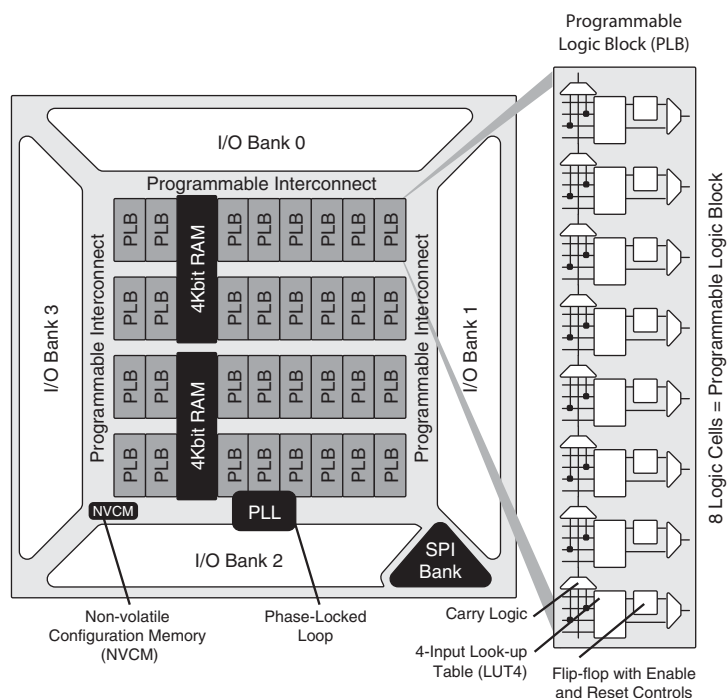
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 family of devices. Popular logic synthesis tools provide synthesis library support for iCE40. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 FPGA family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

## Architecture Overview

The iCE40 family architecture contains an array of Programmable Logic Blocks (PLB), sysCLOCK™ PLLs, Non-volatile Programmable Configuration Memory (NVCM) and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1 shows the block diagram of the iCE40-1K device.

**Figure 2-1. iCE40-1K Device, Top View**



The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either logic blocks or EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 family, there are up to four independent sysIO banks. Note on some packages  $V_{CCIO}$  banks are tied together. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 Kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO.

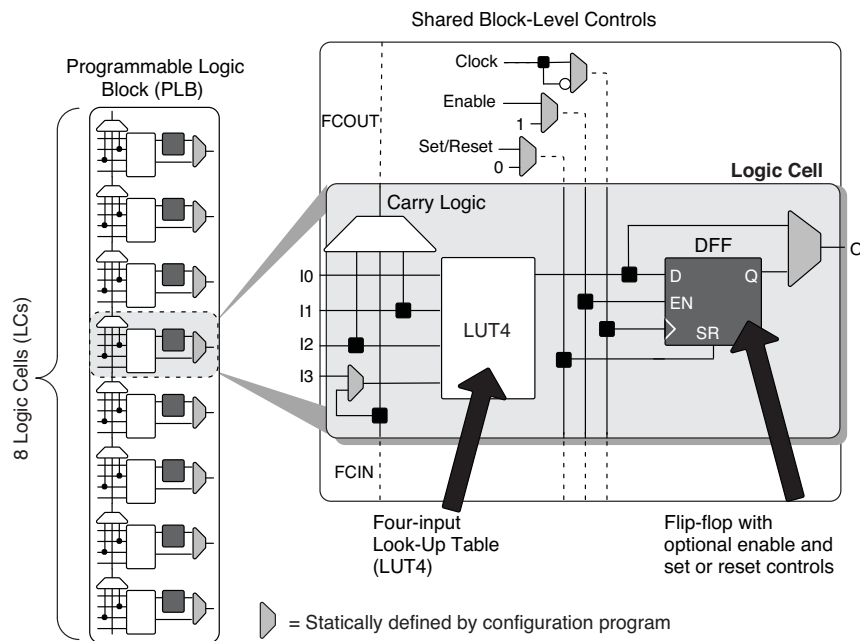
The iCE40 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

Every device in the family has a SPI port that supports programming and configuration of the device. The iCE40 includes on-chip, Nonvolatile Configuration Memory (NVCM).

### PLB Blocks

The core of the iCE40 device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

**Figure 2-2. PLB Block Diagram**



### Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

**Table 2-1. Logic Cell Signal Descriptions**

| Function | Type             | Signal Names    | Description                                                                                                          |
|----------|------------------|-----------------|----------------------------------------------------------------------------------------------------------------------|
| Input    | Data signal      | I0, I1, I2, I3  | Inputs to LUT4                                                                                                       |
| Input    | Control signal   | Enable          | Clock enable shared by all LCs in the PLB                                                                            |
| Input    | Control signal   | SR <sup>1</sup> | Asynchronous or synchronous local set/reset shared by all LCs in the PLB.                                            |
| Input    | Control signal   | Clock           | Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB |
| Input    | Inter-PLB signal | FCIN            | Fast carry in                                                                                                        |
| Output   | Data signals     | O               | LUT4 output or register bypass signals                                                                               |
| Output   | Inter-PFU signal | FCO             | Fast carry out                                                                                                       |

1. If SR is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration or by the Global Reset signal.

### Modes of Operation

Each LC has up to two potential modes of operation: Logic or ROM.

**Logic Mode:** In this mode, the LCs in each PLB are configured as 4-input combinatorial look-up tables. A LUT4 can have 16 possible input combinations. Any four-input logic functions can be generated by programming this lookup table.

**ROM Mode:** ROM mode uses the LUT logic. Preloading is accomplished through the programming interface during PLB configuration.

### Routing

There are many resources provided in the iCE40 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: x1 (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The x1, x4 and x12 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tool take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

### Clock/Control Distribution Network

Each iCE40 device has eight global inputs, two pins on each side of the device. These can be used as clock, reset or enable signals. The dedicated global pins are identified as GBIN[7:0] and the global buffers are identified as-GBUF[7:0]. These eight inputs may be used as general purpose I/O if they are not used to drive the clock nets. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct LVDS25 or subLVDS differential clock input.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to all clock inputs. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

**Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks**

| Global Buffer | LUT Inputs                     | Clock | Clock Enable | Reset |
|---------------|--------------------------------|-------|--------------|-------|
| GBUF0         | Yes, any 4 of 8<br>GBUF Inputs | ✓     | ✓            |       |
| GBUF1         |                                | ✓     |              | ✓     |
| GBUF2         |                                | ✓     | ✓            |       |
| GBUF3         |                                | ✓     |              | ✓     |
| GBUF4         |                                | ✓     | ✓            |       |
| GBUF5         |                                | ✓     |              | ✓     |
| GBUF6         |                                | ✓     | ✓            |       |
| GBUF7         |                                | ✓     |              | ✓     |

The maximum frequency for the global buffers are shown in the iCE40 External Switching Characteristics tables later in this document.

### Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

## Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application. The PIO flip-flops are always reset during configuration, although the output flip-flop can be inverted before leaving the iCE40 device.

## sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 devices have one or more sysCLOCK PLLs. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 6. The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the  $t_{LOCK}$  parameter has been satisfied.

For more details on the PLL, see TN1251, [iCE40 sysCLOCK PLL Design and Usage Guide](#).

**Figure 2-3. PLL Diagram**

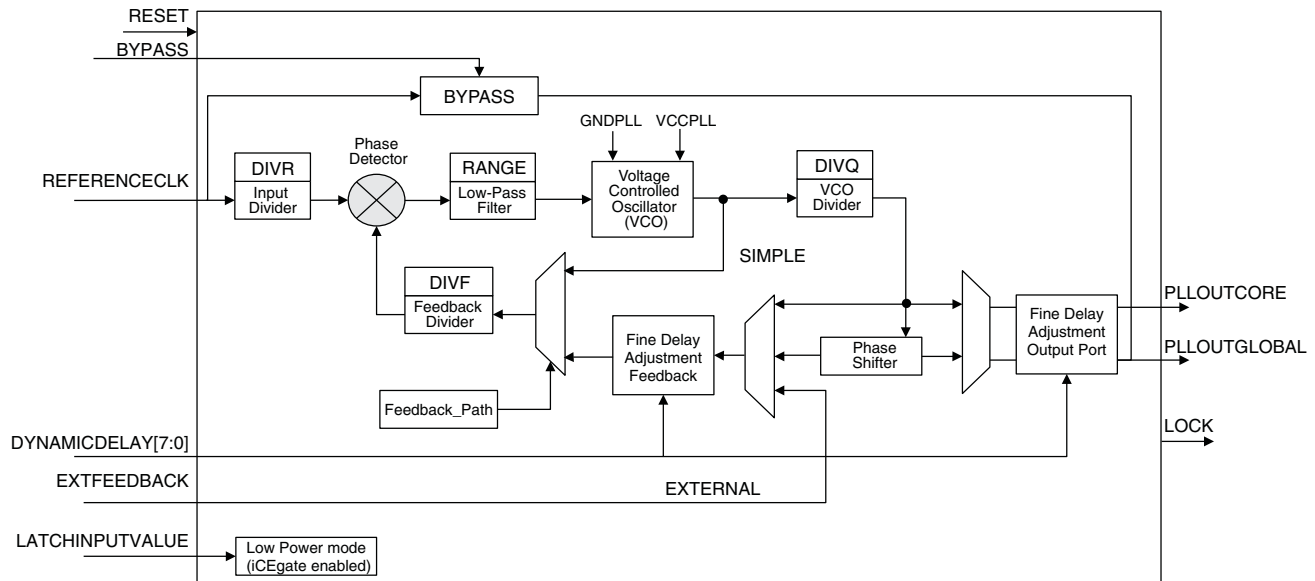


Table 2-3 provides signal descriptions of the PLL block.

**Table 2-3. PLL Signal Descriptions**

| Signal Name       | Direction | Description                                                                                                                                                                                 |
|-------------------|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REFERENCECLK      | Input     | Input reference clock                                                                                                                                                                       |
| BYPASS            | Input     | When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output.<br>0 = PLL generated signal<br>1 = REFERENCECLK                           |
| EXTFEEDBACK       | Input     | External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.                                                                                                |
| DYNAMICDELAY[3:0] | Input     | Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.                                                                                                 |
| LATCHINPUTVALUE   | Input     | When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.                             |
| PLLOUTGLOBAL      | Output    | Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.                               |
| PLLOUTCORE        | Output    | Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port. |
| LOCK              | Output    | When High, indicates that the PLL output is phase aligned or locked to the input reference clock.                                                                                           |
| RESET             | Input     | Active low reset.                                                                                                                                                                           |

## sysMEM Embedded Block RAM Memory

Each iCE40 device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 Kbit in size. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

### sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

**Table 2-4. sysMEM Block Configurations<sup>1</sup>**

| Block RAM Configuration                                              | Block RAM Configuration and Size | WADDR Port Size (Bits) | WDATA Port Size (Bits) | RADDR Port Size (Bits) | RDATA Port Size (Bits) | MASK Port Size (Bits) |
|----------------------------------------------------------------------|----------------------------------|------------------------|------------------------|------------------------|------------------------|-----------------------|
| SB_RAM256x16<br>SB_RAM256x16NR<br>SB_RAM256x16NW<br>SB_RAM256x16NRNW | 256x16 (4K)                      | 8 [7:0]                | 16 [15:0]              | 8 [7:0]                | 16 [15:0]              | 16 [15:0]             |
| SB_RAM512x8<br>SB_RAM512x8NR<br>SB_RAM512x8NW<br>SB_RAM512x8NRNW     | 512x8 (4K)                       | 9 [8:0]                | 8 [7:0]                | 9 [8:0]                | 8 [7:0]                | No Mask Port          |
| SB_RAM1024x4<br>SB_RAM1024x4NR<br>SB_RAM1024x4NW<br>SB_RAM1024x4NRNW | 1024x4 (4K)                      | 10 [9:0]               | 4 [3:0]                | 10 [9:0]               | 4 [3:0]                | No Mask Port          |
| SB_RAM2048x2<br>SB_RAM2048x2NR<br>SB_RAM2048x2NW<br>SB_RAM2048x2NRNW | 2048x2 (4K)                      | 11 [10:0]              | 2 [1:0]                | 11 [10:0]              | 2 [1:0]                | No Mask Port          |

1. For iCE40 EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

### RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Note the sysMEM Embedded Block RAM Memory address 0 cannot be initialized.

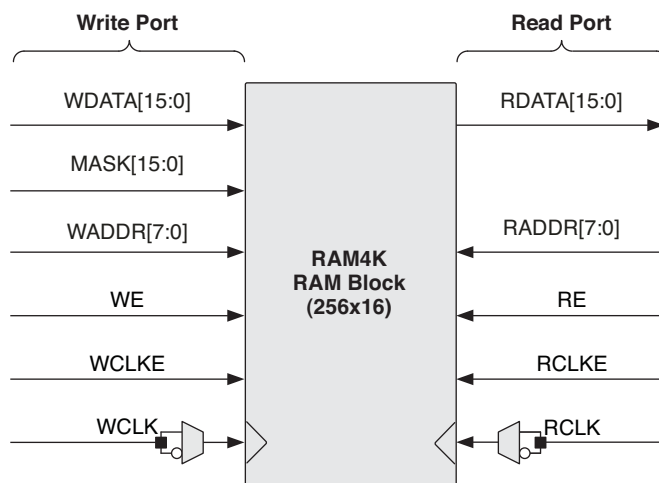
### Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks.

### RAM4k Block

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

**Figure 2-4. sysMEM Memory Primitives**



**Table 2-5. EBR Signal Descriptions**

| Signal Name | Direction | Description                                                                                 |
|-------------|-----------|---------------------------------------------------------------------------------------------|
| WDATA[15:0] | Input     | Write Data input.                                                                           |
| MASK[15:0]  | Input     | Masks write operations for individual data bit-lines.<br>0 = write bit; 1 = don't write bit |
| WADDR[7:0]  | Input     | Write Address input. Selects one of 256 possible RAM locations.                             |
| WE          | Input     | Write Enable input.                                                                         |
| WCLKE       | Input     | Write Clock Enable input.                                                                   |
| WCLK        | Input     | Write Clock input. Default rising-edge, but with falling-edge option.                       |
| RDATA[15:0] | Output    | Read Data output.                                                                           |
| RADDR[7:0]  | Input     | Read Address input. Selects one of 256 possible RAM locations.                              |
| RE          | Input     | Read Enable input.                                                                          |
| RCLKE       | Input     | Read Clock Enable input.                                                                    |
| RCLK        | Input     | Read Clock input. Default rising-edge, but with falling-edge option.                        |

For further information on the sysMEM EBR block, please refer to TN1250, [Memory Usage Guide for iCE40 Devices](#).

## sysIO

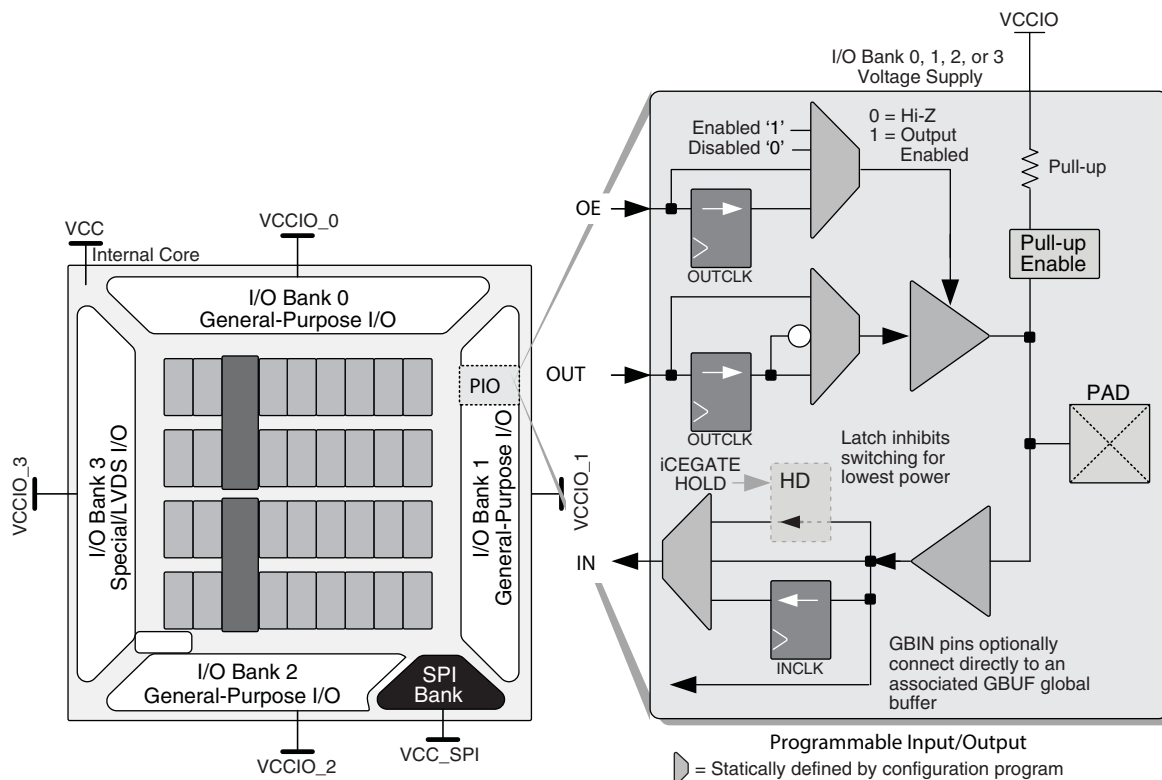
### Buffer Banks

iCE40 devices have up to four I/O banks with independent Vccio rails with an additional configuration bank V<sub>CC\_SPI</sub> for the SPI I/Os.

### Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. The PIOs are placed on all four sides of the device.

**Figure 2-5. I/O Bank and Programmable I/O Cell**



The PIO contains three blocks: an input register block, output register block iCEgate™ and tri-state register block. To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

**Table 2-6. PIO Signal List**

| Pin Name          | I/O Type | Description                   |
|-------------------|----------|-------------------------------|
| OUTPUT_CLK        | Input    | Output register clock         |
| CLOCK_ENABLE      | Input    | Output register clock enable  |
| INPUT_CLK         | Input    | Input register clock          |
| OUTPUT_ENABLE     | Input    | Output enable                 |
| D_OUT_0/1         | Input    | Output data from the core     |
| D_IN_0/1          | Output   | Input data to the core        |
| LATCH_INPUT_VALUE | Input    | Latches/holds the Input Value |

### Input Register Block

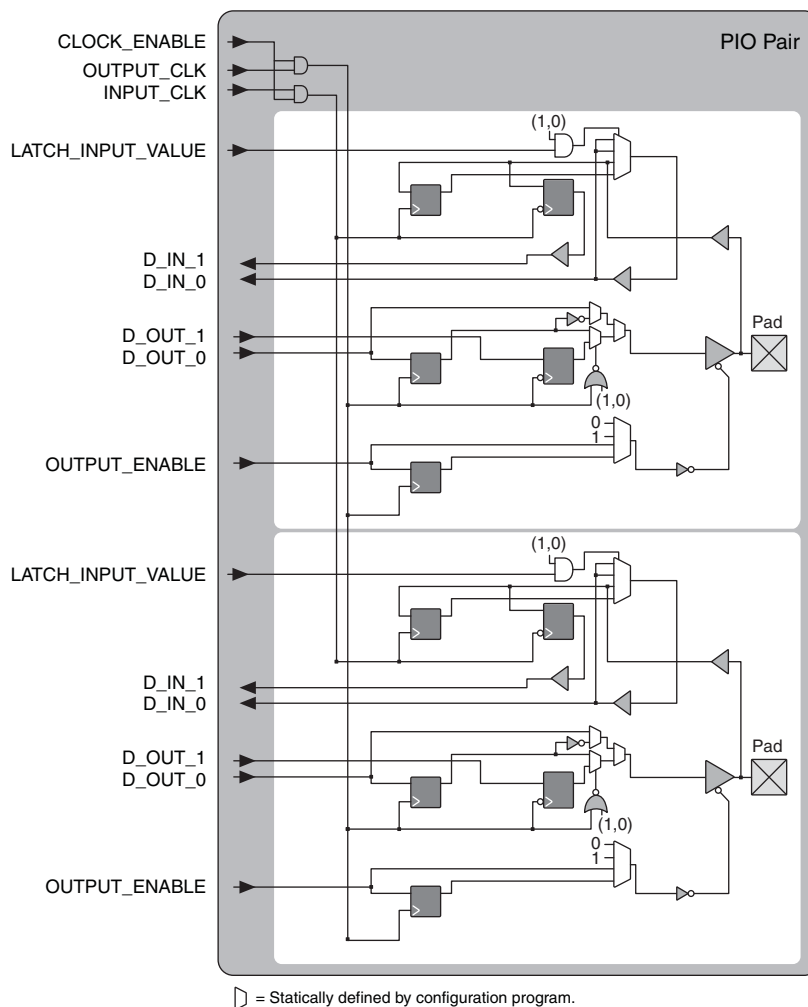
The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock signal, creating two data streams.

### Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysIO buffers. In Generic DDR mode, two registers are used to capture the data on the positive and negative edge of the system clock and then muxed creating one data stream.

Figure 2-6 shows the input/output register block for the PIOs.

**Figure 2-6. iCE I/O Register Block Diagram**



### sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS and LVDS25.

Each bank is capable of supporting multiple I/O standards. In the iCE40 devices, single-ended LVCMOS buffers, differential LVDS25E output buffers and Bank 3 additionally support differential LVDS25 input buffers. Each sysIO bank has its own dedicated power supply.

### Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when  $V_{CC}$ ,  $V_{CCIO\_2}$ ,  $V_{PP\_2V5}$ , and  $V_{CC\_SPI}$  have reached the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all  $V_{CCIO}$  banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to  $V_{CCIO}$ . The I/O pins will maintain the pre-configuration state until  $V_{CC}$  and  $V_{CCIO}$  (for I/O banks containing configuration I/Os) have reached levels, at which time the I/Os will take on the software user-configured settings only after a proper download/configuration. Unused I/Os are automatically blocked and the pullup termination is disabled.

### Supported Standards

The iCE40 sysIO buffer supports both single-ended and Bank 3 supports differential input standards. The single-ended standard supported is LVCMOS. The buffer supports the LVCMOS 1.8, 2.5, and 3.3V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 devices.

**Table 2-7. Supported Input Standards**

| Input Standard                 | $V_{CCIO}$ (Typical) |      |      |
|--------------------------------|----------------------|------|------|
|                                | 3.3V                 | 2.5V | 1.8V |
| <b>Single-Ended Interfaces</b> |                      |      |      |
| LVCMOS33                       | ✓                    |      |      |
| LVCMOS25                       |                      | ✓    |      |
| LVCMOS18                       |                      |      | ✓    |
| <b>Differential Interfaces</b> |                      |      |      |
| LVDS25 <sup>1</sup>            |                      | ✓    |      |
| subLVDS <sup>1</sup>           |                      |      | ✓    |

1. Bank 3 only.

**Table 2-8. Supported Output Standards**

| Output Standard                | $V_{CCIO}$ (Typical) |
|--------------------------------|----------------------|
| <b>Single-Ended Interfaces</b> |                      |
| LVCMOS33                       | 3.3                  |
| LVCMOS25                       | 2.5                  |
| LVCMOS18                       | 1.8                  |
| <b>Differential Interfaces</b> |                      |
| LVDS25E <sup>1</sup>           | 2.5                  |
| subLVDSE <sup>1</sup>          | 1.8                  |

1. These interfaces can be emulated with external resistors in all devices.

### Non-Volatile Configuration Memory

All iCE40 devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, [iCE40 Programming and Configuration Usage Guide](#).

## Power On Reset

iCE40 devices have power-on reset circuitry to monitor  $V_{CC}$ ,  $V_{CCIO\_2}$ ,  $V_{PP\_2V5}$ , and  $V_{CC\_SPI}$  voltage levels during power-up and operation. At power-up, the POR circuitry monitors  $V_{CC}$ ,  $V_{CCIO\_2}$ ,  $V_{PP\_2V5}$ , and  $V_{CC\_SPI}$  (controls configuration) voltage levels. It then triggers download from the on-chip NVCM or external Flash memory after reaching the power-up levels specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

## Programming and Configuration

This section describes the programming and configuration of the iCE40 family.

### Device Programming

The NVCM memory can be programmed through the SPI port.

### Device Configuration

There are various ways to configure the Configuration RAM (CRAM) including:

1. Internal NVCM Download
2. From a SPI Flash (Master SPI mode)
3. System microprocessor to drive a Serial Slave SPI port (SSPI mode)

The image to configure CRAM can be selected by the user on power up (Cold Boot) or once powered up (Warm Boot).

For more details on programming and configuration, see TN1248, [iCE40 Programming and Configuration Usage Guide](#).

## Power Saving Options

iCE40 devices are available in two options for maximum flexibility: LP and HX devices. The LP devices have ultra low static and dynamic power consumption. HX devices are designed to provide high performance. Both the LP and the HX devices operate at 1.2V  $V_{CC}$ .

iCE40 devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. While these features are available in both device types, these features are mainly intended for use with iCE40 LP devices to manage power consumption.

**Table 2-9. iCE40 Power Saving Features Description**

| Device Subsystem | Feature Description                                                                                                                                                                                                             |
|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PLL              | When LATCHINPUTVALUE is enabled, forces the PLL into low-power mode; PLL output held static at last input clock value.                                                                                                          |
| iCEGate          | To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control. |

### Absolute Maximum Ratings<sup>1, 2, 3</sup>

#### iCE40 LP/HX

|                                                  |                |
|--------------------------------------------------|----------------|
| Supply Voltage $V_{CC}$                          | -0.5 to 1.42V  |
| Output Supply Voltage $V_{CCIO}$ , $V_{CC\_SPI}$ | -0.5 to 3.60V  |
| NVCM Supply Voltage $V_{PP\_2V5}$                | -0.5 to 3.60V  |
| PLL Supply Voltage $V_{CCPLL}$                   | -0.5 to 1.30V  |
| I/O Tri-state Voltage Applied                    | -0.5 to 3.60V  |
| Dedicated Input Voltage Applied                  | -0.5 to 3.60V  |
| Storage Temperature (Ambient)                    | -65°C to 150°C |
| Junction Temperature ( $T_J$ )                   | -55°C to 125°C |

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.

### Recommended Operating Conditions<sup>1</sup>

| Symbol                               | Parameter                                                         |                          | Min. | Max. | Units |
|--------------------------------------|-------------------------------------------------------------------|--------------------------|------|------|-------|
| V <sub>CC</sub> <sup>1</sup>         | Core Supply Voltage                                               |                          | 1.14 | 1.26 | V     |
| V <sub>PP_2V5</sub>                  | V <sub>PP_2V5</sub> NVCM Programming and Operating Supply Voltage | Slave SPI Configuration  | 1.71 | 3.46 | V     |
|                                      |                                                                   | Master SPI Configuration | 2.30 | 3.46 | V     |
|                                      |                                                                   | Configure from NVCM      | 2.30 | 3.46 | V     |
|                                      |                                                                   | NVCM Programming         | 2.30 | 3.00 | V     |
| V <sub>PP_FAST</sub> <sup>4</sup>    | Optional fast NVCM programming supply. Leave unconnected.         |                          | N/A  | N/A  | V     |
| V <sub>CCPLL</sub> <sup>5, 6</sup>   | PLL Supply Voltage                                                |                          | 1.14 | 1.26 | V     |
| V <sub>CCIO</sub> <sup>1, 2, 3</sup> | I/O Driver Supply Voltage                                         | V <sub>CCIO0-3</sub>     | 1.71 | 3.46 | V     |
|                                      |                                                                   | V <sub>CC_SPI</sub>      | 1.71 | 3.46 | V     |
| t <sub>JIND</sub>                    | Junction Temperature Industrial Operation                         |                          | -40  | 100  | °C    |
| t <sub>PROG</sub>                    | Junction Temperature NVCM Programming                             |                          | 10   | 30   | °C    |

1. Like power supplies must be tied together. For example, if  $V_{CCIO}$  and  $V_{CC\_SPI}$  are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3.  $V_{CCIO}$  pins of unused I/O banks should be connected to the  $V_{CC}$  power supply on boards.
4.  $V_{PP\_FAST}$ , used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the  $V_{PP\_FAST}$  ball connected to  $V_{CCIO0}$  ball externally.
5. No PLL available on the iCE40-LP384 device.
6.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

### Power Supply Ramp Rates<sup>1, 2</sup>

| Symbol     | Parameter                                       |                                                                                               | Min. | Max. | Units |
|------------|-------------------------------------------------|-----------------------------------------------------------------------------------------------|------|------|-------|
| $t_{RAMP}$ | Power supply ramp rates for all power supplies. | All configuration modes. No power supply sequencing.                                          | 0.40 | 10   | V/ms  |
|            |                                                 | Configuring from NVCM. $V_{CC}$ and $V_{PP\_2V5}$ to be powered 0.25ms before $V_{CC\_SPI}$ . | 0.01 | 10   | V/ms  |
|            |                                                 | Configuring from MSPI. $V_{CC}$ and $V_{PP\_SPI}$ to be powered 0.25ms before $V_{PP\_2V5}$ . | 0.01 | 10   | V/ms  |

1. Assumes monotonic ramp rates.
2. iCE40LP384 status is Advanced, iCE40LP4K/iCE40LP8K status is Preliminary.

### Power-On-Reset Voltage Levels<sup>1, 2</sup>

| Symbol      | Parameter                                                                                                                           |               | Min. | Max. | Units |
|-------------|-------------------------------------------------------------------------------------------------------------------------------------|---------------|------|------|-------|
| $V_{PORUP}$ | Power-On-Reset ramp-up trip point (band gap based circuit monitoring $V_{CC}$ , $V_{CCIO\_2}$ , $V_{CC\_SPI}$ and $V_{PP\_2V5}$ )   | $V_{CC}$      | 0.55 | 0.75 | V     |
|             |                                                                                                                                     | $V_{CCIO\_2}$ | 0.86 | 1.29 | V     |
|             |                                                                                                                                     | $V_{CC\_SPI}$ | 0.86 | 1.29 | V     |
|             |                                                                                                                                     | $V_{PP\_2V5}$ | 0.86 | 1.33 | V     |
| $V_{PORDN}$ | Power-On-Reset ramp-down trip point (band gap based circuit monitoring $V_{CC}$ , $V_{CCIO\_2}$ , $V_{CC\_SPI}$ and $V_{PP\_2V5}$ ) | $V_{CC}$      | —    | 0.75 | V     |
|             |                                                                                                                                     | $V_{CCIO\_2}$ | —    | 1.29 | V     |
|             |                                                                                                                                     | $V_{CC\_SPI}$ | —    | 1.29 | V     |
|             |                                                                                                                                     | $V_{PP\_2V5}$ | —    | 1.33 | V     |

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. iCE40LP384 status is Advanced, iCE40LP4K/iCE40LP8K status is Preliminary.

### ESD Performance

Please refer to the [iCE40 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.

### DC Electrical Characteristics

#### Over Recommended Operating Conditions

| Symbol                                 | Parameter                                    | Condition                                                                         | Min. | Typ. | Max.  | Units   |
|----------------------------------------|----------------------------------------------|-----------------------------------------------------------------------------------|------|------|-------|---------|
| $I_{IL}, I_{IH}$ <sup>1, 3, 4, 5</sup> | Input or I/O Leakage                         | $0V < V_{IN} < V_{CCIO} + 0.2V$                                                   | —    | —    | +/-10 | $\mu A$ |
| $C_1$                                  | I/O Capacitance <sup>2</sup>                 | $V_{CCIO} = 3.3V, 2.5V, 1.8V$<br>$V_{CC} = Typ., V_{IO} = 0$ to $V_{CCIO} + 0.2V$ | —    | 6    | —     | pf      |
| $C_2$                                  | Global Input Buffer Capacitance <sup>2</sup> | $V_{CCIO} = 3.3V, 2.5V, 1.8V$<br>$V_{CC} = Typ., V_{IO} = 0$ to $V_{CCIO} + 0.2V$ | —    | 6    | —     | pf      |
| $V_{HYST}$                             | Input Hysteresis                             | $V_{CCIO} = 1.8V, 2.5V, 3.3V$                                                     | —    | 200  | —     | mV      |
| $I_{PU}$ <sup>4</sup>                  | Internal PIO Pull-up Current                 | $V_{CCIO} = 1.8V, 0 \leq V_{IN} \leq 0.65 V_{CCIO}$                               | -3   | —    | -31   | $\mu A$ |
|                                        |                                              | $V_{CCIO} = 2.5V, 0 \leq V_{IN} \leq 0.65 V_{CCIO}$                               | -8   | —    | -72   | $\mu A$ |
|                                        |                                              | $V_{CCIO} = 3.3V, 0 \leq V_{IN} \leq 0.65 V_{CCIO}$                               | -11  | —    | -128  | $\mu A$ |

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2.  $T_J$  25°C,  $f = 1.0$  MHz.
3. Please refer to  $V_{IL}$  and  $V_{IH}$  in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Does not apply to the IOs in the SPI bank.
5. Some products are clamped to a diode when  $V_{IN}$  is larger than  $V_{CCIO}$ .

### Static Supply Current – LP Devices<sup>1, 2, 3, 4, 7</sup>

| Symbol                  | Parameter                                           | Device      | Typ. $V_{CC}^4$ | Units   |
|-------------------------|-----------------------------------------------------|-------------|-----------------|---------|
| $I_{CC}$                | Core Power Supply                                   | iCE40LP384  | 21              | $\mu A$ |
|                         |                                                     | iCE40LP1K   | 100             | $\mu A$ |
|                         |                                                     | iCE40LP4K   | 360             | $\mu A$ |
|                         |                                                     | iCE40LP8K   | 360             | $\mu A$ |
| $I_{CCPLL}^{5,6}$       | PLL Power Supply                                    | All devices | 10              | $\mu A$ |
| $I_{PP\_2V5}$           | NVCM Power Supply                                   | All devices |                 | $\mu A$ |
| $I_{CCIO}, I_{CC\_SPI}$ | Bank Power Supply <sup>4</sup><br>$V_{CCIO} = 2.5V$ | All devices |                 | $\mu A$ |

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at  $V_{CCIO}$  or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3.  $T_J = 25^\circ C$ , power supplies at nominal voltage.
4. Does not include pull-up.
5. No PLL available on the iCE40-LP384 device.
6.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.
7. iCE40LP384 status is Advanced, iCE40LP4K/iCE40LP8K status is Preliminary.

### Static Supply Current – Preliminary – HX Devices<sup>1, 2, 3, 4</sup>

| Symbol                  | Parameter                                           | Device      | Typ. $V_{CC}^4$ | Units   |
|-------------------------|-----------------------------------------------------|-------------|-----------------|---------|
| $I_{CC}$                | Core Power Supply                                   | iCE40HX1K   | 267             | $\mu A$ |
|                         |                                                     | iCE40HX4K   | 667             | $\mu A$ |
|                         |                                                     | iCE40HX8K   | 1100            | $\mu A$ |
| $I_{CCPLL}^5$           | PLL Power Supply                                    | All devices | 25              | $\mu A$ |
| $I_{PP\_2V5}$           | NVCM Power Supply                                   | All devices |                 | $\mu A$ |
| $I_{CCIO}, I_{CC\_SPI}$ | Bank Power Supply <sup>4</sup><br>$V_{CCIO} = 2.5V$ | All devices |                 | $\mu A$ |

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at  $V_{CCIO}$  or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3.  $T_J = 25^\circ C$ , power supplies at nominal voltage.
4. Does not include pull-up.
5.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

### Programming NVCM Supply Current – Preliminary – LP Devices<sup>1, 2, 3, 4</sup>

| Symbol                  | Parameter                      | Device      | Typ. $V_{CC}^5$ | Units   |
|-------------------------|--------------------------------|-------------|-----------------|---------|
| $I_{CC}$                | Core Power Supply              | iCE40LP384  |                 | $\mu A$ |
|                         |                                | iCE40LP1K   |                 | $\mu A$ |
|                         |                                | iCE40LP4K   |                 | $\mu A$ |
|                         |                                | iCE40LP8K   |                 | $\mu A$ |
| $I_{CCPLL}^{6,7}$       | PLL Power Supply               | All devices |                 | $\mu A$ |
| $I_{PP\_2V5}$           | NVCM Power Supply              | All devices |                 | $\mu A$ |
| $I_{PP\_FAST}^8$        | NVCM Programming Supply        | All devices |                 | $\mu A$ |
| $I_{CCIO}, I_{CC\_SPI}$ | Bank Power Supply <sup>5</sup> | All devices |                 | $\mu A$ |

1. Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4.  $T_J = 25^\circ C$ , power supplies at nominal voltage.
5. Per bank.  $V_{CCIO} = 2.5V$ . Does not include pull-up.
6. No PLL available on the iCE40-LP384 device.
7.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.
8.  $V_{PP\_FAST}$ : used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the  $V_{PP\_FAST}$  ball connected to  $V_{CCIO\_0}$  ball externally.

### Programming NVCM Supply Current – Preliminary – HX Devices<sup>1, 2, 3, 4</sup>

| Symbol                  | Parameter                      | Device      | Typ. $V_{CC}^5$ | Units   |
|-------------------------|--------------------------------|-------------|-----------------|---------|
| $I_{CC}$                | Core Power Supply              | iCE40HX1K   |                 | $\mu A$ |
|                         |                                | iCE40HX4K   |                 | $\mu A$ |
|                         |                                | iCE40HX8K   |                 | $\mu A$ |
| $I_{CCPLL}^6$           | PLL Power Supply               | All devices |                 | $\mu A$ |
| $I_{PP\_2V5}$           | NVCM Power Supply              | All devices |                 | mA      |
| $I_{PP\_FAST}^7$        | NVCM Programming Supply        | All devices |                 | $\mu A$ |
| $I_{CCIO}, I_{CC\_SPI}$ | Bank Power Supply <sup>5</sup> | All devices |                 | mA      |

1. Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4.  $T_J = 25^\circ C$ , power supplies at nominal voltage.
5. Per bank.  $V_{CCIO} = 2.5V$ . Does not include pull-up.
6.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.
7.  $V_{PP\_FAST}$ : used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the  $V_{PP\_FAST}$  ball connected to  $V_{CCIO\_0}$  ball externally.

### Peak Startup Supply Current – LP Devices<sup>4</sup>

| Symbol                                          | Parameter               | Device     | Max  | Units |
|-------------------------------------------------|-------------------------|------------|------|-------|
| I <sub>CCPEAK</sub>                             | Core Power Supply       | iCE40LP384 |      | mA    |
|                                                 |                         | iCE40LP1K  | 6.4  | mA    |
|                                                 |                         | iCE40LP4K  | 15.7 | mA    |
|                                                 |                         | iCE40LP8K  | 15.7 | mA    |
| I <sub>CCPLLPEAK</sub> <sup>1, 2</sup>          | PLL Power Supply        | iCE40LP384 |      | mA    |
|                                                 |                         | iCE40LP1K  | 1.5  | mA    |
|                                                 |                         | iCE40LP4K  | 8.0  | mA    |
|                                                 |                         | iCE40LP8K  | 8.0  | mA    |
| I <sub>PP_2V5PEAK</sub>                         | NVCM Power Supply       | iCE40LP384 |      | mA    |
|                                                 |                         | iCE40LP1K  | 7.7  | mA    |
|                                                 |                         | iCE40LP4K  | 4.2  | mA    |
|                                                 |                         | iCE40LP8K  | 4.2  | mA    |
| I <sub>PP_FASTPEAK</sub> <sup>3</sup>           | NVCM Programming Supply | iCE40LP384 |      | mA    |
|                                                 |                         | iCE40LP1K  | 8.1  | mA    |
|                                                 |                         | iCE40LP4K  | 8.8  | mA    |
|                                                 |                         | iCE40LP8K  | 8.8  | mA    |
| I <sub>CCIOPEAK</sub> , I <sub>CC_SPIPEAK</sub> | Bank Power Supply       | iCE40LP384 |      | mA    |
|                                                 |                         | iCE40LP1K  | 3.3  | mA    |
|                                                 |                         | iCE40LP4K  | 8.2  | mA    |
|                                                 |                         | iCE40LP8K  | 8.2  | mA    |

1. No PLL available on the iCE40-LP384 device.

2. V<sub>CCPLL</sub> is tied to V<sub>CC</sub> internally in packages without PLLs pins.

3. V<sub>PP\_FAST</sub>, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V<sub>PP\_FAST</sub> ball connected to V<sub>CCIO\_0</sub> ball externally.

4. iCE40LP4K/iCE40LP8K status is Preliminary.

## Peak Startup Supply Current – Preliminary – HX Devices

| Symbol                          | Parameter | Device    | Max  | Units |
|---------------------------------|-----------|-----------|------|-------|
| $I_{CCPEAK}$                    |           | iCE40HX1K |      | mA    |
|                                 |           | iCE40HX4K | 22.3 | mA    |
|                                 |           | iCE40HX8K | 22.3 | mA    |
| $I_{CCPLLPEAK}^1$               |           | iCE40HX1K |      | mA    |
|                                 |           | iCE40HX4K | 6.4  | mA    |
|                                 |           | iCE40HX8K | 6.4  | mA    |
| $I_{PP\_2V5PEAK}$               |           | iCE40HX1K |      | mA    |
|                                 |           | iCE40HX4K | 4.1  | mA    |
|                                 |           | iCE40HX8K | 4.1  | mA    |
| $I_{PP\_FASTPEAK}^2$            |           | iCE40HX1K |      | mA    |
|                                 |           | iCE40HX4K | 8.0  | mA    |
|                                 |           | iCE40HX8K | 8.0  | mA    |
| $I_{CCIOPEAK}, I_{CC\_SPIPEAK}$ |           | iCE40HX1K |      | mA    |
|                                 |           | iCE40HX4K | 6.8  | mA    |
|                                 |           | iCE40HX8K | 6.8  | mA    |

1.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

2.  $V_{PP\_FAST}$ , used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the  $V_{PP\_FAST}$  ball connected to  $V_{CCIO\_0}$  ball externally.

## sysIO Recommended Operating Conditions

| Standard              | $V_{CCIO}$ (V) |      |      |
|-----------------------|----------------|------|------|
|                       | Min.           | Typ. | Max. |
| LVC MOS 3.3           | 3.14           | 3.3  | 3.46 |
| LVC MOS 2.5           | 2.37           | 2.5  | 2.62 |
| LVC MOS 1.8           | 1.71           | 1.8  | 1.89 |
| LVDS25E <sup>1</sup>  | 2.37           | 2.5  | 2.62 |
| subLVDSE <sup>1</sup> | 1.71           | 1.8  | 1.89 |

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

## sysIO Single-Ended DC Electrical Characteristics

| Input/<br>Output<br>Standard | $V_{IL}$ |                | $V_{IH}$ <sup>1</sup> |                   | $V_{OL}$ Max.<br>(V) | $V_{OH}$ Min.<br>(V) | $I_{OL}$ Max.<br>(mA) | $I_{OH}$ Max.<br>(mA) |
|------------------------------|----------|----------------|-----------------------|-------------------|----------------------|----------------------|-----------------------|-----------------------|
|                              | Min. (V) | Max. (V)       | Min. (V)              | Max. (V)          |                      |                      |                       |                       |
| LVC MOS 3.3                  | -0.3     | 0.8            | 2.0                   | $V_{CCIO} + 0.2V$ | 0.4                  | $V_{CCIO} - 0.5$     | 8                     | -8                    |
|                              |          |                |                       |                   | 0.2                  | $V_{CCIO} - 0.2$     | 0.1                   | -0.1                  |
| LVC MOS 2.5                  | -0.3     | 0.7            | 1.7                   | $V_{CCIO} + 0.2V$ | 0.4                  | $V_{CCIO} - 0.5$     | 6                     | -6                    |
|                              |          |                |                       |                   | 0.2                  | $V_{CCIO} - 0.2$     | 0.1                   | -0.1                  |
| LVC MOS 1.8                  | -0.3     | $0.35V_{CCIO}$ | $0.65V_{CCIO}$        | $V_{CCIO} + 0.2V$ | 0.4                  | $V_{CCIO} - 0.4$     | 4                     | -4                    |
|                              |          |                |                       |                   | 0.2                  | $V_{CCIO} - 0.2$     | 0.1                   | -0.1                  |

1. Some products are clamped to a diode when  $V_{IN}$  is larger than  $V_{CCIO}$ .

## sysIO Differential Electrical Characteristics

The LVDS25E/subLVDSE differential output buffers are available on all banks but the LVDS/subLVDS input buffers are only available on Bank 3 of iCE40 devices.

### LVDS25

#### Over Recommended Operating Conditions

| Parameter Symbol   | Parameter Description        | Test Conditions    | Min.                 | Typ.         | Max.                 | Units   |
|--------------------|------------------------------|--------------------|----------------------|--------------|----------------------|---------|
| $V_{INP}, V_{INM}$ | Input Voltage                | $V_{CCIO}^1 = 2.5$ | 0                    | —            | 2.5                  | V       |
| $V_{THD}$          | Differential Input Threshold |                    | 250                  | 350          | 450                  | mV      |
| $V_{CM}$           | Input Common Mode Voltage    | $V_{CCIO}^1 = 2.5$ | $(V_{CCIO}/2) - 0.3$ | $V_{CCIO}/2$ | $(V_{CCIO}/2) + 0.3$ | V       |
| $I_{IN}$           | Input Current                | Power on           | —                    | —            | $\pm 10$             | $\mu A$ |

1. Typical.

### subLVDS

#### Over Recommended Operating Conditions

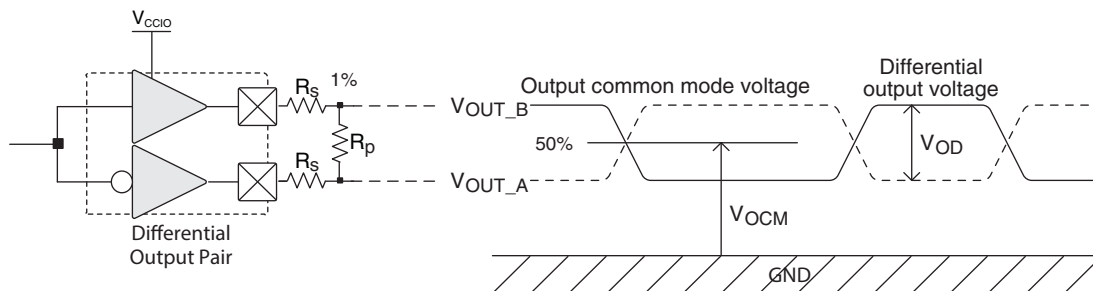
| Parameter Symbol   | Parameter Description        | Test Conditions    | Min.                  | Typ.         | Max.                  | Units   |
|--------------------|------------------------------|--------------------|-----------------------|--------------|-----------------------|---------|
| $V_{INP}, V_{INM}$ | Input Voltage                | $V_{CCIO}^1 = 1.8$ | 0                     | —            | 1.8                   | V       |
| $V_{THD}$          | Differential Input Threshold |                    | 100                   | 150          | 200                   | mV      |
| $V_{CM}$           | Input Common Mode Voltage    | $V_{CCIO}^1 = 1.8$ | $(V_{CCIO}/2) - 0.25$ | $V_{CCIO}/2$ | $(V_{CCIO}/2) + 0.25$ | V       |
| $I_{IN}$           | Input Current                | Power on           | —                     | —            | $\pm 10$              | $\mu A$ |

1. Typical.

### LVDS25E Emulation

iCE40 devices can support subLVDS outputs via emulation on all banks. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS25E standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

**Figure 3-1. LVDS25E Using External Resistors**



**Table 3-1. LVDS25E DC Conditions**

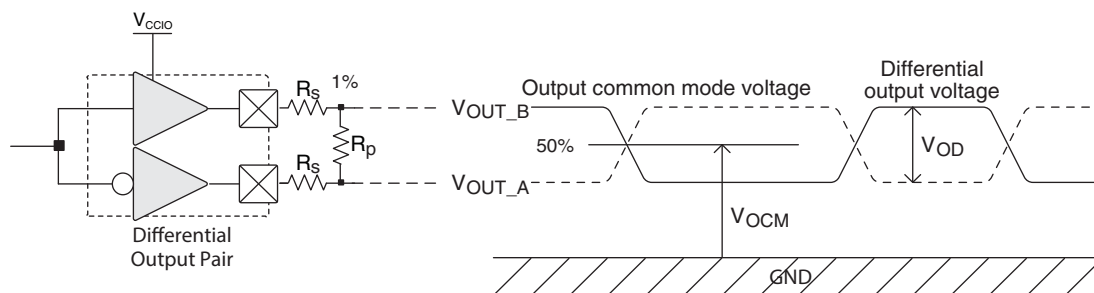
#### Over Recommended Operating Conditions

| Parameter  | Description                 | Typ.  | Units |
|------------|-----------------------------|-------|-------|
| $Z_{OUT}$  | Output impedance            | 20    | Ohms  |
| $R_S$      | Driver series resistor      | 150   | Ohms  |
| $R_P$      | Driver parallel resistor    | 140   | Ohms  |
| $R_T$      | Receiver termination        | 100   | Ohms  |
| $V_{OH}$   | Output high voltage         | 1.43  | V     |
| $V_{OL}$   | Output low voltage          | 1.07  | V     |
| $V_{OD}$   | Output differential voltage | 0.30  | V     |
| $V_{CM}$   | Output common mode voltage  | 1.25  | V     |
| $Z_{BACK}$ | Back impedance              | 100.5 | Ohms  |
| $I_{DC}$   | DC output current           | 6.03  | mA    |

### SubLVDS Emulation

The iCE40 family supports the differential subLVDS standard in Bank 3. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all banks of the devices. The subLVDS input standard is supported by the LVDS25 differential input buffer. The scheme shown in Figure 3-2 is one possible solution for subLVDS output standard implementation. Use LVDS25E mode with suggested resistors for subLVDS operation. Resistor values in Figure 3-2 are industry standard values for 1% resistors.

**Figure 3-2. subLVDS**



**Table 3-2. subLVDS DC Conditions**

#### Over Recommended Operating Conditions

| Parameter  | Description                 | Typ.  | Units |
|------------|-----------------------------|-------|-------|
| $Z_{OUT}$  | Output impedance            | 20    | Ohms  |
| $R_S$      | Driver series resistor      | 270   | Ohms  |
| $R_P$      | Driver parallel resistor    | 120   | Ohms  |
| $R_T$      | Receiver termination        | 100   | Ohms  |
| $V_{OH}$   | Output high voltage         | 1.43  | V     |
| $V_{OL}$   | Output low voltage          | 1.07  | V     |
| $V_{OD}$   | Output differential voltage | 0.35  | V     |
| $V_{CM}$   | Output common mode voltage  | 0.9   | V     |
| $Z_{BACK}$ | Back impedance              | 100.5 | Ohms  |
| $I_{DC}$   | DC output current           | 6.03  | mA    |

## Typical Building Block Function Performance – LP Devices<sup>1, 2</sup>

### Pin-to-Pin Performance (LVCMOS25)

| Function               | Timing | Units |
|------------------------|--------|-------|
| <b>Basic Functions</b> |        |       |
| 16-bit decoder         | 11.0   | ns    |
| 4:1 MUX                | 12.0   | ns    |
| 16:1 MUX               | 13.0   | ns    |

### Register-to-Register Performance

| Function                         | Timing | Units |
|----------------------------------|--------|-------|
| <b>Basic Functions</b>           |        |       |
| 16:1 MUX                         | 190    | MHz   |
| 16-bit adder                     | 160    | MHz   |
| 16-bit counter                   | 175    | MHz   |
| 64-bit counter                   | 65     | MHz   |
| <b>Embedded Memory Functions</b> |        |       |
| 256x16 Pseudo-Dual Port RAM      | 240    | MHz   |

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a  $V_{CC}$  of 1.14V at Junction Temp 85C.

## Typical Building Block Function Performance – HX Devices<sup>1</sup>

### Pin-to-Pin Performance (LVCMOS25)

| Function               | Timing | Units |
|------------------------|--------|-------|
| <b>Basic Functions</b> |        |       |
| 16-bit decoder         | 10.0   | ns    |
| 4:1 MUX                | 9.0    | ns    |
| 16:1 MUX               | 9.5    | ns    |

### Register-to-Register Performance

| Function                         | Timing | Units |
|----------------------------------|--------|-------|
| <b>Basic Functions</b>           |        |       |
| 16:1 MUX                         | 305    | MHz   |
| 16-bit adder                     | 220    | MHz   |
| 16-bit counter                   | 255    | MHz   |
| 64-bit counter                   | 105    | MHz   |
| <b>Embedded Memory Functions</b> |        |       |
| 256x16 Pseudo-Dual Port RAM      | 403    | MHz   |

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a  $V_{CC}$  of 1.14V at Junction Temp 85C.

### Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

### Maximum sysIO Buffer Performance<sup>2</sup>

| I/O Standard           | Max. Speed | Units |
|------------------------|------------|-------|
| <b>Inputs</b>          |            |       |
| LVDS25 <sup>1</sup>    | 400        | MHz   |
| subLVDS18 <sup>1</sup> | 400        | MHz   |
| LVC MOS33              | 250        | MHz   |
| LVC MOS25              | 250        | MHz   |
| LVC MOS18              | 250        | MHz   |
| <b>Outputs</b>         |            |       |
| LVDS25E                | 250        | MHz   |
| subLVDS18E             | 155        | MHz   |
| LVC MOS33              | 250        | MHz   |
| LVC MOS25              | 250        | MHz   |
| LVC MOS18              | 155        | MHz   |

1. Supported in Bank 3 only.

2. Measured with a toggling pattern

### iCE40 Family Timing Adders

Over Recommended Commercial Operating Conditions - LP Devices<sup>1, 2, 3, 4, 5</sup>

| Buffer Type             | Description                          | Timing | Units |
|-------------------------|--------------------------------------|--------|-------|
| <b>Input Adjusters</b>  |                                      |        |       |
| LVDS25                  | LVDS, $V_{CCIO} = 2.5V$              | -0.18  | nS    |
| subLVDS                 | subLVDS, $V_{CCIO} = 1.8V$           | 0.82   | nS    |
| LVC MOS33               | LVC MOS, $V_{CCIO} = 3.3V$           | 0.18   | nS    |
| LVC MOS25               | LVC MOS, $V_{CCIO} = 2.5V$           | 0.00   | nS    |
| LVC MOS18               | LVC MOS, $V_{CCIO} = 1.8V$           | 0.19   | nS    |
| <b>Output Adjusters</b> |                                      |        |       |
| LVDS25E                 | LVDS, Emulated, $V_{CCIO} = 2.5V$    | 0.00   | nS    |
| subLVDS E               | subLVDS, Emulated, $V_{CCIO} = 1.8V$ | 1.32   | nS    |
| LVC MOS33               | LVC MOS, $V_{CCIO} = 3.3V$           | -0.12  | nS    |
| LVC MOS25               | LVC MOS, $V_{CCIO} = 2.5V$           | 0.00   | nS    |
| LVC MOS18               | LVC MOS, $V_{CCIO} = 1.8V$           | 1.32   | nS    |

1. Timing adders are relative to LVC MOS25 and characterized but not tested on every device.

2. LVC MOS timing measured with the load specified in Switching Test Condition table.

3. All other standards tested according to the appropriate specifications.

4. Commercial timing numbers are shown.

5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

### Over Recommended Commercial Operating Conditions - HX Devices<sup>1, 2, 3, 4, 5</sup>

| Buffer Type             | Description                          | Timing | Units |
|-------------------------|--------------------------------------|--------|-------|
| <b>Input Adjusters</b>  |                                      |        |       |
| LVDS25                  | LVDS, $V_{CCIO} = 2.5V$              | 0.13   | nS    |
| subLVDS                 | subLVDS, $V_{CCIO} = 1.8V$           | 1.03   | nS    |
| LVC MOS33               | LVC MOS, $V_{CCIO} = 3.3V$           | 0.16   | nS    |
| LVC MOS25               | LVC MOS, $V_{CCIO} = 2.5V$           | 0.00   | nS    |
| LVC MOS18               | LVC MOS, $V_{CCIO} = 1.8V$           | 0.23   | nS    |
| <b>Output Adjusters</b> |                                      |        |       |
| LVDS25E                 | LVDS, Emulated, $V_{CCIO} = 2.5V$    | 0.00   | nS    |
| subLVDS E               | subLVDS, Emulated, $V_{CCIO} = 1.8V$ | 1.76   | nS    |
| LVC MOS33               | LVC MOS, $V_{CCIO} = 3.3V$           | 0.17   | nS    |
| LVC MOS25               | LVC MOS, $V_{CCIO} = 2.5V$           | 0.00   | nS    |
| LVC MOS18               | LVC MOS, $V_{CCIO} = 1.8V$           | 1.76   | nS    |

1. Timing adders are relative to LVC MOS25 and characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

### iCE40 External Switching Characteristics – LP Devices<sup>1, 2, 3, 7</sup>

#### Over Recommended Operating Conditions

| Parameter                                                          | Description                                   | Device              |      |      | Units |
|--------------------------------------------------------------------|-----------------------------------------------|---------------------|------|------|-------|
|                                                                    |                                               |                     | Min. | Max. |       |
| Clocks                                                             |                                               |                     |      |      |       |
| Global Clocks                                                      |                                               |                     |      |      |       |
| t <sub>MAX_GBUF</sub>                                              | Frequency for Global Buffer Clock network     | All iCE40LP devices | —    |      | MHz   |
| t <sub>W_GBUF</sub>                                                | Clock Pulse Width for Global Buffer           | All iCE40LP devices |      | —    | ns    |
| t <sub>SKEW_GBUF</sub>                                             | Global Buffer Clock Skew Within a Device      | iCE40LP384          | —    |      | ps    |
|                                                                    |                                               | iCE40LP1K           | —    | 230  | ps    |
|                                                                    |                                               | iCE40LP4K           | —    | 340  | ps    |
|                                                                    |                                               | iCE40LP8K           | —    | 340  | ps    |
| Pin-LUT-Pin Propagation Delay                                      |                                               |                     |      |      |       |
| t <sub>PD</sub>                                                    | Best case propagation delay through one LUT-4 | All iCE40LP devices | —    | 9.36 | ns    |
| General I/O Pin Parameters (Using Global Buffer Clock without PLL) |                                               |                     |      |      |       |
| t <sub>SKEW_IO</sub>                                               | Data bus skew across a bank of IOs            | iCE40LP384          | —    |      | ps    |
|                                                                    |                                               | iCE40LP1K           | —    | 200  | ps    |
|                                                                    |                                               | iCE40LP4K           | —    | 280  | ps    |
|                                                                    |                                               | iCE40LP8K           | —    | 280  | ps    |
| t <sub>CO</sub>                                                    | Clock to Output - PIO Output Register         | iCE40LP384          | —    |      | ns    |
|                                                                    |                                               | iCE40LP1K           | —    | 5.91 | ns    |
|                                                                    |                                               | iCE40LP4K           | —    | 6.58 | ns    |
|                                                                    |                                               | iCE40LP8K           | —    | 6.58 | ns    |

**iCE40 External Switching Characteristics – LP Devices (Continued)<sup>1, 2, 3, 7</sup>**
**Over Recommended Operating Conditions**

| Parameter                                                       | Description                              | Device     |       |      | Units |
|-----------------------------------------------------------------|------------------------------------------|------------|-------|------|-------|
|                                                                 |                                          |            | Min.  | Max. |       |
| t <sub>SU</sub>                                                 | Clock to Data Setup - PIO Input Register | iCE40LP384 |       | —    | ns    |
|                                                                 |                                          | iCE40LP1K  | -0.33 | —    | ns    |
|                                                                 |                                          | iCE40LP4K  | -0.63 | —    | ns    |
|                                                                 |                                          | iCE40LP8K  | -0.63 | —    | ns    |
| t <sub>H</sub>                                                  | Clock to Data Hold - PIO Input Register  | iCE40LP384 |       | —    | ns    |
|                                                                 |                                          | iCE40LP1K  | 2.81  | —    | ns    |
|                                                                 |                                          | iCE40LP4K  | 3.48  | —    | ns    |
|                                                                 |                                          | iCE40LP8K  | 3.48  | —    | ns    |
| General I/O Pin Parameters (Using Global Buffer Clock with PLL) |                                          |            |       |      |       |
| t <sub>COPLL</sub>                                              | Clock to Output - PIO Output Register    | iCE40LP1K  | —     |      | ns    |
|                                                                 |                                          | iCE40LP4K  | —     |      | ns    |
|                                                                 |                                          | iCE40LP8K  | —     |      | ns    |
| t <sub>SUPLL</sub>                                              | Clock to Data Setup - PIO Input Register | iCE40LP1K  |       | —    | ns    |
|                                                                 |                                          | iCE40LP4K  |       | —    | ns    |
|                                                                 |                                          | iCE40LP8K  |       | —    | ns    |
| t <sub>HPLL</sub>                                               | Clock to Data Hold - PIO Input Register  | iCE40LP1K  |       | —    | ns    |
|                                                                 |                                          | iCE40LP4K  |       | —    | ns    |
|                                                                 |                                          | iCE40LP8K  |       | —    | ns    |

# iCE40 External Switching Characteristics – LP Devices (Continued)<sup>1, 2, 3, 7</sup>

Over Recommended Operating Conditions

| Parameter                                                                                                                        | Description                           | Device                      |      |      | Units |
|----------------------------------------------------------------------------------------------------------------------------------|---------------------------------------|-----------------------------|------|------|-------|
|                                                                                                                                  |                                       |                             | Min. | Max. |       |
| Generic DDR <sup>4, 6</sup>                                                                                                      |                                       |                             |      |      |       |
| Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using Global Pin for Clock Input – GDDRX1_RX.SCLK.Aligned <sup>3</sup>   |                                       |                             |      |      |       |
| t <sub>DVA</sub>                                                                                                                 | Input Data Valid After CLK            | All iCE40LP devices, Bank 3 | —    |      | UI    |
| t <sub>DVE</sub>                                                                                                                 | Input Data Hold After CLK             |                             |      | —    | UI    |
| f <sub>DATA</sub>                                                                                                                | DDRX1 Input Data Speed                |                             | —    |      | Mbps  |
| f <sub>DDRX1</sub>                                                                                                               | DDRX1 SCLK Frequency                  |                             | —    |      | MHz   |
| Generic DDRTX1 Outputs with Clock and Data Aligned at Pin Using Global Pin for Clock Input – GDDRX1_TX.SCLK.Aligned <sup>3</sup> |                                       |                             |      |      |       |
| t <sub>DIA</sub>                                                                                                                 | Output Data Invalid After CLK Output  | All iCE40LP devices, Bank 3 | —    |      | ns    |
| t <sub>DIB</sub>                                                                                                                 | Output Data Invalid Before CLK Output |                             | —    |      | ns    |
| f <sub>DATA</sub>                                                                                                                | DDRX1 Output Data Speed               |                             | —    |      | Mbps  |
| f <sub>DDRX1</sub>                                                                                                               | DDRX1 SCLK frequency                  |                             | —    |      | MHz   |
| 7:1 LVDS Inputs - GDDR71_RX.SCLK.7:1 <sup>3</sup>                                                                                |                                       |                             |      |      |       |
| t <sub>DVA</sub>                                                                                                                 | Input Data Valid After CLK            | All iCE40LP devices, Bank 3 |      |      | UI    |
| t <sub>DVE</sub>                                                                                                                 | Input Data Hold After CLK             |                             |      |      | UI    |
| f <sub>DATA</sub>                                                                                                                | DDR71 Serial Input Data Speed         |                             |      |      | Mbps  |
| f <sub>DDR71</sub>                                                                                                               | DDR71 CLK Frequency                   |                             |      |      | MHz   |
| f <sub>CLKIN</sub>                                                                                                               | 7:1 Input Clock Frequency (SCLK)      |                             |      |      | MHz   |
| 7:1 LVDS Outputs - GDDR71_TX.SCLK.7:1 <sup>3</sup>                                                                               |                                       |                             |      |      |       |
| t <sub>DVB</sub>                                                                                                                 | Output Data Valid Before CLK Output   | All iCE40LP devices, Bank 3 |      |      | ns    |
| t <sub>DVA</sub>                                                                                                                 | Output Data Valid After CLK Output    |                             |      |      | ns    |
| f <sub>DATA</sub>                                                                                                                | DDR71 Serial Output Data Speed        |                             |      |      | Mbps  |
| f <sub>DDR71</sub>                                                                                                               | DDR71 CLK Frequency                   |                             |      |      | MHz   |
| f <sub>CLKOUT</sub>                                                                                                              | 7:1 Output Clock Frequency (SCLK)     |                             |      |      | MHz   |

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85°C and 1.14V. Other operating conditions can be extracted from the iCECube2 software.

2. General I/O timing numbers based on LVCMOS 2.5, 0pF load.

3. These numbers are for general purpose usage. Duty cycle tolerance is +/-10%.

4. Generic DDR timing numbers based on LVDS25 inputs and LVDS25E outputs (for input, output, and clock ports).

5. Duty cycle is +/- 5% for system usage.

6. Supported on devices with a PLL.

7. iCE40LP4K/iCE40LP8K status is Preliminary.

## iCE40 External Switching Characteristics – Preliminary – HX Devices <sup>1, 2, 3</sup>

Over Recommended Operating Conditions

| Parameter                                                          | Description                                   | Device              |       |      | Units |
|--------------------------------------------------------------------|-----------------------------------------------|---------------------|-------|------|-------|
|                                                                    |                                               |                     | Min.  | Max. |       |
| Clocks                                                             |                                               |                     |       |      |       |
| Primary Clocks                                                     |                                               |                     |       |      |       |
| f <sub>MAX_GBUF</sub>                                              | Frequency for Global Buffer Clock network     | All iCE40HX devices | —     |      | MHz   |
| t <sub>W_GBUF</sub>                                                | Clock Pulse Width for Global Buffer           | All iCE40HX devices |       | —    | ns    |
| t <sub>SKEW_GBUF</sub>                                             | Global Buffer Clock Skew Within a Device      | iCE40HX1K           | —     |      | ps    |
|                                                                    |                                               | iCE40HX4K           | —     | 300  | ps    |
|                                                                    |                                               | iCE40HX8K           | —     | 300  | ps    |
| Pin-LUT-Pin Propagation Delay                                      |                                               |                     |       |      |       |
| t <sub>PD</sub>                                                    | Best case propagation delay through one LUT-4 | All iCE40HX devices | —     | 7.30 | ns    |
| General I/O Pin Parameters (Using Global Buffer Clock without PLL) |                                               |                     |       |      |       |
| t <sub>SKEW_IO</sub>                                               | Data bus skew across a bank of IOs            | iCE40HX1K           | —     |      | ps    |
|                                                                    |                                               | iCE40HX4K           | —     | 290  | ps    |
|                                                                    |                                               | iCE40HX8K           | —     | 290  | ps    |
| t <sub>CO</sub>                                                    | Clock to Output - PIO Output Register         | iCE40HX1K           | —     |      | ns    |
|                                                                    |                                               | iCE40HX4K           | —     | 5.41 | ns    |
|                                                                    |                                               | iCE40HX8K           | —     | 5.41 | ns    |
| t <sub>SU</sub>                                                    | Clock to Data Setup - PIO Input Register      | iCE40HX1K           |       | —    | ns    |
|                                                                    |                                               | iCE40HX4K           | -0.43 | —    | ns    |
|                                                                    |                                               | iCE40HX8K           | -0.43 | —    | ns    |
| t <sub>H</sub>                                                     | Clock to Data Hold - PIO Input Register       | iCE40HX1K           |       | —    | ns    |
|                                                                    |                                               | iCE40HX4K           | 2.38  | —    | ns    |
|                                                                    |                                               | iCE40HX8K           | 2.38  | —    | ns    |
| General I/O Pin Parameters (Using Global Buffer Clock with PLL)    |                                               |                     |       |      |       |
| t <sub>COPLL</sub>                                                 | Clock to Output - PIO Output Register         | iCE40HX1K           | —     |      | ns    |
|                                                                    |                                               | iCE40HX4K           | —     |      | ns    |
|                                                                    |                                               | iCE40HX8K           | —     |      | ns    |
| t <sub>SUPLL</sub>                                                 | Clock to Data Setup - PIO Input Register      | iCE40HX1K           |       | —    | ns    |
|                                                                    |                                               | iCE40HX4K           |       | —    | ns    |
|                                                                    |                                               | iCE40HX8K           |       | —    | ns    |
| t <sub>HPLL</sub>                                                  | Clock to Data Hold - PIO Input Register       | iCE40HX1K           |       | —    | ns    |
|                                                                    |                                               | iCE40HX4K           |       | —    | ns    |
|                                                                    |                                               | iCE40HX8K           |       | —    | ns    |

## iCE40 External Switching Characteristics – Preliminary – HX Devices (Continued)<sup>1, 2, 3</sup>

| Parameter                                                                                                                       | Description                           | Device                      |      |      | Units |
|---------------------------------------------------------------------------------------------------------------------------------|---------------------------------------|-----------------------------|------|------|-------|
|                                                                                                                                 |                                       |                             | Min. | Max. |       |
| Generic DDR <sup>4, 6</sup>                                                                                                     |                                       |                             |      |      |       |
| Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using Global Pin for Clock Input – GDDRX1_RX.SCLK.Aligned <sup>5</sup>  |                                       |                             |      |      |       |
| t <sub>DVA</sub>                                                                                                                | Input Data Valid After CLK            | All iCE40HX devices, Bank 3 | —    |      | UI    |
| t <sub>DVE</sub>                                                                                                                | Input Data Hold After CLK             |                             |      | —    | UI    |
| f <sub>DATA</sub>                                                                                                               | DDRX1 Input Data Speed                |                             | —    |      | Mbps  |
| f <sub>DDRX1</sub>                                                                                                              | DDRX1 SCLK Frequency                  |                             | —    |      | MHz   |
| Generic DDRX1 Outputs with Clock and Data Aligned at Pin Using Global Pin for Clock Input – GDDRX1_TX.SCLK.Aligned <sup>5</sup> |                                       |                             |      |      |       |
| t <sub>DIA</sub>                                                                                                                | Output Data Invalid After CLK Output  | All iCE40HX devices, Bank 3 | —    |      | ns    |
| t <sub>DIB</sub>                                                                                                                | Output Data Invalid Before CLK Output |                             | —    |      | ns    |
| f <sub>DATA</sub>                                                                                                               | DDRX1 Output Data Speed               |                             | —    |      | Mbps  |
| f <sub>DDRX1</sub>                                                                                                              | DDRX1 SCLK frequency                  |                             | —    |      | MHz   |
| 7:1 LVDS Inputs - GDDR71_RX.SCLK.7:1 <sup>3</sup>                                                                               |                                       |                             |      |      |       |
| t <sub>DVA</sub>                                                                                                                | Input Data Valid After CLK            | All iCE40HX devices, Bank 3 |      |      |       |
| t <sub>DVE</sub>                                                                                                                | Input Data Hold After CLK             |                             |      |      |       |
| f <sub>DATA</sub>                                                                                                               | DDR71 Serial Input Data Speed         |                             |      |      |       |
| f <sub>DDR71</sub>                                                                                                              | DDR71 ECLK Frequency                  |                             |      |      |       |
| f <sub>CLKIN</sub>                                                                                                              | 7:1 Input Clock Frequency (SCLK)      |                             |      |      |       |
| 7:1 LVDS Outputs - GDDR71_TX.SCLK.7:1 <sup>3</sup>                                                                              |                                       |                             |      |      |       |
| t <sub>DVB</sub>                                                                                                                | Output Data Valid Before CLK Output   | All iCE40HX devices, Bank 3 |      |      | ns    |
| t <sub>DVA</sub>                                                                                                                | Output Data Valid After CLK Output    |                             |      |      | ns    |
| f <sub>DATA</sub>                                                                                                               | DDR71 Serial Output Data Speed        |                             |      |      | Mbps  |
| f <sub>DDR71</sub>                                                                                                              | DDR71 ECLK Frequency                  |                             |      |      | MHz   |
| f <sub>CLKOUT</sub>                                                                                                             | 7:1 Output Clock Frequency (SCLK)     |                             |      |      | MHz   |

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85°C and 1.14V. Other operating conditions, including industrial, can be extracted from the iCECube2 software.

2. General I/O timing numbers based on LVCMOS 2.5, 0pf load.

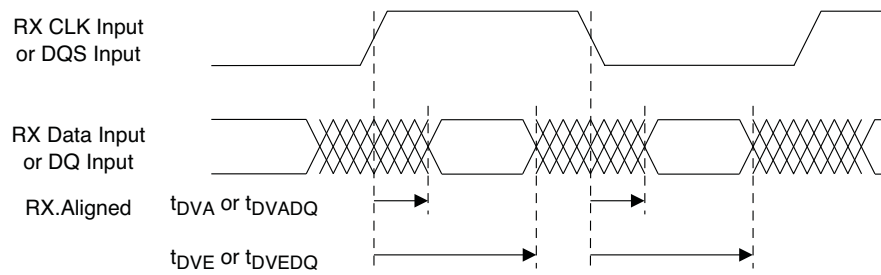
3. These numbers are for general purpose usage. Duty cycle tolerance is +/-10%.

4. Generic DDR timing numbers based on LVDS25 inputs and LVDS25E outputs (for input, output, and clock ports).

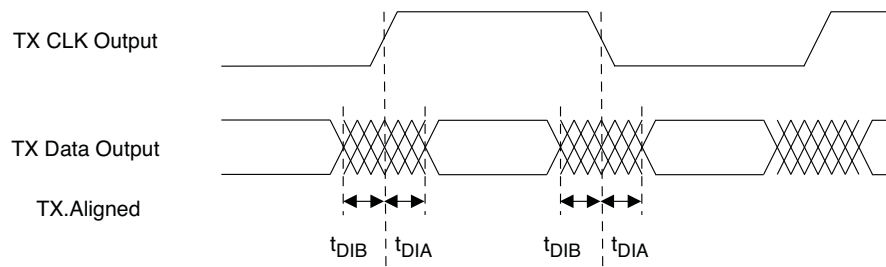
5. Duty cycle is +/- 5% for system usage.

6. Supported on devices with a PLL.

**Figure 3-3. Receiver RX.CLK.Aligned and MEM DDR Input Waveforms**



**Figure 3-4. Transmitter TX.CLK.Aligned Waveforms**



## sysCLOCK PLL Timing – Preliminary

### Over Recommended Operating Conditions

| Parameter                 | Descriptions                                      | Conditions             | Min. | Max. | Units      |
|---------------------------|---------------------------------------------------|------------------------|------|------|------------|
| $f_{IN}$                  | Input Clock Frequency (REFERENCECLK, EXTFEEDBACK) |                        | 10   | 133  | MHz        |
| $f_{OUT}$                 | Output Clock Frequency (PLLOUT)                   |                        | 16   | 275  | MHz        |
| $f_{VCO}$                 | PLL VCO Frequency                                 |                        |      |      | MHz        |
| $f_{PFD}$                 | Phase Detector Input Frequency                    |                        | 10   | 133  | MHz        |
| <b>AC Characteristics</b> |                                                   |                        |      |      |            |
| $t_{DT}$                  | Output Clock Duty Cycle <sup>3</sup>              |                        |      |      | %          |
| $t_{PH}$                  | Output Phase Accuracy                             |                        |      |      | %          |
| $t_{OPJIT}^{1,6}$         | Output Clock Period Jitter                        | $f_{OUT} \leq 100$ MHz | —    |      | UIPP       |
|                           |                                                   | $f_{OUT} > 100$ MHz    | —    |      | UIPP       |
|                           | Output Clock Cycle-to-cycle Jitter                | $f_{OUT} \leq 100$ MHz | —    |      | UIPP       |
|                           |                                                   | $f_{OUT} > 100$ MHz    | —    |      | UIPP       |
|                           | Output Clock Phase Jitter                         | $f_{PFD} \leq 100$ MHz | —    |      | UIPP       |
|                           |                                                   | $f_{PFD} > 100$ MHz    | —    |      | UIPP       |
| $t_{LOCK}^{2,4}$          | PLL Lock-in Time                                  |                        | —    |      | us         |
| $t_{UNLOCK}$              | PLL Unlock Time                                   |                        | —    |      | ns         |
| $t_{IPJIT}^5$             | Input Clock Period Jitter                         | $f_{PFD} \geq 20$ MHz  | —    |      | ps p-p     |
|                           |                                                   | $f_{PFD} < 20$ MHz     | —    |      | UIPP       |
| $t_{HI}$                  | Input Clock High Time                             | 90% to 90%             |      | —    | ns         |
| $t_{LO}$                  | Input Clock Low Time                              | 10% to 10%             |      | —    | ns         |
| $t_{FDTAP}$               | Fine Delay adjustment, per Tap                    |                        | —    |      | ms         |
| $t_{STABLE}^4$            | LATCHINPUTVALUE LOW to PLL Stable                 |                        | —    |      | ms         |
| $t_{STABLE\_PW}^4$        | LATCHINPUTVALUE Pulse Width                       |                        | —    |      | ms         |
| $t_{RST}$                 | RESET Pulse Width                                 |                        |      | —    | ns         |
| $t_{RSTREC}$              | RESET Recovery Time                               |                        |      | —    | ns         |
| $t_{DYNAMIC-SETUP}$       | DYNAMICDELAY Setup Time                           |                        |      | —    | ns         |
| $t_{DYNAMIC-HOLD}$        | DYNAMICDELAY HOLD Time                            |                        |      | —    | ns         |
| $t_{DYNAMIC\_WD}$         | DYNAMICDELAY Pulse Width                          |                        |      | —    | VCO Cycles |

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after  $t_{LOCK}$  for PLL reset and dynamic delay adjustment.
3. Using LVDS25E output buffers.
4. At minimum  $f_{PFD}$ . As the  $f_{PFD}$  increases the time will decrease to approximately 60% the value listed.
5. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
6. Jitter values measured with the internal oscillator operating. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

## SPI Master or NVCM Configuration Time<sup>1, 2, 3</sup>

| Symbol              | Parameter                         | Conditions                    | Typ. | Units |
|---------------------|-----------------------------------|-------------------------------|------|-------|
| $t_{\text{CONFIG}}$ | POR/CRESET_B to Device I/O Active | iCE40LP384 - Default          |      | ms    |
|                     |                                   | iCE40LP384 - Low frequency    |      | ms    |
|                     |                                   | iCE40LP384 - High frequency   |      | ms    |
|                     |                                   | iCE40LP/HX1K - Default        | 53   | ms    |
|                     |                                   | iCE40LP/HX1K - Low frequency  | 25   | ms    |
|                     |                                   | iCE40LP/HX1K - High frequency | 13   | ms    |
|                     |                                   | iCE40LP/HX4K - Default        | 230  | ms    |
|                     |                                   | iCE40LP/HX4K - Low frequency  | 110  | ms    |
|                     |                                   | iCE40LP/HX4K - High frequency | 70   | ms    |
|                     |                                   | iCE40LP/HX8K - Default        | 230  | ms    |
|                     |                                   | iCE40LP/HX8K - Low frequency  | 110  | ms    |
|                     |                                   | iCE40LP/HX8K - High frequency | 70   | ms    |

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.

2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

3. iCE40LP4K/iCE40LP8K, iCE40HX1K/iCE40HX4K/iCE40HX8K status is Preliminary.

## sysCONFIG Port Timing Specifications<sup>1</sup>

| Symbol                         | Parameter                                                                                                                                                                        | Conditions   | Min. | Max. | Units        |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|------|--------------|
| <b>All Configuration Modes</b> |                                                                                                                                                                                  |              |      |      |              |
| $t_{\text{CRESET\_B}}$         | Minimum CRESET_B Low pulse width required to restart configuration, from falling edge to rising edge                                                                             |              | 200  | —    | ns           |
| $t_{\text{DONE\_IO}}$          | Number of configuration clock cycles after CDONE goes High before the PIO pins are activated                                                                                     |              | 49   | —    | Clock Cycles |
| <b>Slave SPI</b>               |                                                                                                                                                                                  |              |      |      |              |
| $t_{\text{CR\_SCK}}$           | Minimum time from a rising edge on CRESET_B until the first SPI write operation, first SPI_SCK. During this time, the iCE40 device is clearing its internal configuration memory | iCE40LP384   |      | —    |              |
|                                |                                                                                                                                                                                  | iCE40LP/HX1K | 800  | —    | us           |
|                                |                                                                                                                                                                                  | iCE40LP/HX4K | 1200 | —    |              |
|                                |                                                                                                                                                                                  | iCE40LP/HX8K | 1200 | —    | us           |
| $f_{\text{MAX}}^2$             | CCLK clock frequency                                                                                                                                                             | Write        | 0    | 25   | MHz          |
|                                |                                                                                                                                                                                  | Read         | 5    | 25   | MHz          |
| $t_{\text{CCLKH}}$             | CCLK clock pulse width high                                                                                                                                                      |              | 20   | —    | ns           |
| $t_{\text{CCLKL}}$             | CCLK clock pulse width low                                                                                                                                                       |              | 20   | —    | ns           |
| $t_{\text{STSU}}$              | CCLK setup time                                                                                                                                                                  |              | 12   | —    | ns           |
| $t_{\text{STH}}$               | CCLK hold time                                                                                                                                                                   |              | 12   | —    | ns           |
| $t_{\text{STCO}}$              | CCLK falling edge to valid output                                                                                                                                                |              | 13   | —    | ns           |

## sysCONFIG Port Timing Specifications<sup>1</sup> (Continued)

| Symbol            | Parameter                        | Conditions                       | Min. | Max. | Units |
|-------------------|----------------------------------|----------------------------------|------|------|-------|
| <b>Master SPI</b> |                                  |                                  |      |      |       |
| $f_{\text{MCLK}}$ | MCLK clock frequency             | Default Frequency                | 4    | 11   | MHz   |
|                   |                                  | Low Frequency                    | 16   | 32   | MHz   |
|                   |                                  | High Frequency                   | 27   | 53   | MHz   |
| $t_{\text{MCLK}}$ | CRESET_B high to first MCLK edge | iCE40LP384 - Default Frequency   |      | —    | us    |
|                   |                                  | iCE40LP384 - Low Frequency       |      | —    | us    |
|                   |                                  | iCE40LP384 - High Frequency      |      | —    | us    |
|                   |                                  | iCE40LP/HX1K - Default Frequency | 800  | —    | us    |
|                   |                                  | iCE40LP/HX1K - Low Frequency     | 800  | —    | us    |
|                   |                                  | iCE40LP/HX1K - High Frequency    | 800  | —    | us    |
|                   |                                  | iCE40LP/HX4K - Default Frequency | 1200 | —    | us    |
|                   |                                  | iCE40LP/HX4K - Low Frequency     | 1200 | —    | us    |
|                   |                                  | iCE40LP/HX4K - High Frequency    | 1200 | —    | us    |
|                   |                                  | iCE40LP/HX8K - Default Frequency | 1200 | —    | us    |
|                   |                                  | iCE40LP/HX8K - Low Frequency     | 1200 | —    | us    |
|                   |                                  | iCE40LP/HX8K - High Frequency    | 1200 | —    | us    |

1. iCE40LP4K/iCE40LP8K, iCE40HX1K/iCE40HX4K/iCE40HX8K status is Preliminary.

2. Does not apply for NVCM.

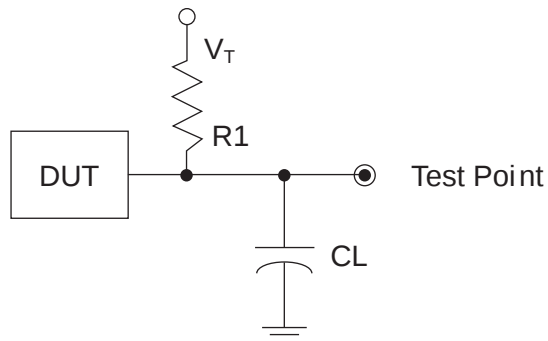
**Table 3-3. Available Oscillator Frequencies**

| Symbol            | Oscillator Mode | Frequency (MHz) |      | Description                                                                            |
|-------------------|-----------------|-----------------|------|----------------------------------------------------------------------------------------|
|                   |                 | Min.            | Max. |                                                                                        |
| $f_{\text{OSCD}}$ | Default         | 4               | 11   | Default oscillator frequency. Slow enough to safely operate with most SPI serial PROM. |
| $f_{\text{OSCL}}$ | Low Frequency   | 16              | 32   | Supported by most SPI serial Flash PROMs.                                              |
| $f_{\text{OSCH}}$ | High Frequency  | 27              | 53   | Supported by some high-speed SPI serial Flash PROMs.                                   |
|                   | Off             | 0               | 0    | Oscillator turned off by default after configuration to save power.                    |

### Switching Test Conditions

Figure 3-5 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3-4.

**Figure 3-5. Output Test Load, LVCMOS Standards**



**Table 3-4. Test Fixture Required Components, Non-Terminated Interfaces**

| Test Condition                   | $R_1$    | $C_L$ | Timing Reference          | $V_T$    |
|----------------------------------|----------|-------|---------------------------|----------|
| LVCMOS settings (L -> H, H -> L) | $\infty$ | 0 pF  | LVCMOS 3.3 = 1.5V         | —        |
|                                  |          |       | LVCMOS 2.5 = $V_{CCIO}/2$ | —        |
|                                  |          |       | LVCMOS 1.8 = $V_{CCIO}/2$ | —        |
| LVCMOS 3.3 (Z -> H)              | 188      | 0 pF  | 1.5                       | $V_{OL}$ |
| LVCMOS 3.3 (Z -> L)              |          |       | 1.5                       | $V_{OH}$ |
| Other LVCMOS (Z -> H)            |          |       | $V_{CCIO}/2$              | $V_{OL}$ |
| Other LVCMOS (Z -> L)            |          |       | $V_{CCIO}/2$              | $V_{OH}$ |
| LVCMOS (H -> Z)                  |          |       | $V_{OH} - 0.15$           | $V_{OL}$ |
| LVCMOS (L -> Z)                  |          |       | $V_{OL} - 0.15$           | $V_{OH}$ |

Note: Output test conditions for all other interfaces are determined by the respective standards.

### Signal Descriptions

| Signal Name                                                                                              | I/O | Descriptions                                                                                                                                                                                                                                                                                                                                                                                              |
|----------------------------------------------------------------------------------------------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>General Purpose</b>                                                                                   |     |                                                                                                                                                                                                                                                                                                                                                                                                           |
| PIOx                                                                                                     | I/O | User IO pin. x determines the Banks 0-3.                                                                                                                                                                                                                                                                                                                                                                  |
| DP[Pair Number][A/B]                                                                                     | I/O | Differential I/O pair. Only available in I/O Bank 3. 'A' = negative input. 'B' = positive input.                                                                                                                                                                                                                                                                                                          |
| NC                                                                                                       | —   | No connect                                                                                                                                                                                                                                                                                                                                                                                                |
| GND                                                                                                      | —   | GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.                                                                                                                                                                                                                                                                                                                          |
| VCC                                                                                                      | —   | VCC – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.                                                                                                                                                                                                                                                                                  |
| VCCIO_x                                                                                                  | —   | VCCIO – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all VCCIOs located in the same bank are tied to the same supply.                                                                                                                                                                                                                                                     |
| <b>PLL and Global Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)</b> |     |                                                                                                                                                                                                                                                                                                                                                                                                           |
| VCCPLLx                                                                                                  | —   | PLL VCC – Power. Dedicated pins. The PLL requires a separate power and ground that is quiet and stable to reduce the output clock jitter of the PLL.                                                                                                                                                                                                                                                      |
| GNDPLLx                                                                                                  | —   | PLL GND – Ground. Dedicated pins. The sysCLOCK PLL has the DC ground connection made on the FPGA, so the external PLL ground connection (GNDPLL) must NOT be connected to the board's ground.                                                                                                                                                                                                             |
| GBINx                                                                                                    | —   | Global pads. Two per side.                                                                                                                                                                                                                                                                                                                                                                                |
| <b>Programming and Configuration</b>                                                                     |     |                                                                                                                                                                                                                                                                                                                                                                                                           |
| CBSEL[0:1]                                                                                               | I   | Optional ColdBoot configuration SElect input, if ColdBoot mode is enabled.                                                                                                                                                                                                                                                                                                                                |
| CRESET_B                                                                                                 | I   | Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 KOhm pull-up resistor to VCCIO_2.                                                                                                                                                                                                                                        |
| CDONE                                                                                                    | I/O | Configuration Done. Dedicated output. Includes a permanent weak pull-up resistor to VCCIO_2. If driving external devices with CDONE output, connect a 10 KOhm pull-up resistor to VCCIO_2.                                                                                                                                                                                                                |
| VCC_SPI                                                                                                  | —   | SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM.                                                                                                                                                                                                                                                                                                              |
| SPI_SCK                                                                                                  | I/O | Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.                                                                                                                                                                                                                                              |
| SPI_SS_B                                                                                                 | I/O | SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to VCC_SPI during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE40 device. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS_B = Low). An output when in SPI Flash configuration mode. |
| SPI_SI                                                                                                   | I/O | Slave SPI serial data input and master SPI serial data output                                                                                                                                                                                                                                                                                                                                             |
| SPI_SO                                                                                                   | I/O | Slave SPI serial data output and master SPI serial data input                                                                                                                                                                                                                                                                                                                                             |

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**Signal Descriptions (Cont.)**

| Signal Name | I/O | Descriptions                                                                                                                                                                                                                                                                            |
|-------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VPP_FAST    | —   | Optional fast NVCM programming supply. V <sub>PP_FAST</sub> , used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 pack-ages MUST have the V <sub>PP_FAST</sub> ball connected to V <sub>CCIO_0</sub> ball externally. |
| VPP_2V5     | —   | VPP_2V5 NVCM programming and operating supply                                                                                                                                                                                                                                           |

### Pin Information Summary

|                                        | iCE40-384LP |                   |                   |      | iCE40-1KLP          |                   |      |      |      |       |       |
|----------------------------------------|-------------|-------------------|-------------------|------|---------------------|-------------------|------|------|------|-------|-------|
|                                        | SG32        | CM36 <sup>2</sup> | CM49 <sup>2</sup> | CM81 | CM36 <sup>1,2</sup> | CM49 <sup>2</sup> | CM81 | CB81 | QN84 | CM121 | CB121 |
| <b>General Purpose I/O per Bank</b>    |             |                   |                   |      |                     |                   |      |      |      |       |       |
| Bank 0                                 | 6           | 4                 | 10                | 12   | 4                   | 10                | 17   | 17   | 17   | 24    | 24    |
| Bank 1                                 | 5           | 7                 | 7                 | 15   | 7                   | 7                 | 15   | 16   | 17   | 25    | 21    |
| Bank 2                                 | 0           | 4                 | 4                 | 8    | 4                   | 4                 | 11   | 8    | 11   | 18    | 19    |
| Bank 3                                 | 6           | 6                 | 12                | 16   | 6                   | 10                | 16   | 17   | 18   | 24    | 24    |
| Configuration                          | 4           | 4                 | 4                 | 4    | 4                   | 4                 | 4    | 4    | 4    | 4     | 4     |
| Total General Purpose Single Ended I/O | 21          | 25                | 37                | 55   | 25                  | 35                | 63   | 62   | 67   | 95    | 92    |
| <b>Differential Inputs per Bank</b>    |             |                   |                   |      |                     |                   |      |      |      |       |       |
| Bank 0                                 | 0           | 0                 | 0                 | 0    | 0                   | 0                 | 0    | 0    | 0    | 0     | 0     |
| Bank 1                                 | 0           | 0                 | 0                 | 0    | 0                   | 0                 | 0    | 0    | 0    | 0     | 0     |
| Bank 2                                 | 0           | 0                 | 0                 | 0    | 0                   | 0                 | 0    | 0    | 0    | 0     | 0     |
| Bank 3                                 | 3           | 3                 | 6                 | 8    | 3                   | 5                 | 8    | 9    | 7    | 12    | 12    |
| Configuration                          | 0           | 0                 | 0                 | 0    | 0                   | 0                 | 0    | 0    | 0    | 0     | 0     |
| Total Differential Inputs              | 3           | 3                 | 6                 | 8    | 3                   | 5                 | 8    | 9    | 7    | 12    | 12    |
| <b>Dedicated Inputs per Bank</b>       |             |                   |                   |      |                     |                   |      |      |      |       |       |
| Bank 0                                 | 0           | 0                 | 0                 | 0    | 0                   | 0                 | 0    | 0    | 0    | 0     | 0     |
| Bank 1                                 | 0           | 0                 | 0                 | 0    | 0                   | 0                 | 0    | 0    | 0    | 0     | 0     |
| Bank 2                                 | 2           | 2                 | 2                 | 2    | 2                   | 2                 | 2    | 2    | 2    | 2     | 2     |
| Bank 3                                 | 0           | 0                 | 0                 | 0    | 0                   | 0                 | 0    | 0    | 0    | 0     | 0     |
| Configuration                          | 0           | 0                 | 0                 | 0    | 0                   | 0                 | 0    | 0    | 0    | 0     | 0     |
| Total Dedicated Inputs                 | 2           | 2                 | 2                 | 2    | 2                   | 2                 | 2    | 2    | 2    | 2     | 2     |
| <b>Vccio Pins</b>                      |             |                   |                   |      |                     |                   |      |      |      |       |       |
| Bank 0                                 | 1           | 1                 | 1                 | 1    | 1                   | 1                 | 1    | 1    | 1    | 2     | 1     |
| Bank 1                                 | 1           | 1                 | 1                 | 1    | 0                   | 1                 | 1    | 1    | 1    | 2     | 1     |
| Bank 2                                 | 1           | 1                 | 1                 | 1    | 1                   | 1                 | 1    | 1    | 1    | 2     | 1     |
| Bank 3                                 | 1           | 0                 | 0                 | 1    | 0                   | 0                 | 1    | 1    | 1    | 2     | 2     |
| VCC                                    | 1           | 1                 | 2                 | 3    | 1                   | 2                 | 3    | 2    | 4    | 4     | 4     |
| VCC_SPI                                | 1           | 1                 | 1                 | 1    | 1                   | 1                 | 1    | 1    | 1    | 1     | 1     |
| VPP_2V5                                | 1           | 1                 | 1                 | 1    | 1                   | 1                 | 1    | 1    | 1    | 1     | 1     |
| VPP_FAST <sup>3</sup>                  | 0           | 0                 | 0                 | 1    | 1                   | 0                 | 1    | 0    | 1    | 1     | 1     |
| VCCPLL                                 | 0           | 0                 | 0                 | 0    | 0                   | 1                 | 1    | 0    | 0    | 1     | 1     |
| GND                                    | 2           | 3                 | 3                 | 4    | 3                   | 4                 | 5    | 9    | 4    | 8     | 11    |
| NC                                     | 0           | 0                 | 0                 | 10   | 0                   | 0                 | 0    | 0    | 0    | 0     | 3     |
| Total Count of Bonded Pins             | 32          | 36                | 49                | 81   | 36                  | 49                | 81   | 81   | 84   | 121   | 121   |

1. V<sub>CCIO0</sub> and V<sub>CCIO1</sub> are connected together.
2. V<sub>CCIO2</sub> and V<sub>CCIO3</sub> are connected together.
3. V<sub>PP\_FAST</sub>, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V<sub>PP\_FAST</sub> ball connected to V<sub>CCIO\_0</sub> ball externally.

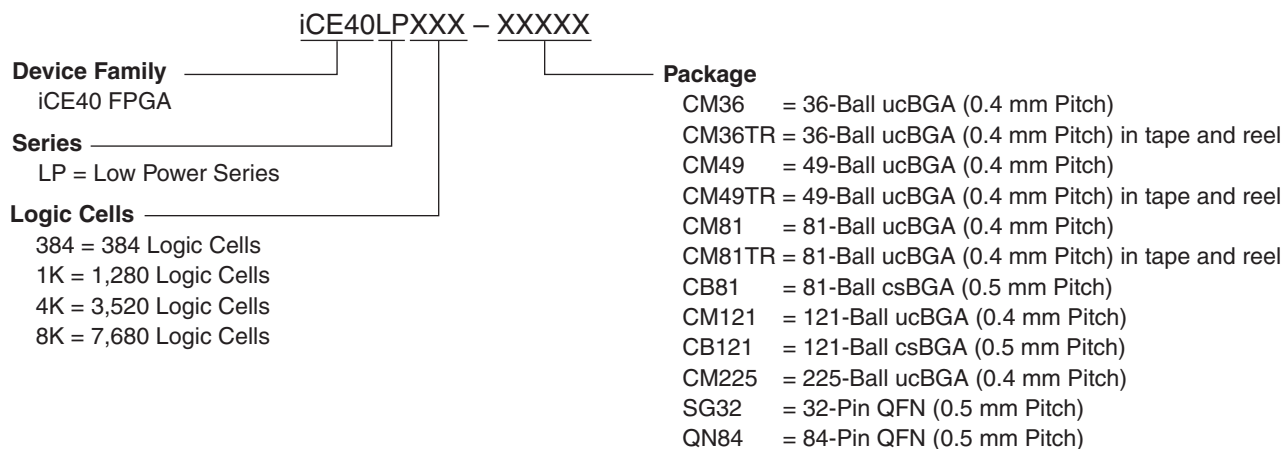
### Pin Information Summary, Continued

|                                        | iCE40-4KLP |       |       | iCE40-8KLP |       | iCE40-1KHX |       |       | iCE40-4KHX |       | iCE40-8KHX |       |       |
|----------------------------------------|------------|-------|-------|------------|-------|------------|-------|-------|------------|-------|------------|-------|-------|
|                                        | CM81       | CM121 | CM225 | CM121      | CM225 | VQ100      | CB132 | TQ144 | CB132      | TQ144 | CB132      | CM225 | CT256 |
| <b>General Purpose I/O per Bank</b>    |            |       |       |            |       |            |       |       |            |       |            |       |       |
| Bank 0                                 | 17         | 23    | 46    | 23         | 46    | 19         | 24    | 23    | 24         | 27    | 24         | 46    | 52    |
| Bank 1                                 | 15         | 21    | 42    | 21         | 42    | 19         | 25    | 25    | 25         | 29    | 25         | 42    | 52    |
| Bank 2                                 | 9          | 19    | 40    | 19         | 40    | 12         | 20    | 20    | 18         | 19    | 18         | 40    | 46    |
| Bank 3                                 | 18         | 26    | 46    | 26         | 46    | 18         | 22    | 24    | 24         | 28    | 24         | 46    | 52    |
| Configuration                          | 4          | 4     | 4     | 4          | 4     | 4          | 4     | 4     | 4          | 4     | 4          | 4     | 4     |
| Total General Purpose Single Ended I/O | 63         | 93    | 178   | 93         | 178   | 72         | 95    | 96    | 95         | 107   | 95         | 178   | 206   |
| <b>Differential Inputs per Bank</b>    |            |       |       |            |       |            |       |       |            |       |            |       |       |
| Bank 0                                 | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     |
| Bank 1                                 | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     |
| Bank 2                                 | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     |
| Bank 3                                 | 9          | 13    | 23    | 13         | 23    | 9          | 11    | 12    | 12         | 14    | 12         | 23    | 26    |
| Configuration                          | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     |
| Total Differential Inputs              | 9          | 13    | 23    | 13         | 23    | 9          | 11    | 12    | 12         | 14    | 12         | 23    | 26    |
| <b>Dedicated Inputs per Bank</b>       |            |       |       |            |       |            |       |       |            |       |            |       |       |
| Bank 0                                 | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     |
| Bank 1                                 | 0          | 0     | 1     | 0          | 1     | 0          | 1     | 1     | 1          | 1     | 1          | 1     | 1     |
| Bank 2                                 | 2          | 2     | 2     | 2          | 2     | 2          | 2     | 2     | 2          | 2     | 2          | 2     | 2     |
| Bank 3                                 | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     |
| Configuration                          | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     | 0          | 0     | 0          | 0     | 0     |
| Total Dedicated Inputs                 | 2          | 2     | 3     | 2          | 3     | 2          | 3     | 3     | 3          | 3     | 3          | 3     | 3     |
| <b>Vccio Pins</b>                      |            |       |       |            |       |            |       |       |            |       |            |       |       |
| Bank 0                                 | 1          | 1     | 3     | 1          | 3     | 2          | 2     | 2     | 2          | 2     | 2          | 3     | 4     |
| Bank 1                                 | 1          | 1     | 3     | 1          | 3     | 2          | 2     | 2     | 2          | 2     | 2          | 3     | 4     |
| Bank 2                                 | 1          | 1     | 3     | 1          | 3     | 2          | 2     | 2     | 2          | 2     | 2          | 3     | 4     |
| Bank 3                                 | 1          | 2     | 4     | 2          | 4     | 3          | 3     | 2     | 3          | 2     | 3          | 4     | 4     |
| VCC                                    | 3          | 4     | 8     | 4          | 8     | 4          | 5     | 4     | 5          | 4     | 5          | 8     | 6     |
| VCC_SPI                                | 1          | 1     | 1     | 1          | 1     | 1          | 1     | 1     | 1          | 1     | 1          | 1     | 1     |
| VPP_2V5                                | 1          | 1     | 1     | 1          | 1     | 1          | 1     | 1     | 1          | 1     | 1          | 1     | 1     |
| VPP_FAST <sup>1</sup>                  | 1          | 1     | 1     | 1          | 1     | 1          | 1     | 1     | 1          | 1     | 1          | 1     | 1     |
| VCCPLL                                 | 1          | 2     | 2     | 2          | 2     | 0          | 1     | 1     | 2          | 2     | 2          | 2     | 2     |
| GND                                    | 5          | 12    | 18    | 12         | 18    | 10         | 14    | 10    | 15         | 11    | 15         | 18    | 20    |
| NC                                     | 0          | 0     | 0     | 0          | 0     | 0          | 2     | 19    | 0          | 6     | 0          | 0     | 0     |
| Total Count of Bonded Pins             | 81         | 121   | 225   | 121        | 225   | 100        | 132   | 144   | 132        | 144   | 132        | 225   | 256   |

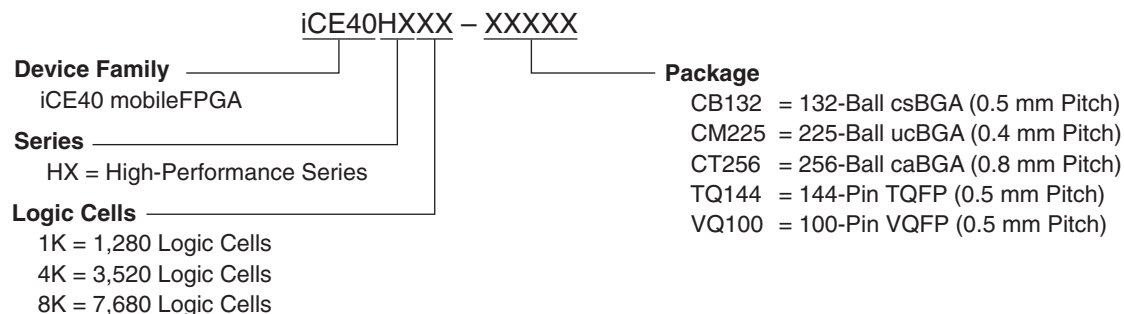
1. VPP\_FAST, used only for fast production programming, must be left floating or unconnected in applications.

### iCE40 Part Number Description

#### Ultra Low Power (LP) Devices



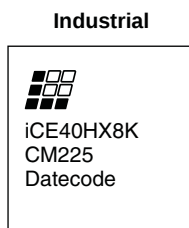
#### High Performance (HX) Devices



All parts shipped in trays unless noted.

### Ordering Information

iCE40 devices have top-side markings for the industrial grade, as shown below:



Note: Markings are abbreviated for small packages.

**Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging**

| Part Number       | LUTs | Supply Voltage | Package            | Leads | Temp. |
|-------------------|------|----------------|--------------------|-------|-------|
| iCE40LP384-CM36   | 384  | 1.2V           | Halogen-Free ucBGA | 36    | IND   |
| iCE40LP384-CM36TR | 384  | 1.2V           | Halogen-Free ucBGA | 36    | IND   |
| iCE40LP384-CM49   | 384  | 1.2V           | Halogen-Free ucBGA | 49    | IND   |
| iCE40LP384-CM49TR | 384  | 1.2V           | Halogen-Free ucBGA | 49    | IND   |
| iCE40LP384-CM81   | 384  | 1.2V           | Halogen-Free ucBGA | 81    | IND   |
| iCE40LP384-CM81TR | 384  | 1.2V           | Halogen-Free ucBGA | 81    | IND   |
| iCE40LP384-SG32   | 384  | 1.2V           | Halogen-Free QFN   | 32    | IND   |
| iCE40LP1K-CM36    | 1280 | 1.2V           | Halogen-Free ucBGA | 36    | IND   |
| iCE40LP1K-CM36TR  | 1280 | 1.2V           | Halogen-Free ucBGA | 36    | IND   |
| iCE40LP1K-CM49    | 1280 | 1.2V           | Halogen-Free ucBGA | 49    | IND   |
| iCE40LP1K-CM49TR  | 1280 | 1.2V           | Halogen-Free ucBGA | 49    | IND   |
| iCE40LP1K-CM81    | 1280 | 1.2V           | Halogen-Free ucBGA | 81    | IND   |
| iCE40LP1K-CM81TR  | 1280 | 1.2V           | Halogen-Free ucBGA | 81    | IND   |
| iCE40LP1K-CB81    | 1280 | 1.2V           | Halogen-Free csBGA | 81    | IND   |
| iCE40LP1K-CM121   | 1280 | 1.2V           | Halogen-Free ucBGA | 121   | IND   |
| iCE40LP1K-CB121   | 1280 | 1.2V           | Halogen-Free csBGA | 121   | IND   |
| iCE40LP1K-QN84    | 1280 | 1.2V           | Halogen-Free QFN   | 84    | IND   |
| iCE40LP4K-CM81    | 3520 | 1.2V           | Halogen-Free ucBGA | 81    | IND   |
| iCE40LP4K-CM81TR  | 3520 | 1.2V           | Halogen-Free ucBGA | 81    | IND   |
| iCE40LP4K-CM121   | 3520 | 1.2V           | Halogen-Free ucBGA | 121   | IND   |
| iCE40LP4K-CM225   | 3520 | 1.2V           | Halogen-Free ucBGA | 225   | IND   |
| iCE40LP8K-CM121   | 7680 | 1.2V           | Halogen-Free ucBGA | 121   | IND   |
| iCE40LP8K-CM225   | 7680 | 1.2V           | Halogen-Free ucBGA | 225   | IND   |

**High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging**

| Part Number     | LUTs | Supply Voltage | Package            | Leads | Temp. |
|-----------------|------|----------------|--------------------|-------|-------|
| iCE40HX1K-CB132 | 1280 | 1.2V           | Halogen-Free csBGA | 132   | IND   |
| iCE40HX1K-VQ100 | 1280 | 1.2V           | Halogen-Free VQFP  | 100   | IND   |
| iCE40HX1K-TQ144 | 1280 | 1.2V           | Halogen-Free TQFP  | 144   | IND   |
| iCE40HX4K-CB132 | 3520 | 1.2V           | Halogen-Free csBGA | 132   | IND   |
| iCE40HX4K-TQ144 | 3520 | 1.2V           | Halogen-Free TQFP  | 144   | IND   |
| iCE40HX8K-CB132 | 7680 | 1.2V           | Halogen-Free csBGA | 132   | IND   |
| iCE40HX8K-CM225 | 7680 | 1.2V           | Halogen-Free ucBGA | 225   | IND   |
| iCE40HX8K-CT256 | 7680 | 1.2V           | Halogen-Free caBGA | 256   | IND   |

## For Further Information

A variety of technical notes for the iCE40 family are available on the Lattice web site.

- TN1248, [iCE40 Programming and Configuration](#)
- TN1250, [Memory Usage Guide for iCE40 Devices](#)
- TN1251, [iCE40 sysCLOCK PLL Design and Usage Guide](#)
- TN1252, [iCE40 Hardware Checklist](#)
- TN1253, [Using Differential I/O \(LVDS, Sub-LVDS\) in iCE40 Devices](#)
- TN1074, [PCB Layout Recommendations for BGA Packages](#)
- [iCE40 Pinout Files](#)
- [Thermal Management](#) document
- [Lattice design tools](#)
- [IBIS](#)
- [Package Datasheet](#)
- [Schematic Symbols](#)



# iCE40 LP/HX Family Data Sheet

## Revision History

March 2013

Data Sheet DS1040

| Date       | Version | Section                          | Change Summary                                                                                                                                             |
|------------|---------|----------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| July 2011  | 01.0    | —                                | Initial release.                                                                                                                                           |
| July 2011  | 01.01   | —                                | Added 640, 1K and 4K to Table 13 configuration times. Updated Table 1 maximum I/Os.                                                                        |
| July 2011  | 01.1    | —                                | Moved package specifications to iCE40 pinout Excel files.<br>Updated Table 1 maximum I/Os.                                                                 |
| Aug 2012   | 01.2    | —                                | Updated company name.                                                                                                                                      |
| July 2011  | 01.21   | —                                | Updated Figure 3 and Figure 4 to specify iCE40.                                                                                                            |
| July 2011  | 01.3    | —                                | Production release.<br>Updated notes on Table 3: Recommended Operating Conditions.<br>Updated values in Table 4, Table 5, Table 12, Table 13 and Table 17. |
| July 2011  | 01.31   | —                                | Updated Table 1.                                                                                                                                           |
| March 2013 | 02.0    | —                                | Merged SiliconBlue iCE40 LP and HX data sheets and updated to Lattice format.                                                                              |
|            | 02.1    | DC and Switching Characteristics | Recommended operating conditions added requirement for Master SPI.                                                                                         |
|            |         |                                  | Updated Recommended Operating Conditions for $V_{PP\_2V5}$ .                                                                                               |
|            |         |                                  | Updated Power-On-Reset Voltage Levels and sequence requirements.                                                                                           |
|            |         |                                  | Updated Static Supply Current conditions.                                                                                                                  |
|            |         |                                  | Changed unit for $t_{SKEW\_IO}$ from ns to ps.                                                                                                             |
|            |         |                                  | Updated range of CCLK $f_{MAX}$ .                                                                                                                          |
|            |         | Ordering Information             | Updated ordering information to include tape and reel part numbers.                                                                                        |